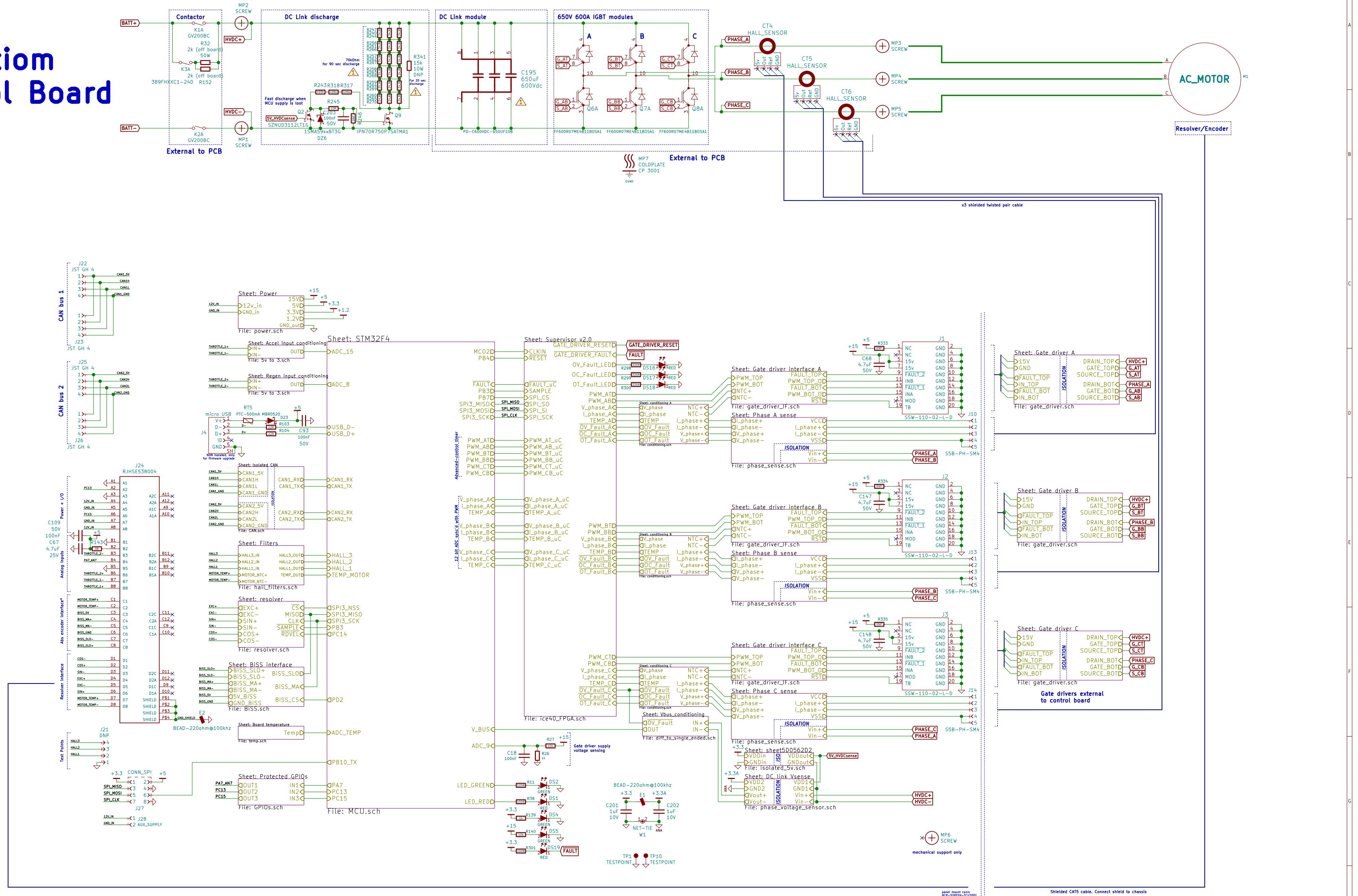


PD-Axiom Control Board



Sheet: spares

File: spares.sch

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Title: PD-Axiom

Sheet: /

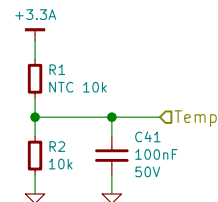
PowerDesigns.ca - CC-BY-SA

Rev: 1

Id: 1/34

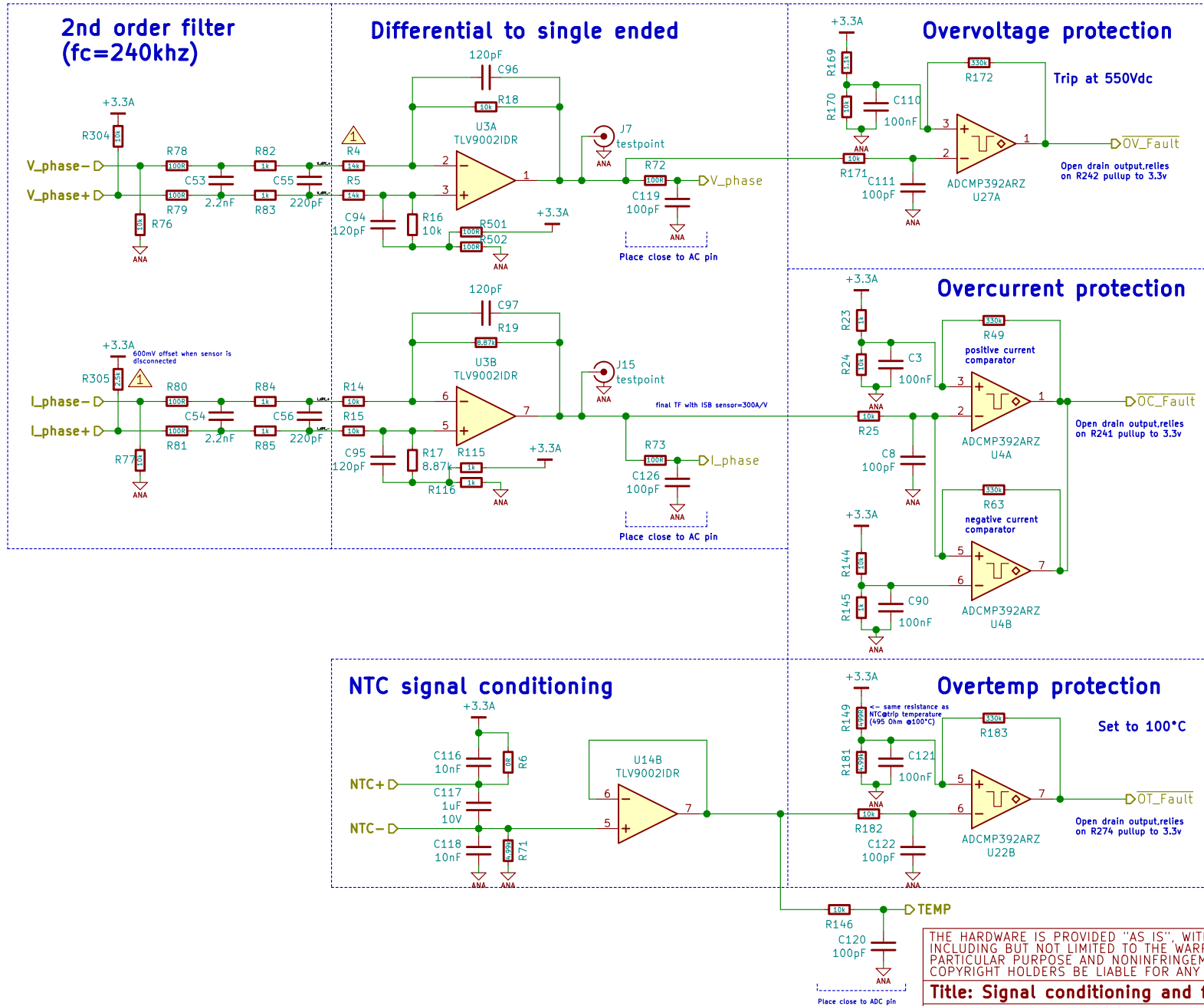
Date: 2019-08-15

PCB temperature sensor



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Title: Controller temperature sensing	Rev: 1
Sheet: /Board temperature/	Id: 2/34
PowerDesigns.ca - CC-BY-SA	Date: 2019-08-15

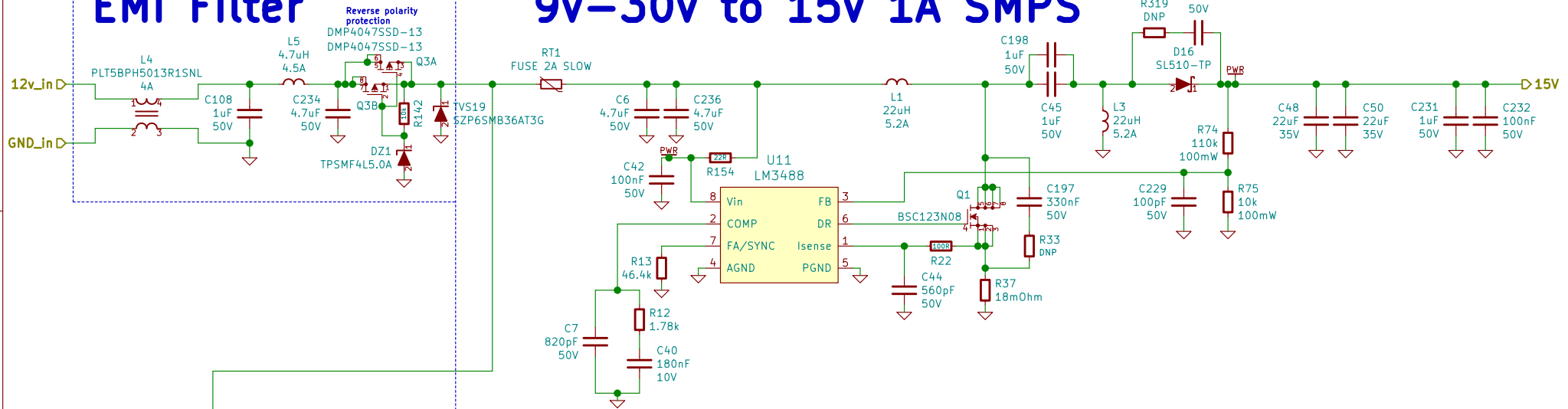


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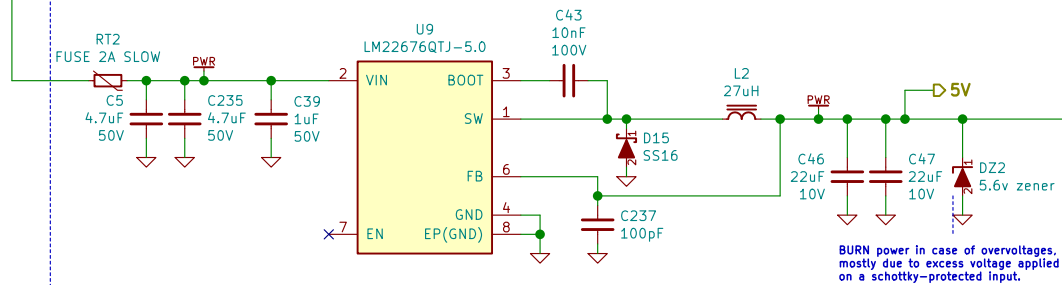
Title: Signal conditioning and fault trips	Rev: 1
Sheet: /conditioning A/	Id: 3/34
PowerDesigns.ca - CC-BY-SA	Date: 2019-08-15

EMI Filter

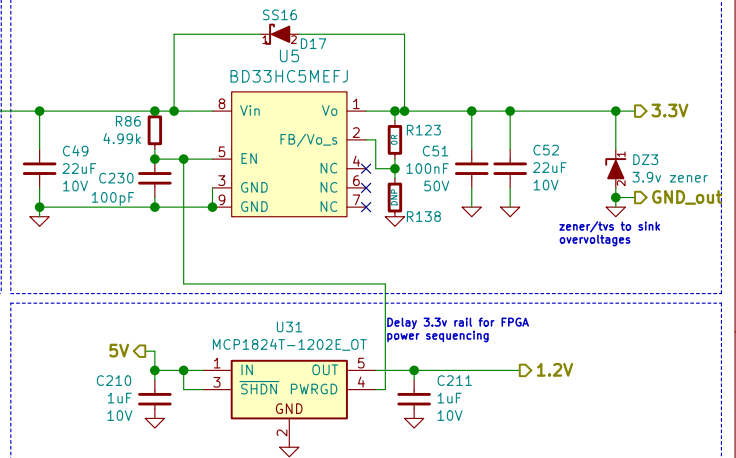
9v-30v to 15v 1A SMPS



9v-30v to 5.0v 3A SMPS



3.3v LDO regulator



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Title: Power supplies

Rev: 1

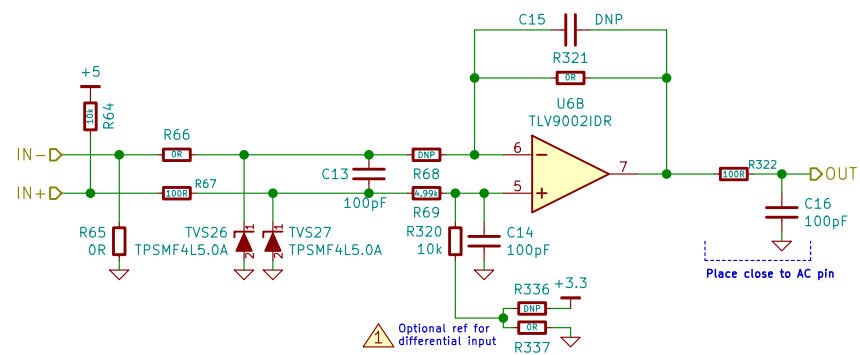
Sheet: /Power/

Id: 4/34

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Date: 2019-08-15

5v to 3.3v with overvoltage protection and filtering



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Title: 5v to 3.3v conditioning

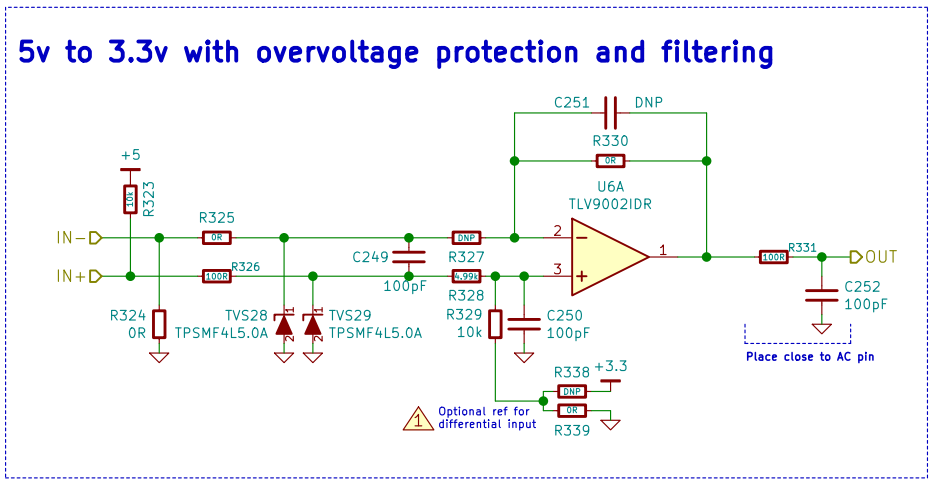
Rev: 1

Sheet: /Accel input conditioning/

Id: 6/34

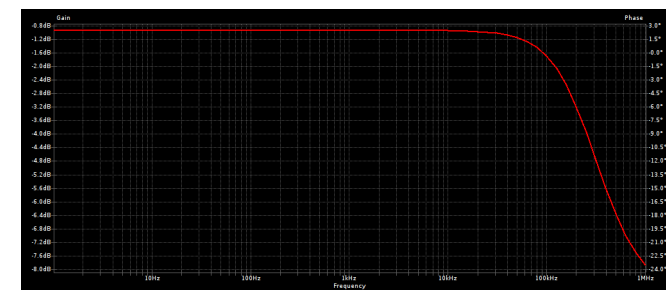
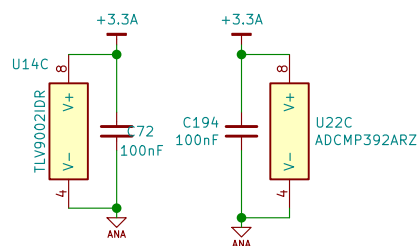
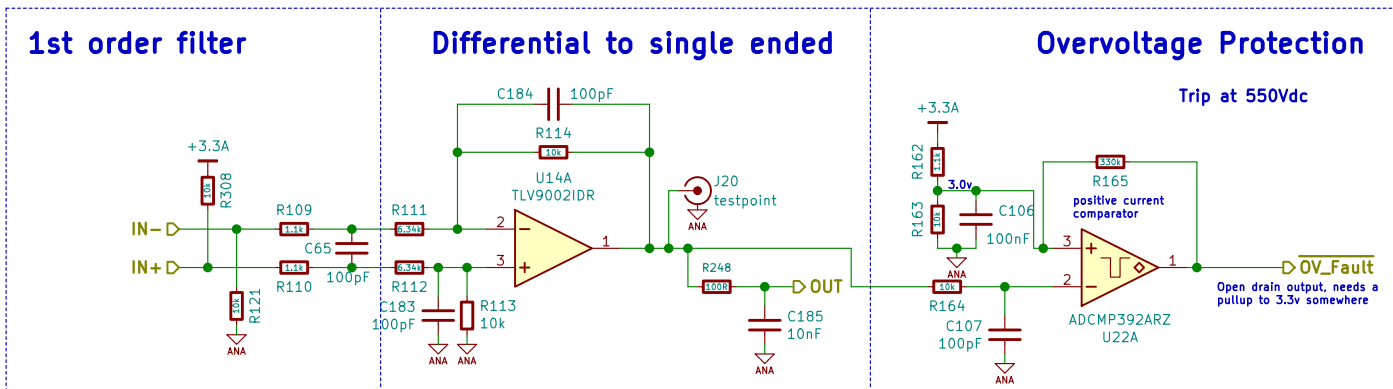
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Date: 2019-08-15



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Title: 5v to 3.3v conditioning	Rev: 1
Sheet: /Regen input conditioning/	Id: 7/34
PowerDesigns.ca - CC-BY-SA	Date: 2019-08-15



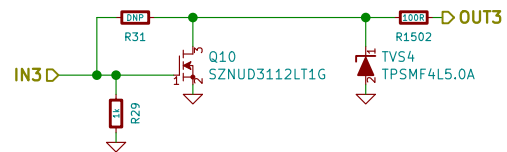
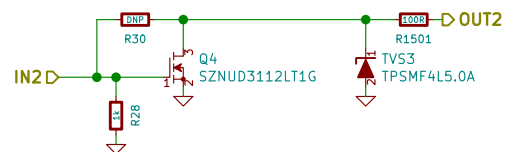
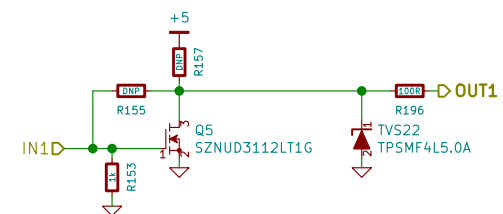
$f_c = 170\text{kHz}$

see simulation projects in /simulation/ folder

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Title: Differential to single ended	Rev: 1
Sheet: /Vbus_conditioning/	Id: 8/34
PowerDesigns.ca - CC-BY-SA	Date: 2019-08-15

Protected, 1A Open drain outputs



These circuits can be reconfigured
to work as a 12V open drain output for fans,
relays or pumps.
Remember TPSMF4L5.0A is a 5v zener

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Title: Protected outputs

Rev: 1

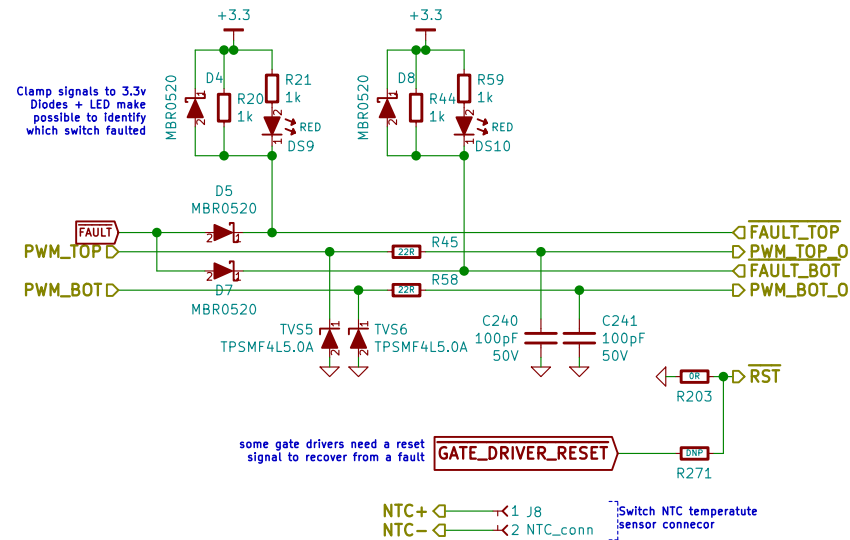
Sheet: /Protected GPIOs/

Id: 9/34

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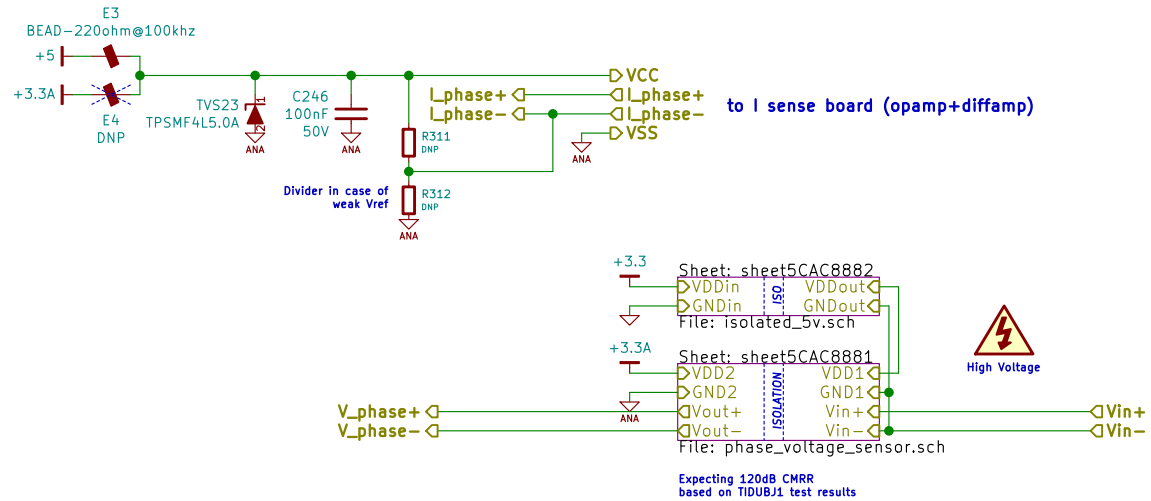
Date: 2019-08-15

GATE DRIVER INTERFACE



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Title: Gate Driver Interface	Rev: 1
Sheet: /Gate driver interface A/	Id: 10/34
PowerDesigns.ca - CC-BY-SA	Date: 2019-08-15

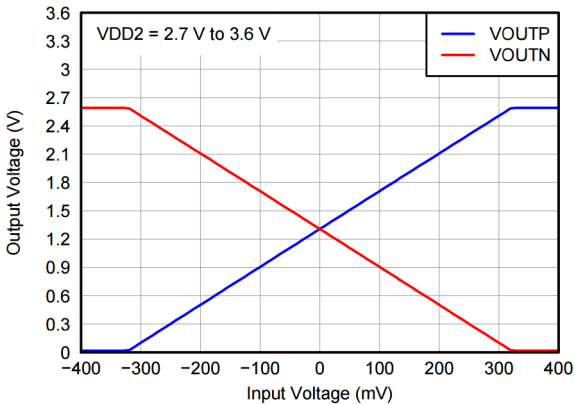
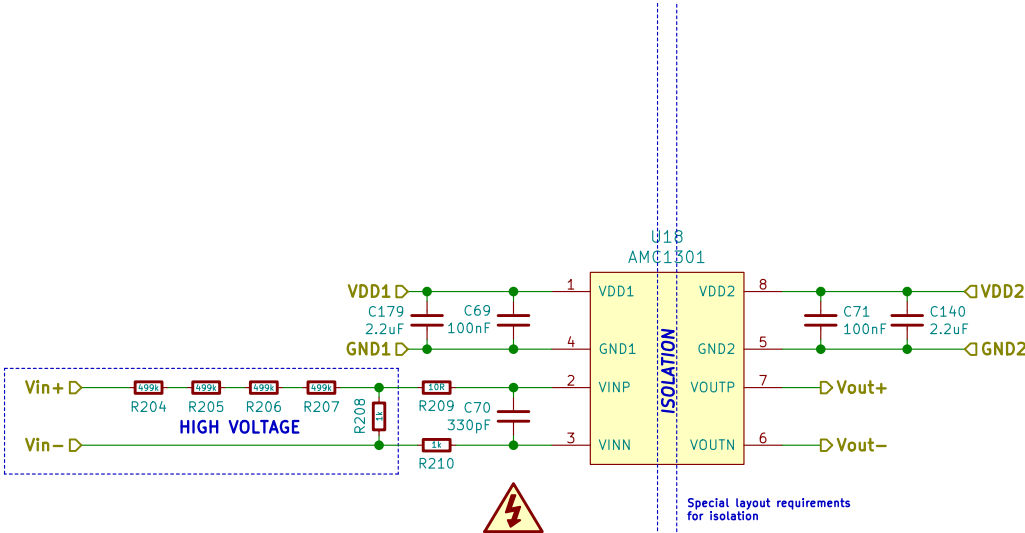


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Title: High Voltage sensing and current sensor input	Rev: 1
Sheet: /Phase A sense/	Id: 11/34
PowerDesigns.ca - CC-BY-SA	Date: 2019-08-15

0–650V phase voltage measurement using isolation amplifier

1 Features

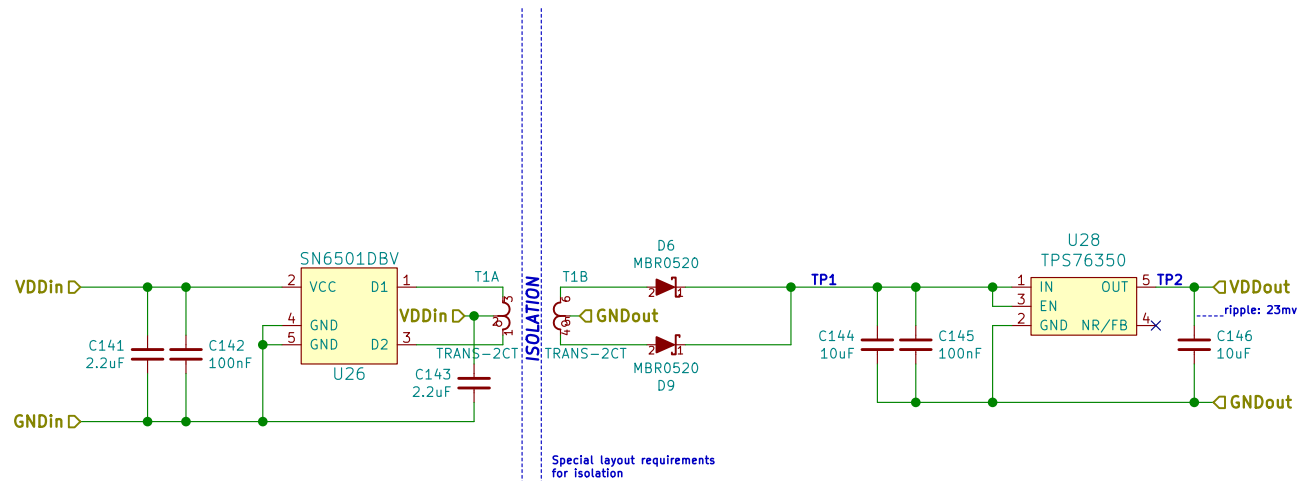
- $\pm 250\text{-mV}$ Input Voltage Range Optimized for Shunt Resistors
- Very Low Nonlinearity: 0.075% Maximum at 5 V
- Low Offset Error: 1.5 mV Maximum
- Low Noise: 3.1 mV_{RMS} Typical
- Low High-Side Supply Current: 8 mA Maximum at 5 V
- Input Bandwidth: 60 kHz Minimum
- Fixed Gain: 8 (0.5% accuracy)
- High Common Mode Rejection Ratio: 108 dB
- 3.3-V Operation on Low-Side
- Certified Galvanic Isolation:
 - UL1577 and VDE V 0884-10 Approved
 - Isolation Voltage: 4250 V_{PEAK} (AMC1200B)
 - Working Voltage: 1200 V_{PEAK}
 - Transient Immunity: 10 kV/ μs Minimum
- Typical 10-Year Lifespan at Rated Working Voltage (see Application Report SLLA197)
- Fully Specified Over the Extended Industrial Temperature Range



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Title: High Voltage sensing	Rev: 1
Sheet: /Phase A sense/sheet5CAC8881/	Id: 12/34
PowerDesigns.ca - CC-BY-SA	Date: 2019-08-15

ISOLATED POWER SUPPLY



Transformer selection:
2500Vrms Isolation 3 -> 5v (LDO) 760390015
5000Vrms Isolation 3 -> 5v (LDO) 750313626 (higher CMRR?)

Figure 9. Output Voltage vs Load Current

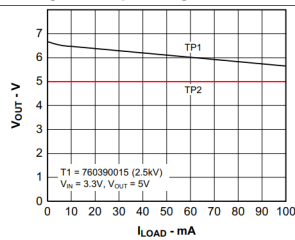
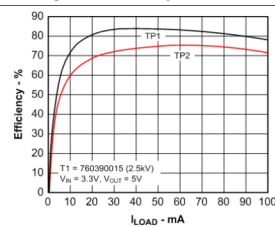


Figure 10. Efficiency vs Load Current



TP1: rectified node
TP2: LDO output

11.2 Layout Example

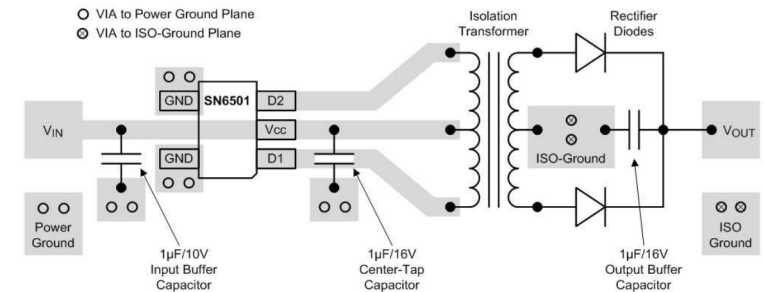
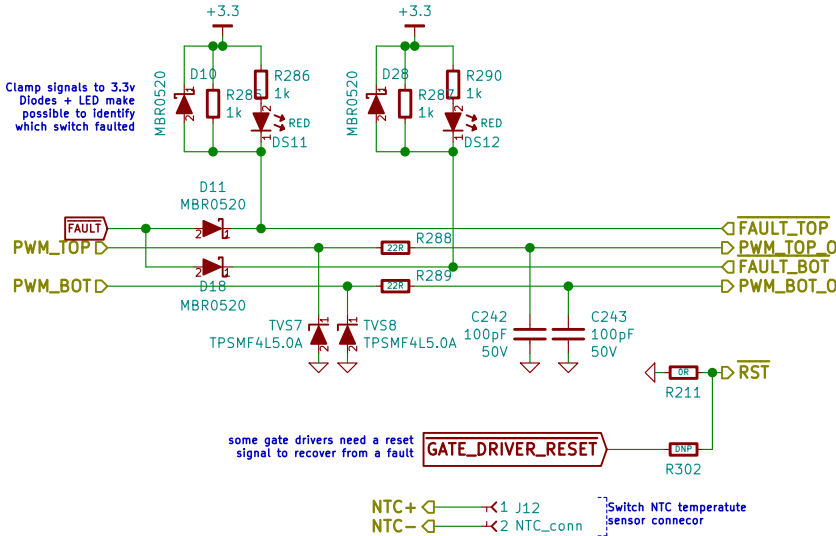


Figure 57. Layout Example of a 2-Layer Board (SN6501)

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Title: Isolated DC/DC supply	Rev: 1
Sheet: /Phase A sense/sheet5CAC8882/	Id: 13/34
PowerDesigns.ca - CC-BY-SA	Date: 2019-08-15

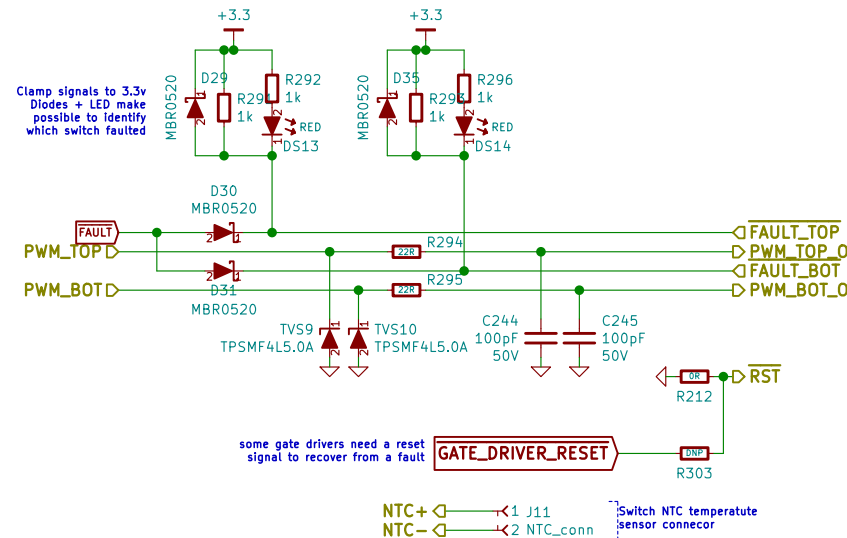
GATE DRIVER INTERFACE



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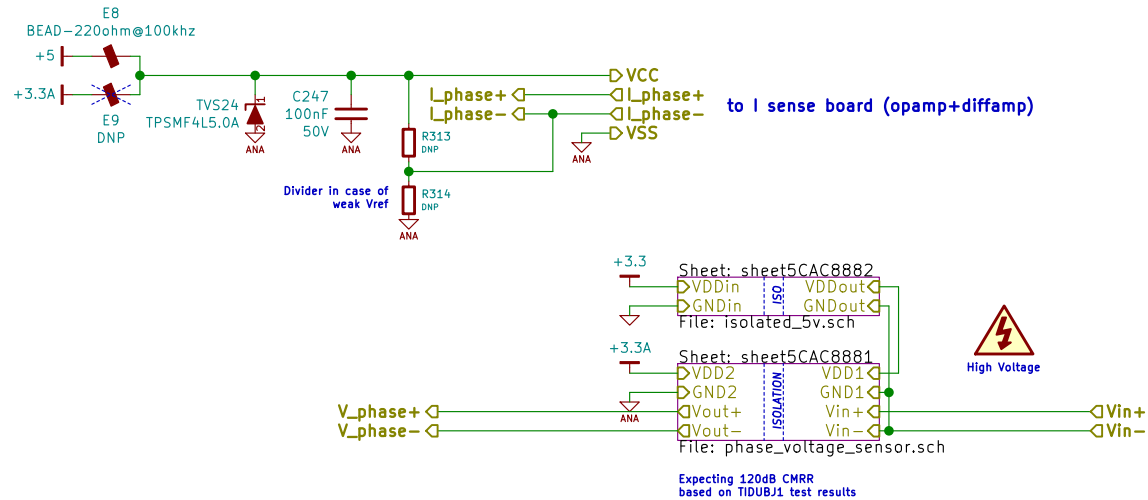
Title: Gate Driver Interface	Rev: 1
Sheet: /Gate driver interface B/	Id: 14/34
PowerDesigns.ca – CC-BY-SA	Date: 2019-08-15

GATE DRIVER INTERFACE



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Title: Gate Driver Interface	Rev: 1
Sheet: /Gate driver interface C/	Id: 15/34
PowerDesigns.ca - CC-BY-SA	Date: 2019-08-15



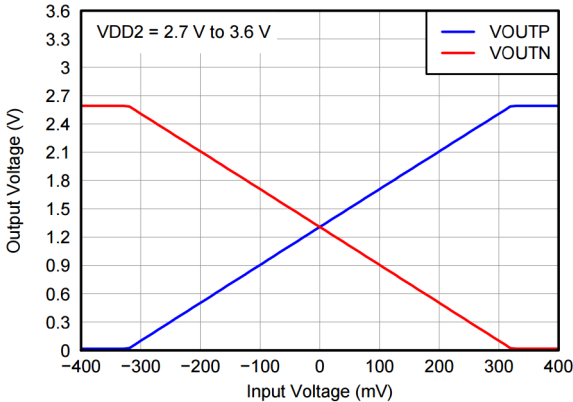
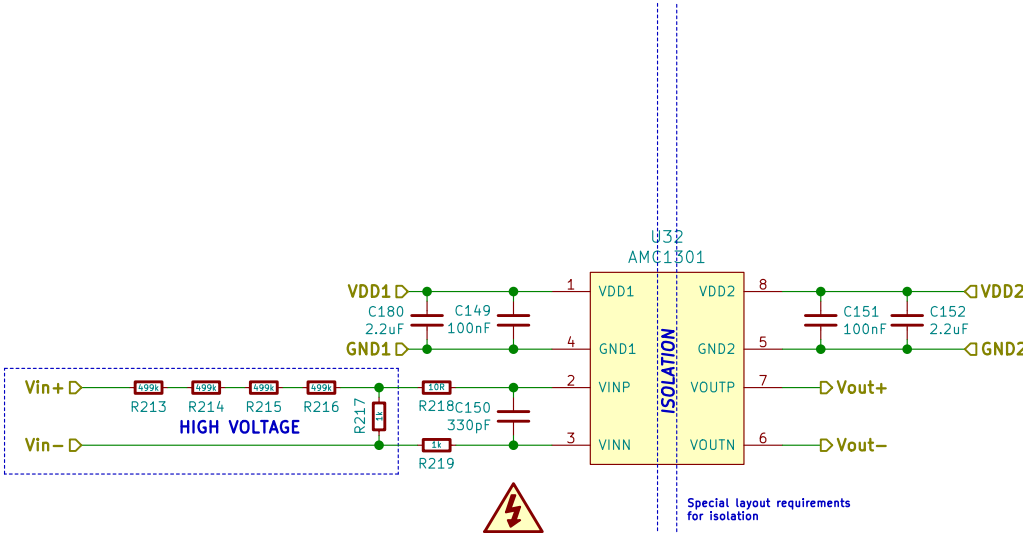
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Title: High Voltage sensing and current sensor input	Rev: 1
Sheet: /Phase B sense/	Id: 16/34
PowerDesigns.ca - CC-BY-SA	Date: 2019-08-15

0–650V phase voltage measurement using isolation amplifier

1 Features

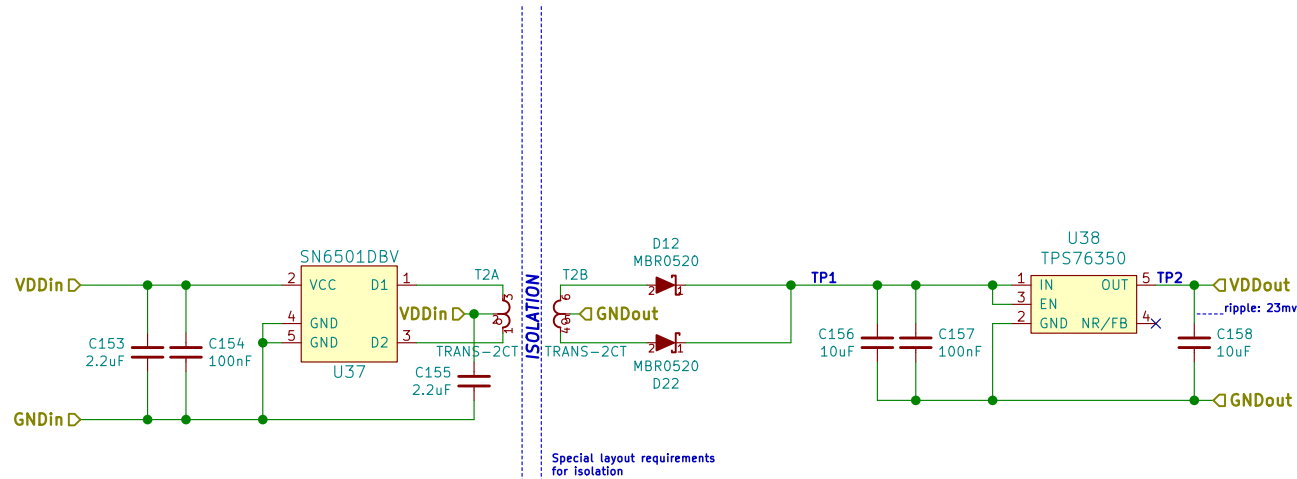
- ± 250 -mV Input Voltage Range Optimized for Shunt Resistors
- Very Low Nonlinearity: 0.075% Maximum at 5 V
- Low Offset Error: 1.5 mV Maximum
- Low Noise: 3.1 mV_{RMS} Typical
- Low High-Side Supply Current: 8 mA Maximum at 5 V
- Input Bandwidth: 60 kHz Minimum
- Fixed Gain: 8 (0.5% accuracy)
- High Common Mode Rejection Ratio: 108 dB
- 3.3-V Operation on Low-Side
- Certified Galvanic Isolation:
 - UL1577 and VDE V 0884-10 Approved
 - Isolation Voltage: 4250 V_{PEAK} (AMC1200B)
 - Working Voltage: 1200 V_{PEAK}
 - Transient Immunity: 10 kV/ μ s Minimum
- Typical 10-Year Lifespan at Rated Working Voltage (see Application Report SLLA197)
- Fully Specified Over the Extended Industrial Temperature Range



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Title: High Voltage sensing	Rev: 1
Sheet: /Phase B sense/sheet5CAC8881/	Id: 17/34
PowerDesigns.ca - CC-BY-SA	Date: 2019-08-15

ISOLATED POWER SUPPLY



Transformer selection:
2500Vrms Isolation 3 -> 5v (LDO) 760390015
5000Vrms Isolation 3 -> 5v (LDO) 750313626 (higher CMRR?)

Figure 9. Output Voltage vs Load Current

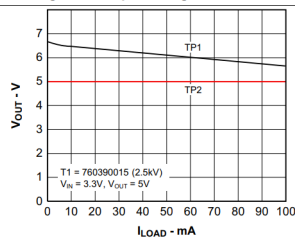
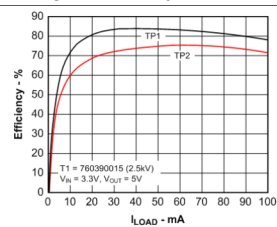


Figure 10. Efficiency vs Load Current



TP1: rectified node
TP2: LDO output

11.2 Layout Example

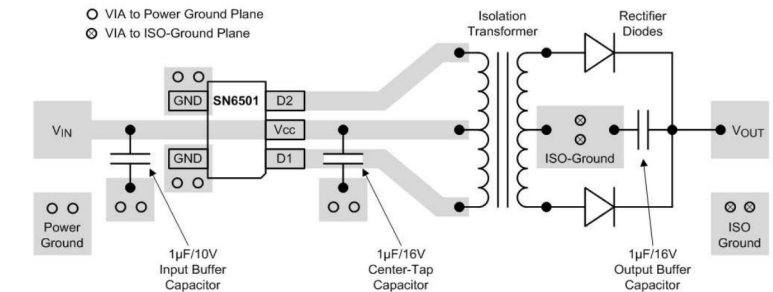
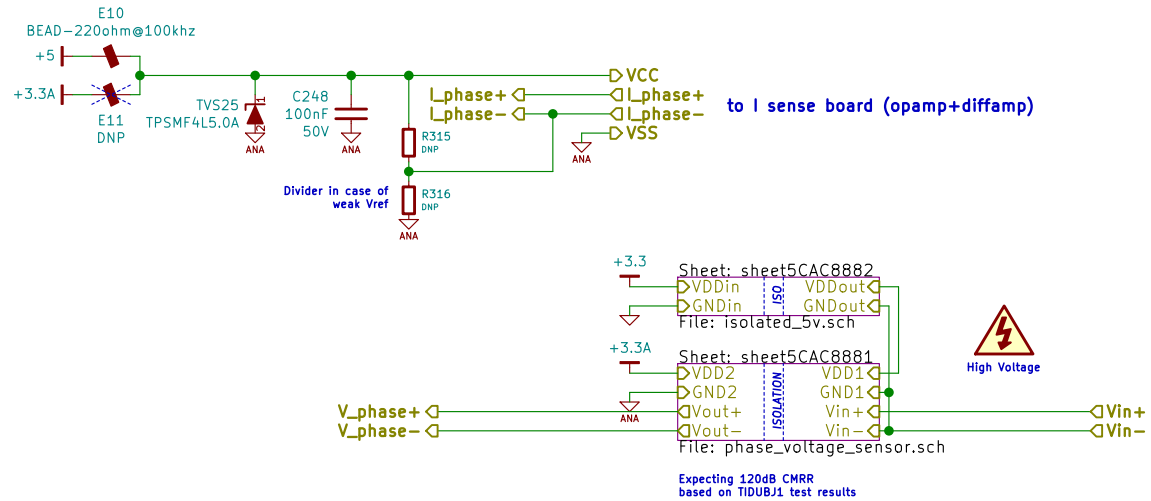


Figure 57. Layout Example of a 2-Layer Board (SN6501)

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Title: Isolated DC/DC supply	Rev: 1
Sheet: /Phase B sense/sheet5CAC8882/	Id: 18/34
PowerDesigns.ca - CC-BY-SA	Date: 2019-08-15



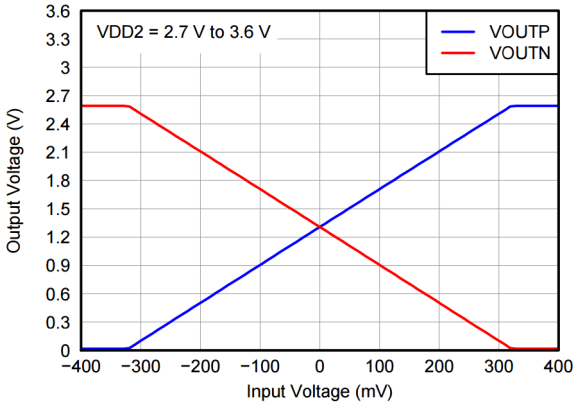
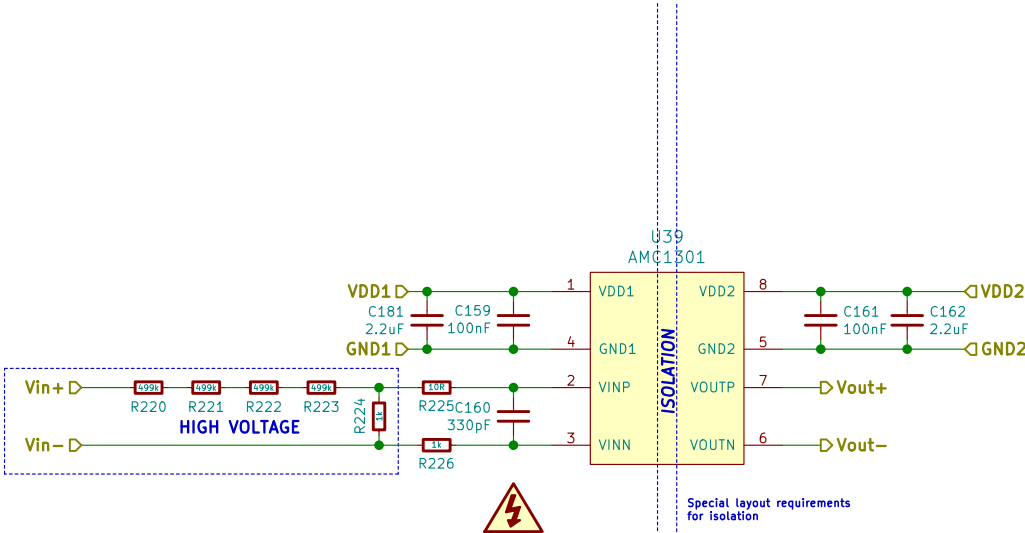
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Title: High Voltage sensing and current sensor input	Rev: 1
Sheet: /Phase C sense/	Id: 19/34
PowerDesigns.ca - CC-BY-SA	Date: 2019-08-15

0–650V phase voltage measurement using isolation amplifier

1 Features

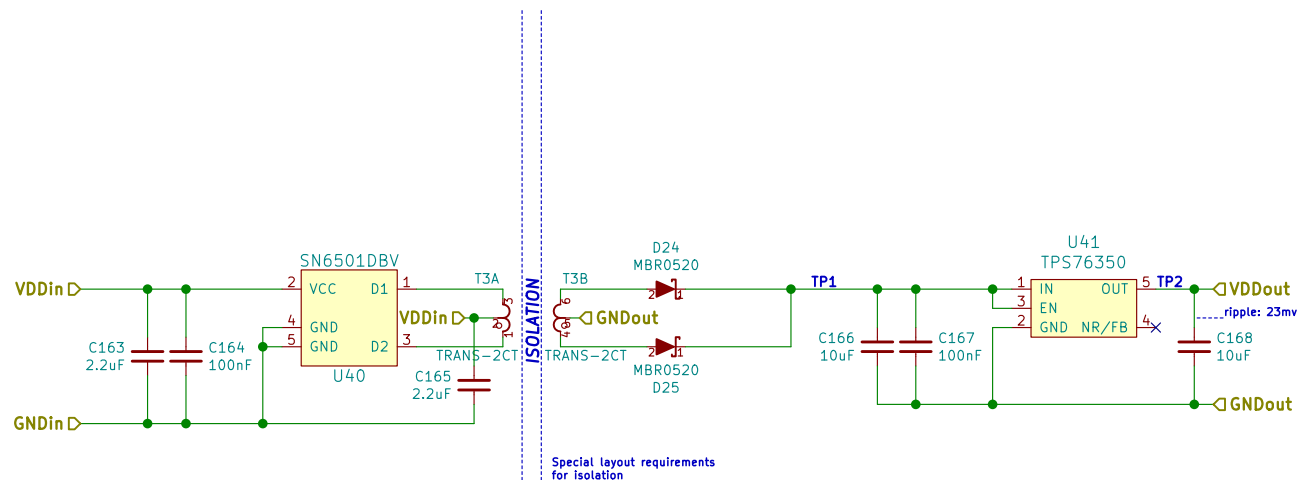
- ± 250 -mV Input Voltage Range Optimized for Shunt Resistors
- Very Low Nonlinearity: 0.075% Maximum at 5 V
- Low Offset Error: 1.5 mV Maximum
- Low Noise: 3.1 mV_{RMS} Typical
- Low High-Side Supply Current: 8 mA Maximum at 5 V
- Input Bandwidth: 60 kHz Minimum
- Fixed Gain: 8 (0.5% accuracy)
- High Common Mode Rejection Ratio: 108 dB
- 3.3-V Operation on Low-Side
- Certified Galvanic Isolation:
 - UL1577 and VDE V 0884-10 Approved
 - Isolation Voltage: 4250 V_{PEAK} (AMC1200B)
 - Working Voltage: 1200 V_{PEAK}
 - Transient Immunity: 10 kV/ μ s Minimum
- Typical 10-Year Lifespan at Rated Working Voltage (see Application Report SLLA197)
- Fully Specified Over the Extended Industrial Temperature Range



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Title: High Voltage sensing	Rev: 1
Sheet: /Phase C sense/sheet5CAC8881/	Id: 20/34
PowerDesigns.ca - CC-BY-SA	Date: 2019-08-15

ISOLATED POWER SUPPLY



Transformer selection:
2500Vrms Isolation 3 -> 5v (LDO) 760390015
5000Vrms Isolation 3 -> 5v (LDO) 750313626 (higher CMRR?)

Figure 9. Output Voltage vs Load Current

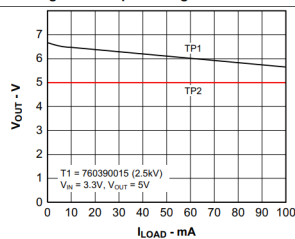
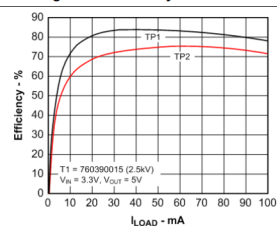


Figure 10. Efficiency vs Load Current



TP1: rectified node
TP2: LDO output

11.2 Layout Example

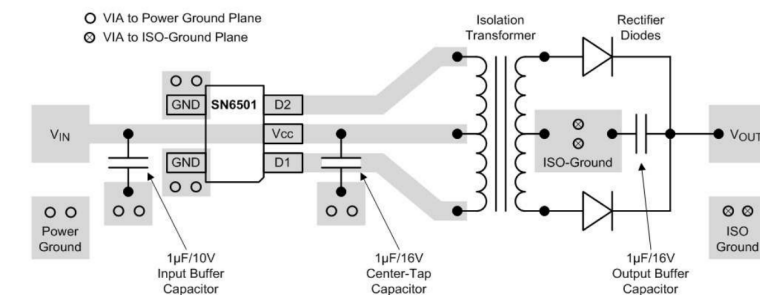


Figure 57. Layout Example of a 2-Layer Board (SN6501)

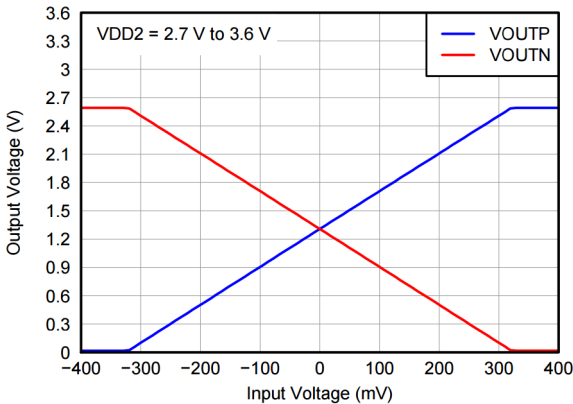
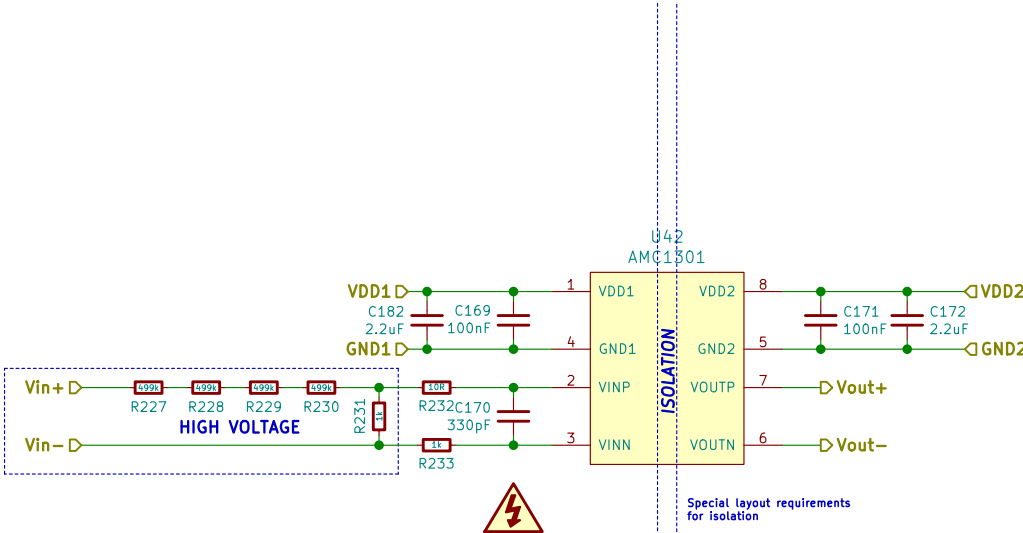
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Title: Isolated DC/DC supply	Rev: 1
Sheet: /Phase C sense/sheet5CAC8882/	Id: 21/34
PowerDesigns.ca - CC-BY-SA	Date: 2019-08-15

0–650V phase voltage measurement using isolation amplifier

1 Features

- ± 250 -mV Input Voltage Range Optimized for Shunt Resistors
- Very Low Nonlinearity: 0.075% Maximum at 5 V
- Low Offset Error: 1.5 mV Maximum
- Low Noise: 3.1 mV_{RMS} Typical
- Low High-Side Supply Current: 8 mA Maximum at 5 V
- Input Bandwidth: 60 kHz Minimum
- Fixed Gain: 8 (0.5% accuracy)
- High Common Mode Rejection Ratio: 108 dB
- 3.3-V Operation on Low-Side
- Certified Galvanic Isolation:
 - UL1577 and VDE V 0884-10 Approved
 - Isolation Voltage: 4250 V_{PEAK} (AMC1200B)
 - Working Voltage: 1200 V_{PEAK}
 - Transient Immunity: 10 kV/ μ s Minimum
- Typical 10-Year Lifespan at Rated Working Voltage (see Application Report SLLA197)
- Fully Specified Over the Extended Industrial Temperature Range



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Title: High Voltage sensing

Rev: 1

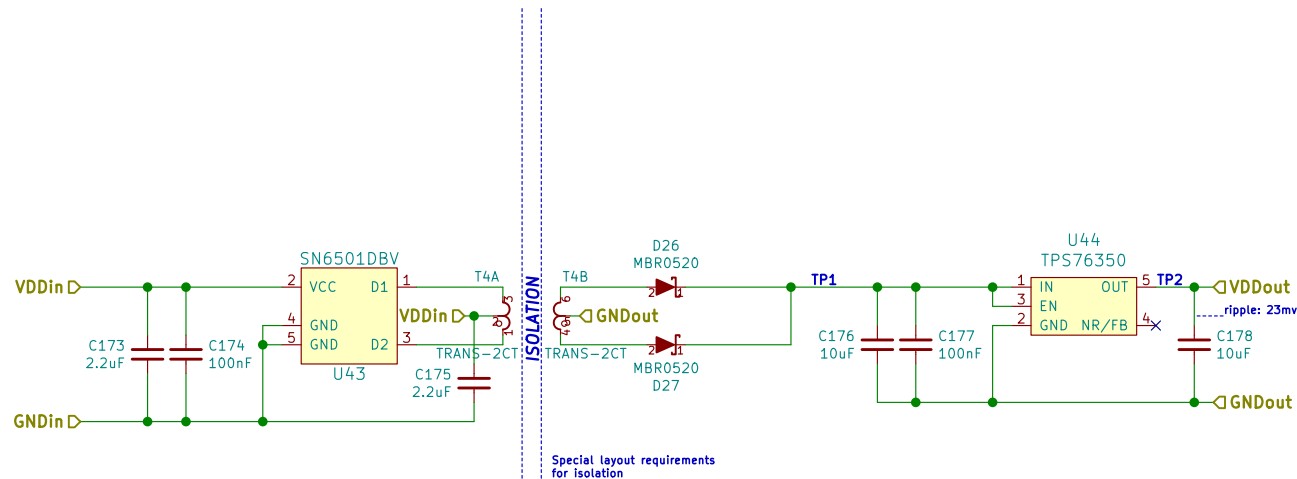
Sheet: /DC link Vsense/

Id: 22/34

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Date: 2019-08-15

ISOLATED POWER SUPPLY



Transformer selection:
2500Vrms Isolation 3 -> 5v (LDO) 760390015
5000Vrms Isolation 3 -> 5v (LDO) 750313626 (higher CMRR?)

Figure 9. Output Voltage vs Load Current

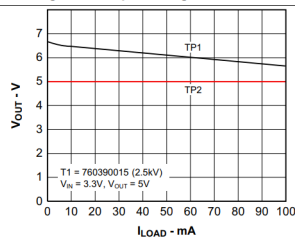
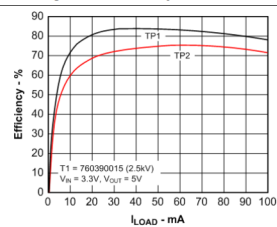


Figure 10. Efficiency vs Load Current



TP1: rectified node
TP2: LDO output

11.2 Layout Example

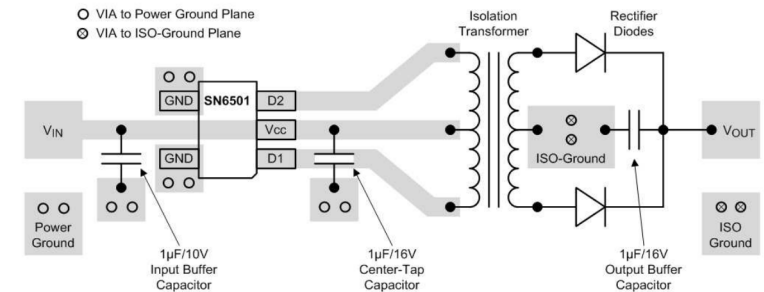


Figure 57. Layout Example of a 2-Layer Board (SN6501)

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Title: Isolated DC/DC supply	Rev: 1
Sheet: /sheet5D0562D2/	Id: 23/34
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A

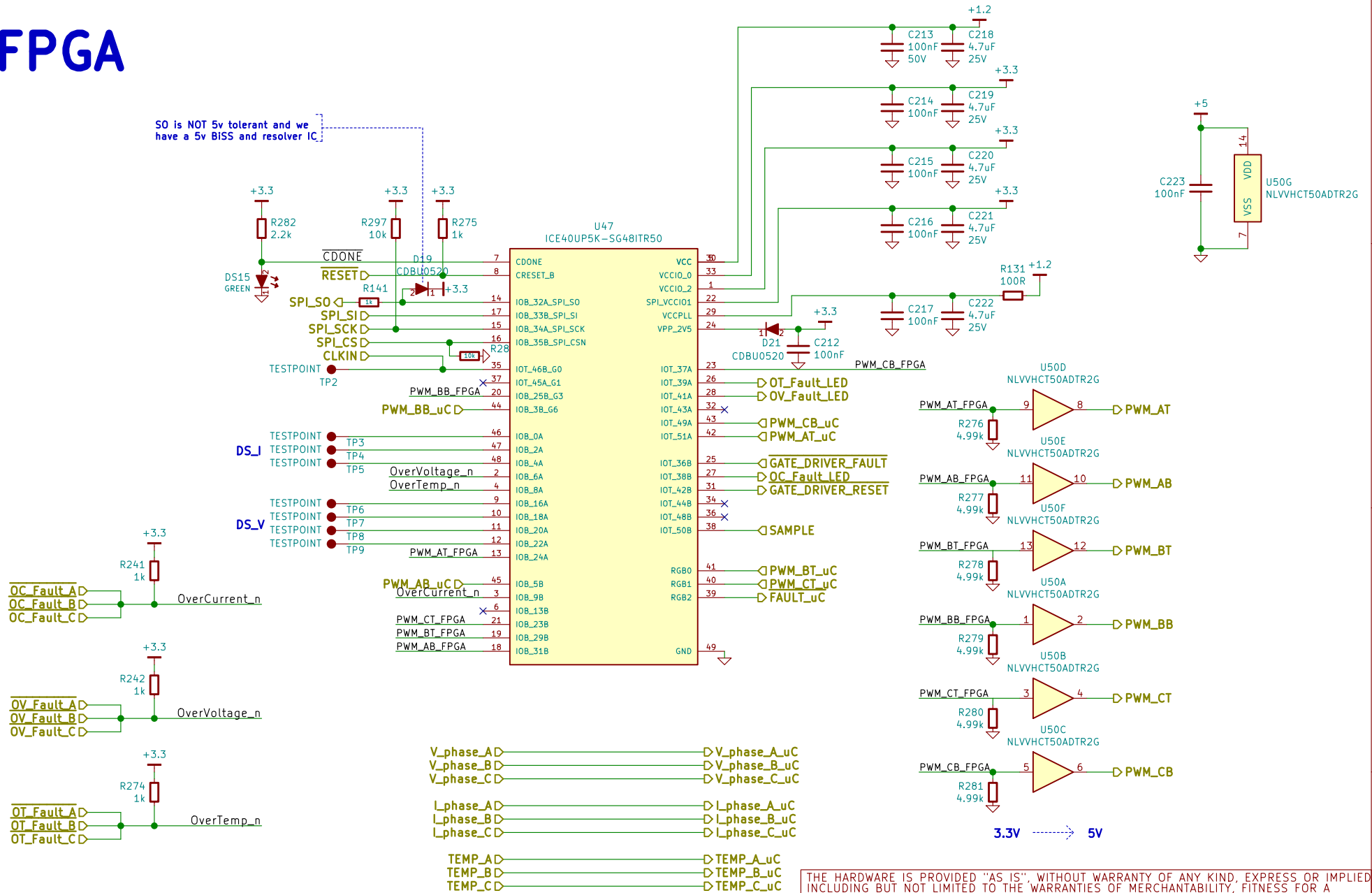


C

D

FPGA

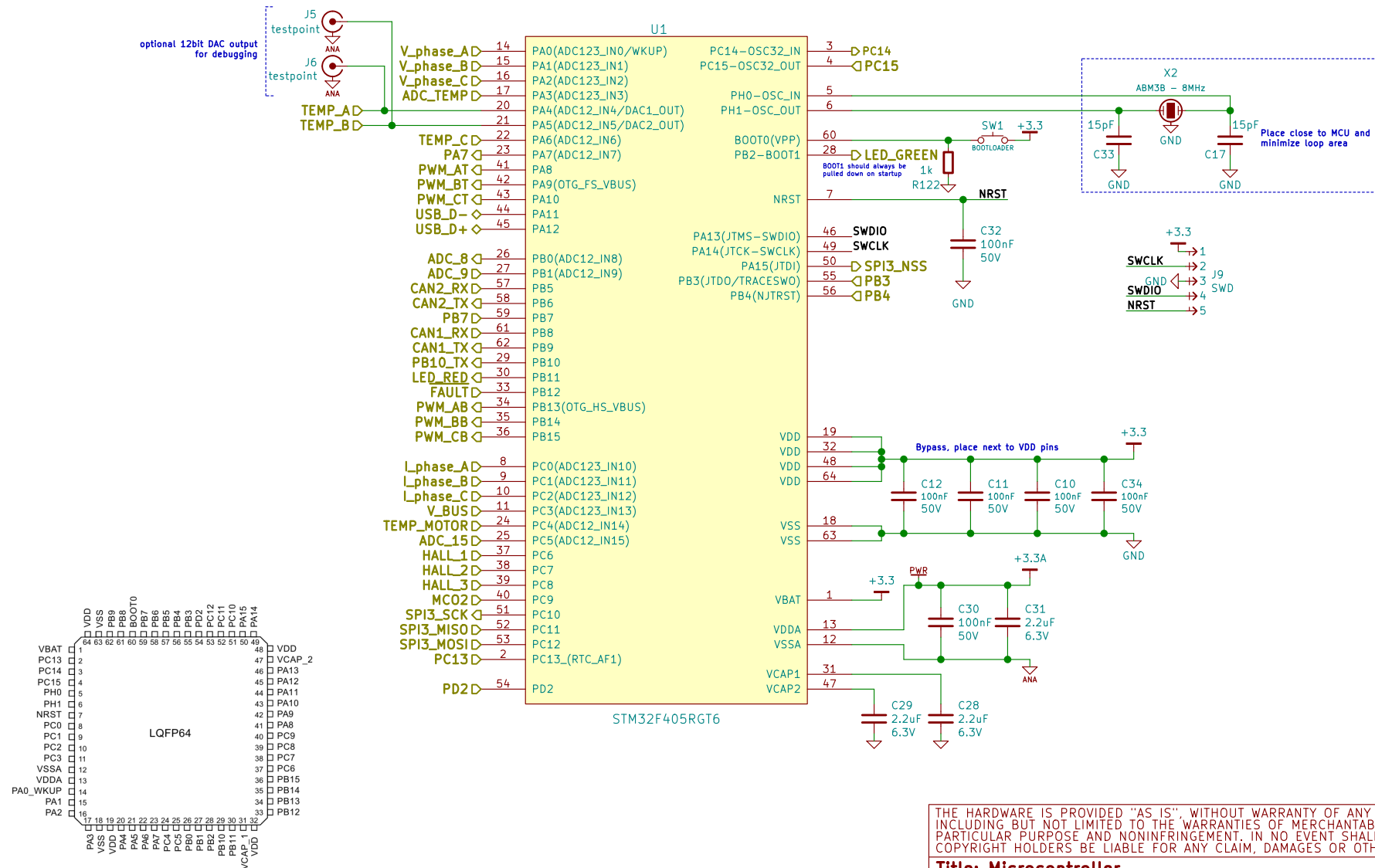
SO is NOT 5v tolerant and we have a 5v BiSS and resolver IC



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Title: FPGA supervisor	Rev: 1
Sheet: /Supervisor v2.0/	Id: 25/34
PowerDesigns.ca - CC-BY-SA	Date: 2019-08-15

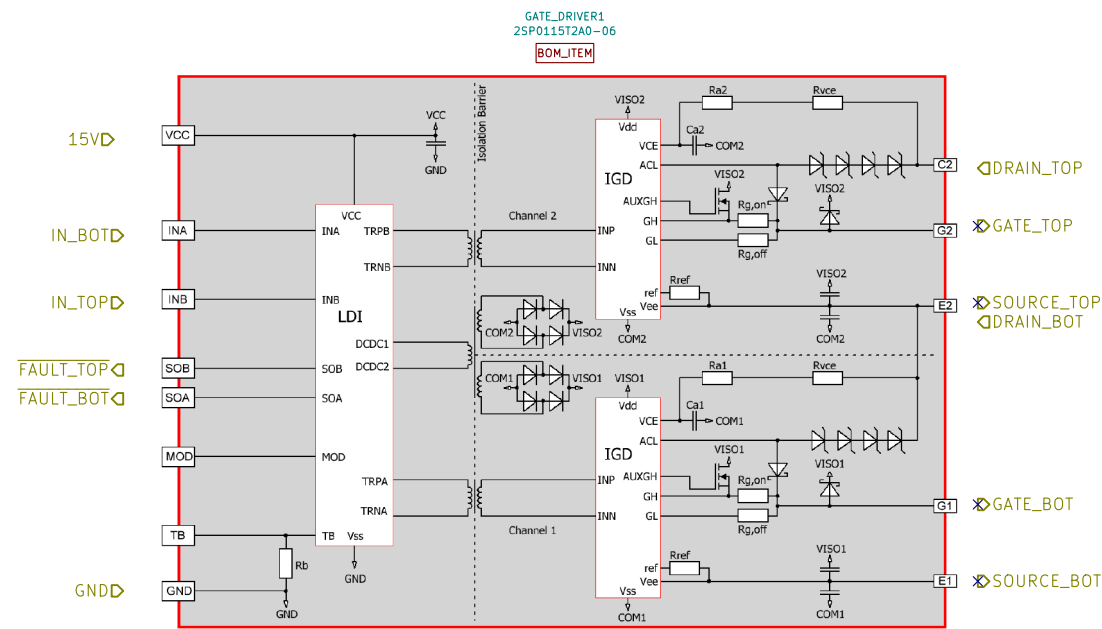
STM32F405 MCU



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Title: Microcontroller	Rev: 1
Sheet: /STM32F4/	Id: 26/34
PowerDesigns.ca - CC-BY-SA	Date: 2019-08-15

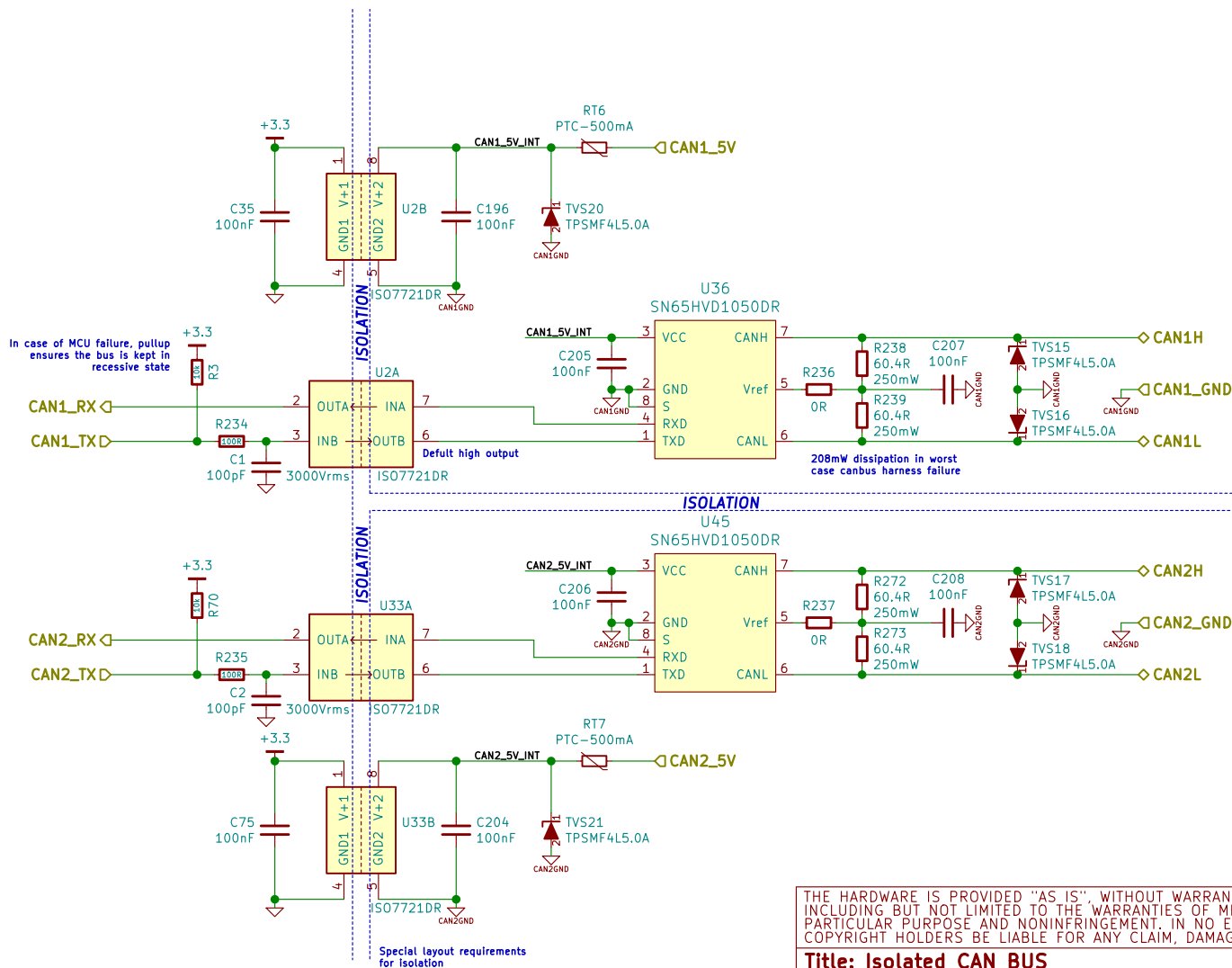
GATE DRIVER



External to control board

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Title: Gate driver	Rev: 1
Sheet: /Gate driver A/	Id: 28/34
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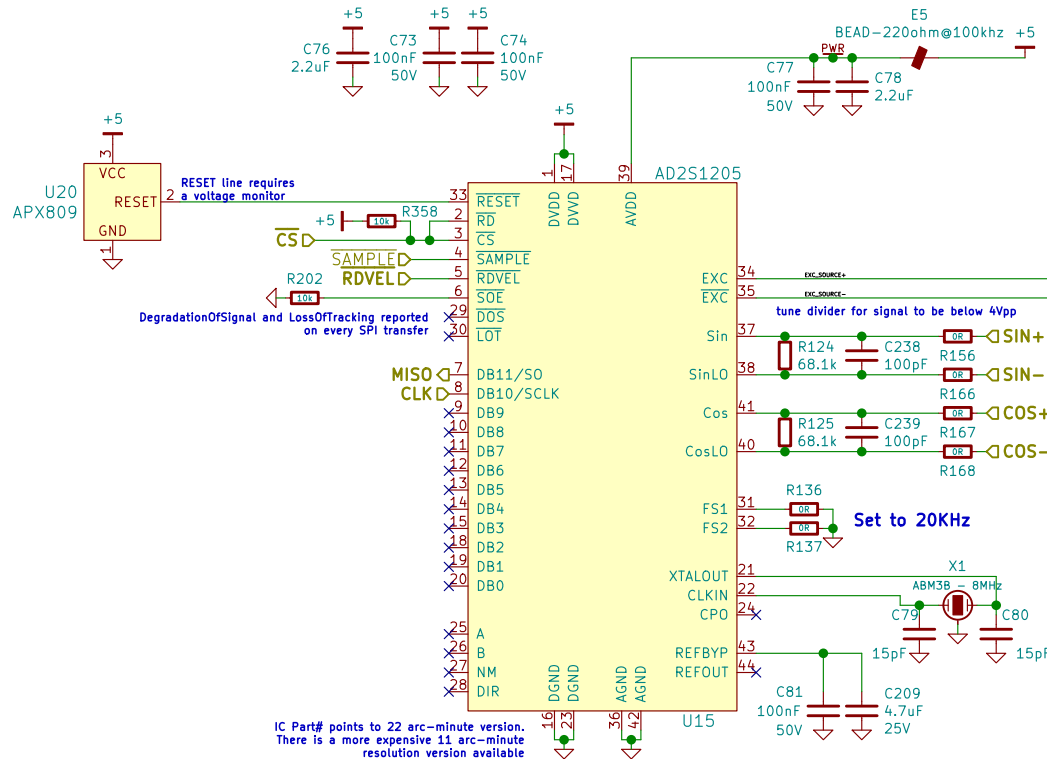
REDUNDANT ISOLATED CAN BUS TRANSCEIVER



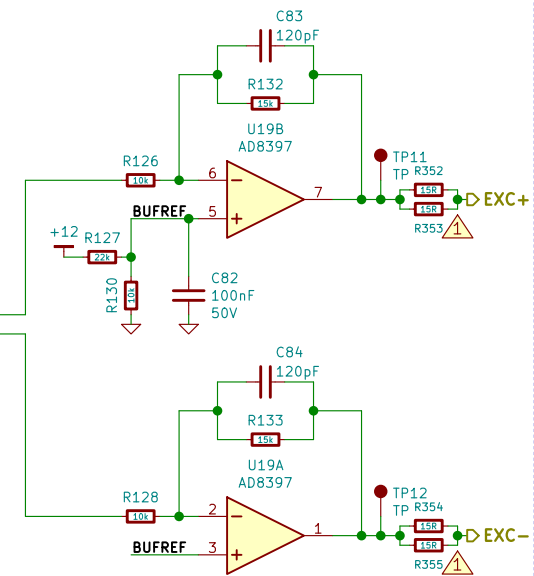
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Title: Isolated CAN BUS	Rev: 1
Sheet: /Isolated CAN/	Id: 29/34
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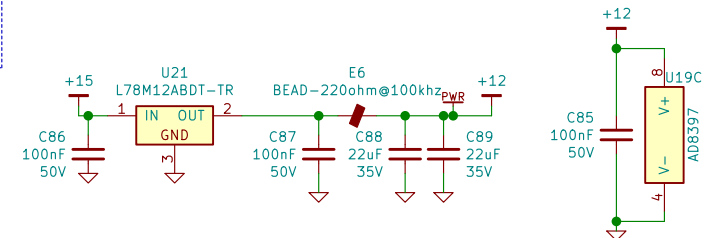
Resolver interface



Buffer



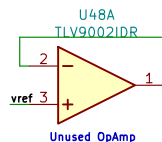
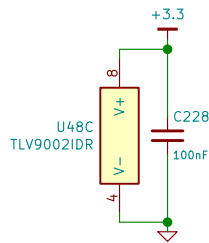
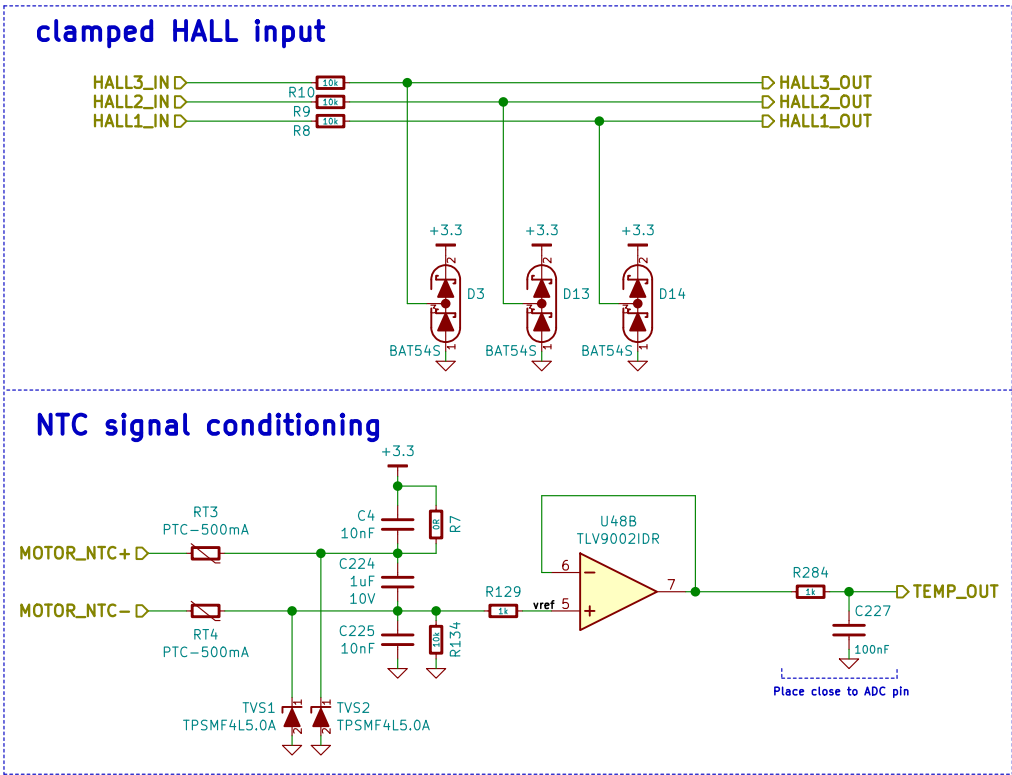
This is an alternative buffer suggested here:
<http://www.analog.com/en/analog-dialogue/articles/precision-rtdc-measures-angular-position-and-velocity.html>
 Its more expensive, but much simpler and smaller



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Title: Resolver	Rev: 1
Sheet: /resolver/	Id: 30/34
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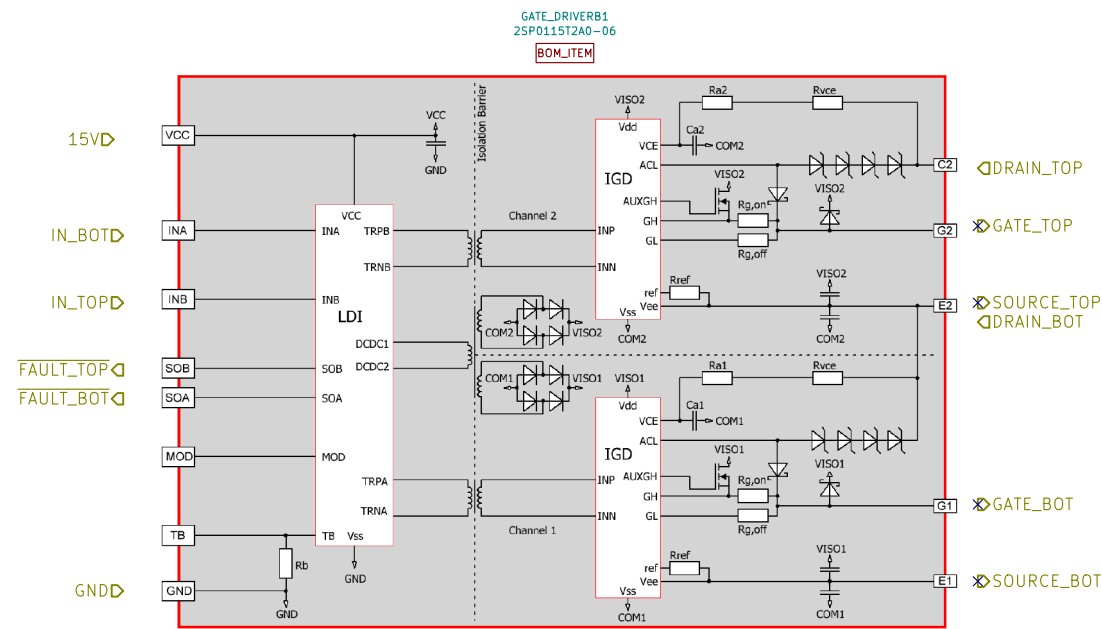
HALL position input and motor temp sensor



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Title: Hall sensor and motor temperature	Rev: 1
Sheet: /Filters/	Id: 31/34
PowerDesigns.ca - CC-BY-SA	Date: 2019-08-15

GATE DRIVER



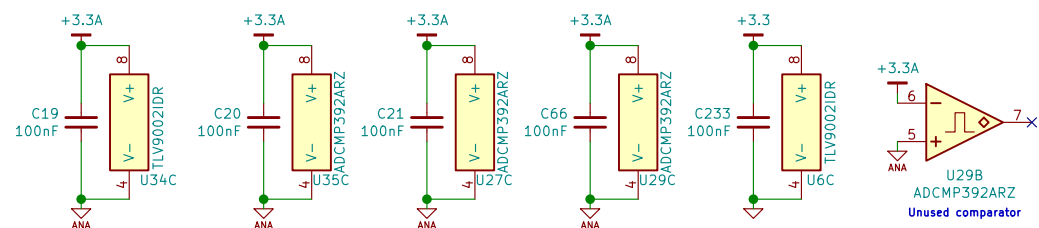
External to control board

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Title: Gate driver	Rev: 1
Sheet: /Gate driver B/	Id: 32/34
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D



Title: Gate driver	Rev: 1
Sheet: /Gate driver C/	Id: 33/34
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Title: Spares	Rev: 1
Sheet: /spares/	Id: 34/34
PowerDesigns.ca - CC-BY-SA	Date: 2019-08-15