

Fadi Katto

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Quartus Prime Lite Edition - C:/Users/Fadi/Desktop/Lab 3/Lab3 - Voltmeter

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Project Navigator | Files

Files

- voltage2distance.vhd
- binary_bcd.vhd
- SevenSegment_decoder.vhd
- SevenSegment.vhd
- Voltmeter_tb.vhd
- averager.vhd
- DE10_LITE.qsf
- DE10_LITE.sdc
- adc_qsys/synthesis/adc_qsys.qip
- voltmeter.vhd
- mux2to1.vhd
- mux2to1_tb.vhd
- multiple_registers.vhd
- stp1.stp
- averager_multiple.vhd

Tasks

Compilation

Task

- Compile Design
- Analysis & Synthesis
- Edit Settings
- View Report
- Analysis & Elaboration
- Partition Merge
- Netlist Viewers
- RTL Viewer
- State Machine Viewer

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Slow 1200mV 85C Model Fmax Summary

| | Fmax | Restricted Fmax | Clock Name | Note |
|---|------------|-----------------|---|------|
| 1 | 68.2 MHz | 68.2 MHz | clk | |
| 2 | 75.36 MHz | 75.36 MHz | altera_reserved_tck | |
| 3 | 163.69 MHz | 163.69 MHz | ADC_Conversion_ins[u0]altpll_sys[sd1]pll7[clk0] | |

This panel reports FMAX for every clock in the design, regardless of the user-specified clock periods. FMAX is only computed for paths where the source and destination registers or ports are driven by the same clock. Paths of different clocks, including generated clocks, are ignored. For paths between a clock and its inversion, FMAX is computed as if the rising and falling edges are scaled along with FMAX, such that the duty cycle (in terms of a percentage) is maintained. Altera recommends that you always use clock constraints and other slack reports for sign-off analysis.

Messages

System (74) Processing (274)

Type ID Message

- 332102 Design is not fully constrained for hold requirements
- Quartus Prime Timing Analyzer was successful. 0 errors, 136 warnings
- 293000 Quartus Prime Full compilation was successful. 0 errors, 438 warnings



