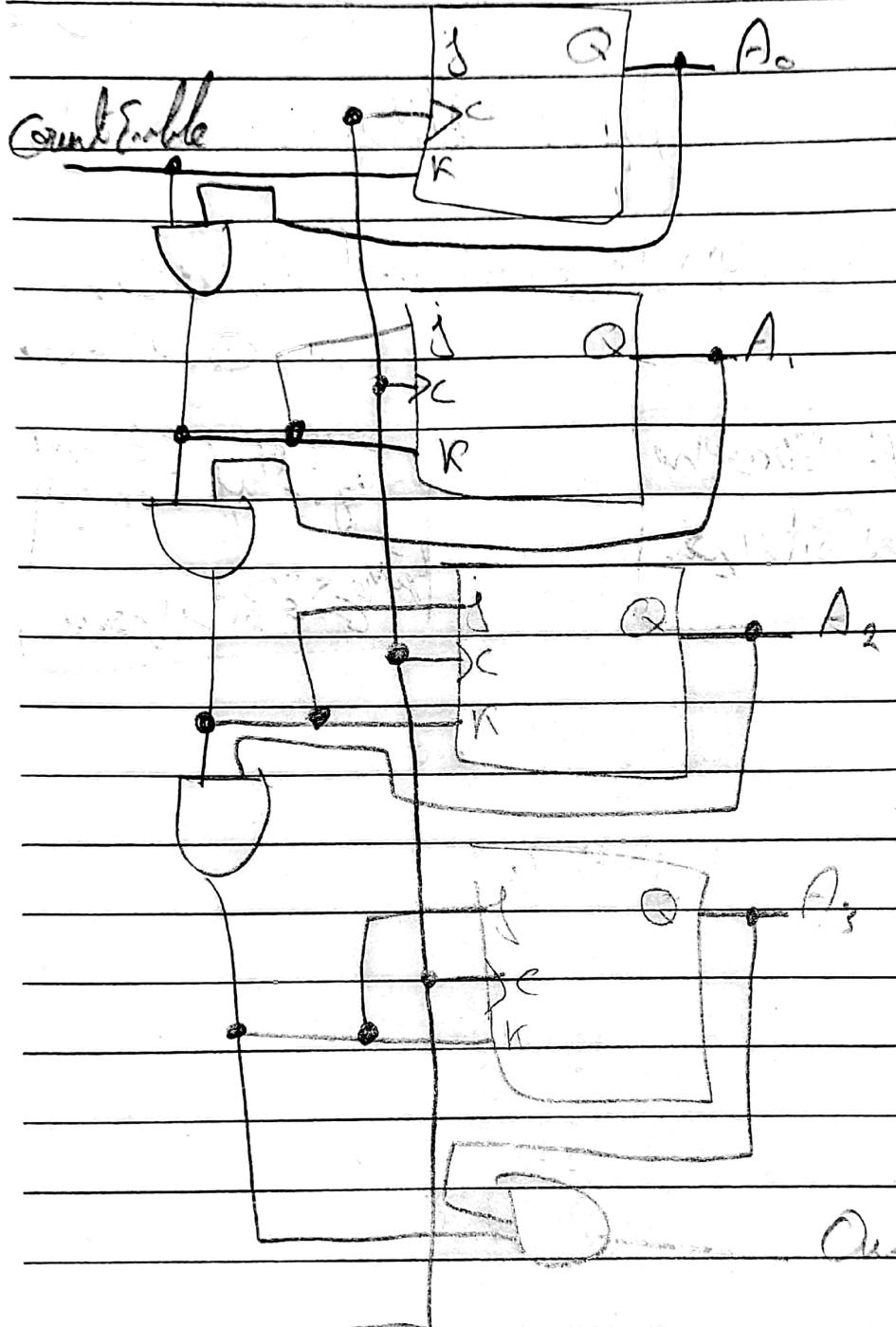


Binary Counter

PAGE

DATE



clock

27/9/2021 Register || jk(11) Value || clock Pulse J5

$A_3 \quad A_2 \quad A_1 \quad A_0$

0

0

0

0

 $\} + 1$

0

0

0

 $\} + 1$

0

0

1

 $\} + 1$

0

0

1

 $\} + 1$

0

1

0

 $\} + 1$

0

1

0

 $\} + 1$

0

1

1

 $\} + 1$

1

0

0

 $\} + 1$

1

0

0

 $\} + 1$

1

0

1

 $\} + 1$

1

1

0

 $\} + 1$

1

1

1

 $\} + 1$

single words + 1 Row 3
 (Left side Binary adding) over all Row II

$$0+0=0$$

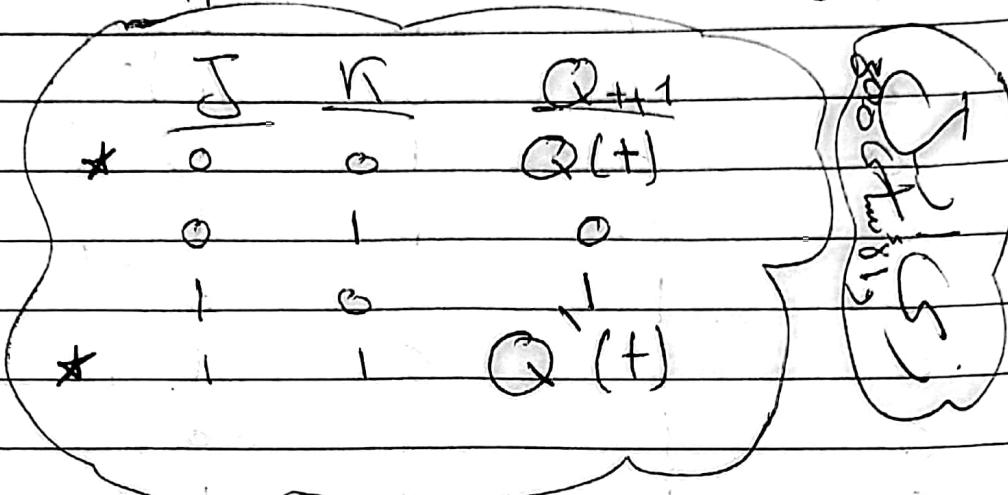
$$1+0=1$$

$$0+1=1$$

$$1+1=0, \text{ carry } 1$$

flip flop

~~JK flip flop also called Register J1~~



Count Enable →

(zero →)

~~flip flop~~ → Register J1

(one →)

→ Value J1

~~Count Enable~~ →

J, K J1 فتحة 2 بit و JK J1 فتحة 1 bit و J, K, Enable J1
 لـ J1 لـ K1 complement نـ J1 و Q1 فـ 2 بـ 1 و J1 فـ 1 و K1 فـ 1
 لـ K1 لـ J1 complement لـ K1 new Bit J1 ← Rule 1st
 لـ J1 Bit 1 Comp. J1 فـ 1 1/2 Bit 1st ←
 2 بـ 1 فـ 1 و 2 بـ 1

~~Saljiji And Gates~~

~~Lis Al Tisw Rib~~

يتولى برج الالى قوى و one Bit لـ complement

one Bit لـ Complement one Bit لـ comp

one Bit لـ Complement one Bit لـ comp

one Bit لـ Complement one Bit لـ comp

clock Pulse و ترتيب 1 1 1 1 1 العداد يزيد و ترتيب الاولى

4 Bit - Binary Counter with Parallel load

الجامعة الإسلامية

Chair

Synchronous

جيكل جي جي
clock جي
جي جي

Synchronous

recieve trans
clock Pulse gives

one year old 16

جی و ٹیکلک پالک ۱۱ جیسے
جی ۱۰۲۳ جیسے

load Value) \Rightarrow 1-0 Da \Rightarrow clockpulse (لـ 1 يـ 0 one \Rightarrow 1-0
1, 5d, I, spis A, 11g I o j i اسـ

Increment (clockPulse) (أي كإيج one لوكارن ~~فوق~~ ~~فوق~~)
Register (Value) (فترة وفترة)

	clock	Clear	load	Increment	operation
1	↑	0	0	0	No change
2	1	0	0	1	مخرج دخل
3	↑	0	1	X	مخرج زéro A
4	↑	1	X	X	مخرج العداد
Row 1		Clear = 0, load = 0, Increment = 0			
				No change	

[Row 2] Clear = 0, Load = 0, Increment = 1
Digital Counter 112910

Row 3 Clearo, load-~~at~~, Inc ~~OpCo~~
And ~~OpCo~~ In

الرابع (أ) و (ب) إلى كل من
غيرهوا على أن (ج) And P which
في الرابعة (ج) And P which
وتابع (أ) و (ب) إلى كل من
ورابع And إلى جايند 1 و ت (ج) And 1
(ج) And 1 و ت (ج) And 1
الرابع (أ) و (ب) إلى كل من

$$\Rightarrow (\text{I or zero}) = \underline{\underline{\text{I}}}$$

$$k \Rightarrow (I' \text{ or zero}) = I'$$

لـ الـ π وـ τ مـ خـ تـ فـ يـ اـ دـ اـ عـ لـ اـ لـ π مـ بـ حـ يـ زـ يـ اـ لـ τ الـ π الـ τ مـ بـ حـ يـ زـ يـ اـ لـ π مـ بـ حـ يـ زـ يـ اـ لـ τ

(Row 4) clear = 1, load = X, inc = X

كتاب العداد و الحساب

RAM

Random Access Memory

Data input
lines

Address lines

Read

Write

Memory Unit

2^k words

n bits per word

Data output

lines

Memory (Space) \Rightarrow Bytes \rightarrow

Words \Rightarrow (5, Words) Bytes

is مثلاً ٥ بوكس (bits) by word

is ١ بوكس (bit) ~~is ١ بوكس~~ \Rightarrow ١ Word

(one byte) \Rightarrow ١ Byte Value

Memory \Rightarrow Sequence of Words

16 bit \Leftarrow 2 bytes

32 bit \Leftarrow 4 bytes

give arch

jy31

32 bit

(ex) 2 bytes 16Bit = 8 bits

$$16\text{ Bit} = 2 \times 8$$

لذا كل بyte يحتوى على 8 Bits

فأنا 16Bit = 2 \times 8 bits Integer

Address 8 Bits
Memory 8 Bits

32 Bits Plus 16 Bits \rightarrow 48 Bits

Word

Value

Memory

Address

Word

Bits 32

Read

\rightarrow Value (one byte)

Memory in Word

Write

\rightarrow active Value (one byte)

Memory of Word

Address lines

Address \rightarrow 16 Bits

Will one up to (1) Write is Read is 1 bit
Zero

Input lines (Bit) Scaniahic پرلے
جس کی اس نے اس کا مارے Value باز کر Word کے

clock Pulse کے

سینے address لیں کرے Word اٹھے Value کے
Write لے کرے کے Bits کے Input کے Pulse

address لے کرے و خانے
Clock Input Address کے دیجی C = Write, R = Read
Read کے کرے Word کے Bits کے outPut
lines

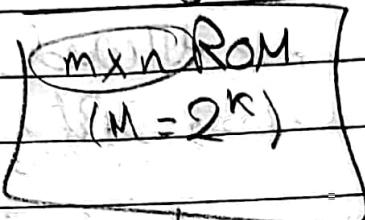
= Crie Word
2 Address lines

Address lines R
2 Word

~~RAM~~

Read Only Memory

Address lines



Data Out Put lines

Read Address is given to RAM
Word value is read from RAM
Word size of RAM
is 32 bits

(32 Bits) / 8 = Word of 16 bits (size)

$$\cancel{2^k} \times \cancel{2^k} = \cancel{2^{2k}} = 2^{16}$$

$$\therefore k = 4, 2^4 = 16 \text{ (Word address lines)}$$

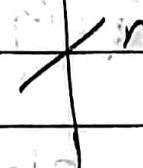
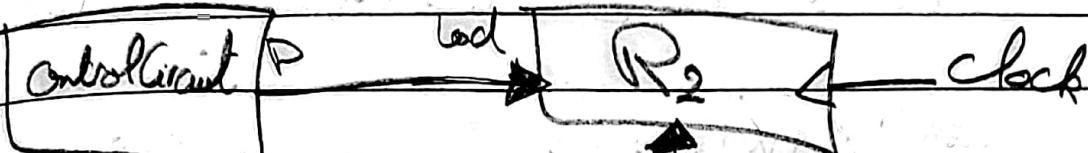
Inputs: Enable (1), Address (16)
lines

Output: Word (as 16 Bits) / Real

Register Transfer

language

Block Diagram (Transfer data from R_1 to R_2 When $P=1$)



R_1

Register \rightarrow Register \rightarrow Data Jis



$R_2 \rightarrow R_1$ no Data going one side - P 111

Dest. \leftarrow Source

~~P~~ \rightarrow Control Input

~~JL~~ \rightarrow (R1 output) \rightarrow ~~JL~~ -
R2 \rightarrow input ~~Q~~

~~n~~ \rightarrow ~~(R1 output)~~, ~~(JL output)~~ -

~~D~~ \rightarrow ~~(R1 output)~~ \rightarrow ~~Q~~ \rightarrow R2 \rightarrow n inputs -
جاتع (الباقي)

(n-bits) \rightarrow n-Flipflops \rightarrow Reg 15

~~output~~ \rightarrow input \rightarrow ~~Q~~ \rightarrow ~~Q~~ -
F. S. 1 \rightarrow F. L. (Many wires) \rightarrow n -

control circuit load is R_{23}

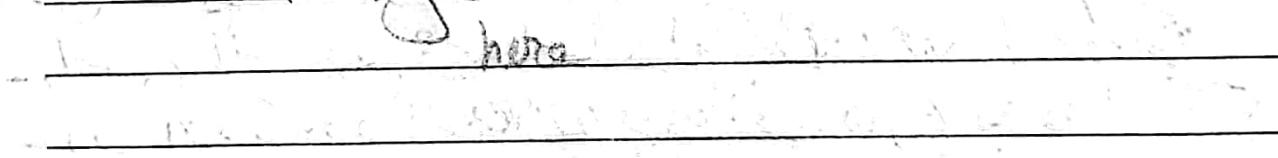
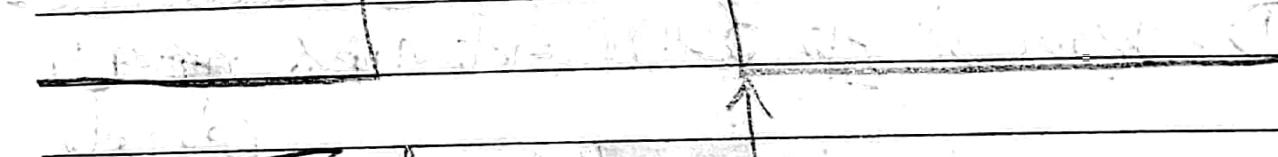
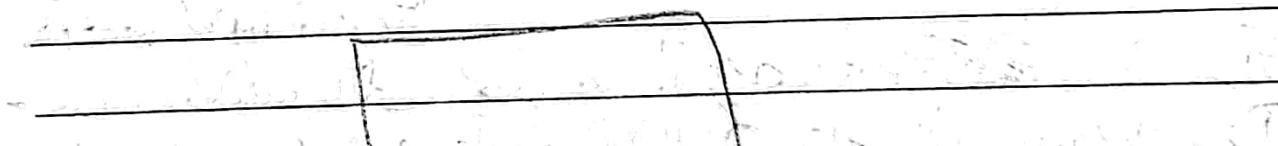
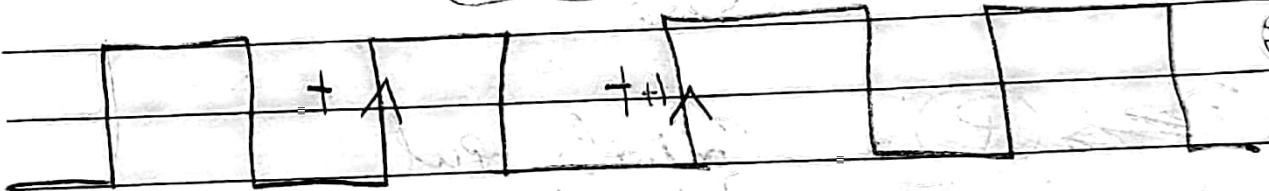
ne) P_{21} (control input) \rightarrow set J_2

~~$P_2 \rightarrow$ load (will be zero in J_2 state)~~
 ~~R_{23} load input will be P_{21} is zero? Control~~

~~R_{23} (0.300 - gen load) is zero, P_{21} is 1
 Load Transfer وفایر R_{23} (data) is 1~~

~~if one (gen load) \rightarrow Gen P_{21} , if
 R_{23} (0.1 Value) \rightarrow R_{23} clock pulse~~

timing diagram



load) || (3V battery one) 300 mW || few control circuit))

~~Alveolar sub R₁ and ~~the~~, one (one)~~

العنود

clock \rightarrow a big
cycle

~~darkcycle only zone) dog (size, ~~bad~~)~~

الله اعلم بـ نحو و نحو Réécycles

القدسيّة بناءً على (١٠٠)

~~load) (reg' -> R₂) (lbusig (11 clock cycle) -> bus~~

العنصر الرابع هو R_1 و R_2 وهو يخزن رقمين في كل دورة (cycle) في寄存器 (Registers) ~~أو寄存器~~ ~~أو寄存器~~

R, Jízepi, Rz

görs, cycles (1) \rightarrow jöapti (control circuit)
görs, (1) cycle, cycles (1)

Bus

Register D

D₃ D₂
1 0
D₁ D₀C₃ C₂
1 0
C₁ C₀

Register C

A₃
1 0
A₂A₂
1 0
A₁

Register B

B₃ B₂
1 0
B₁ B₀

Register A

A₃
1 0
A₂4 line
common
bus

Buy

PAGE _____
DATE _____

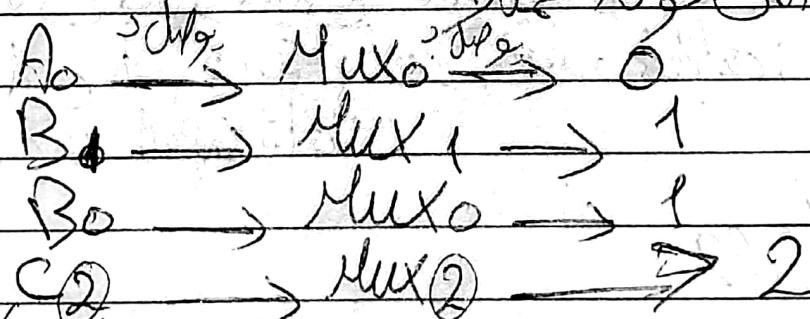
Conventional Source Register (جهاز المصدر)
Input / Output Register (جهاز إدخال وExit) Destination Register (جهاز الوجهة)
Multiplexer (جهاز التحويل) Dest. (وجهة) Input (إدخال)

The Mix (جهاز التحويل) is F.F = 15.
With Address A.B.C.D, it has 16 MUXes
~~But it has 3 bits of address~~ (But it has 4 bits of address)
RD 3 Bit (3)

Selectors (جهاز اختيار) to Mix

Decimal	S ₁	S ₀	Reg
0	0	0	A
1	0	1	B
2	1	0	C
3	1	1	D

Output 3 (Registers A, B, C, D) to Mix
Choosing one of four outputs based on the address number
The output of the multiplexer to the destination register



T Bay

PAGE

DATE

cycle

~~stop clock~~ also 812

~~UIC (Registers) load is, so, set to 0, 1, 0, 1, 0, 1, 0, 1~~

~~Dots) (سی جوں Reg. تکمیل (ج) کلکٹ پلیس (جی) لے جائیں~~

لوكاينز افلاك لـ Reg لـ lines | zip لـ ziped lines |
بتوجReg نوبلج بالـ input (Reg) وـ لـ input (Reg)
باتجـ one وـ last بـ one (Reg) زانـ باـ

~~طب لو عايز أقول رج 2 Reg 11 blood كل يوم اول رج 2 Reg one~~

ملحق لوگوی ایندکس (Index Register) و سرچ سرچ (Search Register) را در ذخیره سازی (Memory) نمایش داده ایم.

~~Scal class~~ - source Reg-11

algos () و نیز الی Bay یا outputs زیرا

Dest Reg. \leftarrow sum of inputs + (Reg 1) Reg 1.

، Max Inputs of Source جايزات

Light, sleek, comfortable and best for jobs.

~~Our inputs are~~

~~July 2022~~