

# Stored Programs

Memory  $\rightarrow$  Sequence of Words  
 Data  $\downarrow$   $i_0 i_1 i_2 \dots i_n$

1 Word  $\rightarrow$  Memory has words up to

~~first Data, Data, Integer, floating point words~~  
 Binary Operands

~~Input Memory, integer, Data, CIP, Address, Registers, Memory~~  
 Operation parts ~~Labels, Address, Registers, Memory~~  
 Instructions

~~First 11 bits of sequence of instructions~~  
 11 bits of instruction  $\rightarrow$  Program  
~~Size of instruction~~  $\rightarrow$  ~~Size of memory~~

~~Size of = Size of Instruction~~  $\rightarrow$  ~~Size of~~ Word

Instruction (Program)	Memory
	6096 $\times$ 16
Operands	Words
Data	Bits
	Address of each word:
	0 $\rightarrow$ 6095

~~Hot Addresses - Hot Words~~  
but

Max Address Number = (Word Words - 1)

-: Example

لهم ما هي الـ Word (Word) أو الـ Variable (Variable). Array هي Address التي تشير إلى

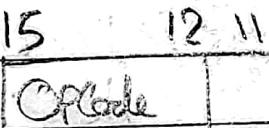
19

$$9 = 4096$$

$\text{O} \rightarrow 6095 \text{ مللي ارتكام} \rightarrow \text{III} \rightarrow \text{B} \rightarrow 128.61 \text{ دوال}$

~~Address 19 Memory 18 Word 1~~ ~~Memory 19~~ ~~Memory 18~~ ~~Memory 17~~

IS Data // is Memory // is Instructions // is CPU



Productive forecast

~~Operation 11 is now completed~~ 16 Bif gen  
~~labeled as completed~~

GBits

OpCode (Bit 15 ← Bit 12)  $\Rightarrow$  Operation

~~GRTS~~ → PDU Operations [2] 1 day

جزوی از اسناد مذکور در اینجا آمده است

العنوان هو المدخلات لـ Address Register، وهو المسند إلى Register Address.

ex:  $AC \leftarrow AC + B$

15                          21                          0

OPCode of Add | Address of B

العنوان هو المدخلات لـ Address Register.

Processor Register  
(Accumulator or AC)

العنوان هو المدخلات لـ Address Register.

Accumulator (Processor Register) of AC

العنوان هو المدخلات لـ Address Register.

Word B of Current Operand

العنوان هو المدخلات لـ Address Register.

15 ← 0 we Represent

15

Binary Operand

# Addressing Modes

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DATE \_\_\_\_\_

Instruction Address Format

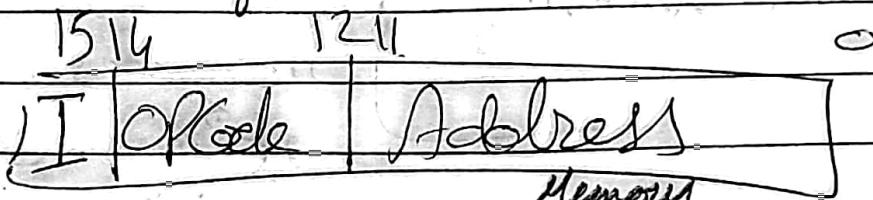
12 Bits for Address ( $0 \rightarrow 11$ )

→ Words  $\downarrow$   
Memory

3 Bits (3<sup>3</sup>) is OPCode (12 → 14)  
2<sup>3</sup> op codes is used ( $12 \rightarrow 14$ ) 4<sup>3</sup>

①

D15 → Bit 14



Effective  
Address

457 Operand

[Ar]

→ Read Access

# Addressing Codes

Indication of Address Format

12 Bits for Address ( $0 \rightarrow 11$ )

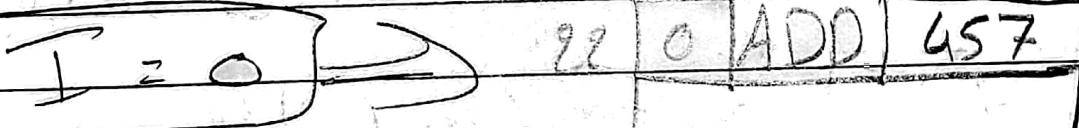
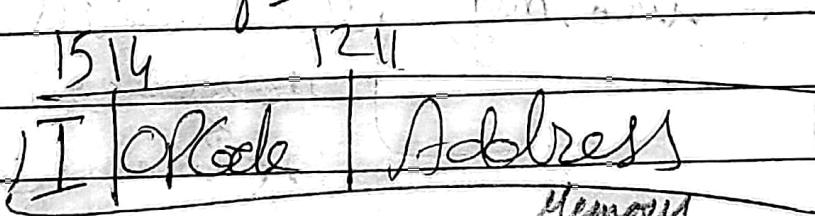
Words  $\rightarrow$  Memory

3 Bits ( $0^1 \rightarrow 0^3$ ) of OPCode

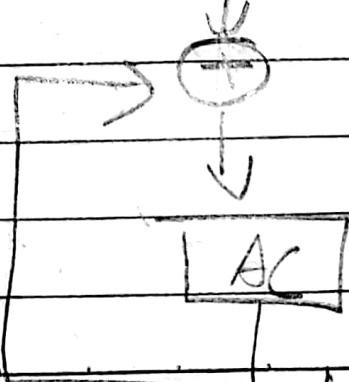
Address  $2^3$  opn  $\rightarrow$  5 bits ( $12 \rightarrow 17$ )  $4^2$

①

D15 is Bit 17



Effective  
Address



Direct Access

## Direct Address

PAGE

DATE

$I = 0 \rightarrow$  22 ipsis Address // Instruct  
Add Direct Address OpCode //  
457 ipsis Address //

~~22 ipsis Address // Instruct  
OpCode // 457 ipsis Address //~~

~~22 ipsis Address // Value // 457 ipsis Address //~~

~~22 ipsis Address // Value // 457 ipsis Address //~~

$I = 1 \rightarrow$  Indirect Addressing  
35 ipsis Address // Instruct  
Add Direct OpCode //

~~300 ipsis Address // Instruct  
Address (300) is 300  
300 ipsis Address // 300 + 350  
operand // 300 ipsis Address //~~

~~300 ipsis Address // Instruct  
300 ipsis Address // 300 + 350  
operand // 300 ipsis Address //~~

# Memory

$I = 17$

1 ADD 300

## Indirect Addressing

Addr.  $\rightarrow$  لِجُسْلَه < 300

1350

لِجُسْلَه  $\rightarrow$  بَاعِدُ الْأَوْلَى

الْأَدْرَسُ لِلْأَوْلَى

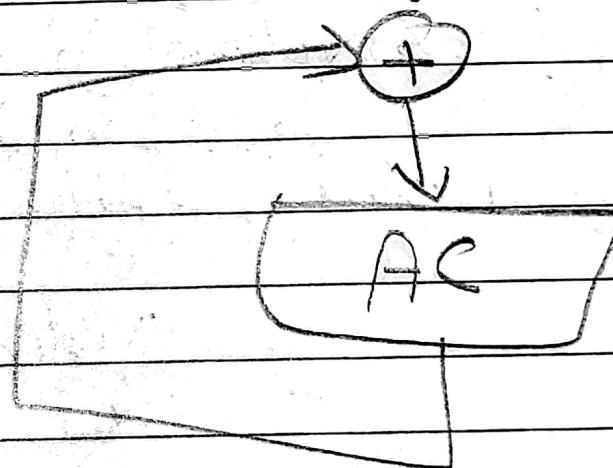
(300) لِلْأَدْرَسِي (1350) < 1350

Operand

الْأَدْرَسُ لِلْأَوْلَى

لِلْأَوْلَى

1350  $\rightarrow$  Effective  
Address



الْأَدْرَسُ لِلْأَوْلَى  $\rightarrow$  دُرْسُ الْأَوْلَى  
AC  $\rightarrow$  دُرْسُ الْأَوْلَى

Effective Address  $\rightarrow$  Address of Operand

Indirect Addressing  $\rightarrow$  سُوكِيْسِوك

loop Addressing Arrays  $\rightarrow$  مُنْتَهِيَّةِ الْأَيْمَانِ الْأَنْتَارِيُّونِيِّونِ

$$\begin{aligned} AC &\leftarrow AC + A_1 \\ AC &\leftarrow AC + A_2 \\ AC &\leftarrow AC + A_3 \end{aligned}$$

Instruction Addressing  $\rightarrow$  Direct  $\rightarrow$  Instruction Addressing  $\rightarrow$  Word Operation  
Instruction Addressing  $\rightarrow$  Word Operation  
Instruction Addressing  $\rightarrow$  Iteration

- Address  $\rightarrow$  element  $\rightarrow$  Indirect

Instruction  $\rightarrow$  Address  $\rightarrow$  Address  $\rightarrow$  Address  $\rightarrow$  Address

-  $\rightarrow$  Instruction

memory  $\rightarrow$  change  $\rightarrow$  address  $\rightarrow$  memory

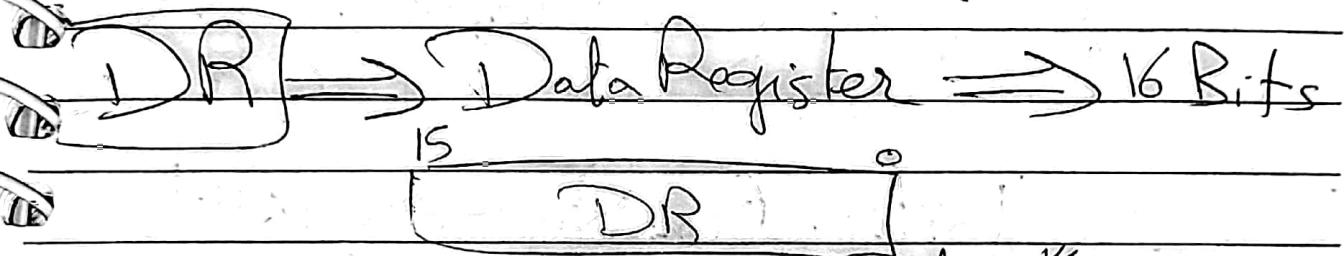
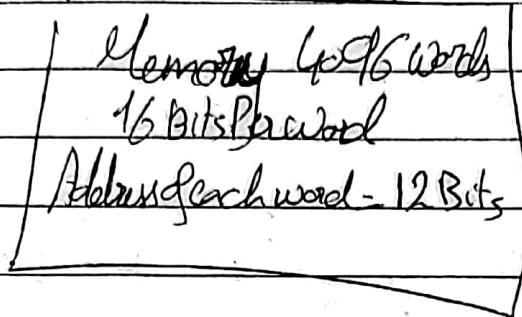
Memory  $\rightarrow$  Address  $\rightarrow$  Address

Address  $\rightarrow$  Address  $\rightarrow$  Address

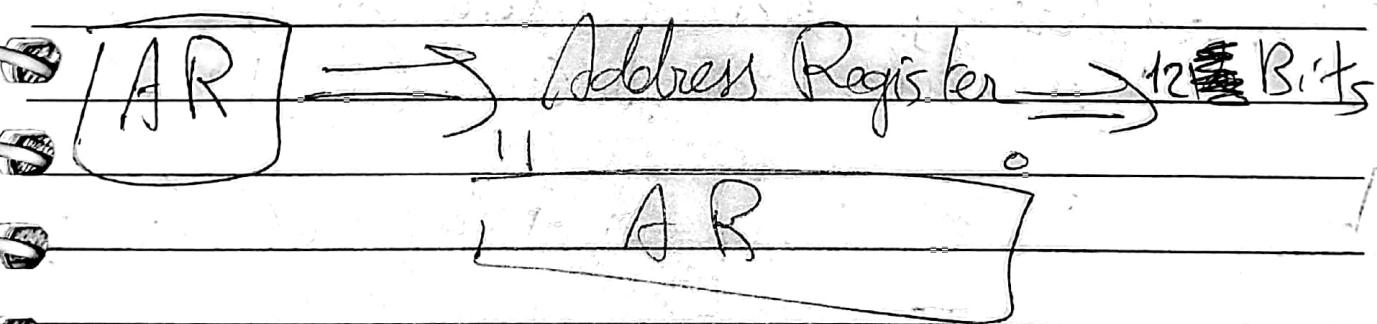
Address  $\rightarrow$  Address  $\rightarrow$  Address

Symbol  $\rightarrow$  12 Bits

# Basic Computer Registers



Word 11 of one Integer is Data 16 bits  
Memory operand 9 bits operand Integer address  
operation code (Memory) 1 word 16 bits



Memory word config is Memory Address 12 bits  
Address 12 bits → Memory Address 12 bits  
Memory 12 bits → Memory 12 bits  
Address 12 bits → 12 Bits per word 2<sup>12</sup> bits

Writing Memory → Input Address 12 bits →  
next to one word copy

15



AC  $\rightarrow$  Accumulator Reg  $\Rightarrow$  16 Bits

~~Accumulator, weight, X register, DR 16 bits~~

IR  $\rightarrow$  Instruction Reg  $\Rightarrow$  16 Bits



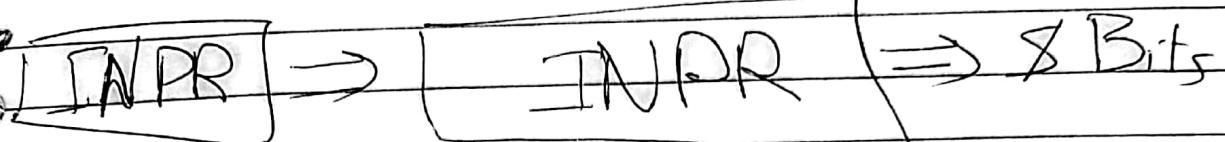
1. IOP(Instruction Address), all 16 bits. Instruction Address  
~~(Instruction Address)~~ Circuit Selection

PC  $\rightarrow$  PC  $\rightarrow$  Program Counter  $\Rightarrow$  12 Bits

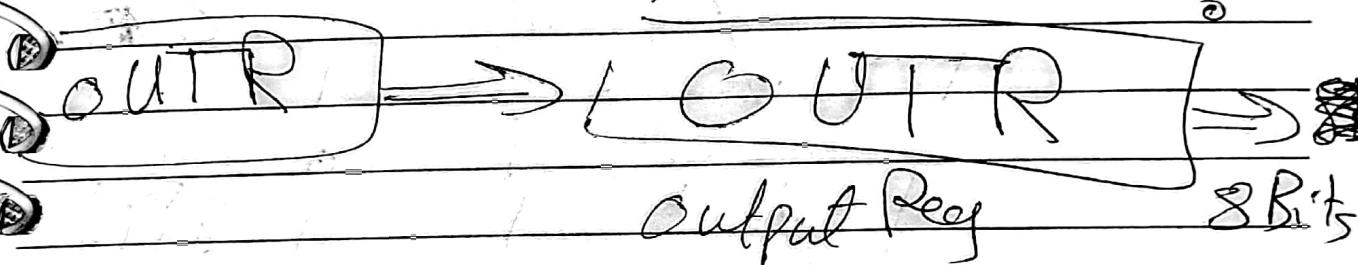
~~DR 16 bits (Instruction) Address  $\Rightarrow$  12 bits~~  
~~DR 16 bits (Instruction) Address  $\Rightarrow$  12 bits~~

TR  $\rightarrow$  TR  $\rightarrow$  Temporary Reg 16 Bits

~~Temporary Register~~ Temporary Data 16 Bits



Keyboard via ALP Input line  
Input Reg  
Character



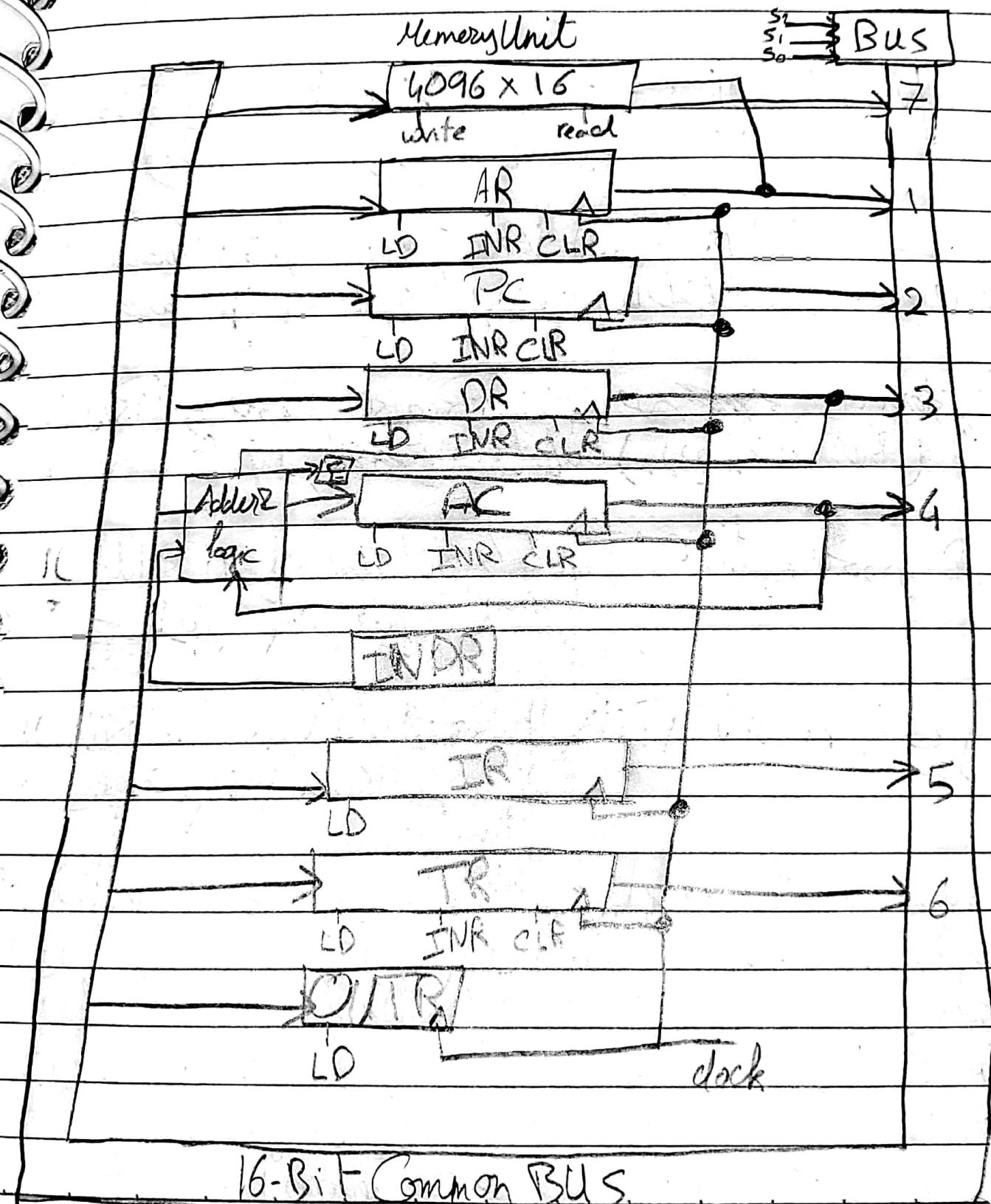
Output Reg

De Quedo in Output Character  
Terminal via Screen

BUS SYSTEM

## Common Bus System

Registers  $\rightarrow$  (B like, C like) Registers  $\rightarrow$  (D like)  
Registers  $\rightarrow$  (A like)



16-Bit Common BUS

Registers are Register like Memory but  
 16 Bits Output (which is BUs) is connected  
 (bus) word to memory Address  
 output of reg = Storage of Reg

16 Bits word, Registers are 16 Bits word  
~~16 bits word~~

~~Registers are like Memory 16 Bit Word, Memory is  
 BUs, its like output bus, Input is like Address~~

Registers are ~~like~~ Registers like BUs  
 (BUs is like bus) output is ~~like~~ Input is ~~like~~

~~Registers are like Memory 16 Bit Word, Memory is  
 BUs, its like output bus, Input is like Address~~

Registers are 16 Bits like Memory like BUs  
 16 Bits like Memory like BUs

Bus output is 6 Regs (like ~~like~~ like  
 of like Memory) (like ~~like~~ like BUs) like  
 like ~~like~~ BUs Input & output like  
 like 2<sup>3</sup> = 8 like 8 like 3 like 3 like 3 like  
 like 1 → 6 like 3 like 1 like 1 like 1 like  
 like Memory like 16 Bit ALU like Memory like  
 like 7 like  
 like 16 Bits like 16 Bits like 16 Bits like  
 like 16 Bits like 16 Bits like 16 Bits like

is 16 bits (Bus) to Bus  
Req is N Bits

Inputs 15 - 2, 10 Input 1, 10 Bits  
Req are multiplexed

Selection

2 bits Cn 2 bits Pn Selection

Mux Regs select from Register

#selection

2 - No of Regs

7 Reg + Memory

Output

+

6 Regs

Selection 1 bit (115) to 1 bit (11)

1 bit Bus to 1 bit (Register) 1 bit (Value)

is Register Value Output

Bus

Reg N. 1 bit (11) to 1 bit (11)

is 1 bit (11) to 1 bit (11) (Register)

1 bit (11) to 1 bit (11) (Register) 1 bit (11)

Bus to 1 bit (11) (Output)

CTR

~~جیسے کہیں منہ میں کوئی INPR نہیں رہے گا~~, INPR نہیں رہے گا  
BIL نہیں رہے گا

Memory کے لئے Bus کے لئے Digital Output AR

Memory کے لئے Signal Read لے گا Address کے لئے Signal Write لے گا

AR Address Help کے لئے Read و Write کے لئے AR جگہ پر دیا جائے گا

Output address Bus کے Output address AC کے  
لئے one AC کے INPR کے Input اسی واسطے, DR کے  
لئے one DR کے Input DR کے Help کے لئے Output  
DR کے DR کے AC کے دلیل

Address کے لئے DR Memory کے اپنے دلیل  
OR کے لئے Bus کے Select کے لئے AR  
Read data کے Memory Output کے Bus کے

Memory کے Output کے Clockycle کے لئے  
Digital Bus DR کے DP کے 3 bit load کے لئے  
 $i = DR \text{ load}$

(111)  $\bar{i} = \text{Selection}$   
Address  $\bar{i} = AR \text{ (Address)}$   
DR  $\bar{i} = DR \text{ (Data)}$

IR

Memory or Joi

Outs of Instruction in PC 1 in Address field  
AR Is BUS 1 and BU 2 Is PC

BU 2 Is PC with 2 Selections  
if AR 1 cycle 1 to 1 = load of AR  
obj of all Address 1 to 5 PC is open 15 Cycles  
if PC is memory then DR can be 1 = load of IR

IR

Memory 1 in Bus 1 = BUS Selection

Addr 1 (memory) 1 to 5 (U & B) (D) = Read  
U & B (field) 2 to 5 (PC) 1 to 5 (AR) 1 to 5 (U)  
IR 1 to Memory 1 in Cycle Instruction

1 to 5 (Register) Bus Selection Set 0  
Value 1 to 5 (Register)

1 to 5 (Register) Bus Selection Set 1  
Value 1 to 5 (Register)

input 1

asli ~~DR~~ of Bus 1 in Register AC  
AC always 4

AC = DR 1 to 5, DR 1 to 5, DR 1 to 5  
AC 1 to 5, DR 1 to 5, DR 1 to 5 = AC + DR 1 to 5  
DR (value) 1 to 5, AC 1 to 5, DR 1 to 5  
DR 1 to 5, AC 1 to 5

~~ACU~~ دفع نیازی ACU Reg شود لیکن  
 want to plug in DR instead of DR لیکن درین DR لیکن  
 DRU پرین ACU DR و دنی BUS

LD → load

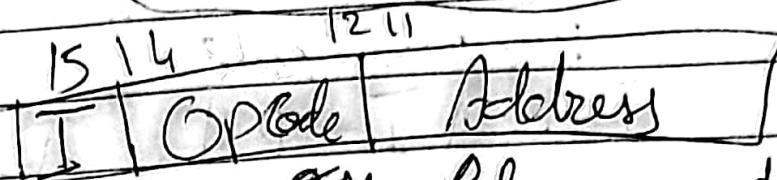
ICR → Increment (+1)

CUR → Clear (zero)

fewest's circuit)  $\rightarrow$  1 clock cycle  $\rightarrow$  IR  
 In one clock cycle, clear delay  $\rightarrow$  1 clock cycle

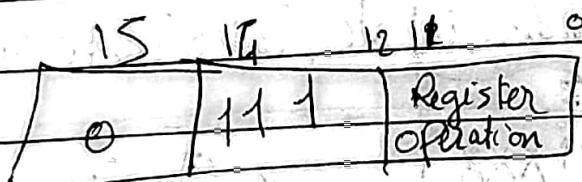
End  
 E → Add (sum) + (Carry)  $\rightarrow$  sum  
 sum = sum + carry

# BASIC Computer Instructions



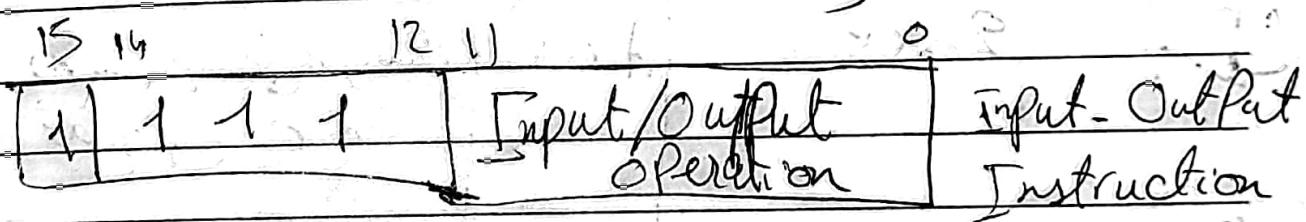
(Memory Reference instruction)  
 (Opcode = 000  $\rightarrow$  110)

Register Operations (sis  
 (Memory))



Register-Reference  
 Instruction

Reg. (Register) Operations (Memory) I/O



Operations (Memory) I/O (All)

Operations (Memory) I/O (0) 110  $\rightarrow$  000

I/O (end) 111 [3] 110 111 8 (2)

Register Reference

Register Reference Ref.)

I/O

Opcode  $\rightarrow$  111

opcode  $\Rightarrow$  111

13  $\rightarrow$  0

I  $\Rightarrow$  1

16 Bit OpCode | 12 Bit Address

N XXX

Each X is 4 Bits

## Memory-Reference Instructions

PAGE \_\_\_\_\_

DATE \_\_\_\_\_

Hexadecimal Code

Symbol	I = 0	I = 1	Description
--------	-------	-------	-------------

AND

0 XXX

8 XXX

2plc AND op. 2plc

29Bitz

SEL

= X J3

Memory Address

12Bit (OpCode) > I

Hexadecimally 21 & 20 Address 11

(32bit Value) > 2plc

AND 1plc Instruction

AC (j3plc), AC (j2plc)

ADD

1 XXX

9 XXX

Cpu (15) j3plc

ADD dev

LDA

2 XXX

A XXX

Memory (j3plc) Cpu

AC (j3plc)

STL

3 XXX

B XXX

AC w 2plc

(write) Memory (j3plc)

BUN

4 XXX

C XXX (j3plc) AC (j2plc)

Instruction

(j3plc) (j2plc) AC

(32bit Value) > 2plc

Address 11 & 13 AC

2plc 11 & 13 AC

Hex

Symbol

 $I = 0$  $I = 1$ Description

BSA

5XXX

1XXXX

Function Call

(Set M1 instruction)

Call to Subroutine

Save Registers in Call

Temporary Variables

ISZ

6XXX

EXXX

Word Increment

Address

Subtract 1

Temporary Variable

Temporary Variable

Temporary Variable

## Register Reference Instruction

7 bits Hexcode | 1 bit opCode = 111, I = 0 | 11

12 bits | Instruction | 12 bits |  
4 bits | Address | 4 bits | Register |  
4 bits | Address | 12 bits | 12 bits | Represent  
Bit 13 is bit 16 Address | Bit 12 is bit 15 Register |  
12 zeros, also word Address | 12 Reg Operation  
Address is one, bit 13 is bit 16, Bit 12  
is bit 15 Register | Bits 12 bits

## Remember

Binary to Hexadecimal

1 byte = 4 bits | 16 bits  
Binary | 4 bits | 4 bits | 4 bits | 4 bits

Ex

1000 0000 0000 0000

Bin

8

0

0

Hex

LCIA

3 char ACI → 3 bits

# Microprocessor

PAGE \_\_\_\_\_

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Symbol	Hex Code	Desc.
CLA	7800	AC = 00000000
CLE	7400	AC = 11111111 Carry = 1
CMR	7200	AC = 00000000
CLE	7100	Complement of E
CIR	7080	AC Shift Right Circular Shift Right AC
CIL	7040	Circular Shift Left E, AC
INC	7020	Increment ACU
SPA	7010	Next Instruction for loop & Branch

SUA Zoo 7008 - weg 2500 ie

SZA Zoo 4 3009 8501 ie

SZE Zoo 9 8501 ie  
sp. fistic Value 1E

HLT Zoo 1

Shuttle Shuttles  
Halt figures

(Les) ورقة طاولة

INC IN CMA CLE CLA

مدى انتشار SPA ie -  
SUA

Woolworths الذهاب  
HLT

Woolworths 8501 ie  
1,2,4,8 دينار (807) 2 Bit جو 1000  
Zer الباقي 3 Bits

# Input Output Instruction

Bit 7 وفاي 111 = opode 11, I = 11  
 (11, 15 هـ) F 15 هـ  
 (11, 15 هـ) F 15 هـ

(Clear اول ) IOP INP SKO SKI OUT INP)

Symbol	Hex	Desc
INP	F800	Reg 1 to Char Nipple
OUT	F400	Char 2 to Reg 1 INPR
SKI	F200	Skip on Input Flag

SKO F100 ~ Output

IOP Fc80 Interrupt On

TOP F040 ~ OF

Handling of Input & Output on Screen  
from Keyboard

8 Interrupts Handling