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FAEZE FAGHIH

EDUCATION

- 2016 –2018
  M.Sc. in Computer Engineering – Computer Architecture, Department of CE, Sharif University of Technology
  GPA: 18.13/20.00
- 2011 – 2016
  B.Sc. in Computer Engineering - Hardware, Department of ECE, University of Tehran, Tehran, Iran.
  GPA: 15.93/20.00 , **Last 2 Years GPA:** 17.60/20.00
- 2007 – 2011
  High School Diploma, Farzanegan High School**,** under the supervision of NODET(National Organization for Developing Exceptional Talents), Amol, Iran.
  GPA: 19.38/20.00

RESEARCH INTERESTS

- Computer Architecture
- Applications of Field-Programmable Gate Arrays (FPGAs)
- Parallel Processing
- Distributed Systems

HONORS AND AWARDS

- Ranked 1st among the B.S students of Hardware engineering, University of Tehran [2015]
- Ranked 2nd among the Master Students of Hardware engineering, Sharif University of Technology [2016]
- Ranked 9th in National Master Entrance Exam
- Ranked 326th among near 300000 Participants in the “National Universities Entrance Exam” in Math & Physics [2011]
- Selected as a qualified person at the first stage of “Iranian National Physics Olympiad” [2010]

TECHNICAL SKILLS

- Programming languages: C/C++, Verilog, VHDL, Python
- Tools: Vivado, Modelsim, Altera Quartus, Antlr, CodeVision, HSpice, Flexus
- Web programming: Ruby on Rails, HTML, CSS

TEACHING EXPERIENCES

Supervisor:

- Seminar – DNN Compilation and Mapping
- Practice of Software Development
- Two ongoing bachelor thesis

Teaching Assistant In Following Courses:

- FPGA Based Embedded System Design
- CAD
- Computer Architecture Laboratory
- Computer Architecture
- Digital Logic Circuit

Physics Tutor

- Tutor for students who participate in physics Olympiad

RESEARCH EXPERIENCES

- I am currently a researcher at the Karlsruhe Institute of Technology (KIT) working with Professor Jorge Henkel. I am working on a design space exploration tool for DNN accelerators.
- Designing Instruction-prefetcher with low area overhead for server workloads.
- Mehdi Modarressi, Faeze Faghih, Maryam Modarressi “Hardware Accelerator for Biological Protein Sequence Alignment on Reconfigurable Networks-on-Chip”, 2015
- Implementation of a power-Efficient Accelerator Design for Neural Network in VHDL.

SELECTED ACADEMIC PROJECTS

- Design and implementation of **vector processor accelerator** hardware on FPGA with Avalon and NIOS compatibility in Verilog, FPGA based embedded system design, Fall 2014
- Design and implementation of a **real time noise-cancelation FIR filter** in FPGA as accelerator with RS-232 port in Verilog, FPGA based embedded system design,Fall 2014
- Implementation of several papers related to cache replacement policy in c++, Advanced Computer Architecture, Fall 2016
- Implementation of a **Network-on-Chip** using VHDL, Computer Aided Design, Fall 2014
- Design and implementation of a **web based social network** for the students who want to apply for a university, using Ruby on Rails, Internet Engineering course, Spring 2015
- Design and implementation of an **Online Service Provider**, using C++ socket programming, operating system course, Fall 2013
- Implementation of a **compiler**, Antlr, Design of Compilers Course, Fall 2013
- Implementation of **multithreaded social network application** using C++ socket programming, Advanced Programming Course, Spring 2012
- Design and implementation of **Search Engine on text files**, using B+ tree data structure, Data Structures and Algorithm Courses, Fall 2012

COURSE WORK

Advanced Computer Architecture(20/20), Database Systems(18.2/20), FPGA based embedded system design(18.4/20), Computer Network(19.9/20), Data and network security(18/20), Computer Architecture Lab(20/20), Computer Aided Design(19.6/20), Digital Logic Design Lab(19/20), Interface Circuit(17.0/20)