SoC Lab

Lab3 Report

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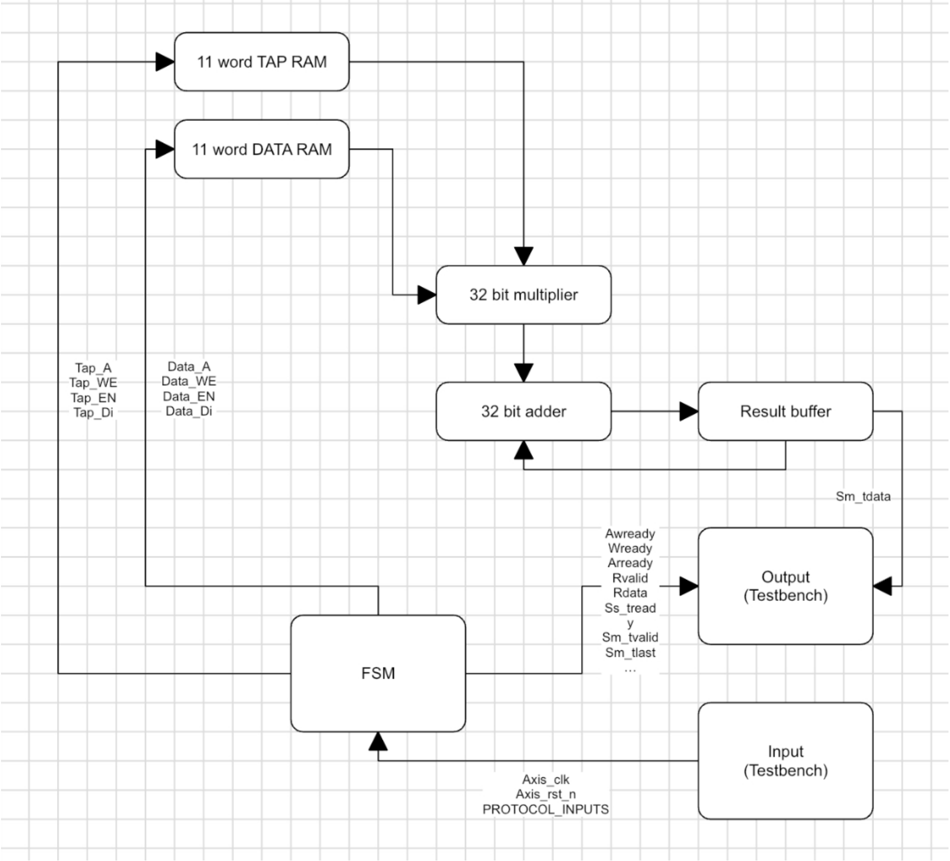
1. Block Diagram
   - Datapath – dataflow
   - Control signals



2. Describe Operation
   - How to receive data-in and tap parameters and place into SRAM
     i. The implementation of tapRAM is rather simple, all we have to do is follow the protocol and change the corresponding signals to store the data. For example, EN has to be high to access bram, and WE has to be 1111 if we want to write a 32 bit data to bram.
     ii. For shiftRAM, besides from performing the real "shift" in bram which cost lots of time, here I choose to shift the address and place the new data in the address that stores the oldest data instead. By controlling the address that accesses out data, we can construct a bram without shifting all the data in our bram whenever there is a new incoming data.
   - How to access shiftRAM and tapRAM to do computation
     iii. To get the data from RAMs and use them in calculation, we need to acknowledge that there is a one period delay from the time we send

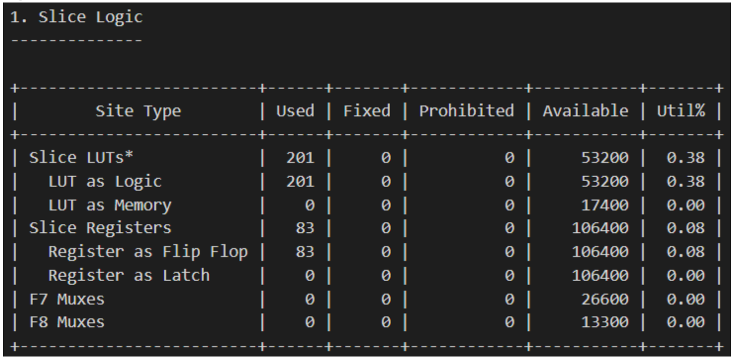
the address into bram to bram outputs the desired data. Thus if we want to utilize a data stored in bram at cycle time k, we have to send the new address at cycle time k-1.

iv. As for bram control signals, since we store or read a whole data once at a time, we can set WE to 1111 or 0000 according to our action. We should also pull the enable signal whenever we need access to our bram.

- How ap_done is generated

v. In my design, the whole flow is controlled by an FSM. There’s a stage called “FINAL_STAGE” in the FSM that indicates that the whole process comes to an end. We raise ap_done when the process reaches this state.

3. Resource Usage



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1. Slice Logic
--------------

+-------------------------+------+-------+------------+-----------+-------+
|        Site Type        | Used | Fixed | Prohibited | Available | Util% |
+-------------------------+------+-------+------------+-----------+-------+
| Slice LUTs*             |  201 |     0 |          0 |     53200 |  0.38 |
|   LUT as Logic          |  201 |     0 |          0 |     53200 |  0.38 |
|   LUT as Memory         |    0 |     0 |          0 |     17400 |  0.00 |
| Slice Registers         |   83 |     0 |          0 |    106400 |  0.08 |
|   Register as Flip Flop |   83 |     0 |          0 |    106400 |  0.08 |
|   Register as Latch     |    0 |     0 |          0 |    106400 |  0.00 |
| F7 Muxes                |    0 |     0 |          0 |     26600 |  0.00 |
| F8 Muxes                |    0 |     0 |          0 |     13300 |  0.00 |
+-------------------------+------+-------+------------+-----------+-------+
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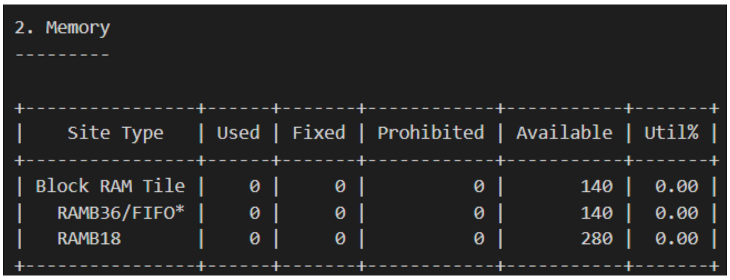

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2. Memory
---------

+----------------+------+-------+------------+-----------+-------+
|    Site Type   | Used | Fixed | Prohibited | Available | Util% |
+----------------+------+-------+------------+-----------+-------+
| Block RAM Tile |    0 |     0 |          0 |       140 |  0.00 |
|   RAMB36/FIFO* |    0 |     0 |          0 |       140 |  0.00 |
|   RAMB18       |    0 |     0 |          0 |       280 |  0.00 |
+----------------+------+-------+------------+-----------+-------+
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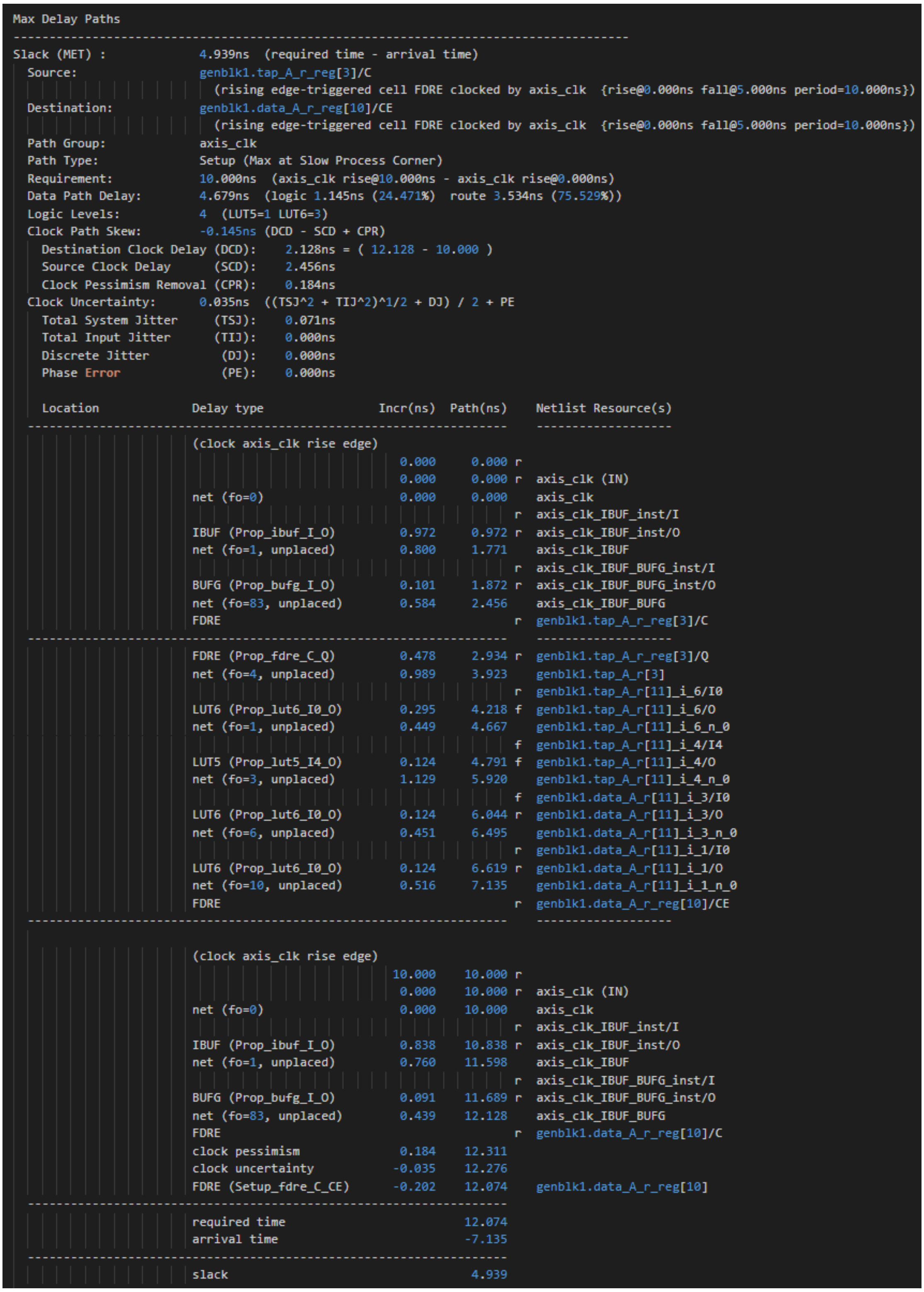
4. Timing Report

- Synthesis Frequency
  - ■ 100MHz
- Timing on longest path, slack



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Max Delay Paths
--------------------------------------------------------------------------------------
Slack (MET) :             4.939ns  (required time - arrival time)
  Source:                 genblk1.tap_A_r_reg[3]/C
                            (rising edge-triggered cell FDRE clocked by axis_clk  {rise@0.000ns fall@5.000ns period=10.000ns})
  Destination:            genblk1.data_A_r_reg[10]/CE
                            (rising edge-triggered cell FDRE clocked by axis_clk  {rise@0.000ns fall@5.000ns period=10.000ns})
  Path Group:             axis_clk
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            10.000ns  (axis_clk rise@10.000ns - axis_clk rise@0.000ns)
  Data Path Delay:        4.679ns  (logic 1.145ns (24.471%)  route 3.534ns (75.529%))
  Logic Levels:           4  (LUT5=1 LUT6=3)
  Clock Path Skew:        -0.145ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    2.128ns = ( 12.128 - 10.000 )
    Source Clock Delay      (SCD):    2.456ns
    Clock Pessimism Removal (CPR):    0.184ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter          (DJ):    0.000ns
    Phase Error              (PE):    0.000ns

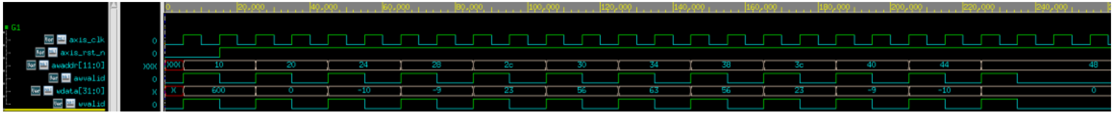
    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                         (clock axis_clk rise edge)
                                                      0.000     0.000 r
                                                      0.000     0.000 r  axis_clk (IN)
                         net (fo=0)                   0.000     0.000    axis_clk
                                                                      r  axis_clk_IBUF_inst/I
                         IBUF (Prop_ibuf_I_O)         0.972     0.972 r  axis_clk_IBUF_inst/O
                         net (fo=1, unplaced)         0.800     1.771    axis_clk_IBUF
                                                                      r  axis_clk_IBUF_BUFG_inst/I
                         BUFG (Prop_bufg_I_O)         0.101     1.872 r  axis_clk_IBUF_BUFG_inst/O
                         net (fo=83, unplaced)        0.584     2.456    axis_clk_IBUF_BUFG
                         FDRE                                         r  genblk1.tap_A_r_reg[3]/C
  -------------------------------------------------------------------    -------------------
                         FDRE (Prop_fdre_C_Q)         0.478     2.934 r  genblk1.tap_A_r_reg[3]/Q
                         net (fo=4, unplaced)         0.989     3.923    genblk1.tap_A_r[3]
                                                                      r  genblk1.tap_A_r[11]_i_6/I0
                         LUT6 (Prop_lut6_I0_O)        0.295     4.218 f  genblk1.tap_A_r[11]_i_6/O
                         net (fo=1, unplaced)         0.449     4.667    genblk1.tap_A_r[11]_i_6_n_0
                                                                      f  genblk1.tap_A_r[11]_i_4/I4
                         LUT5 (Prop_lut5_I4_O)        0.124     4.791 f  genblk1.tap_A_r[11]_i_4/O
                         net (fo=3, unplaced)         1.129     5.920    genblk1.tap_A_r[11]_i_4_n_0
                                                                      f  genblk1.data_A_r[11]_i_3/I0
                         LUT6 (Prop_lut6_I0_O)        0.124     6.044 r  genblk1.data_A_r[11]_i_3/O
                         net (fo=6, unplaced)         0.451     6.495    genblk1.data_A_r[11]_i_3_n_0
                                                                      r  genblk1.data_A_r[11]_i_1/I0
                         LUT6 (Prop_lut6_I0_O)        0.124     6.619 r  genblk1.data_A_r[11]_i_1/O
                         net (fo=10, unplaced)        0.516     7.135    genblk1.data_A_r[11]_i_1_n_0
                         FDRE                                         r  genblk1.data_A_r_reg[10]/CE
  -------------------------------------------------------------------    -------------------

                         (clock axis_clk rise edge)
                                                     10.000    10.000 r
                                                      0.000    10.000 r  axis_clk (IN)
                         net (fo=0)                   0.000    10.000    axis_clk
                                                                      r  axis_clk_IBUF_inst/I
                         IBUF (Prop_ibuf_I_O)         0.838    10.838 r  axis_clk_IBUF_inst/O
                         net (fo=1, unplaced)         0.760    11.598    axis_clk_IBUF
                                                                      r  axis_clk_IBUF_BUFG_inst/I
                         BUFG (Prop_bufg_I_O)         0.091    11.689 r  axis_clk_IBUF_BUFG_inst/O
                         net (fo=83, unplaced)        0.439    12.128    axis_clk_IBUF_BUFG
                         FDRE                                         r  genblk1.data_A_r_reg[10]/C
                         clock pessimism              0.184    12.311
                         clock uncertainty           -0.035    12.276
                         FDRE (Setup_fdre_C_CE)      -0.202    12.074    genblk1.data_A_r_reg[10]
  -------------------------------------------------------------------
                         required time                         12.074
                         arrival time                          -7.135
  -------------------------------------------------------------------
                         slack                                  4.939
```

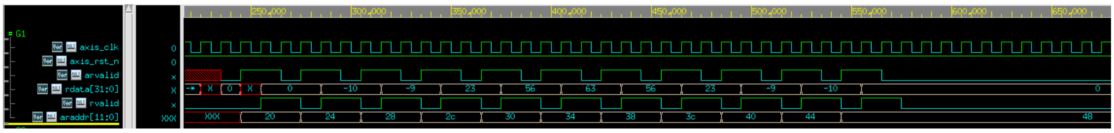
5. Simulation Waveform

- Coefficient program, and read back

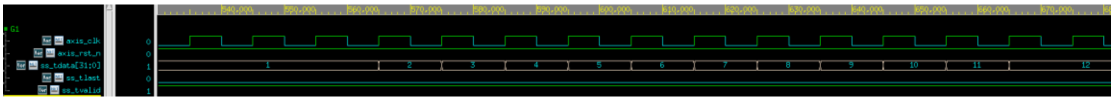
   i. Program

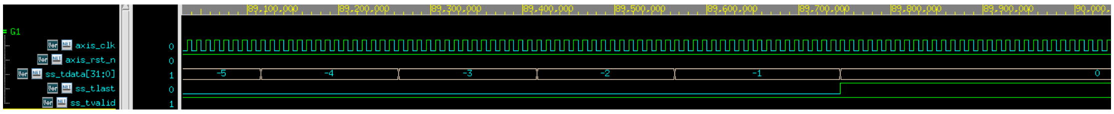


   ii. Read back

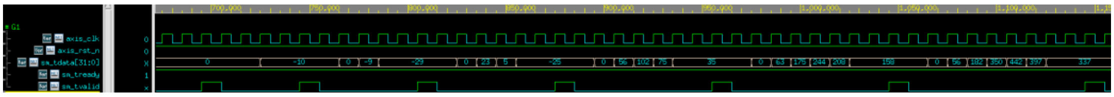


- Data-in stream-in



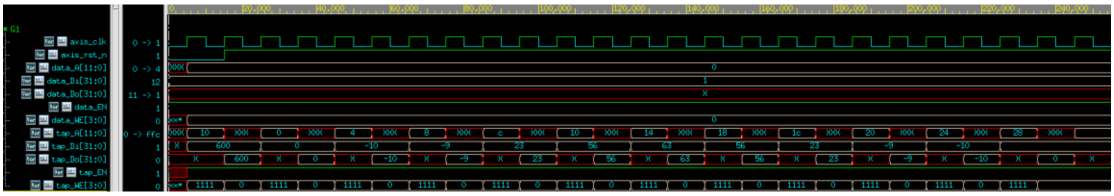


- Data-out stream-out

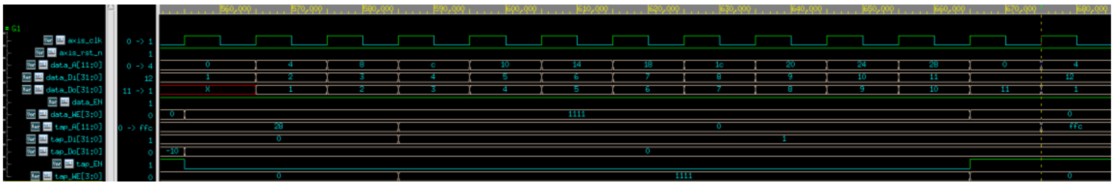


- RAM access control

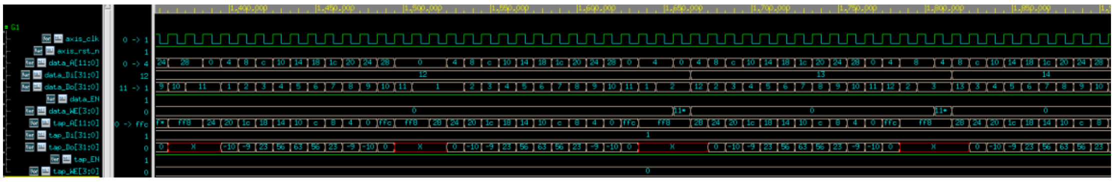
iii. TAP write



iv. DATA write

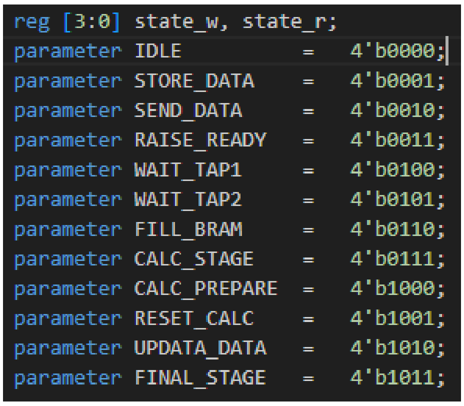


v. TAP & DATA read



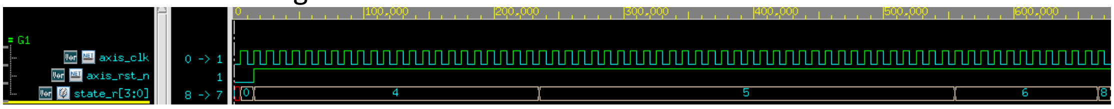
- FSM

vi. State code reference

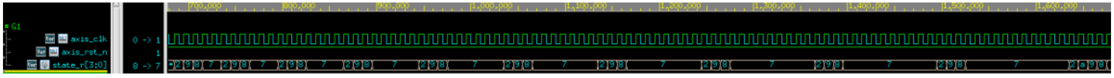


```
reg [3:0] state_w, state_r;
parameter IDLE          =   4'b0000;
parameter STORE_DATA    =   4'b0001;
parameter SEND_DATA     =   4'b0010;
parameter RAISE_READY   =   4'b0011;
parameter WAIT_TAP1     =   4'b0100;
parameter WAIT_TAP2     =   4'b0101;
parameter FILL_BRAM     =   4'b0110;
parameter CALC_STAGE    =   4'b0111;
parameter CALC_PREPARE  =   4'b1000;
parameter RESET_CALC    =   4'b1001;
parameter UPDATA_DATA   =   4'b1010;
parameter FINAL_STAGE   =   4'b1011;
```

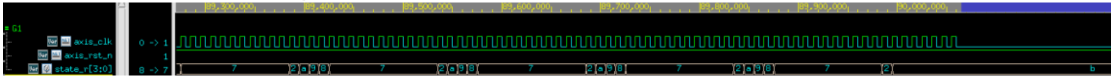
vii. INIT stage



viii. CALCULATE stage



ix. END stage



- measure # of clock cycles from ap_start to ap_done

x. cycle count: 8942 clock cycles