# Matthias Horlacher

Architect at Cadence Design Systems

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## Summary

Over 15 years of experience designing and implementing software in the field of Electronic Design Automation (EDA).

Specialties:
- Software design and implementation of high performance technical compute applications.
- Parallel programming in both multithreaded and distributed environments.
- Performance analysis and optimization with respect to runtime and memory footprint.
- Extensive knowledge of EDA algorithms in the field of RC parasitic extraction.

Goals:
- To make significant contributions in a fast-paced, customer-oriented work environment.

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## Experience

**Architect at Cadence Design Systems**
August 2012 - Present

**R&D Engineer at Synopsys**
April 2012 - August 2012 (5 months)

Supported QCP™ during ramp down.

**Sr. Member of Consulting Staff at Magma Design Automation, Inc.**
June 2006 - March 2012 (5 years 10 months)

Principal software architect of MAGMA's next-generation parasitic extraction tool QCP™. Defined and implemented the majority of the underlying data structures, geometric processing algorithms, parallelization strategies, and parasitic modeling code. Responsible for the continued performance improvements with respect to runtime, scalability and memory efficiency, as well as the implementation of and improvements to the modeling code and the addition of new features as requested by our customers.

Technologies: C++, STL, GDB, GPROF, SunStudio, Purify, Coverity, ClearCase, Linux

**Staff Engineer at Sun Microsystems, Inc.**
July 2000 - June 2006 (6 years)

- Lead a team of 3 to 5 developers in the development, implementation, and qualification of a patternbased 3D full chip parasitic interconnect extraction engine similar to Cadence/Simplex Fire & Ice. Defined the

overall server/client architecture for parallel execution, and specified the external interfaces and XML broadcast protocols. A paper describing the architecture was submitted to DAC 2006. Was responsible for the project planning and milestones. In particular designed and implemented the capacitance extraction module including a novel extensible pattern matching framework. Correlated the capacitance module against QuickCap and Simplex. Helped in the development of a Raphaelbased flow used for the automatic generation of the capacitance lookup tables used in the patternbased extractor.

- Implemented a C++ based GDSII scanner featuring a generic query language. This tool is used in many extraction and physical design verification flows at Sun.

- Maintained, supported, and further developed a Simplex based RC extraction flow. In particular implemented a mixed extraction option, which for the first time allows parts of the design to be extracted down to the transistor level while others remain grayboxed. Contributed fundamental building blocks to the flow rewrite and helped in leading the team towards the development of a much more extensible and maintainable code base.

- Defined, implemented, documented, and maintained an incremental timing tool. This Perl based tool utilized wire models for incremental capacitance and resistance extraction and timing reruns. The tool was used for CTOs during tape out mode.

- Implemented a poly resistance ERC rule check flow based on the Simplex Fire resistance extraction tool. A patent application was filed in 2001.

**3D TCAD Development Engineer at Silvaco Data Systems**
October 1997 - July 2000 (2 years 10 months)

- Implementation of physicsbased models for backend processing, including etching, deposition, and oxidation into Silvaco's 3D process simulator.

- Code maintenance of parasitic interconnect extraction tool based on a 3D finite element field solver.

- Development, implementation, and maintenance of the regression tests used in both the process and interconnect simulators.

## Education

**Karlsruhe Institute of Technology (KIT)**
MS, Physics (Solid State), 1990 - 1997

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Contact Matthias on LinkedIn