# ECSE 548: Introduction to VLSI Systems
# Project Proposal - Group 1

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## 1 Project Definition

Traditional error mitigation techniques such as Error Correcting Code (ECC) provide limited error coverage rate at the cost of performance and area overhead. Another solution widely used in industry, namely Dual Modular Redundancy (DMR) in Lockstep, consists of two redundant cores executing the same application in lockstep. The results of both cores are compared and the data gets commited to the outside world only when the two results match. Resolving the issue of performance impact, lockstep execution has been shown to be a great waste of computational power. Therefore, in this project we propose to implement Execution fingerprinting which will greatly enhance the performance of a DMR system.

## 2 Targets

During the course of this project, the plan is to:

- Design a single core execution fingerprinting system that uses CRC for fingerprinting
- Design 2 CRC layouts to fit the MIPS8 multicycle processor to generate the fingerprints
- Store the generated fingerprints in a buffer
- Evaluate the performance impact, area overhead and error coverage of the system

The fingerprinting module will monitor the output ports of the current MIPS8 processor. The output will be compressed using the CRC circuit, generating a fingerprint. This fingerprint will then be stored in a buffer.

The two CRC layouts could differ in the specific algorithm used for the implementation and in the CRC bit size, among other things. A preliminary study will be done to pick an appropriate approach before delving into the layout. Logic minimization will be used to make the schematic as simple as possible, and the gates will be sized appropriately to achieve minimal delay.

Before the mid-project status report, we target finishing the layouts of both CRC circuits for a functional fingerprinting circuit. From that point, we will be able to optimize the circuit according to the behavior of the MIPS8 core. Then, a series of benchmarks will be executed in order to analyse the performance impact, area overhead and error coverage of the circuit.