ECSE 548: Introduction to VLSI Systems
Project Proposal - Group 1

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1 Project Definition

Traditional error mitigation techniques such as Error Correcting Code (ECC) has limited error coverage rate at the cost of performance and area overhead. Another solution widely used in industry namely Dual Modular Redundancy (DMR) in Lockstep consists of two redundant cores executing the same application in lockstep. Both results are compared and only on a match that the data will be commited to the outside world. Resolving the issue of performance impact, lockstep execution has been shown to be a great waste of computational power. Therefore in this project we propose to implement Execution fingerprinting which will greatly enhance the performance of a DMR.

2 Targets

For the course of this project we plan to:

- A single core execution fingerprinting will be designed using CRC
- 2 CRC layout will be designed to fit the MIPS8 multicycle processor that will generate the fingerprints
- The generated fingerprints will be stored in a buffer
- The performance impact, area overhead and error coverage will be evaluated

The fingerprinting design will consist of monitering the output ports of the current MIPS8 processor. Then it will be compressed using the CRC circuit, generating a fingerprint. This fingerprint will then be stored in a buffer. By the mid-project status report, we target to finish the layout of both CRC circuits for a functional fingerprinting circuit. From that point, we will be able to optimize the circuit according to the behavior of the MIPS8 core. Then, a series of benchmarks will be executed in order to analyse the performance impact, area overhead and error coverage of the circuit.