CENTER OF NANOELECTRONICS & DEVICES

CND 111:Digital

Project : Implementation of DSP Slice

Section : 17

Group Name: group_17_111_6

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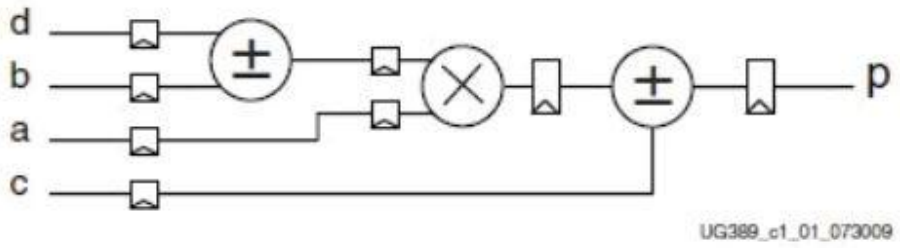
Digital Project

Implementation of DSP Slice

Introduction:

FPGAs are efficient for digital signal processing (DSP) applications because they can implement custom, fully parallel algorithms. DSP applications use many binary multipliers and accumulators that are best implemented in dedicated DSP slices. All 7 series FPGAs have many dedicated, full-custom, low-power DSP slices, combining high speed with small size while retaining system design flexibility. The DSP slices enhance the speed and efficiency of many applications beyond digital signal processing, such as wide dynamic bus shifters, memory address generators, wide bus multiplexers, and memory-mapped I/O registers.



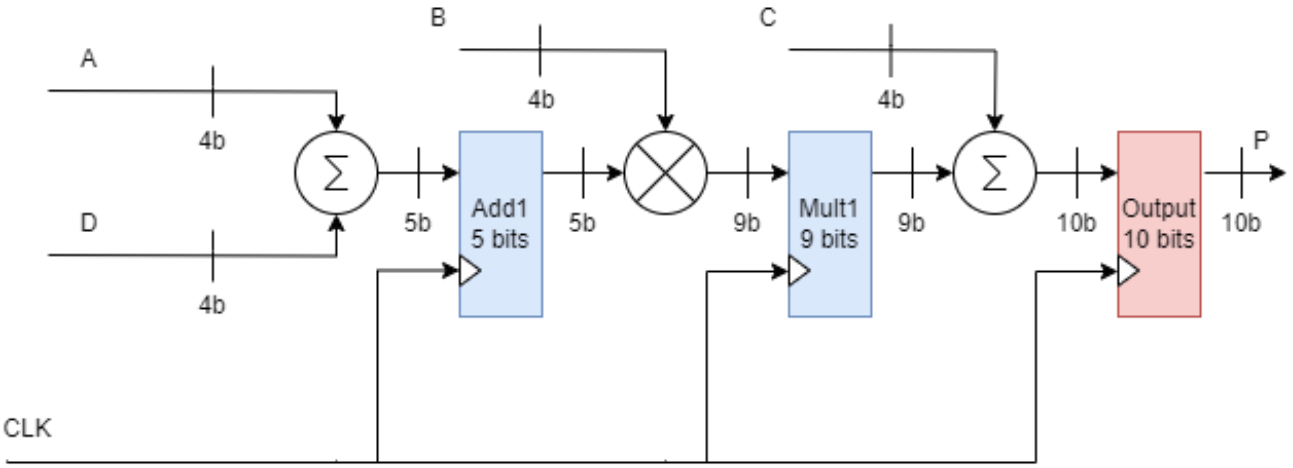
Some highlights of the DSP functionality include:

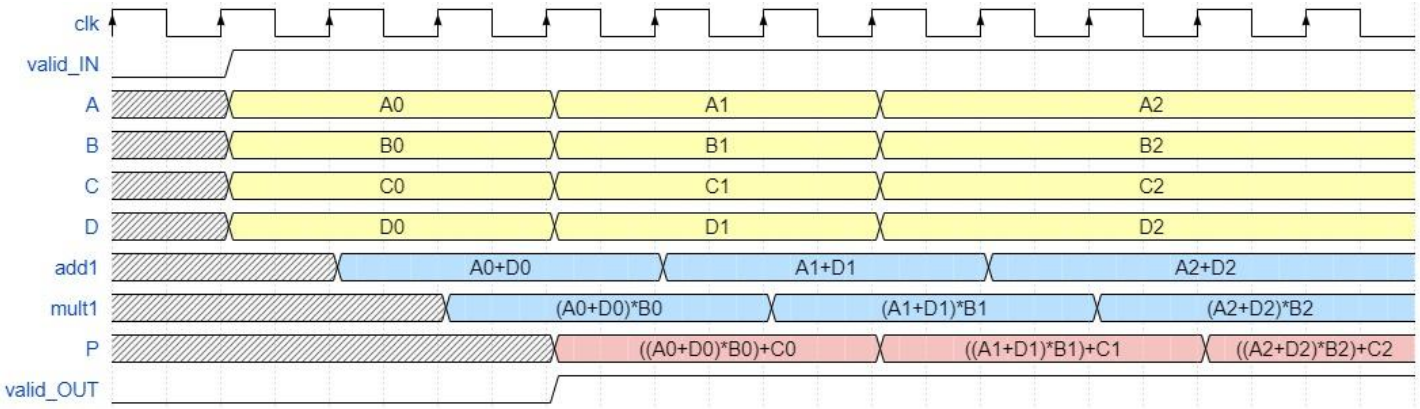
- **25 × 18 two's-complement multiplier:**
  Dynamic bypass
- **48-bit accumulator:**
  Can be used as a synchronous up/down counter
- **Power saving pre-adder:**
  Optimizes symmetrical filter applications and reduces DSP slice requirements
- **Single-instruction-multiple-data (SIMD) arithmetic unit:**
  Dual 24-bit or quad 12-bit add/subtract/accumulate
- **Optional logic unit:**
  Can generate any one of ten different logic functions of the two operands
- **Pattern detector:**
  Convergent or symmetric rounding
  96-bit-wide logic functions when used in conjunction with the logic unit
- **Advanced features:**
  Optional pipelining and dedicated buses for cascading

1-Verilog code to describe the architecture of the DSP48E1

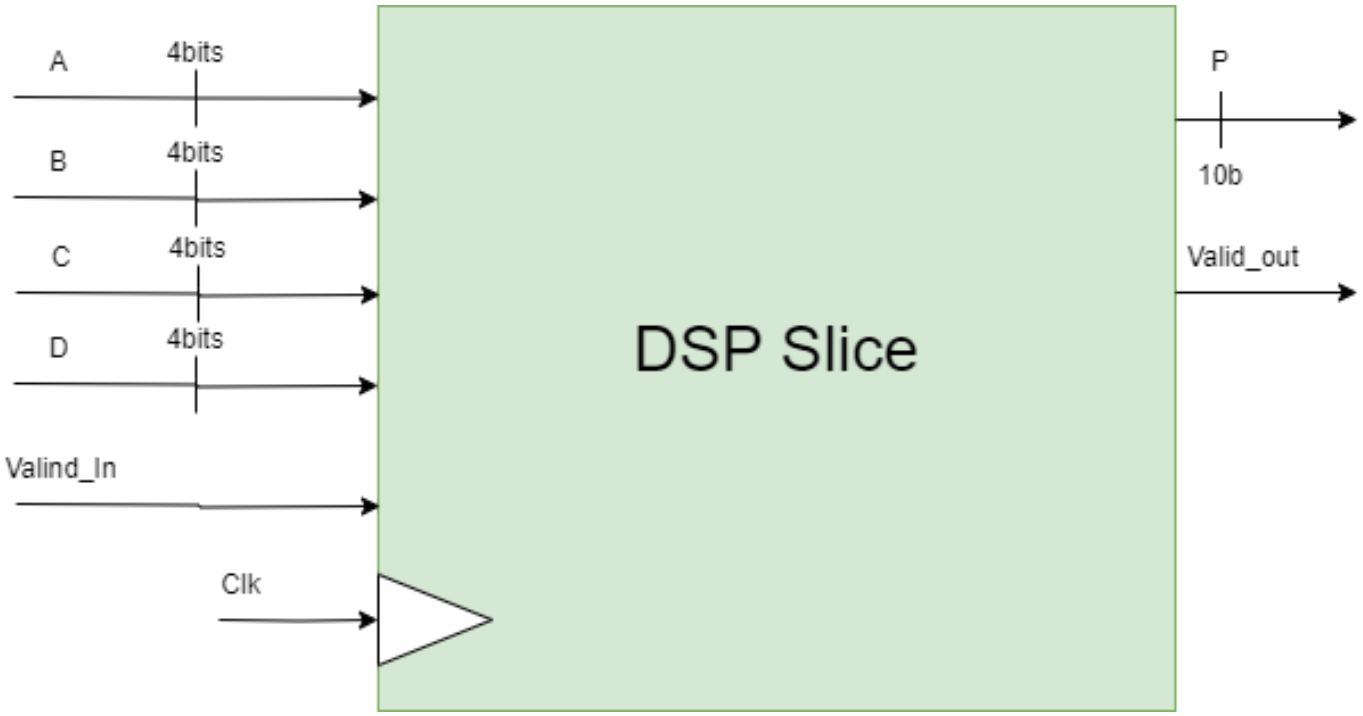
```
module Digital_project #( parameter IN_WIDTH=32 )
(input  clk, rst, valid_in,
output  valid_out,
input  signed [IN_WIDTH          - 1: 0] a, //S31 = 32 bits
input  signed [IN_WIDTH          - 1: 0] b, //S31 = 32 bits
input  signed [IN_WIDTH          - 1: 0] c, //S31 = 32 bits
input  signed [IN_WIDTH          - 1: 0] d, //S31 = 32 bits
output signed [(2*IN_WIDTH)+2  - 1: 0] p);

reg signed [IN_WIDTH   + 1   - 1: 0]        add1 = 0; //S32 = 33 bits
reg signed [(2*IN_WIDTH) + 1   - 1: 0]   mult1 = 0;    //(S31*S32) = S(31+32+1) = 1 + 64 = S64 = 65
bits
reg signed [(2*IN_WIDTH) + 2   - 1: 0]    add2 = 0; //S64 + S32 = S(64 +1) = 66 bits

reg add1v  = 0;
reg mult1v = 0;
reg add 2 v  = 0;

assign p = add2;
assign valid_out = add2v;


always@(posedge(clk),negedge(rst))
begin
   if(rst == 1'b0) begin
           add1    <= 0;
           mult1   <= 0;
           add2    <= 0;
           add1v  <=  0;
   end
   else if (valid_in == 1) begin
           add1    <=        a + d;
           add1v  <=  1;
           mult1   <=  add1 * b;
           add2    <= mult1 + c;
   end
   else begin
          add1     <=  add1;
          mult1    <= mult1;
          add2     <=  add2;
           add1v  <=  0;
   end
end
always@(posedge(clk),negedge(rst))
begin
   if(rst == 1'b0) begin
   end
   else if (valid_in == 1)  begin
           mult1v <= (add1v==1) ? 1'b1 : 1'b0;
           add2v <= (mult1v==1) ? 1'b1 : 1'b0;

   end
   else begin
                    mult1v <= 1'b0;
                    add2v <=  1'b0;
   end
end
endmodule
```

2-schematic





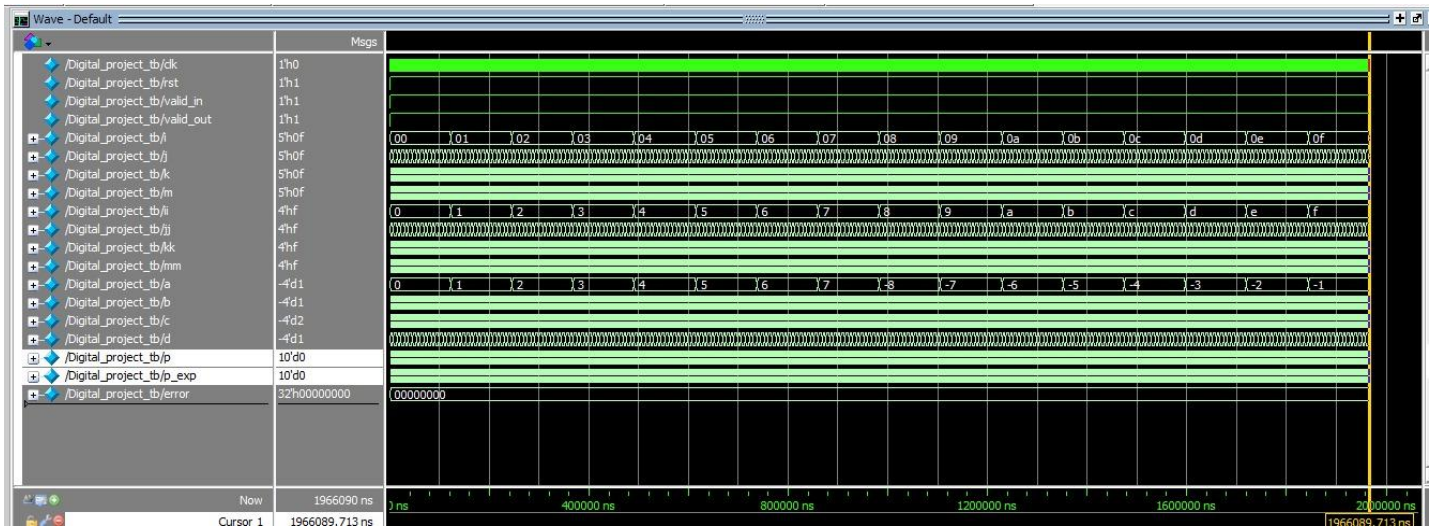
3-symbol of design



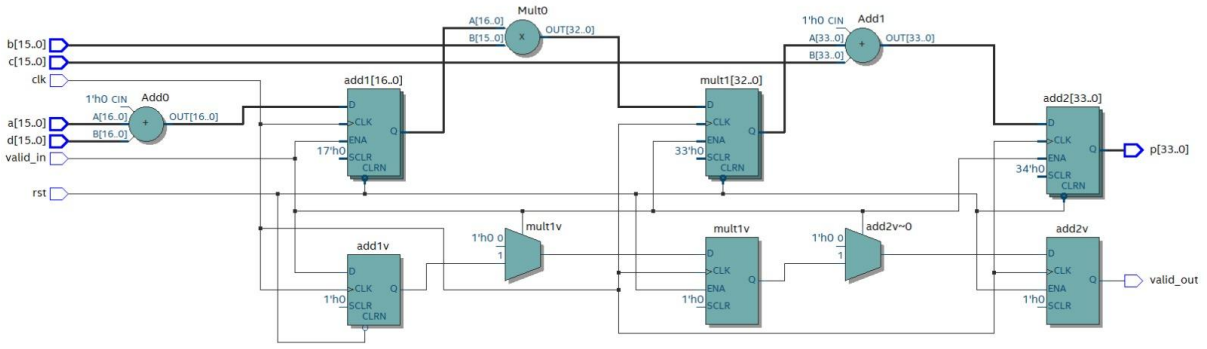
4-testbench

```
`timescale 1ns/1ps
module Digital_project_tb;
parameter IN_WIDTH = 4;
reg  clk, rst, valid_in;
wire valid out;
reg  signed [IN_WIDTH            - 1: 0] a = 0;
reg  signed [IN_WIDTH            - 1: 0] b = 0;
reg  signed [IN_WIDTH            - 1: 0] c = 0;
reg  signed [IN_WIDTH            - 1: 0] d = 0;
wire signed [(2*IN_WIDTH)+2  - 1: 0] p ;

reg [IN_WIDTH : 0] i = 0;
reg [IN_WIDTH : 0] j = 0;
reg [IN_WIDTH : 0] k = 0;
reg [IN_WIDTH : 0] m = 0;


reg signed [IN_WIDTH-1 : 0] ii = 0;
reg signed [IN_WIDTH-1 : 0] jj = 0;
reg signed [IN_WIDTH-1 : 0] kk = 0;
reg signed [IN_WIDTH-1 : 0] mm = 0;


reg signed [(2*IN_WIDTH)+2  - 1: 0] p_exp = 0;

integer error = 0;

always #5 clk = ~clk;//period = 10;

Digital Project #(.IN_WIDTH(IN_WIDTH)) DUT
( .clk(clk), .rst(rst), .valid_in(valid_in), .valid_out(valid_out), .a(a), .b(b), .c(c), .d(d), .p(p));

initial begin
clk <= 1;
rst <= 0;
valid in <= 0;
a <= 0;
b <= 0;
c <= 0;
d <= 0;
#10
rst <= 1;
valid in <= 1;

for (i = 0; i <= ((2**(IN_WIDTH))- 1); i = i + 1) begin
   for (j = 0; j <= ((2**(IN_WIDTH))- 1); j = j + 1) begin
          for (k = 0; k <= ((2**(IN_WIDTH))- 1); k = k + 1) begin
                  for (m = 0; m <= ((2**(IN_WIDTH))- 1); m = m + 1) begin
                   //@(posedge clk)
                          ii <= i[IN_WIDTH - 1 : 0];
                          kk <= k[IN_WIDTH - 1 : 0];
                          mm <= m[IN_WIDTH - 1 : 0];
                          jj <= j[IN_WIDTH - 1 : 0];
                          a <= ii;
                          b <= kk;
                          c <= mm;
                          d <= jj;
                          p_exp <= #10 ((ii + jj) * kk ) + mm;
                          #30
                          if ((p != p_exp) && (valid_out == 1)) begin
          $display("test failed");
```

```
                error = error + 1;
                            end

                        end
                    end
                end
            end

            if (error == 0) begin
                $display("test Passed");
            end
            $stop;
            end
            endmodule
```



5-the RTL schematic and synthesis results.



6-Explore the synthesis reports (Resource usage, power consumption, maximum clock)

Synthesis Report

```
+-----------------------------------------------------------+
; Analysis & Synthesis Resource Usage Summary;
+---------------------------------------------+-------------+
; Resource                                    ; Usage        ;
+---------------------------------------------+-------------+
; Estimate of Logic utilization (ALMs needed) ; 109         ;
;                                             ;             ;
; Combinational ALUT usage for logic          ; 148         ;
;         -- 7 input functions                ; 0           ;
;         -- 6 input functions                ; 0           ;
;         -- 5 input functions                ; 0           ;
;         -- 4 input functions                ; 0           ;
;         -- <=3 input functions              ; 148         ;
;                                             ;             ;
; Dedicated logic registers                   ; 201         ;
;                                             ;             ;
; I/O pins                                    ; 198         ;
;                                             ;             ;
; Total DSP Blocks                            ; 3           ;
;                                             ;             ;
; Maximum fan-out node                        ; valid in~input ;
; Maximum fan-out                             ; 201         ;
; Total fan-out                               ; 1635        ;
; Average fan-out                             ; 2.19        ;
+---------------------------------------------+-------------+
; Analysis & Synthesis Resource Utilization by Entity
+----------------------------+--------------------+-----------+
; Compilation Hierarchy Node ; Combinational ALUTs ; Dedicated Logic Registers ; Block Memory
Bits ; DSP Blocks ; Pins ; Virtual Pins ; Full Hierarchy Name ; Entity Name           ; Library Name ;
+----------------------------+--------------------+---------------------------+------------------+------------+------+---------
-
; |Digital_project           ; 148 (148)          ; 201 (201)                 ; 0                ; 3          ; 198  ; 0
          ; |Digital Project ; Digital_project ; work              ;
+----------------------------+--------------------+---------------------------+------------------+------------+------+---------
-
Note: For table entries with two numbers listed, the numbers in parentheses indicate the number of
resources of the given type used by the specific entity alone. The numbers listed outside of
parentheses indicate the total resources of the given type used by the specific entity and all of its
sub-entities in the hierarchy.
+-------------------------------------------------+
; Analysis & Synthesis DSP Block Usage Summary      ;
+---------------------------------+-------------+------------+------------+
; Statistic                                       ; Number Used ;
+---------------------------------+-------------+------------+------------+
; Sum of two 18x18                               ; 1          ;
; Two Independent 18x18                          ; 2          ;
; Total number of DSP blocks                     ; 3          ;
;                                 ;             ;
; Fixed Point Signed Multiplier                  ; 1          ;
; Fixed Point Unsigned Multiplier                ; 1          ;
; Fixed Point Mixed Sign Multiplier              ; 2          ;
+---------------------------------+-------------+------------+------------+
```

Timing Report

+---+
; Clocks
;
+------------+------+--------+-----------+-------+-------+------------+-----------+-------------+-------+--------+-----------+------------+----------+--------+---------+
; Clock Name ; Type ; Period ; Frequency ; Rise ; Fall ; Duty Cycle ; Divide by ; Multiply by ; Phase ; Offset ; Edge List ; Edge Shift ; Inverted ; Master ; Source ; Targets ;
+------------+------+--------+-----------+-------+-------+------------+-----------+-------------+-------+--------+-----------+------------+----------+--------+---------+
; ك وم ن ; Base ; 10.000 ; 100.0 MHz ; 0.000 ; 5.000 ; ; ; ; ; ; ; ; ; ; ; { clk } ;
+------------+------+--------+-----------+-------+-------+------------+-----------+-------------+-------+--------+-----------+------------+----------+--------+---------+

+---+
; Slow 1100mV 85C Model Fmax Summary ;
+------------+-----------------+------------+------+
; Fmax ; Restricted Fmax ; Clock Name ; Note ;
+------------+-----------------+------------+------+
; 130.24 MHz ; 130.24 MHz ك وم ن ; ;
+------------+-----------------+------------+------+

This panel reports FMAX for every clock in the design, regardless of the user-specified clock periods. FMAX is only computed for paths where the source and destination registers or ports are driven by the same clock. Paths of different clocks, including generated clocks, are ignored. For paths between a clock and its inversion, FMAX is computed as if the rising and falling edges are scaled along with FMAX, such that the duty cycle (in terms of a percentage) is maintained. Altera recommends that you always use clock constraints and other slack reports for sign-off analysis.

; Timing Closure Recommendations ;

HTML report is unavailable in plain text report export.

+-----------------------------------+
; Slow 1100mV 85C Model Setup Summary ;
+-------+-------+--------------------+
; Clock ; Slack ; End Point TNS ;
+-------+-------+--------------------+
; clk ; 2.322 ; 0.000 ;
+-------+-------+--------------------+

+-----------------------------------+
; Slow 1100mV 85C Model Hold Summary ;
+-------+-------+--------------------+
; Clock ; Slack ; End Point TNS ;
+-------+-------+--------------------+
; clk ; 0.505 ; 0.000 ;
+-------+-------+--------------------+

; Slow 1100mV 85C Model Recovery Summary ;

No paths to report.

; Slow 1100mV 85C Model Removal Summary ;

No paths to report.

+--+
; Slow 1100mV 85C Model Minimum Pulse Width Summary ;
+-------+-------+----------------------------------+
; Clock ; Slack ; End Point TNS   ;
+-------+-------+----------------------------------+
; clk   ; 4.241 ; 0.000   ;
+-------+-------+----------------------------------+

; Slow 1100mV 85C Model Metastability Summary ;

No synchronizer chains to report.

+---+
; Slow 1100mV 0C Model Fmax Summary   ;
+------------+-----------------+------------+------+
; Fmax   ; Restricted Fmax ; Clock Name ; Note ;
+------------+-----------------+------------+------+
; 123.66 MHz ; 123.66 MHz   clk   ;   ;
+------------+-----------------+------------+------+

This panel reports FMAX for every clock in the design, regardless of the user-specified clock periods. FMAX is only computed for paths where the source and destination registers or ports are driven by the same clock. Paths of different clocks, including generated clocks, are ignored. For paths between a clock and its inversion, FMAX is computed as if the rising and falling edges are scaled along with FMAX, such that the duty cycle (in terms of a percentage) is maintained. Altera recommends that you always use clock constraints and other slack reports for sign-off analysis.

+-----------------------------------+
; Slow 1100mV 0C Model Setup Summary ;
+-------+-------+-------------------+
; Clock ; Slack ; End Point TNS   ;
+-------+-------+-------------------+
; clk   ; 1.913 ; 0.000   ;
+-------+-------+-------------------+

+-----------------------------------+
; Slow 1100mV 0C Model Hold Summary ;
+-------+-------+-------------------+
; Clock ; Slack ; End Point TNS   ;
+-------+-------+-------------------+
; clk   ; 0.479 ; 0.000   ;
+-------+-------+-------------------+

; Slow 1100mV 0C Model Recovery Summary ;

No paths to report.

```
----------------------------------------
; Slow 1100mV 0C Model Removal Summary ;
----------------------------------------
No paths to report.


+-------------------------------------------------+
; Slow 1100mV 0C Model Minimum Pulse Width Summary ;
+-------+-------+---------------------------------+
; Clock ; Slack ; End Point TNS                     ;
+-------+-------+---------------------------------+
; clk   ; 4.101 ; 0.000                           ;
+-------+-------+---------------------------------+


---------------------------------------------
; Slow 1100mV 0C Model Metastability Summary ;
---------------------------------------------
No synchronizer chains to report.


+-------------------------------------+
; Fast 1100mV 85C Model Setup Summary ;
+-------+-------+---------------------+
; Clock ; Slack ; End Point TNS         ;
+-------+-------+---------------------+
; clk   ; 6.620 ; 0.000                 ;
+-------+-------+---------------------+


+------------------------------------+
; Fast 1100mV 85C Model Hold Summary ;
+-------+-------+--------------------+
; Clock ; Slack ; End Point TNS       ;
+-------+-------+--------------------+
; clk   ; 0.233 ; 0.000               ;
+-------+-------+--------------------+


----------------------------------------
; Fast 1100mV 85C Model Recovery Summary ;
----------------------------------------
No paths to report.


----------------------------------------
; Fast 1100mV 85C Model Removal Summary ;
----------------------------------------
No paths to report.


+-------------------------------------------------+
; Fast 1100mV 85C Model Minimum Pulse Width Summary ;
+-------+-------+---------------------------------+
; Clock ; Slack ; End Point TNS                     ;
+-------+-------+---------------------------------+
; clk   ; 4.411 ; 0.000                           ;
+-------+-------+---------------------------------+


---------------------------------------------
; Fast 1100mV 85C Model Metastability Summary ;
---------------------------------------------
```

No synchronizer chains to report.

+-----------------------------------+
; Fast 1100mV 0C Model Setup Summary ;
+-------+-------+-------------------+
; Clock ; Slack ; End Point TNS ;
+-------+-------+-------------------+
; clk ; 6.821 ; 0.000 ;
+-------+-------+-------------------+

+-----------------------------------+
; Fast 1100mV 0C Model Hold Summary ;
+-------+-------+-------------------+
; Clock ; Slack ; End Point TNS ;
+-------+-------+-------------------+
; clk ; 0.204 ; 0.000 ;
+-------+-------+-------------------+

; Fast 1100mV 0C Model Recovery Summary ;

No paths to report.

; Fast 1100mV 0C Model Removal Summary ;

No paths to report.
+---+
; Fast 1100mV 0C Model Minimum Pulse Width Summary ;
+-------+-------+---------------------------------+
; Clock ; Slack ; End Point TNS ;
+-------+-------+---------------------------------+
; clk ; 4.413 ; 0.000 ;
+-------+-------+---------------------------------+

; Fast 1100mV 0C Model Metastability Summary ;

No synchronizer chains to report.

+---+
; Multicorner Timing Analysis Summary ;
+------------------+-------+-------+----------+---------+---------------------+
; Clock ; Setup ; Hold ; Recovery ; Removal ; Minimum Pulse Width ;
+------------------+-------+-------+----------+---------+---------------------+
; Worst-case Slack ; 1.913 ; 0.204 ; N/A ; N/A ; 4.101 ;
; clk ; 1.913 ; 0.204 ; N/A ; N/A ; 4.101 ;
; Design-wide TNS ; 0.0 ; 0.0 ; 0.0 ; 0.0 ; 0.0 ;
; clk ; 0.000 ; 0.000 ; N/A ; N/A ; 0.000 ;
+------------------+-------+-------+----------+---------+---------------------+

Power Report

Power Analyzer Summary	
Power Analyzer Status	Successful - Fri Dec 15 09:39:46 2023
Quartus Prime Version	22.1std.2 Build 922 07/20/2023 SC Lite Edition
Revision Name	Digital_project
Top-level Entity Name	Digital_project
Family	Cyclone V
Device	5CGXFC7C7F23C8
Power Models	Final
Total Thermal Power Dissipation	391.26 mW
Core Dynamic Thermal Power Dissipation	5.86 mW
Core Static Thermal Power Dissipation	349.68 mW
I/O Thermal Power Dissipation	35.71 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

7-Design metrics (resources usage, power, operating frequency) evaluation

clk frequency = 100 MHz
Total power consumption = 391.26 mW
Resource Utilization:
LUT less than 1%
DSP Blocks 2%