

## **CND 101:Analog**

**Project : Ring Oscillator**

**Section : 17**

**Group Name: group\_17\_101\_3**

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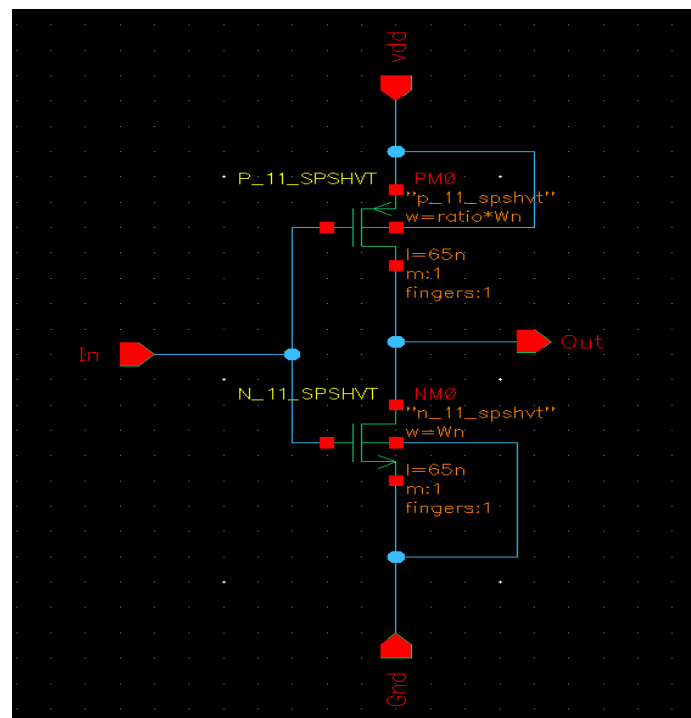
**Submitted to : Dr. Reda**

# Analog Project Ring Oscillator

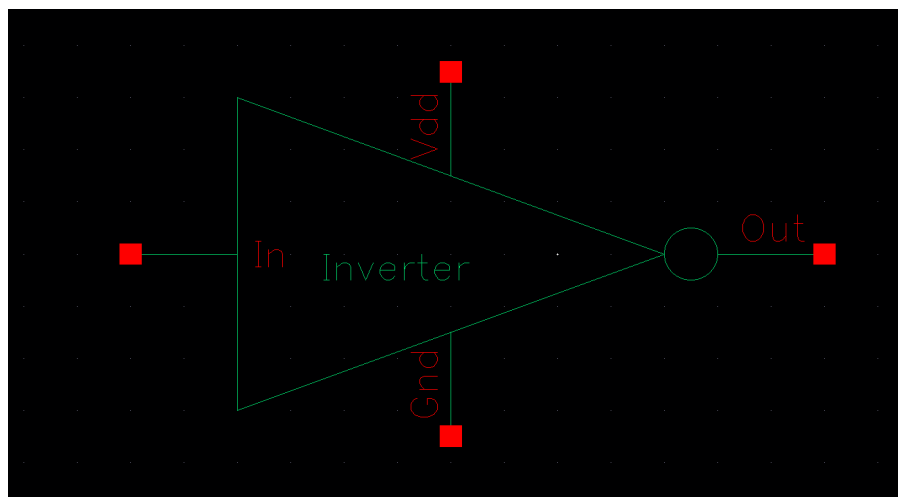
## Intro for Ring Oscillator

The definition of the ring oscillator is “an odd number of inverters are connected in a series form with positive feedback & output oscillates between two voltage levels either 1 or zero to measure the speed of the process. In place of inverters, we can define it with NOT gates also. These oscillators have an ‘n’ odd number of inverters. For instance, if this oscillator has 3 inverters then it is called a three-stage ring oscillator. If the inverter count is seven then it is a seven stage ring oscillator. The number of inverter stages in this oscillator mainly depends on the frequency which we want to generate from this oscillator

### Schematics of inverter:

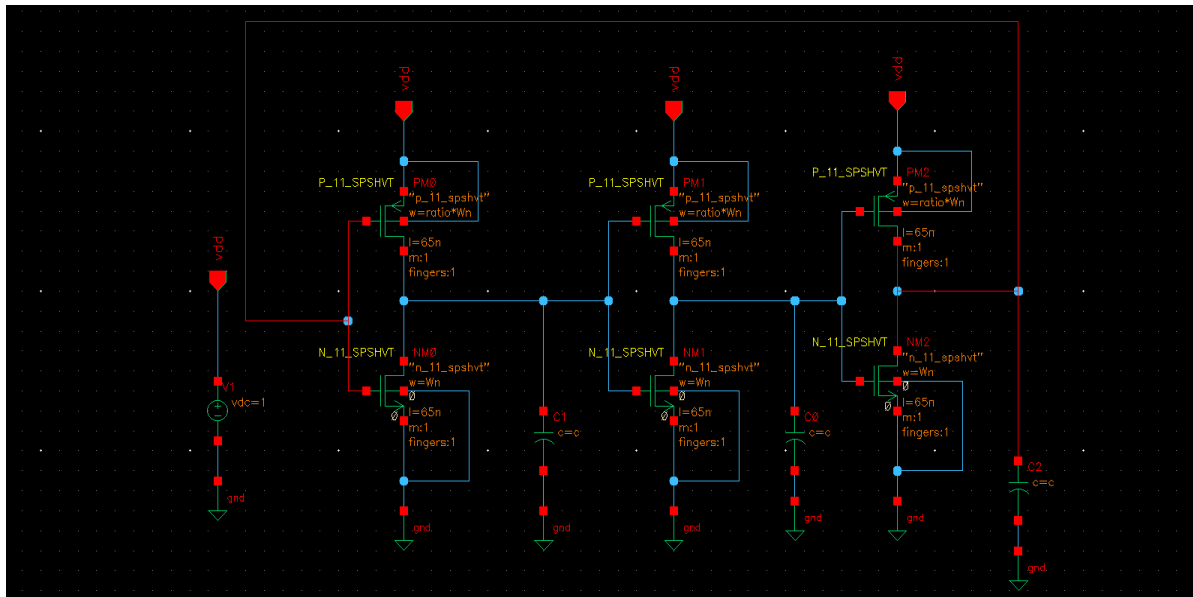


### Symbol of inverter:

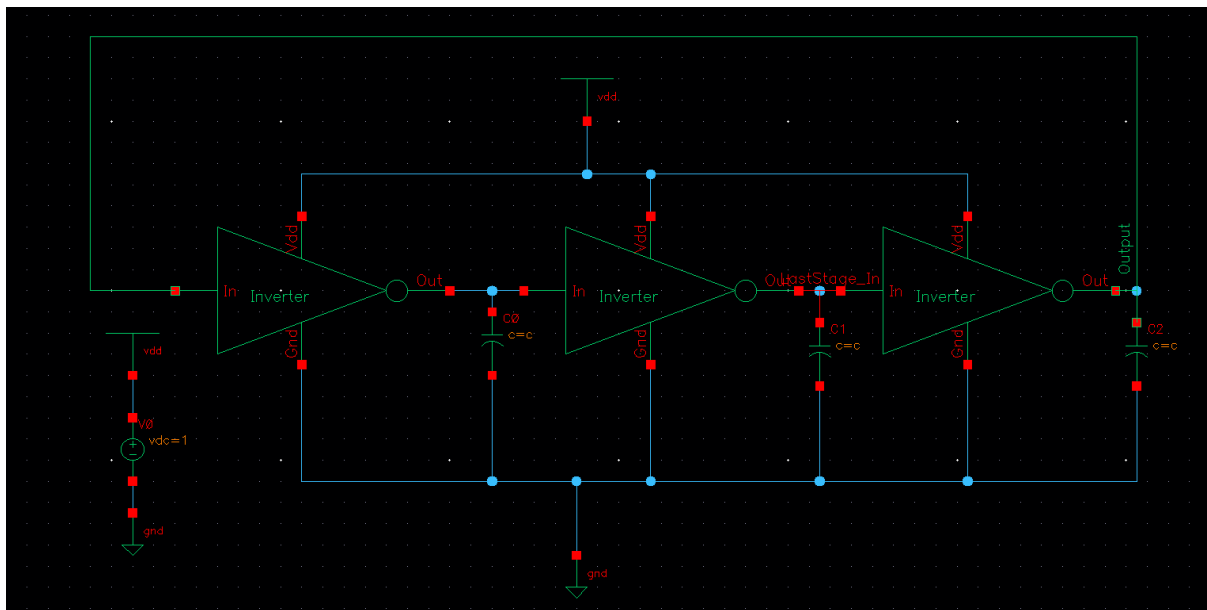


# Schematics of Oscillator:

we using three-stage ring oscillator

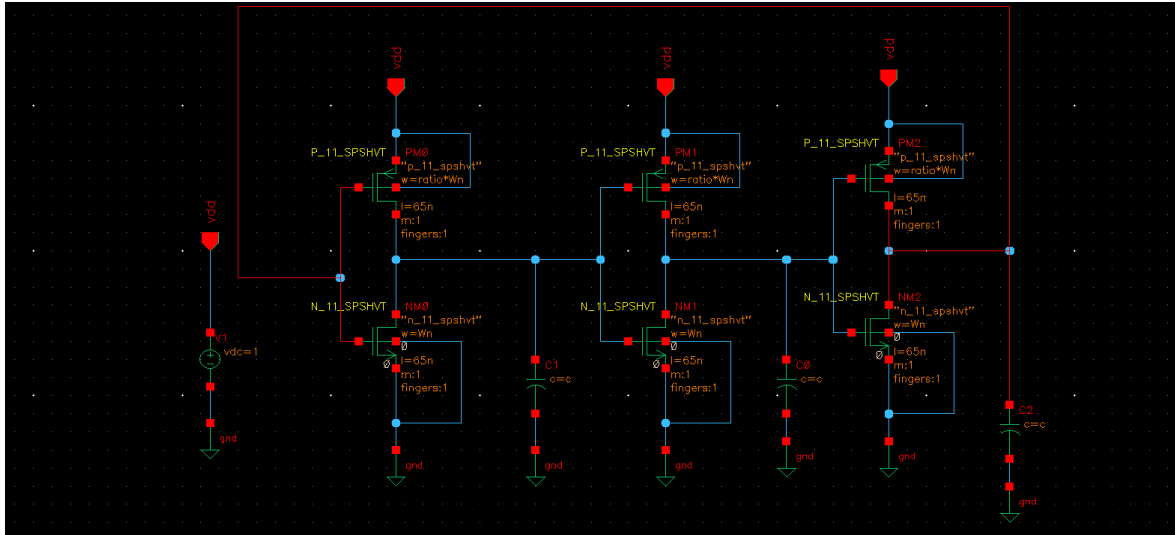


## Symbol of Oscillator:

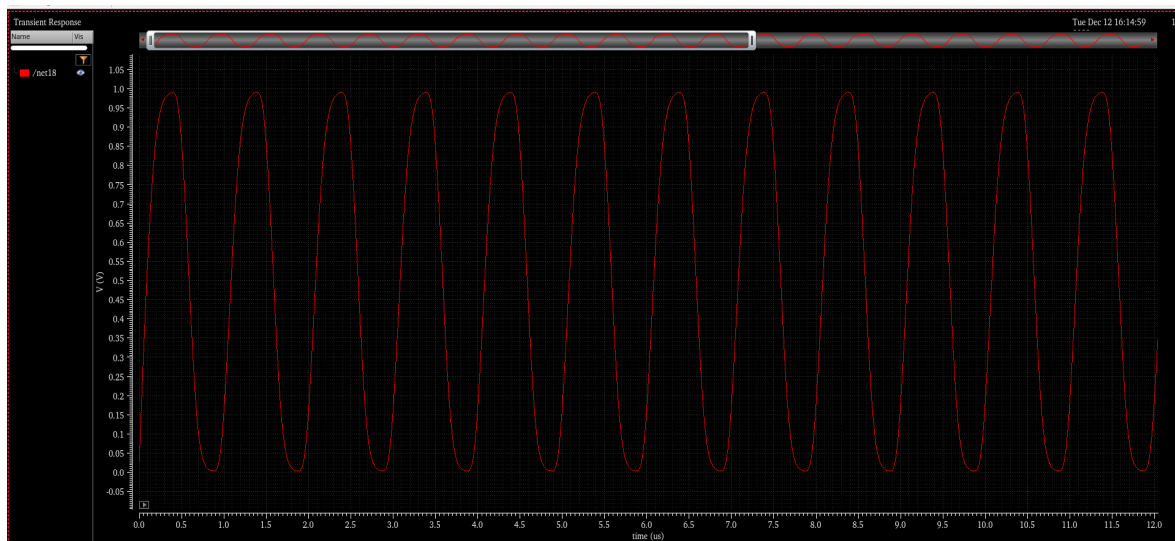


# 1M Hz Frequency:

## Schematics



## Wave



# Calculate result

The image shows the Cadence Virtuoso simulation interface. The top menu bar includes Launch, Session, Setup, Analyses, Variables, Outputs, Simulation, Results, Tools, Calibre, and Help. The top right corner displays the Cadence logo. Below the menu bar is a toolbar with various icons. The main workspace is divided into three panels:

- Design Variables:** A table with two columns: Name and Value.
- Analyses:** A table with three columns: Type, Enable, and Arguments.
- Outputs:** A table with five columns: Name/Signal/Expr, Value, Plot, Save, and Save Options.

At the bottom of the interface, there are two dropdown menus: "Plot after simulation:" set to "Auto" and "Plotting mode:" set to "Replace".

Name	Value
1 c	4.79n
2 ratio	2
3 Wn	65u

Type	Enable	Arguments
1 tran	<input checked="" type="checkbox"/>	0 10u

Name/Signal/Expr	Value	Plot	Save	Save Options
1 LastStage_In		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	allv
2 Output		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	allv
3 Delay	169.862n	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
4 Frequency	1.00131M	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
5 Power	14.3324m	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
6 V0/PLUS		<input type="checkbox"/>	<input checked="" type="checkbox"/>	yes

> Results in /home/disk/simulation/SIM\_IC61/Inv

1-Capacitor value : **4.79nF**

2-Pmos size ( $\text{Ratio} * W_n = 2 * 65\mu\text{m} = 130\mu\text{m}$ )

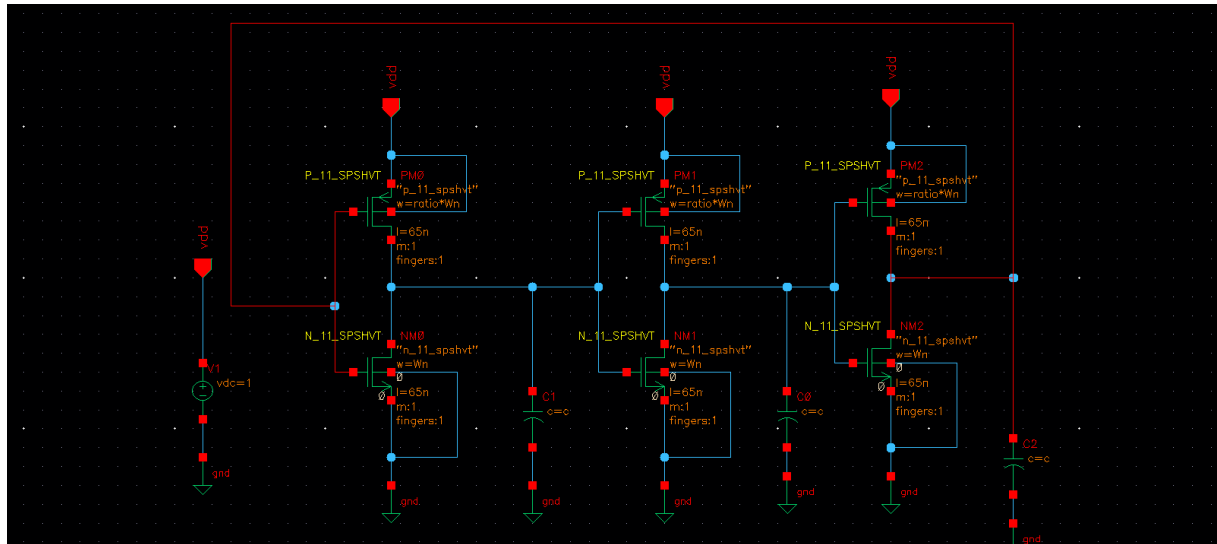
3-Nmos size ( $W_n = 65\mu\text{m}$ )

4-Power : **14.3324mW**

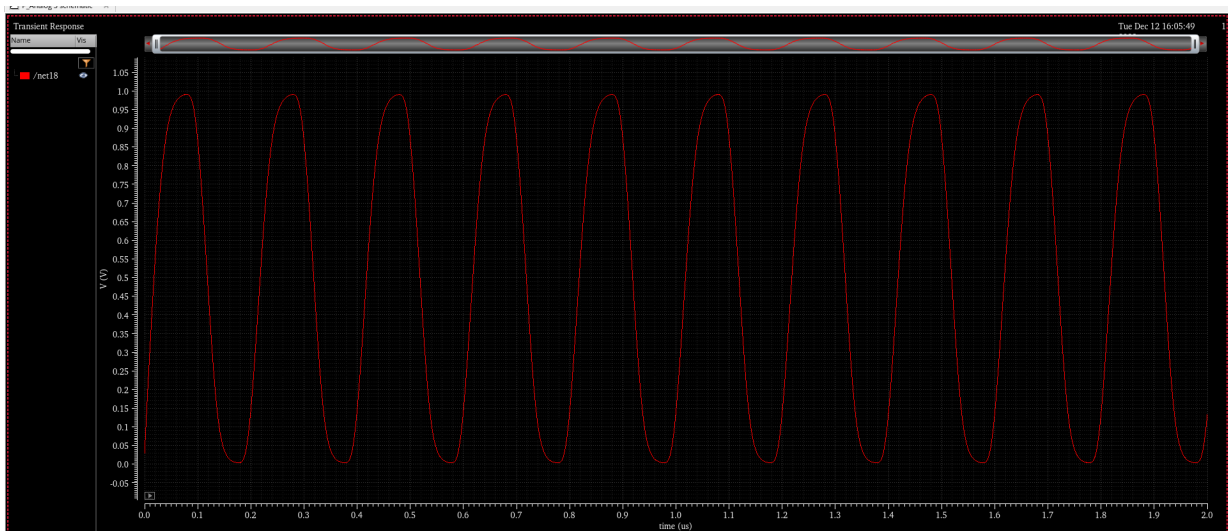
5-Delay : **169.862ns**

6-Number of stage(number of transistor) : **3 stage / 6 transistor**

# 5M Hz Frequency: Schematics



## Wave



## Calculate result

The screenshot shows the Cadence simulation environment. The top menu bar includes Launch, Session, Setup, Analyses, Variables, Outputs, Simulation, Results, Tools, Calibre, and Help. The top toolbar contains icons for file operations and simulation settings. The temperature is set to 27°C.

**Design Variables**

	Name	Value
1	c	961p
2	ratio	2
3	Wn	65u

**Analyses**

	Type	Enable	Arguments
1	tran	<input checked="" type="checkbox"/>	0 10u

**Outputs**

	Name/Signal/Expr	Value	Plot	Save	Save Options
1	LastStage_In		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	allv
2	Output		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	allv
3	Delay	34.0872n	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
4	Frequency	4.98881M	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
5	Power	14.2947m	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
6	V0/PLUS		<input type="checkbox"/>	<input checked="" type="checkbox"/>	yes

Plot after simulation: Auto Plotting mode: Replace

> Results in /home/disk/simulation/SIM\_IC61/In

1-Capacitor value : **961pF**

2-Pmos size (Ratio \* Wn = 2 \* 65μm = 130μm)

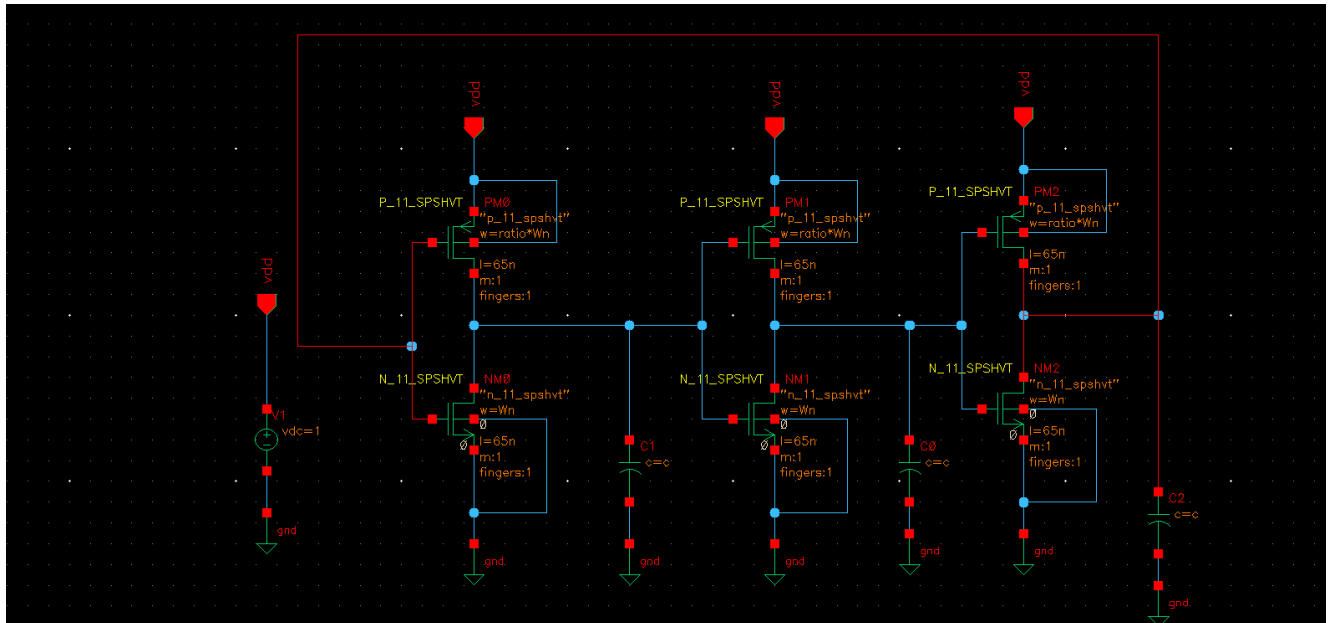
3-Nmos size (Wn = 65μm)

4-Power : **14.2947mW**

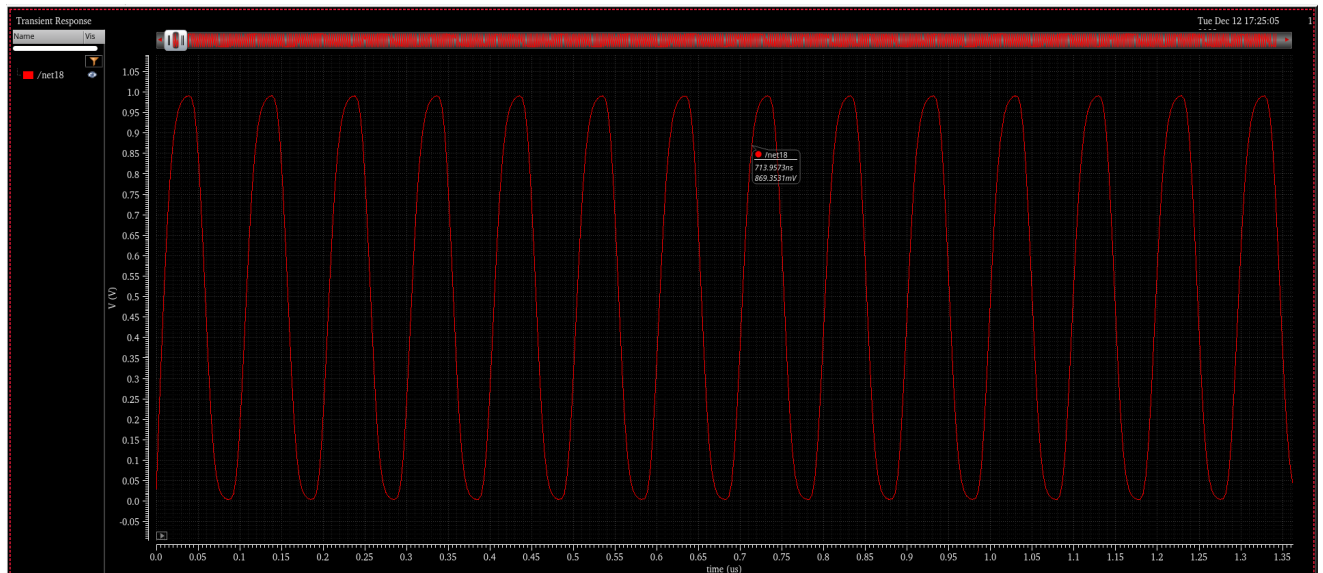
5-Delay : **34.0872ns**

6-Number of stage(number of transistor) : **3 stage / 6 transistor**

# 10M Hz Frequency: Schematics



## Wave





## Calculate result

The image shows the Cadence Virtuoso simulation interface. The top menu bar includes Launch, Session, Setup, Analyses, Variables, Outputs, Simulation, Results, Tools, Calibre, and Help. The Cadence logo is in the top right corner. Below the menu bar is a toolbar with icons for file operations, simulation, and results. The main window is divided into three panels:

- Design Variables:** A table with two columns: Name and Value.
- Analyses:** A table with three columns: Type, Enable, and Arguments.
- Outputs:** A table with five columns: Name/Signal/Expr, Value, Plot, Save, and Save Options.

At the bottom of the interface, there are two dropdown menus: "Plot after simulation:" set to "Auto" and "Plotting mode:" set to "Replace".

Name	Value
1 c	475p
2 ratio	2
3 Wn	65u

Type	Enable	Arguments
1 tran	<input checked="" type="checkbox"/>	0 10u

Name/Signal/Expr	Value	Plot	Save	Save Options
1 LastStage_In		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	allv
2 Output		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	allv
3 Delay	16.85 15n	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
4 Frequency	10.0894M	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
5 Power	14.2834m	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
6 V0/PLUS		<input type="checkbox"/>	<input checked="" type="checkbox"/>	yes

> Results in /home/disk/simulation/SIM\_IC61/In

Plot after simulation: Auto Plotting mode: Replace

1-Capacitor value : **475pF**

2-Pmos size (Ratio \* Wn = 2 \* 65μm = 130μm)

3-Nmos size (Wn = 65μm)

4-Power : **14.2834mW**

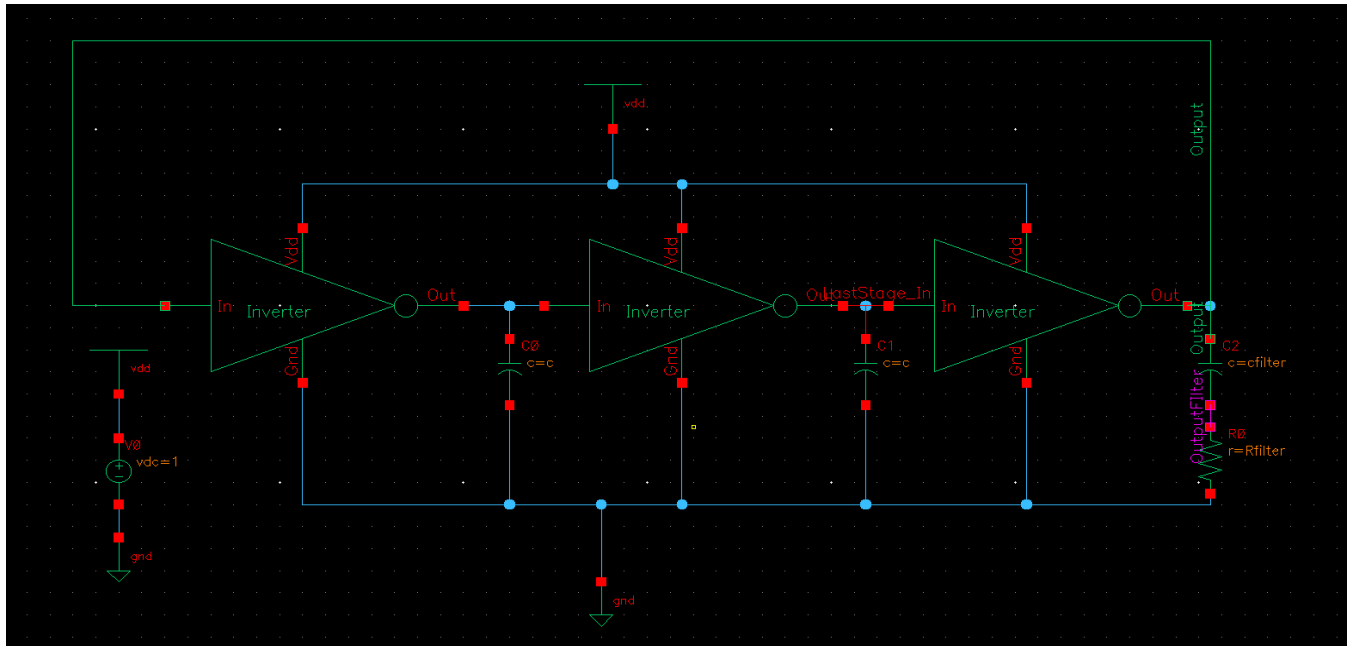
5-Delay : **16.8515ns**

6-Number of stage(number of transistor) : **3 stage / 6 transistor**

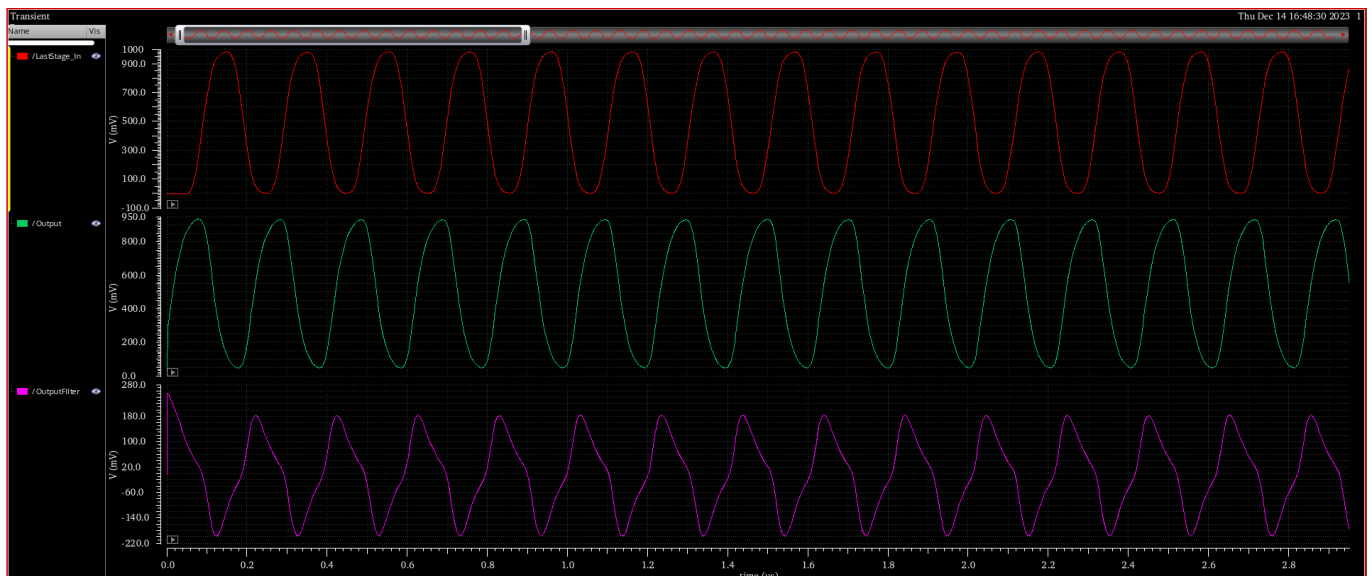
# Using Filter :

## 5MHz using high pass filter

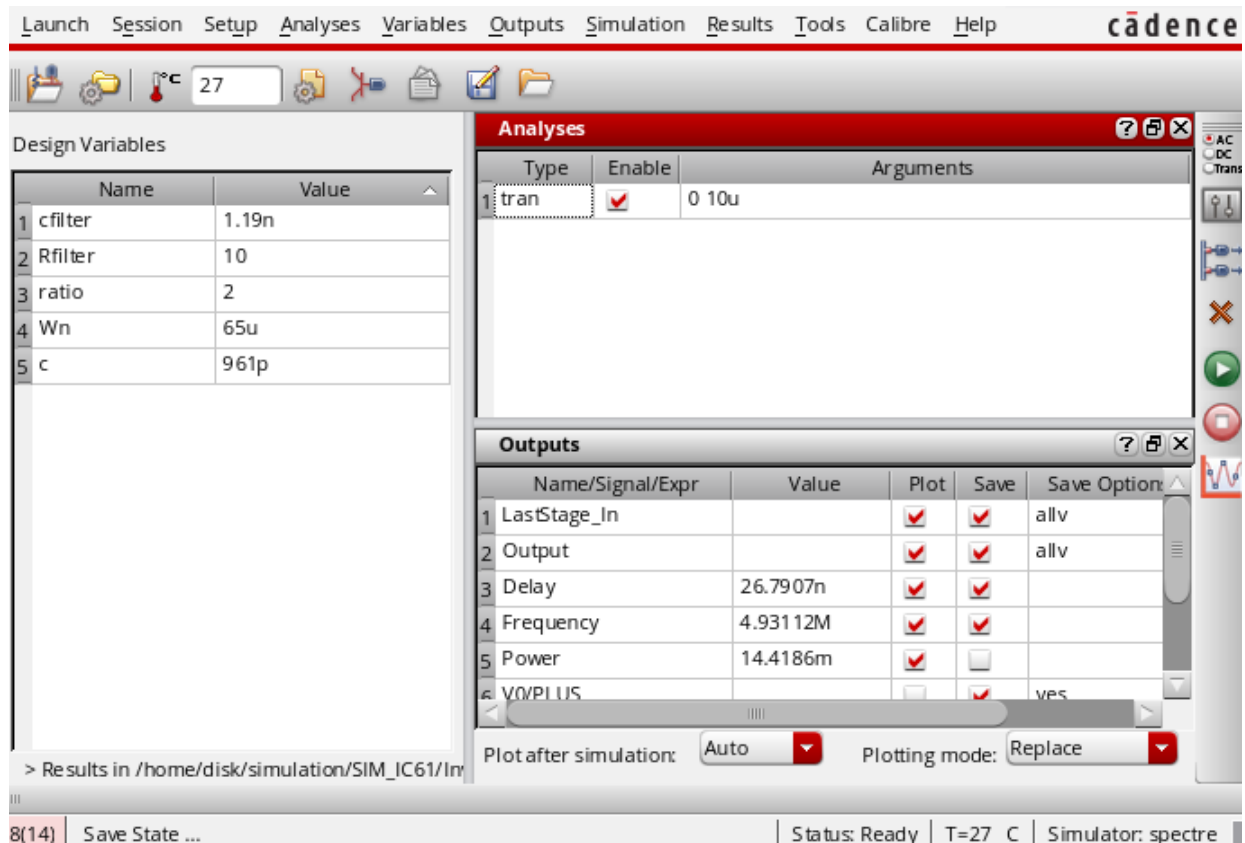
### Schematics



### Output Wave



# Calculate result



Oscillators Parameters:

- 1-Capacitor value : **961pF**
- 2-Pmos size ( $\text{Ratio} * W_n = 2 * 65\mu\text{m} = 130\mu\text{m}$ )
- 3-Nmos size ( $W_n = 65\mu\text{m}$ )
- 4-Power : **14.4186mW**
- 5-Delay : **26.79ns**
- 6-Number of stage(number of transistor) : **3 stage / 6 transistor**

High Pass Filter Parameters:

- 1-Capacitor value : **961pF**
- 2-Resistor value : **10Ω**

# Application:

## Clock signal generator

A clock signal generator is an electronic oscillator that produces a clock signal for use in synchronizing a circuit's operation. The signal can range from a simple symmetrical square wave to more complex arrangements. The basic parts that all clock generators share are a resonant circuit and an amplifier

## Discuss & conclusion

We try using 5 stage ring oscillator and 7 stage but output signal is square wave not sinusoid

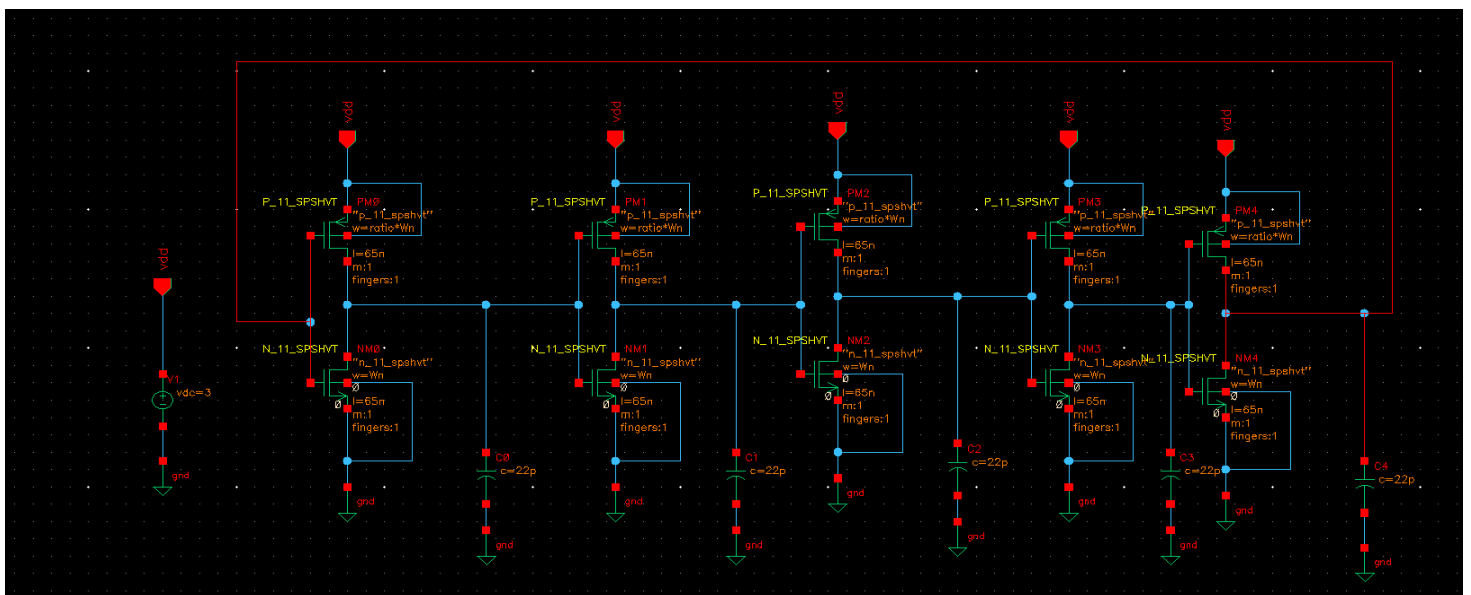
so using 3 stage ring oscillator then change in the value of capacitor and are of transistors

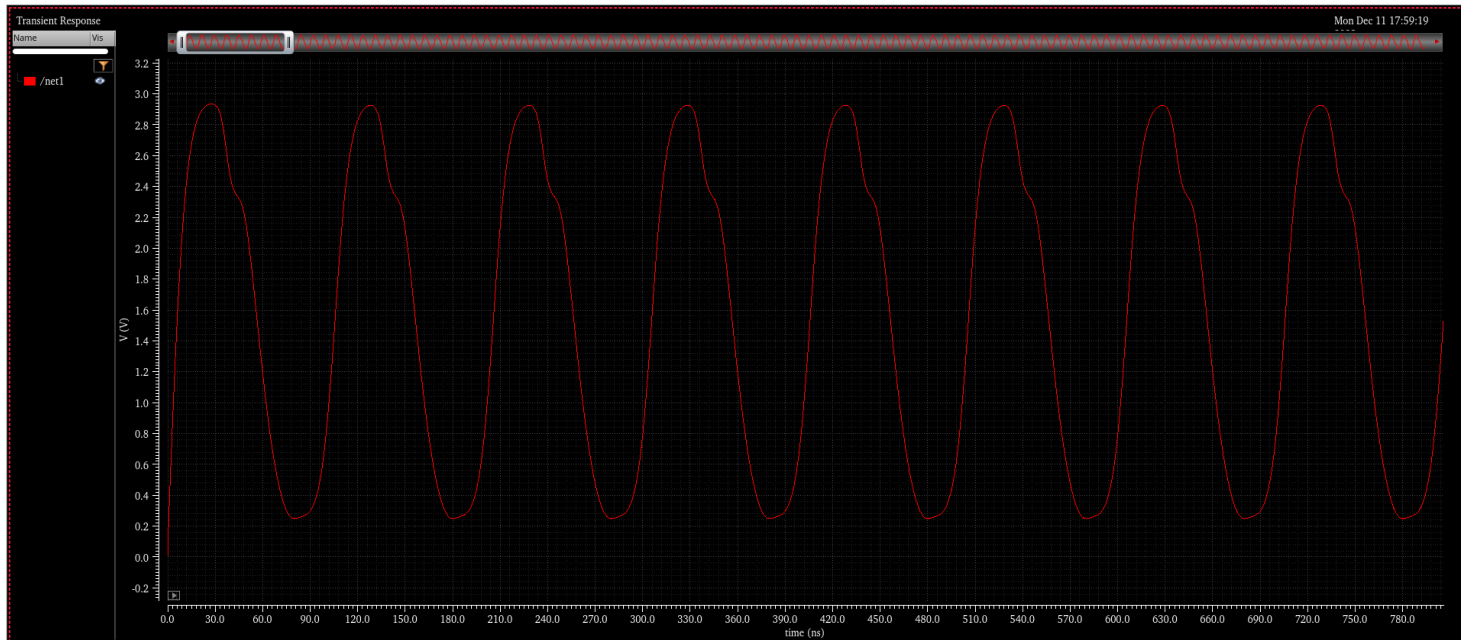
the inverter based delay,  $t_d$ , can be found out, and hence by conventional

methods we can find out the ring oscillator frequency, by the age old formula  $f = 1/2 N * t_d$

Let's assume that the delay each inverter gives is  $t_d$ . So, the net delay associated with  $N$  stages will be  $N * t_d * 2$ . This is because  $t_d$  is nothing but the difference in time of the toggle points of the input and corresponding output. We know the net phase shift should be of the order of  $2\pi$ . But the net phase shift per oscillator must be of the order of  $\pi/N$ ; as the remaining shift is obtained by the DC inversion. Now, this is one of the basic requirements that would come into play while we calculate the delay.

Now, our work involves studying of frequency response in case of an  $N$ -stage oscillator. We have seen already that frequency depends on  $t_d$ . We can say that every stage in the ring oscillator has a resistance and capacitance associated with it, which ultimately causes the delay. Now, to start with we use inverter stages using 60nm CMOS technology, with  $W_{pmos} = 65nm$ , and  $W_{nmos} = 65nm$





## conclusion:

- 1- 3 stage ring oscillator is the best of the output signal
- 2-The frequency is inversely proportional to the number of stages