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CSE 350: Digital Electronics and Pulse techniques

Exp-01: Implementing Diode Logic (DL) gates

Objectives

1. Construct Diode Logic (DL) gates.
2. Understanding the circuit operations.

Equipment and component list

Equipment

1. Digital Multimeter
2. DC power supply

Component

- NPN Transistor (C828) - x1 piece
- Diode 1N4003 - x2 pieces
- Resistors -
  - 450 Ω - x2 piece
  - 15 KΩ - x1 piece
  - 2.2 KΩ - x1 piece
  - 100 KΩ - x1 piece

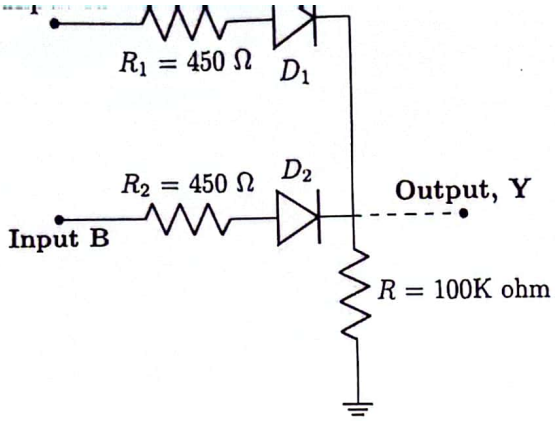


Fig 1: OR gate

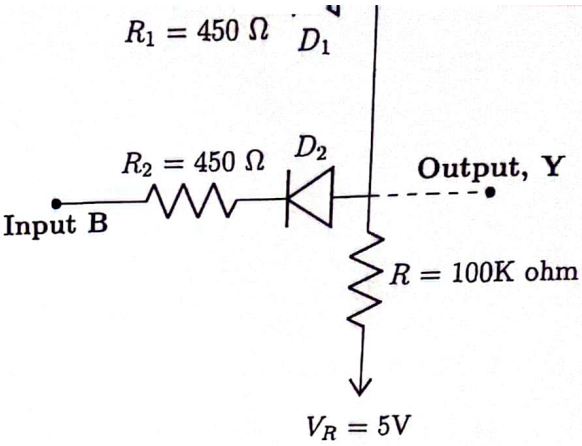


Fig 2: AND gate

Task-01: OR gate

THEORY

In digital logic, a 2-input OR gate outputs a logical HIGH if at least one of the inputs is HIGH. Otherwise, the output of the OR gate is logical LOW.
In this task, we will implement a Diode Logic (DL) OR gate. In Fig. 1, we can see two input nodes (A and B) and one output node (Y) of the OR gate. We will consider 5V as logical HIGH input and 0V as logical LOW input in our experiment. Now, if any of the inputs are set to 5V, the corresponding diode is turned on. As a result, a current flows through that diode. This current ultimately flows through R towards the ground, thus creating a voltage drop across the R resistor. As R_1 and R_2 resistors are very small compared to R, the voltage drop across R will be close to 5V. In this case, we will consider the obtained output voltage at node Y to be logically HIGH. Next, if all the inputs are set to 0V, no current flows through the diodes and resistor R. As a result, the voltage drop across R will be zero. So, the output voltage will be 0V, which we will consider to be logically LOW.

Task-02: AND gate

THEORY

In digital logic, a 2-input AND gate outputs a logical LOW if at least one of the inputs is LOW. Otherwise, the output of the AND gate is logical HIGH.
Similar to the previous task, we will implement a Diode Logic (DL) AND gate. If any of the inputs are set to 0V, the corresponding diode is turned on. As a result, a current flows through that diode from the V_R voltage source. This current flows through R and creates a voltage drop across the resistor. As R_1 and R_2 resistors are very small compared to R, the voltage drop across R will be close to 5V. As a result, the obtained output voltage at node Y will be close to 0V which we will consider as logically LOW. Next, if all the inputs are set to 5V, no current flows through the diodes and resistor R. Therefore, the voltage drop across R will be zero. So, the output voltage will be the same as V_R or 5V, which is logically HIGH.

Task-03: Inverter (NOT gate)

THEORY

In digital logic, an inverter or NOT gate is a logic gate which implements logical negation. It has a single input and a single output where the output is the exact opposite of the input. Meaning, if the input is Logical High, the output will be Logical Low and vice versa. The RTL implementation of an inverter circuit is shown in Figure 03.
Here the input is applied to the base of a Transistor or, BJT (Q_1) through the resistor R_1 and the output is available at the collector terminal (point Y). We connect the ground terminal to the emitter node directly and to the base node through the resistor R_2. Hence, when the input V_i is LOW (0V), the 'Base' terminal

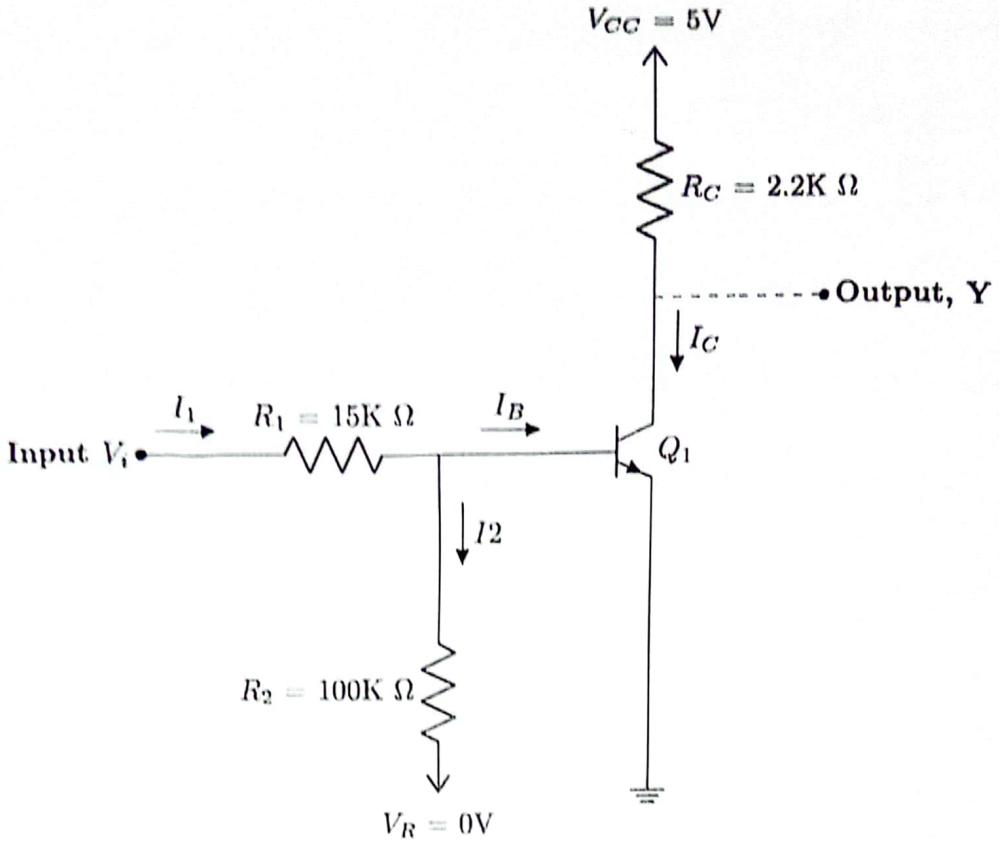


Fig 3: Inverter (NOT gate)

of the transistor cannot be at a voltage higher than zero. For Q1 to be turned ON, the Base-Emitter voltage difference must be greater then 0.5V. Thus, the BJT cannot turn ON when the input is LOW and operates in cutoff mode. This means Q_1 acts like an open circuit and the current passing through the R_C resistor (I_C) is zero. As a result, there will be no voltage drop in the resistor R_C and the voltage of the output point (Y) will be same as V_{CC} = 5V (High).
On the other hand, if a HIGH input (5V) is applied at the input terminal (V_i), Q_1 will be driven into saturation mode. In this mode, the Collector-Emitter voltage difference (V_{CE}) is nearly 0.2V. As the emitter is connected to the ground terminal, the emitter voltage (V_E) is zero. Hence, the collector voltage will be close to 0.2V(LOW). Thus, the output of the circuit is always the opposite of the input.

Procedure:

1. Connect the circuit as shown in Fig: 1, 2 & 3.
2. Observe the output for all possible input combinations and thus verify the type of gate.
3. Fill up the following tables for OR gate, AND gate and Inverter.

Data Tables

$V_A(V)$	$V_B(V)$	$V_{R1}(V)$	$V_{R2}(V)$	$I_{R1}(mA)$	$I_{R2}(mA)$	$V_Y(V)$
0	0	0	0	0	0	0
0	5	0	0.7	0	1.55	4.1
5	0	0.7	0	1.55	0	4.1
5	5	0.35	0.35	0.77	0.77	4.29

Table 1: Table for OR Gate

$V_A(V)$	$V_B(V)$	$V_{R1}(V)$	$V_{R2}(V)$	$I_{R1}(mA)$	$I_{R2}(mA)$	$V_Y(V)$
0	0	0.7	0.7	1.55	1.55	0
0	5	0.7	0	1.55	0	0.67
5	0	0	0.7	0	1.55	0.67
5	5	0	0	0	0	5

Table 2: Table for AND Gate

V_i (V)	V_{R1} (V)	V_{R2} (V)	V_{Rc} (V)	I_1 (mA)	I_2 (mA)	I_B (mA)	I_C (mA)	V_Y (V)
0	0	0	0	0	0	0	0	5
5	4.3	0	4.8	0.286	0.043	0.043	2.18	0.2

Table 3: Table for RTL inverter

Report

Please answer the following questions briefly in the given space.

1. Verify that the transistor will be operating in the saturation and cutoff region in two cases for the inverter circuit (Use experimental data for verification).

Ans. From data at V_A and $V_B = 0.0V$, $I_B = I_C$ and $I_E = I_B + I_C$ =

So this is cutoff region. So in V_i = Low then transistor in cutoff region. When $V_i = 5.03V$ then $I_B = 0.266mA$ and $I_C = 2.31mA$. We know at saturation region $\frac{I_C}{I_B} < \beta$ .so, It is in saturation region.

2. For OR gate circuit, should I_{R_1} and I_{R_2} be equal theoretically when $V_A = V_B = 5V$? Did you obtain a similar result in your experiment? Explain briefly.

Ans. At $V_A = V_B = 5V$, we get values for I_{R_1}, $I_{R_2} = 0mA$

$R_1 = R_2$ which are connected across 5V & 0.7V voltage drop across resistor is same. So, current will be same. But I didn't get similar result in experiment. It both has little different and not similar with if 1 voltage has changed with other voltage input.

3. (For both OR & AND gate circuits) Will the diodes D_1 and D_2 turn ON, if $V_A = V_B = 6V$ and $V_R = 5V$? Explain briefly.

Ans. For OR gate,

$V_R = 5V$; $I_R = \frac{5-0}{100} = 0.05mA$

V_B ; $I_{R_1} = I_{R_2} = 0.025mA$

$\therefore 0.025 = \frac{6-x}{0.450} \Rightarrow x = 5.99V$

It is great than 5+0.7V so, D_1 & D_2 will be on.

For AND Gate,

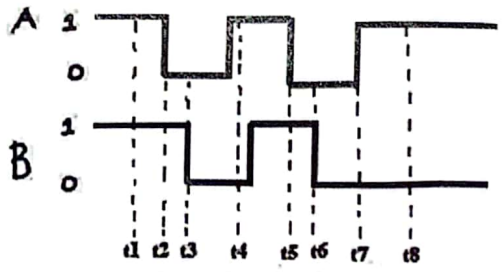
$x = 5.99 \not< 0.7$.

So D_1 and D_2 will be off.

4. What is the function of $V_R = 0V$ at the base of an inverter in figure 3?
Ans.

$V_R = 0V$ means input voltage V_i is Low, the base-emitter voltage V_{BE} is insufficient to turn on the transistor. It is cutoff region.

5. Assuming OR gate, Draw the output.



Ans.

time	A	B	output
t_1	1	1	1
t_2	0	1	1
t_3	0	0	0
t_4	1	0	1
t_5	0	1	1
t_6	0	0	0
t_7	1	0	1
t_8	1	1	1

Data Tables

$V_A(V)$	$V_B(V)$	$V_{R1}(V)$	$V_{R2}(V)$	$I_{R1}(mA)$	$I_{R2}(mA)$	$V_Y(V)$
0	0	0	0	0	0	0.07
0	5.03	0	677 mV	0	1.447	3.73
5.03	0	666mV	0	1.442	0	3.72
5.03	5.03	368 mV	376.4mV	0.796	0.814	4.06

Table 4: Table for OR Gate

$V_A(V)$	$V_B(V)$	$V_{R1}(V)$	$V_{R2}(V)$	$I_{R1}(mA)$	$I_{R2}(mA)$	$V_Y(V)$
0	0	5.7mV	21.4mV	0.012	0.045	0.419
0	5.03	21.5mV	0.4mV	0.465	0.008	0.4
5.03	0	0	21.4mV	0	0.045	0.446
5.03	5.03	0	0.4mV	0.011	0	4.97

Table 5: Table for AND Gate

V_i (V)	V_{R1} (V)	V_{R2} (V)	V_{RC} (V)	I_1 (mA)	I_2 (mA)	I_B (mA)	I_C (mA)	V_Y (V)
0	0	1.7 mV	2.1mV	0	1.72	-1.72	0.976	5.02
5.03	4.08	0.68	4.97	0.272	0.006	0.266	2.31	34mV

Table 6: Table for RTL inverter

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