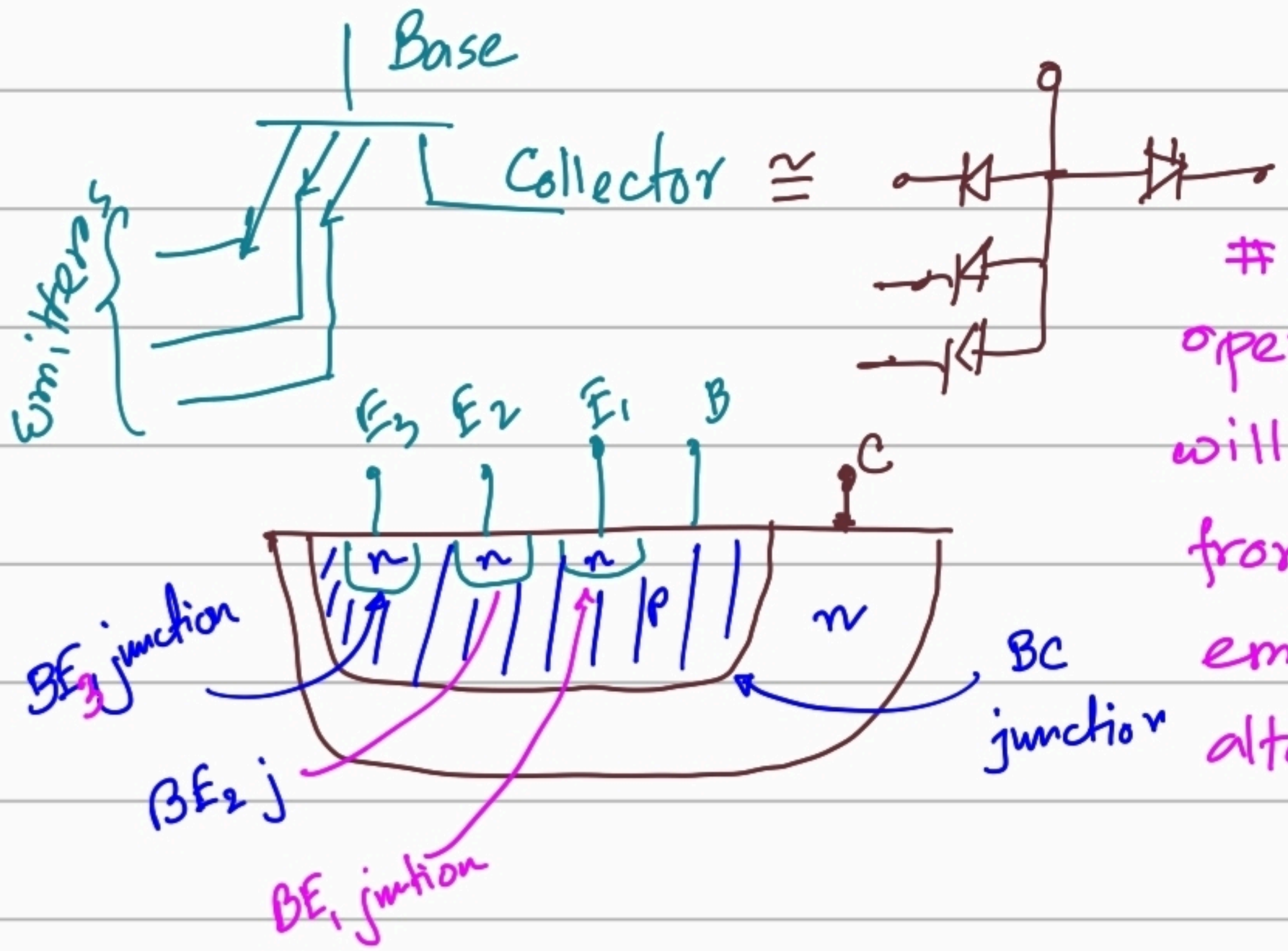
"Transistor-Transistor Logic"

Bipolar, → Saturated → TTL

BJT Switching time is faster than DTL.

The input terminals are connected to the emitter terminal of a transistor and the output terminal is connected to a switching transistor.

input terminals will be connected to multi-emitter transistor.



Transistor's operating mode will be determined from three emitter inputs altogether.

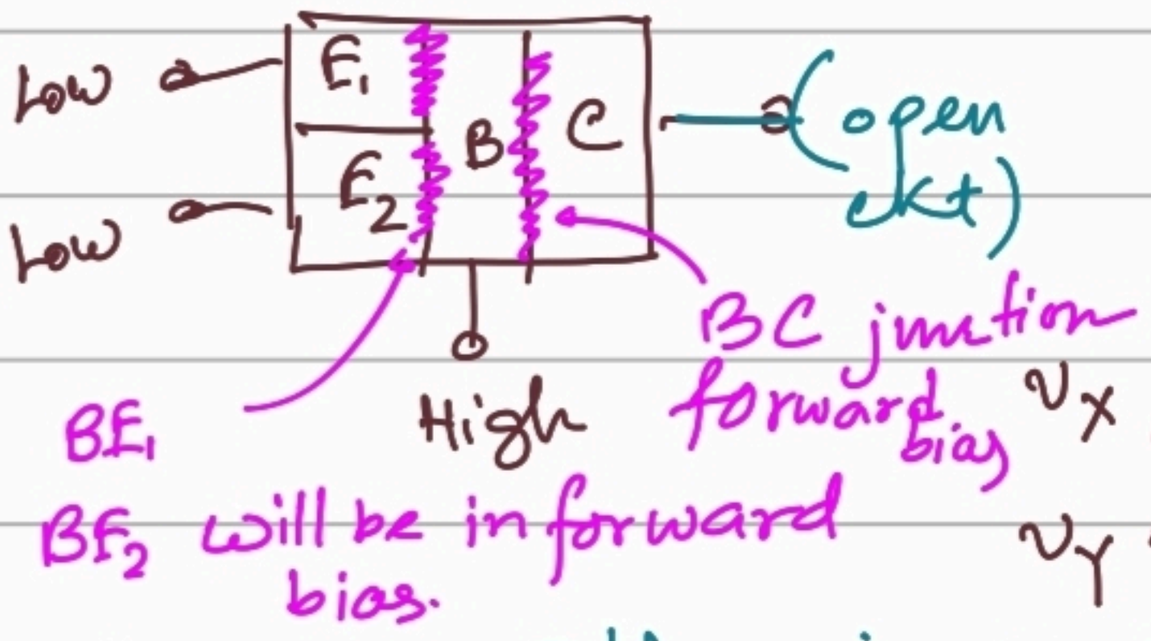
Basic Operation:

find out the current and voltage of the following gate. Verify that it works like a NAND gate.

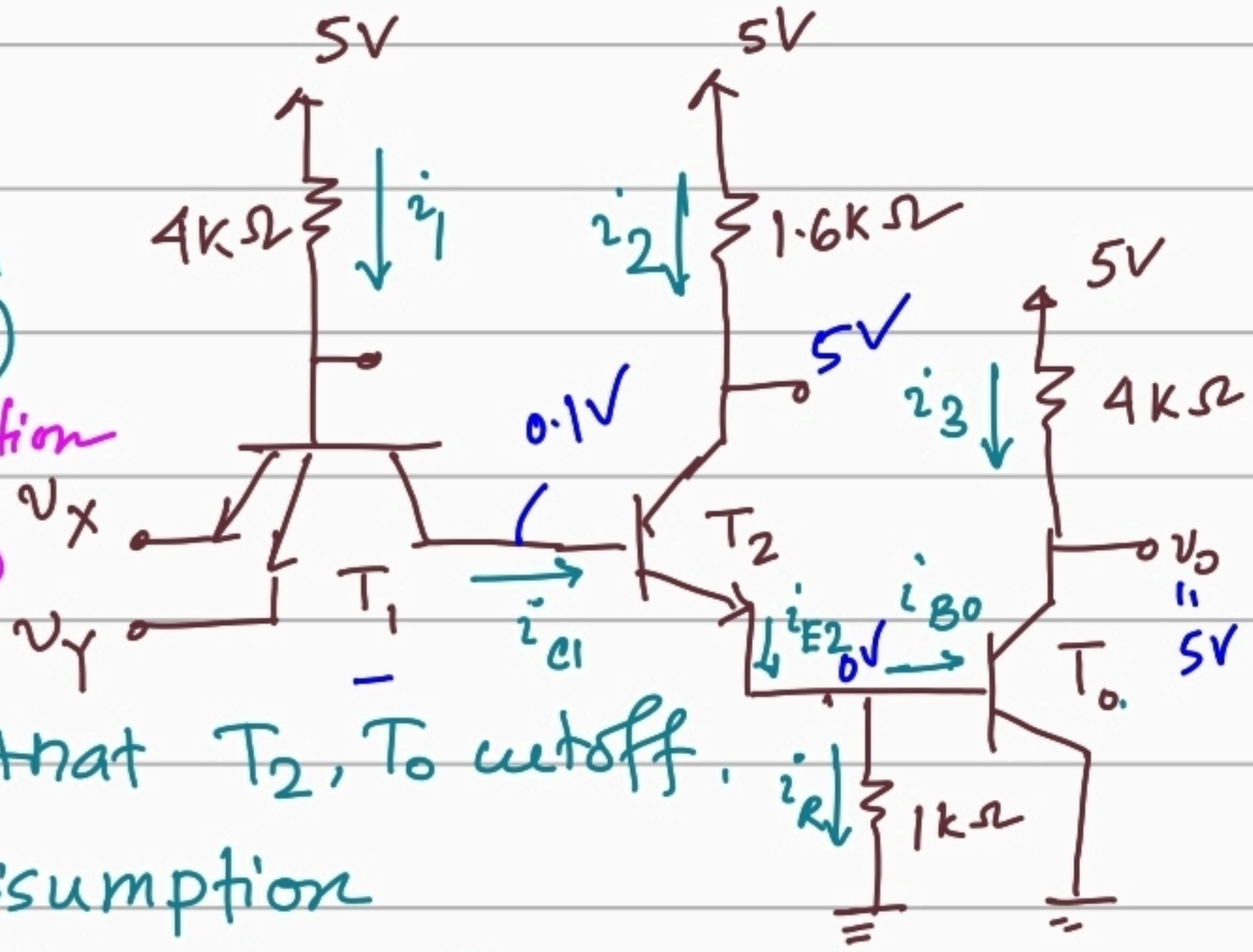
Case ①. $v_x = v_Y = 0.1V$ [Neaman] $v_{CE}(sat) = 0.1V$

$v_{BE}(sat) = 0.8V$

For T_1 transistor



BE_2 will be in forward bias.



Our assumption is that T_2, T_0 cutoff.

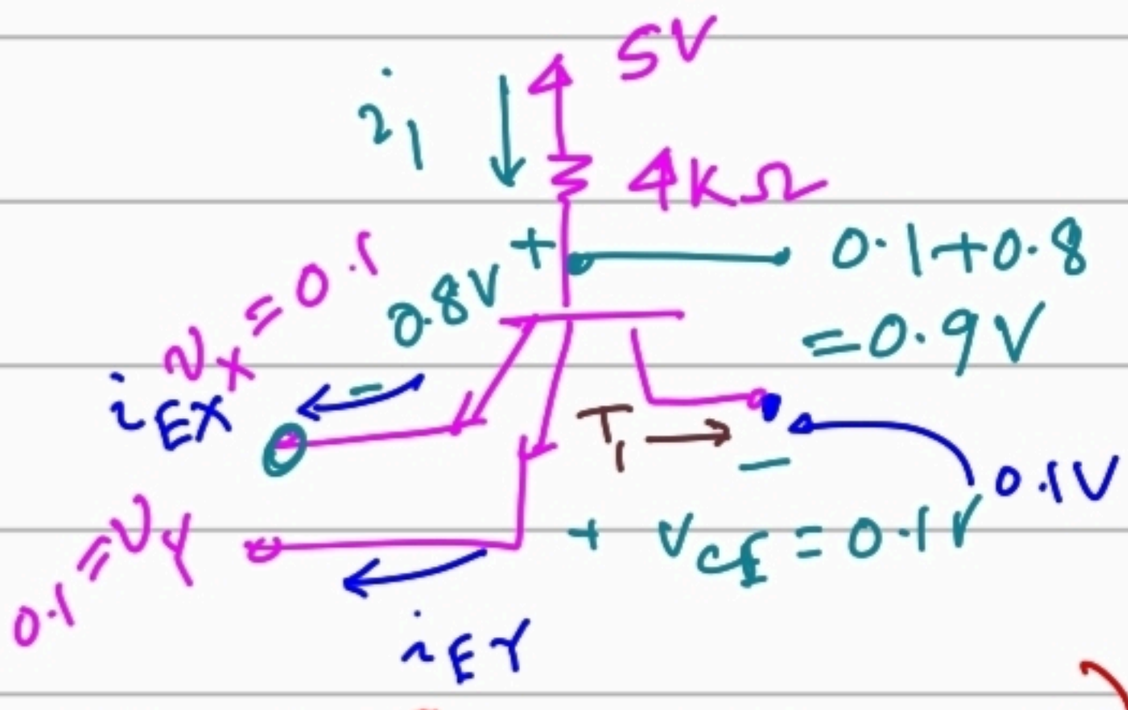
According to our assumption

$$i_2 = i_3 = i_R = i_{B0} = i_{E2} = i_{C1} = 0 \text{ mA}$$

Bonus Question: B-C terminal's bias ?

Ans: If B-C reverse bias, T_1 will be in forward active but for forward active we need. $i_C = \beta i_B$. But $i_C = 0$. Therefore not possible.

Hence T_1 must be in saturation mode. ⇒ Bc-junction is in forward bias



$$i_1 = \frac{5 - 0.9}{4K\Omega} = 1.125 \text{ mA}$$

$$i_{EX} = i_{EY} = \frac{i_1}{2} = 0.5625 \text{ mA}$$

$\beta_{forced} = \frac{i_C}{i_B} = 0 < \beta_F$. Our assumption is valid.

Case ② ($v_x = 0.2V$, $v_y = 5V$) / $v_y = 0.2V$, $v_x = 5V$

$T_1 \rightarrow$ saturation.

T_0, $T_2 \rightarrow$ cutoff.

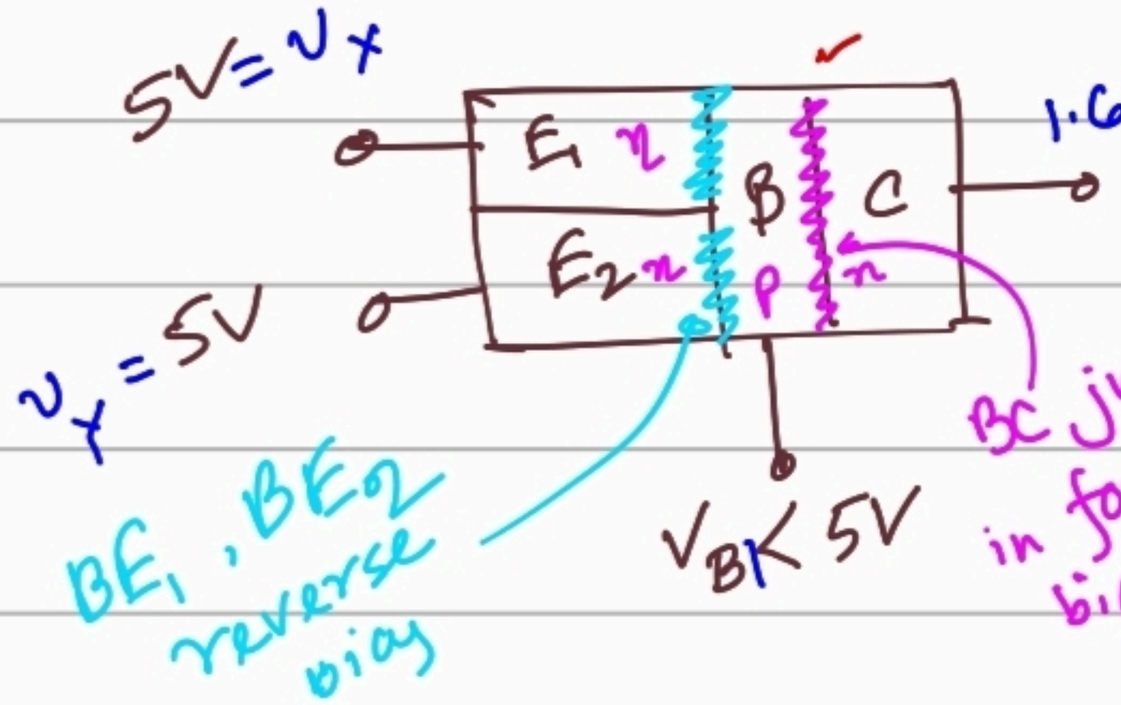
$$i_2 = i_3 = i_{B0} = i_{E2} = i_{C1} = i_R = 0$$

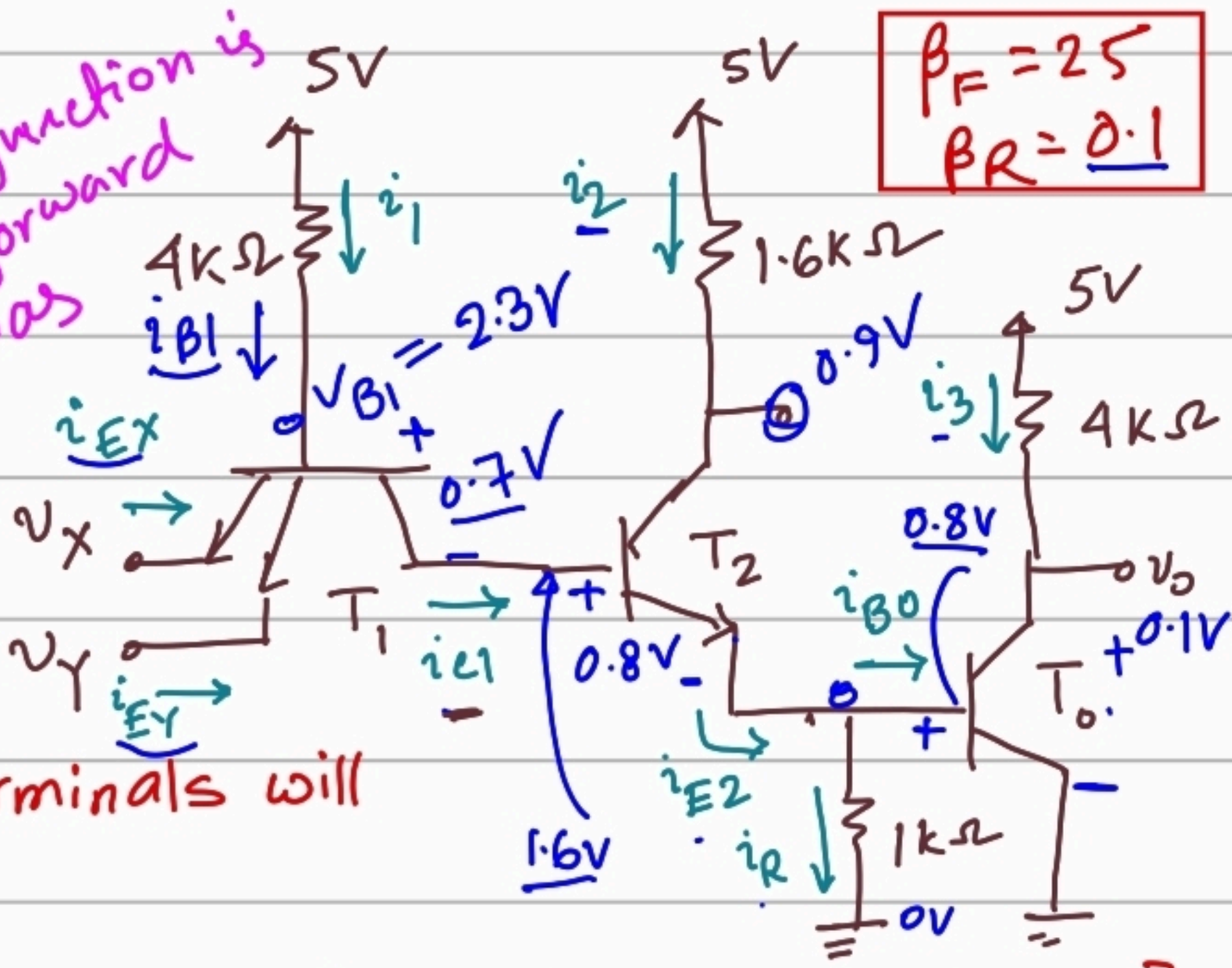
$i_1 = 1.125$ mA. $\boxed{i_{EX} = i_1,\ i_{EY} = 0}$

Case 3: $v_X = v_Y = 5V$ | Assumption:

$T_0, T_2 \rightarrow$ saturation

$v_{CE}(sat) = 0.1\,V$, $v_{BE}(sat) = 0.8V$





T_1 transistor must be in rerverse active mode.

Collector and Emitter terminals will switch their roles.

$V_{BC}(\text{reverse active}) = 0.7V$. [because BC junction is in forward bias]

$(i_{EX} = \beta_R i_B = i_{EY})$ β_R = reverse active current gain.

$i_{B1} = i_1 = \frac{5 - 2.3}{4k} = 0.675mA$, $i_2 = \frac{5 - 0.9}{1.6k} = 2.5625mA$.

$i_3 = \frac{5 - 0.1}{4k} = 1.225mA$, $i_{EX} = i_{EY} = \beta_R i_{B1} = 0.0675mA$

$i_{C1} = i_{EX} + i_{EY} + i_{B1} = 0.81mA$, $i_{E2} = i_2 + i_{C1} = 3.3725\,mA$,

$i_R = \frac{0.8 - 0}{1k} = 0.8mA$, $i_{B0} = i_{E2} - i_R = 2.5725mA$

$\beta_{forced}(T_2) = \frac{i_2}{i_{C1}} = \frac{2.5625}{0.81} = 3.16 < \beta_F = 25$

$\beta_{forced}(T_0) = \frac{i_3}{i_{B0}} = \frac{1.225}{2.5725} \approx 0.47 < \beta_F = 25$

Our assumptions are valid.

v_X	v_Y	v_0
0.1	0.1	5
0.1	5	5
5	0.1	5
5	5	0.1

This circuit works like a NAND gate.