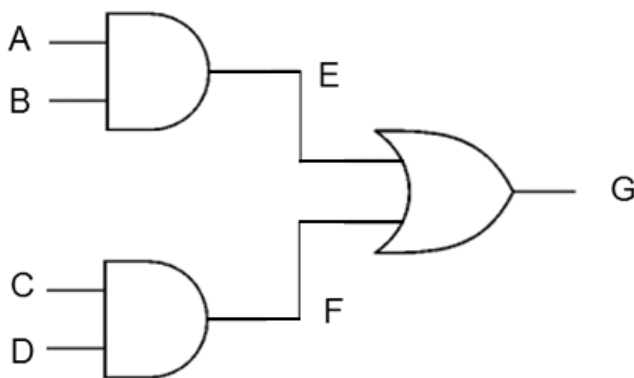Here suppose R1 = 10k, R2 = 20k, Rx = 1k, Cx = 1 nF, VH = 10V and VL = -5V

Find out the duty cycle of inverted output signal of the above circuit.

CMOS logic design

1. Design a CMOS logic circuit to implement the given compound gate in Figure below. First derive the logical expression of output Y and then design the CMOS network.

2. a) Design a static CMOS logic circuit that implements the logic function Y= AB

   b) Design a static CMOS logic circuit that implements the logic function Y= (A+B)

3. Design a static CMOS logic circuit that will implement the following logic

   a. NAND gate ($Y = \overline{AB}$)

   b. XOR gate ($Y = A\overline{B} + \overline{A}B$)

3. Design a static CMOS logic circuit that will implement the following logic

   a. NOR gate ($Y = \overline{A + B}$)

   b. XNOR gate ($Y = AB + \overline{AB}$)

4. Design static CMOS circuit for the following expression,

   a. Y = AB + CD

b. Y = AB +C

c. Y = (A+B)C

d. Y = (A+B)(C+D)

e. Y = $\overline{AB + CD}$

f. Y = $\overline{AB + C}$

g. Y = $\overline{(A + B)C}$

h. Y = $\overline{(A + B)(C + D)}$

i. $Y = \overline{A} + \overline{B} + \overline{C}$

5.

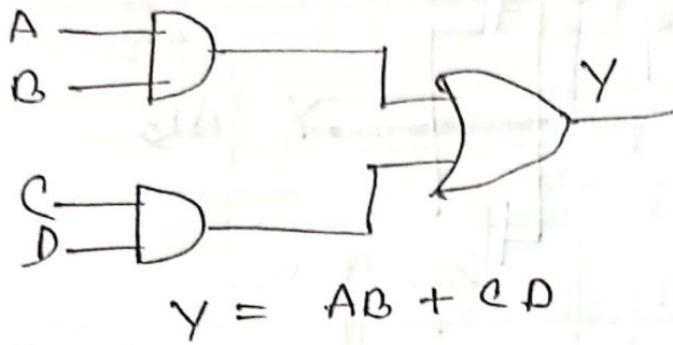**Truth Table**

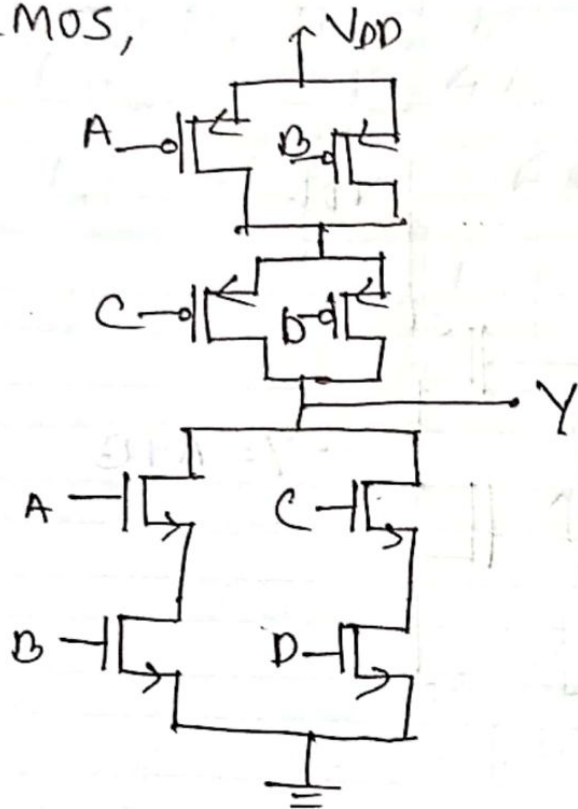| Input A	Input B	Output
0	0	1
0	1	0
1	0	0
1	1	1

Design a static CMOS logic circuit that will implement the above truth table.

CMOS logic design

1.

$$Y = AB + CD$$

CMOS,

2. a) $Y = A \cdot B$

$Y = AB$
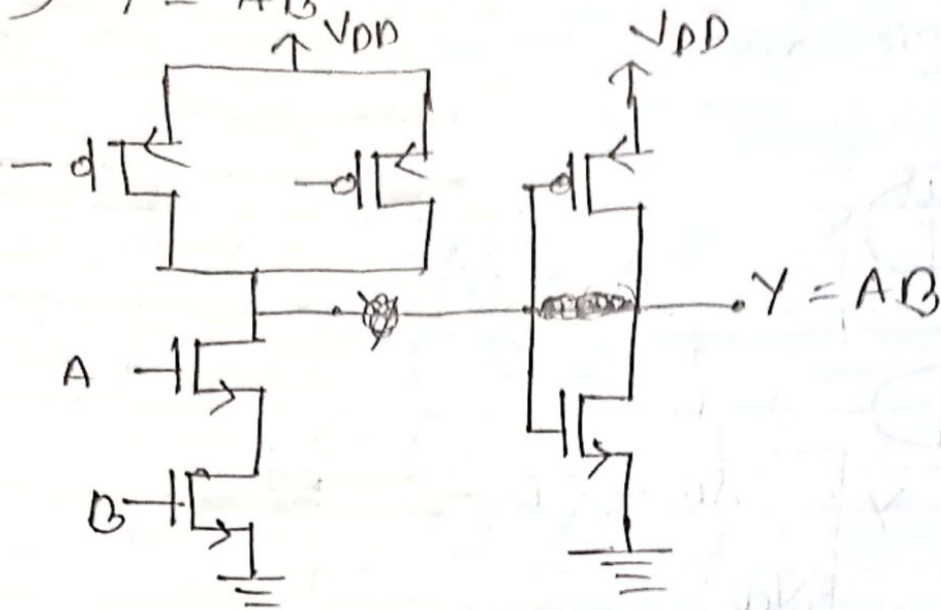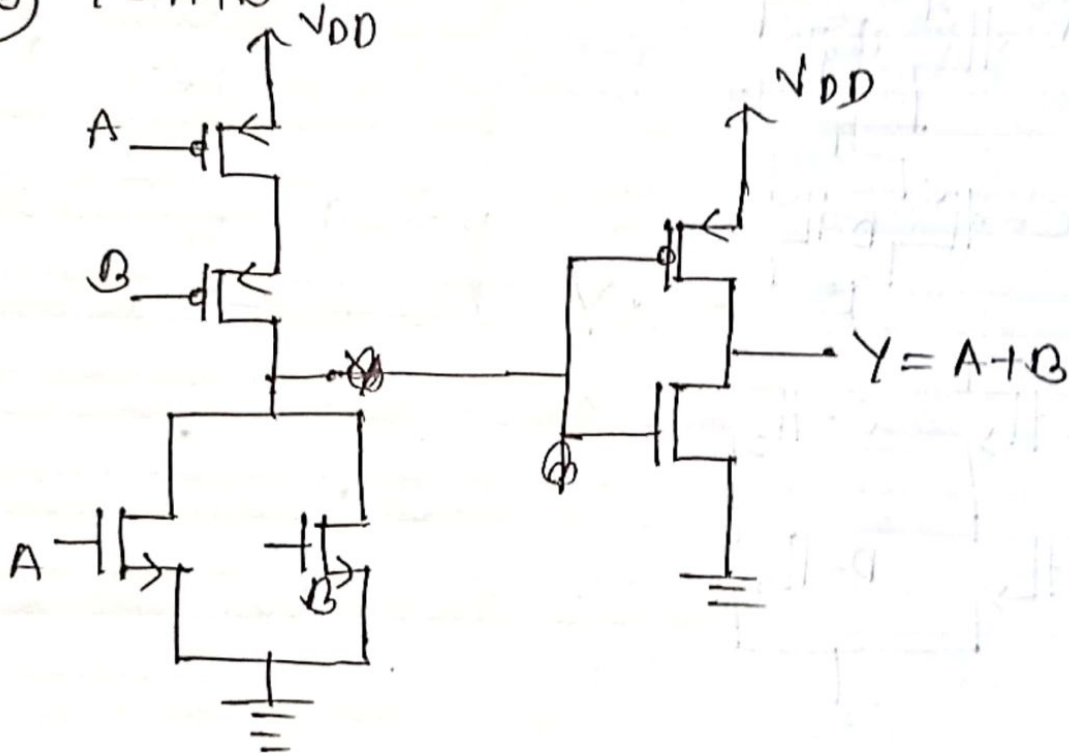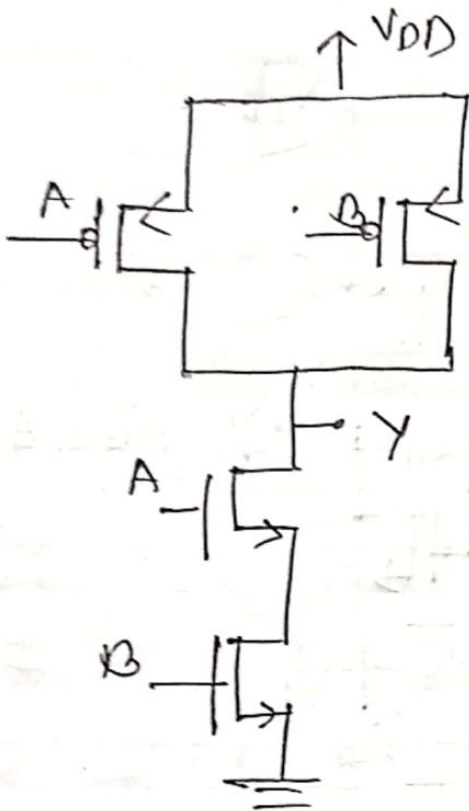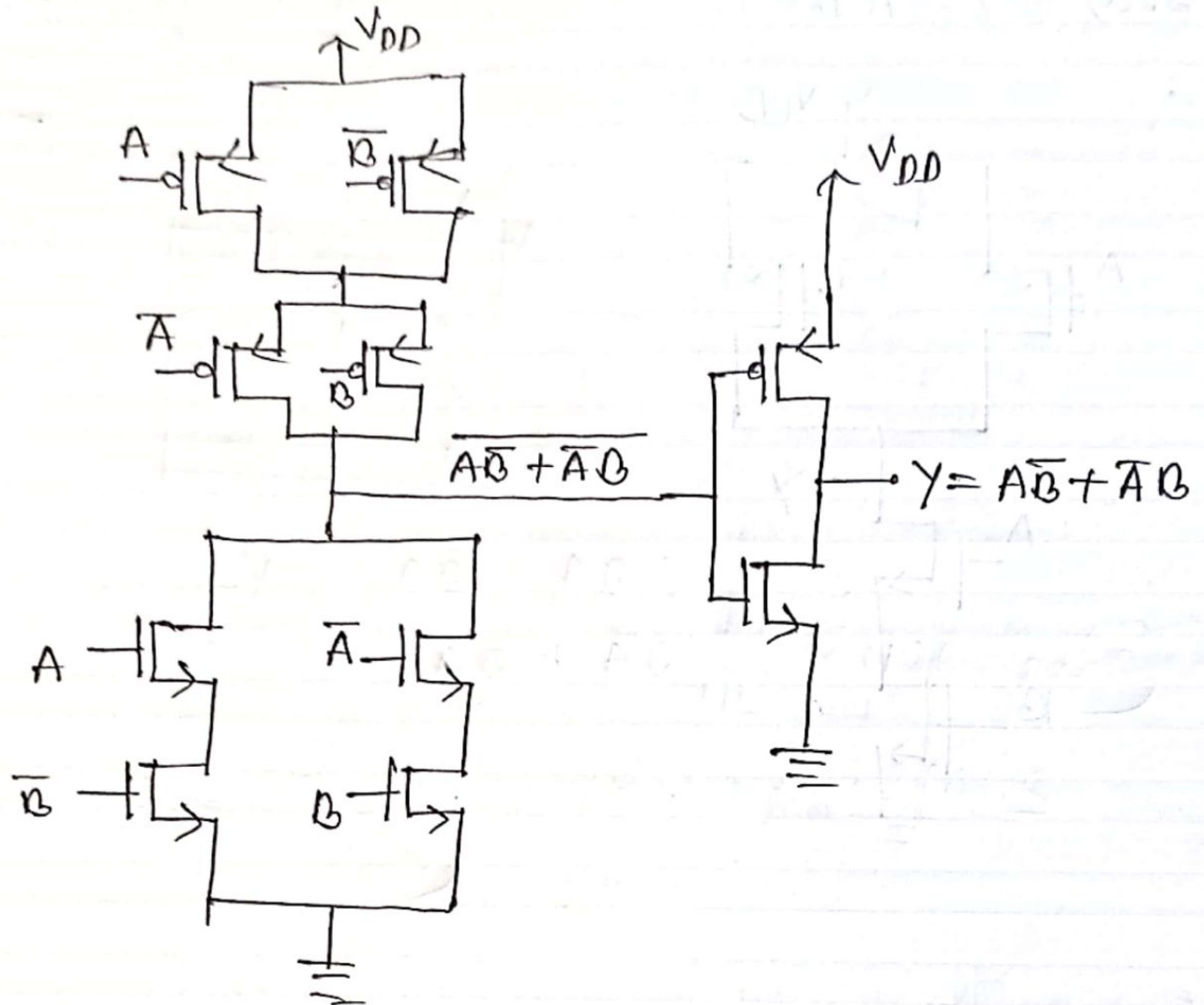
2. b) $Y = A + B$

$Y = A + B$

3. a) $Y = \overline{A \cdot B}$

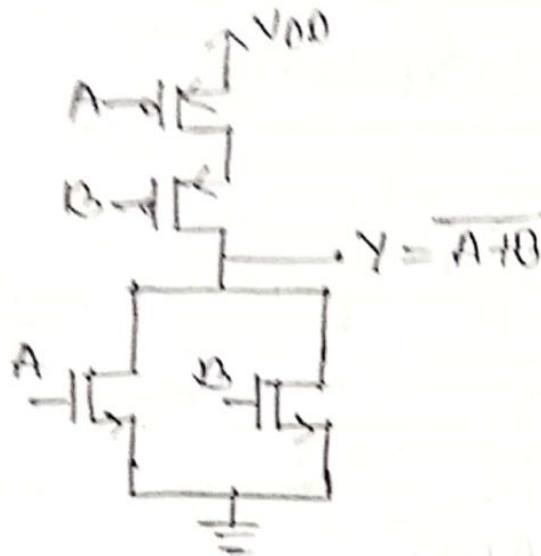8. b) $Y = A\bar{B} + \bar{A}B$

$\overline{A\bar{B} + \bar{A}B}$

$Y = A\bar{B} + \bar{A}B$

[2 number is done]

2. a) $Y = \overline{A+B}$

$Y = \overline{A+B}$

3. $Y = AB + \overline{A}\,\overline{B}$ (connection)
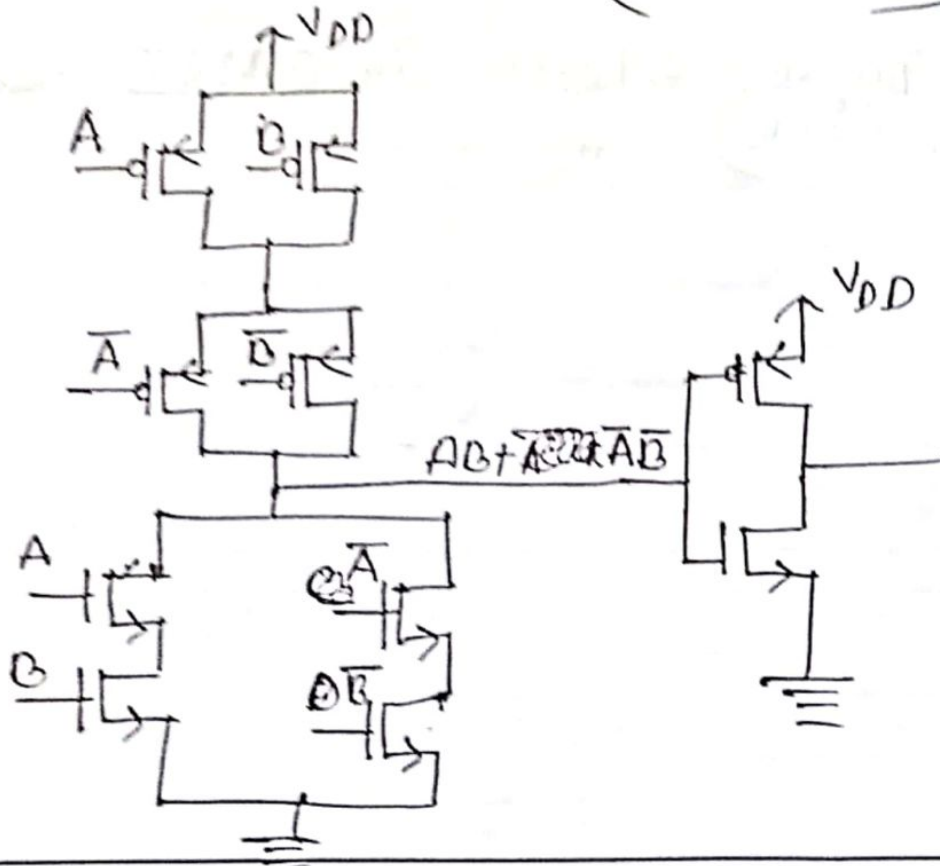
$AB + \overline{A}\,\overline{B}$

4. Try Yourself

5.

A	B	Y
0	0	(1)
0	1	0
1	0	0
1	1	(1)

$$y = \overline{A}\,\overline{B} + AB$$
$$= AB + \overline{A}\,\overline{B} \quad (\text{XNOR Gate})$$

See previous solution for CMOS
(*3 (6))