



BRAC UNIVERSITY

CSE 350: Digital Electronics and Pulse techniques

Exp-02: Implementing Diode Transistor Logic (DTL) gates

Objectives

1. Constructing a Diode Transistor Logic (DTL) gate.
2. Understanding the circuit operations.

Equipment and component list

Equipment

1. Digital Multimeter
2. DC power supply

Component

- NPN Transistor (C828) - x1 piece
- Diode 1N4003 - x4 pieces
- Resistors -
 - ◆ 2 K Ω - x2 pieces
 - ◆ 20 K Ω - x1 piece

Task-01: DTL NAND gate

THEORY

In this task, we will implement a Diode Transistor Logic (DTL) NAND gate. As can be seen in Fig. 1, a 2-input NAND gate outputs a logical HIGH if at least one of the inputs is LOW. Otherwise, the output of the NAND gate is logical LOW. It can be created by passing the output of a AND gate through an Inverter or NOT gate. One can build all other logic gates using such NAND gates. The DTL implementation of a NAND circuit is shown in Fig. 2.

Diode-transistor logic (DTL) is a class of digital circuits that is the direct predecessor of transistor-transistor logic (TTL) and the successor of resistor-transistor logic (RTL). The output side of the basic DTL NAND circuit

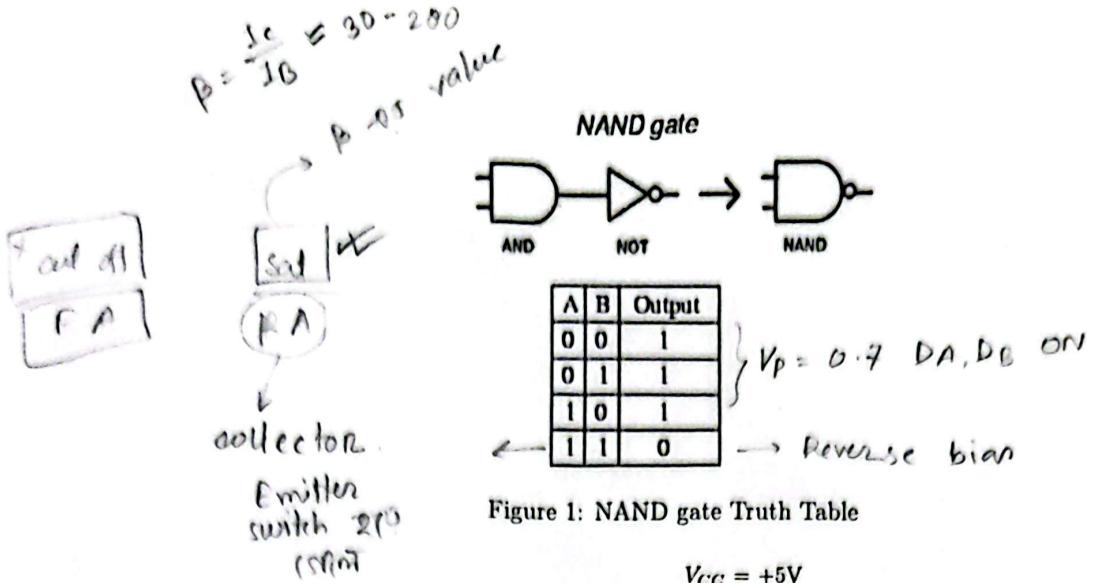


Figure 1: NAND gate Truth Table

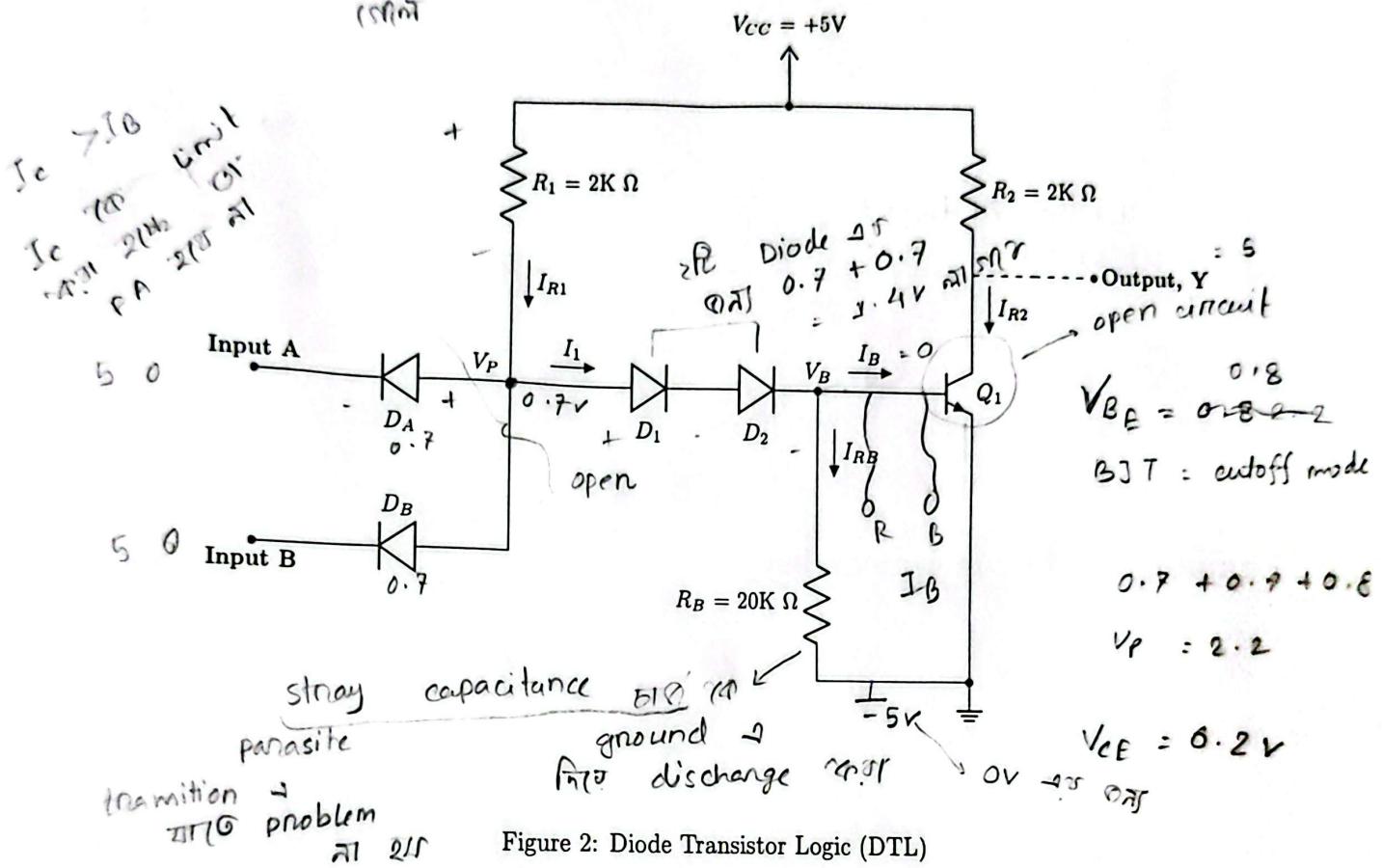


Figure 2: Diode Transistor Logic (DTL)

has a similar structure to the RTL inverter circuit, but it uses diode-logic AND on the input side. Thus, DTL circuits implement NAND gates by combining both DL and RTL logic, something that is not possible to do using solely RTL circuits or DL circuits. DTL also has better noise margin and fanout characteristics compared to RTL. (Noise margin indicates a circuit's immunity to noise, and fanout is the number of identical gates that a circuit can drive without facing errors).

On the input side of Fig. 2, we can see two diodes in reverse bias connection with respect to input - this acts as an AND gate circuit according to diode logic. The output of this AND gate is fed to the inverter input V_B (base terminal of BJT Q_1) through the diodes D_1 and D_2 creating the NAND circuit. The output is obtained at the collector terminal of Q_1 .

When both inputs are HIGH (5V), the cathode voltage of the diodes D_A and D_B become higher than their anode voltages. As a result, both input diodes operate in the reverse bias region (turned off/disconnected), and the node V_P has a high voltage level. This causes the transistor Q_1 to operate in the saturation mode and the the NAND gate generates a LOW output. In this case, the voltage of point P (V_P) is close to 2.2V as the voltage of base terminal (V_B) in saturation is nearly 0.8V and there is a voltage drop of 0.7V in each of diodes D_1 and D_2 .

When either input is LOW (0V), the corresponding input diode operates in the forward bias (turned on), and there is a voltage drop of 0.7V across the diode. Hence, the voltage at the node V_P becomes only 0.7V

higher than the LOW voltage at the input and drops much below the 2.2V required to turn on the BJT Q1. This causes the the transistor Q1 to work in the cutoff region and it acts like an open circuit. Hence, the current passing through the R_2 resistor (I_{R2}) is zero. As a result, there will be no voltage drop in the resistor R_2 and the voltage of the output point (Y) will be same as VCC = 5V (High).

Task-02: DTL Inverter

THEORY

As mentioned in the previous task, when either of the input terminals are HIGH, the corresponding diode operates in the reverse bias region - meaning it is virtually disconnected from the circuit. So we can say that if one of the inputs are set to logical HIGH, we can ignore that diode altogether, and the remaining diode input acts as a single input to the RTL inverter. Thus the resulting circuit acts as an inverter circuit (NOT gate). A roundabout way of explaining this is via the truth table of the NAND gate (Fig. 1) - when one input is set to HIGH, the output follows the inverted logic of the remaining input.

Procedure:

1. Measure the resistance values and fill up the table 1.
2. Connect the circuit as shown in Fig. 2.
3. Observe the output for all possible input combinations and fill up table-2 for NAND gate.
4. Operate the gate in Fig. 2 as an inverter by connecting either of the inputs to +5V and using the remaining one as input terminal. Fill up table-3.

Data Tables

Table 1: Resistance Data

For all your future calculations, please use the observed values only (for theoretical calculations too).

Notation	Expected Resistance ($k \Omega$)	Observed Resistance ($k \Omega$)
R_1	2	1.97
R_2	2	1.97
R_B	20	19.27

BJT

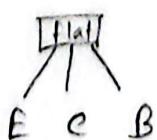


Table 2: NAND Gate Data

V_A (V)	V_B (V)	V_{DA} (V)	V_{DB} (V)	V_P (V)	I_{R1} (mA)	I_{R2} (mA)	V_B (mV)	V_Y (V)
0	0	0.502	0.505	0.511	2.27	0	12.1	5.00
0	5v	0.522	-4.51	0.536	2.265	0	14.9	5.01
5v	0	-4.46	0.570	0.587	2.240	0	22.5	5.01
5	5	-3.22	-3.22	1.89	1.578	2.513	0.846	0.048

Table 3: Inverter Data

Input A (V)	Input B (V)	V_P (V)	V_B (V)	Output Y (V)
5	0	0.57	23.8mv	4.98
5	5	1.832	0.943	54.7mv


Signature 6-11-24

Report

Please answer the following questions briefly in the given space.

- Using experimental data, find the operating mode of Q1 when input A is HIGH and input B is LOW. Additionally, find whether diodes DA and DB are ON or OFF (by using the voltage across them).

Ans.

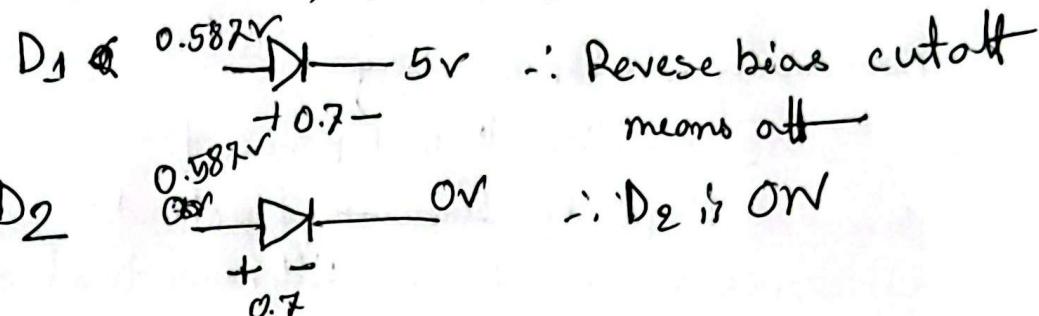
Given, $V_A = 5V$, $V_B = 0V \therefore V_{DA} = -4.46V$ (off) [according to table]

$$V_{DB} = 0.570V \text{ (ON)}$$

$\therefore D_A$ will be off and D_B will be on.

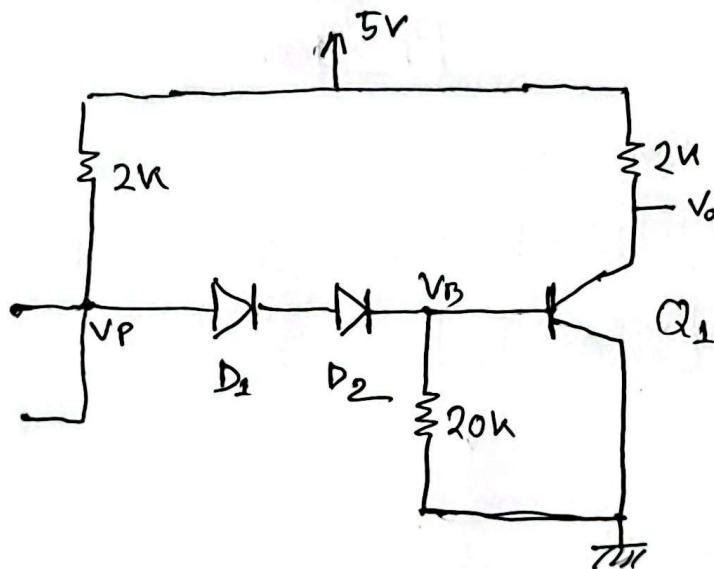
$V_P = 0.582V$; But theoretically V_P need to be higher or equal to $(0.7 + 0.7 + 0.8) \approx 2.2V$ to turn on D_1 and D_2 .

Thus, D_1 and D_2 are in cutoff and V_B Q1 is in cutoff mode. Proof $V_P = 0.582V$, $V_A = 5V$, $V_B = 0V$



- Assume that the output of the circuit shown in Fig: 2 is LOW. Draw the partial circuit consisting of only those components which remain active.

Ans.



$$V_A = \text{off}$$

$$V_O = 0.048V$$

$$V_B = \text{off}$$

$$D_1 = \text{ON}$$

$$D_2 = \text{ON}$$

$$Q_1 = \text{ON (sat)}$$

3. What should be the relation between the currents I_{R1} , I_B and I_{RB} when all inputs are HIGH? Did you obtain a similar result in your experiment? Explain briefly. (use a Multi-meter as Ammeter to measure I_B).
 Ans.

Using KCL,

$$I_{R1} = I_B + I_{RB}$$

$$\therefore I_B = I_{R1} - I_{RB}$$

$$\Rightarrow 1.578 - 0.0423$$

$$\Rightarrow 1.535 \text{ mA}$$

$$I_{R1} = 1.578 \text{ mA}$$

$$I_{R2} = 2.513$$

$$I_{RB} = \frac{0.846}{20}$$

$$= 0.0423 \text{ mA}$$

Using multimeter as Ammeter

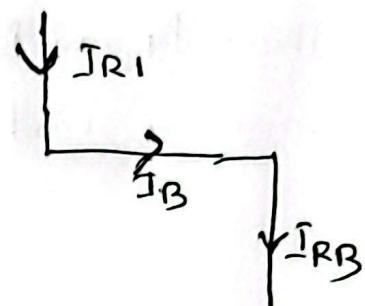
$$I_B = 1.55 \text{ mA}$$

\therefore Theoretically and Experimentally

I_B is quite similar, In Experiment

resistance, voltage can fluctuate

sometimes, but this doesn't difference that much.



$$\therefore I_{R1} = I_B + I_{RB}$$

4. Use the relation between the currents I_{R1} , I_B and I_{RB} when all inputs are HIGH to verify the operating mode of Q1. [Assume beta (β_F) ≥ 100]

Ans.

$$I_{R1} = 1.578 \text{ mA}$$

$$\beta_F \geq 100$$

$$I_B = 1.535 \text{ mA} \quad [\text{from Q3}]$$

$$I_{RB} = 0.0423 \text{ mA} \quad [\text{from Q3}]$$

$$I_{R2} = 2.513 \text{ mA} \quad [I_{R2} = I_c]$$

$$I_c = \beta I_B$$

$$\beta = \frac{I_c}{I_B} = \frac{2.513}{1.535} = 0.978 < \beta_F$$

As $\frac{I_c}{I_B} < \beta_F$, we can say that Q1 is in Saturation Mode

5. Will the circuit still work properly as NAND gate if the diodes D_1 and D_2 are removed? Measure the output voltage for the four different cases and verify.

Ans.

According to experimental Data,

If we remove D_1 and D_2

A	B	Output
0	0	4.72V
0	5	4.34V
5	0	4.37V
5	5	0.052V

Now as we can see
after removing D_1 and D_2

The circuit is still work like a NAND
gate (verified)

NAND Truth Table

A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

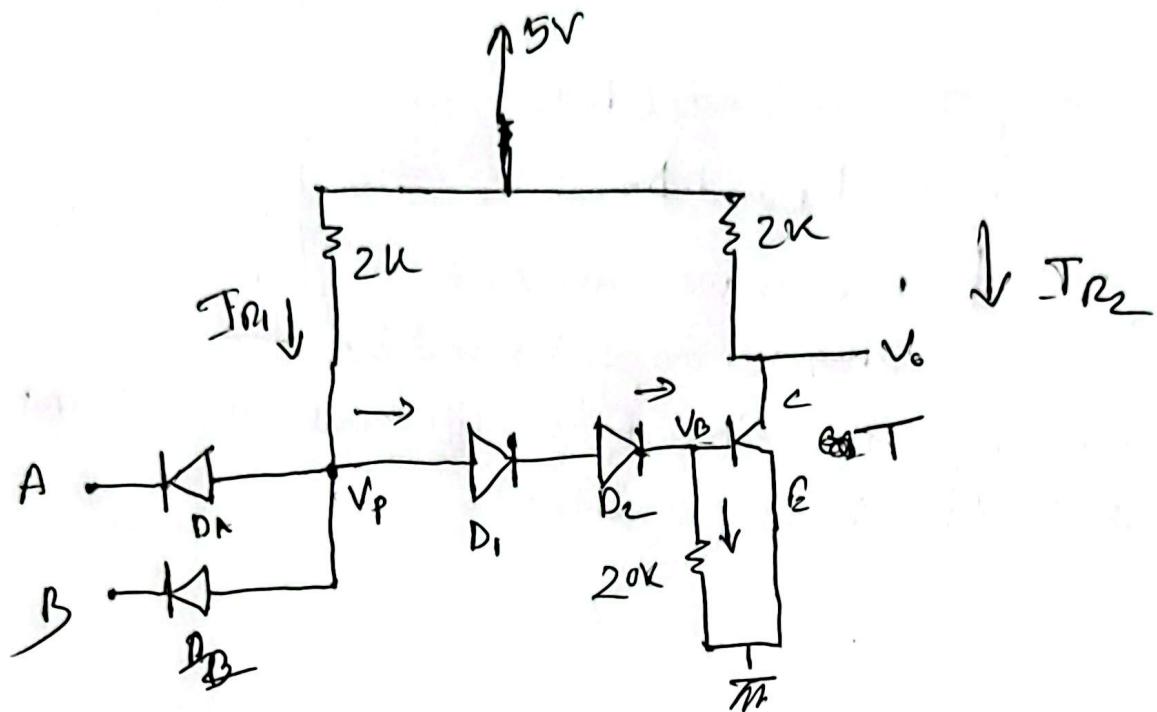
6. Vary the input A from 0V to 5V while keeping input B fixed at 5V. What is the maximum value of input A for which the output remains HIGH? [consider any voltage above 1V as HIGH]

Ans.

A	B	<u>Output</u>
0	5	5V
5	5	0.0526V

Set B constant and increasing value from 0V - 5V, at point 0.95V the output drop into low. Thus, the maximum value of input A for the output high is < 0.95V.

7. Verify the result of table 2 using theoretical calculation and comment on the result (Use extra pages if necessary).



V_A	V_B	I_{R2}	T_{R2}	V_D	V_o
0V	0V	0.7mA	$2.15mA$	0V	0V
0V	5V	0.7mA	$2.15mA$	5V	5V

Case 1

$$V_A = 0V, V_B = 0V, V_P = 0 + 0.7V = 0.7V$$

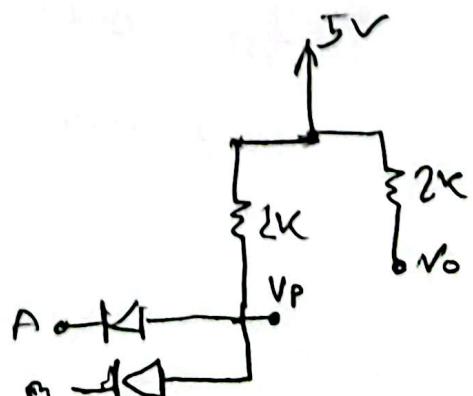
D_1, D_2, T_R2 need voltage to be turn on = $(0.7 + 0.7) / 0.8 = 2.2V$

Thus D_1, D_2 and T_R2 will not turn on cause $V_P < 2.2$

$$V_D = 5V \text{ [Since open circuit]}$$

$$I_{R2} \approx 0mA$$

$$I_{R1} = \frac{5 - 0.7}{2} = 2.15mA$$



(b)

Case 2

$$V_A = 0V, V_B = 5V$$

V_B will be cut off since it is in reverse bias

V_A will turn on, and $V_P = 0.7V$

D_1, D_2 and Q_T will not turn on cause

V_P needs to be $\geq 2.2V$

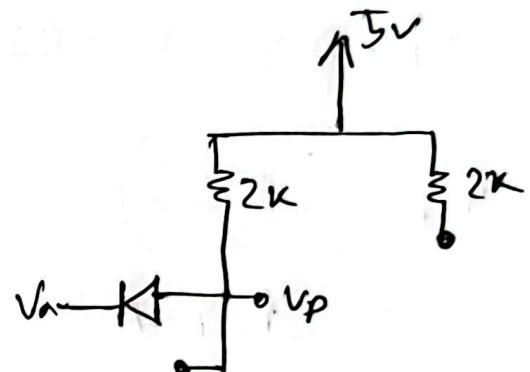
$$\therefore V_P = 0.7$$

$$I_{R_1} = \frac{5 - 0.7}{2} = 2.15 \text{ mA}$$

$$I_{R_2} = 0 \text{ mA}$$

$$V_B = 0V$$

$$V_{\text{output}} = 5V$$



Case 3

Similar but this time $V_A = 5V$ and

$V_B = 0V$; So V_A will be cut off V_B will turn

$$\therefore V_P = 0.7$$

$$I_{R_1} = 2.15 \text{ mA}$$

$$I_{R_2} = 0 \text{ mA}$$

$$V_B = 0V$$

$$V_{\text{output}} = 5V$$

Case G $V_A = 0.5V, V_B = 5V$

Now, D_A and D_B both will be off - cut off

According to our assumption V_P must be $2.2V$

$B_J + I_S$ in SAT mode

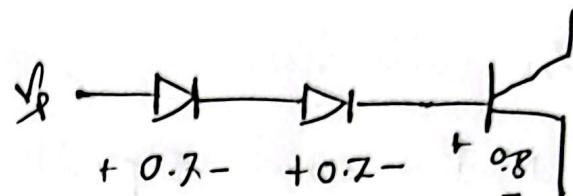
$$\therefore V_{BE} = 0.8V$$

$$V_{CE} = 0.2V$$

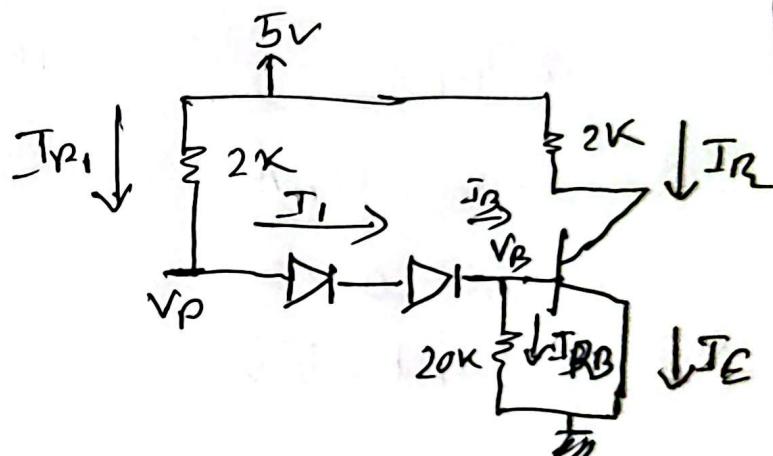
$$\therefore V_B = 0.8V, V_C = 0.2V$$

$$I_{R_1} = \left(\frac{5 - 2.2}{2} \right) \\ = 1.4 \text{ mA}$$

$$I_{R_2} = \left(\frac{5 - 0.2}{2} \right) \\ = 2.4 \text{ mA}$$



$$V_P = (0.7 + 0.2 + 0.8) \\ \Rightarrow 2.2V$$



$$I_E = 0; V_C = V_O = 0.2V$$

Table NAND Gate

V_A	V_B	V_P	I_{R_1}	I_{R_2}	V_B	V_o
0v	0v	0.7v	2.15mA	0mA	0v	5v
0v	5v	0.7v	2.15mA	0mA	0v	5v
5v	0v	0.7v	2.15mA	0mA	0v	5v
5v	5v	2.2v	-1.4mA	2.4mA	0.8v	0.2v

So, the table from experimental and the table from theoretical calculation are mostly identical because of the internal resistance the values are little bit fluctuated.

Learnings: Learned about Diode Transistor Logic
How this work as NAND Gate we can also
use this as a inverter by keeping one
input constant.

Challenges: Getting accurate data from
multimeter was definitely a challenge task
and it is known we can divide the circuit
in multiple division. We have to build a
full circuit and if it is giving wrong data
then we have to check each component
whether it is in right position or not so
after all, this is a little time consuming.

Future findings: In future if any project
needs any kind of NAND gate or Inverter
then DTL will be in our checklist. Moreover,
we got a depth of knowledge about BJT
and Diode, hopefully this will help us in
future.

Mistakes: At the first beginning we got some abnormal value after check we found two of the component were shorted and we fixed that to get desired values.