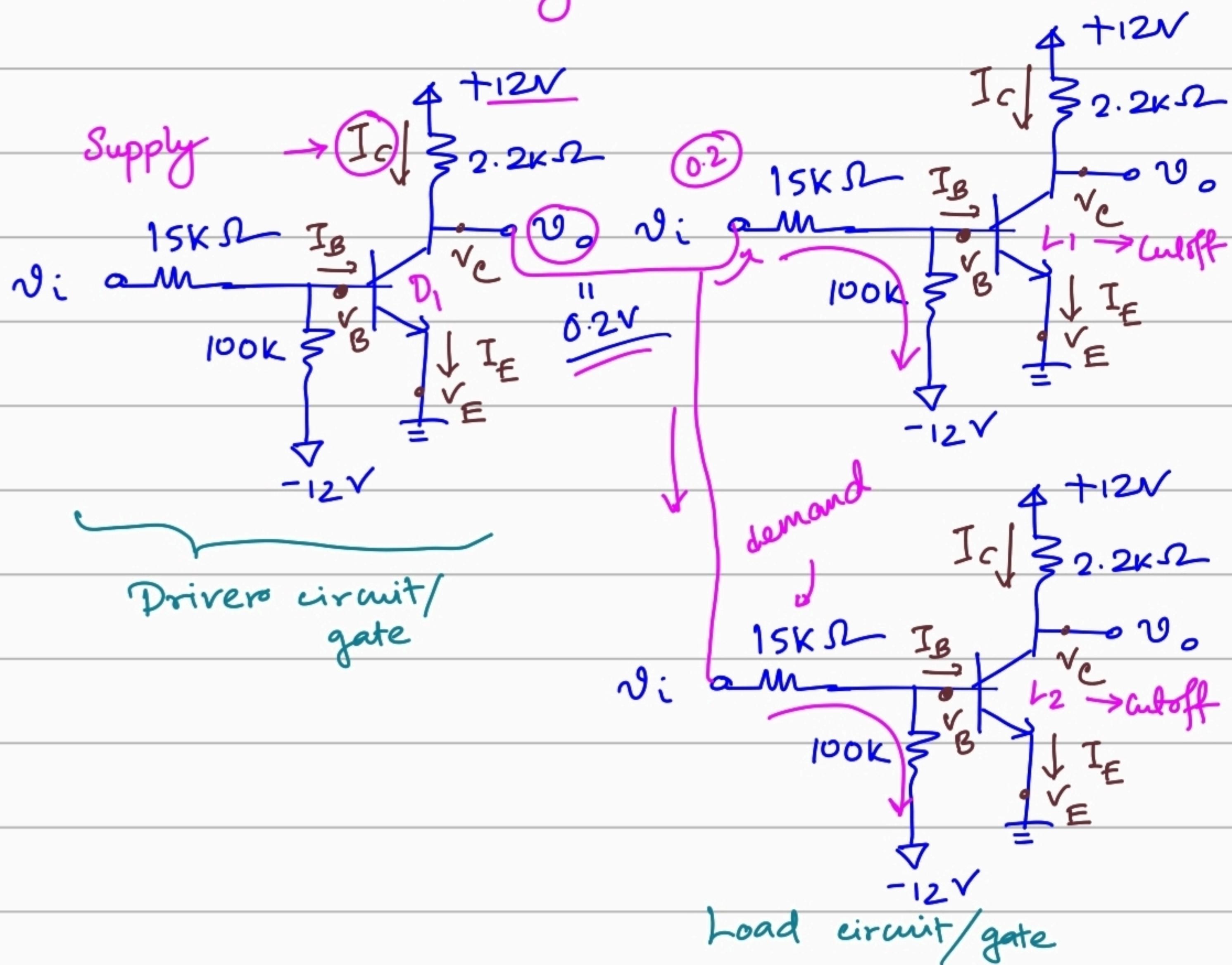


Fanout: The number of input terminals are connected to a output terminal.

Maximum fanout (fanout): The maximum number of logic inputs of the logic family that an output terminal can drive, is called maximum fanout.
reliably

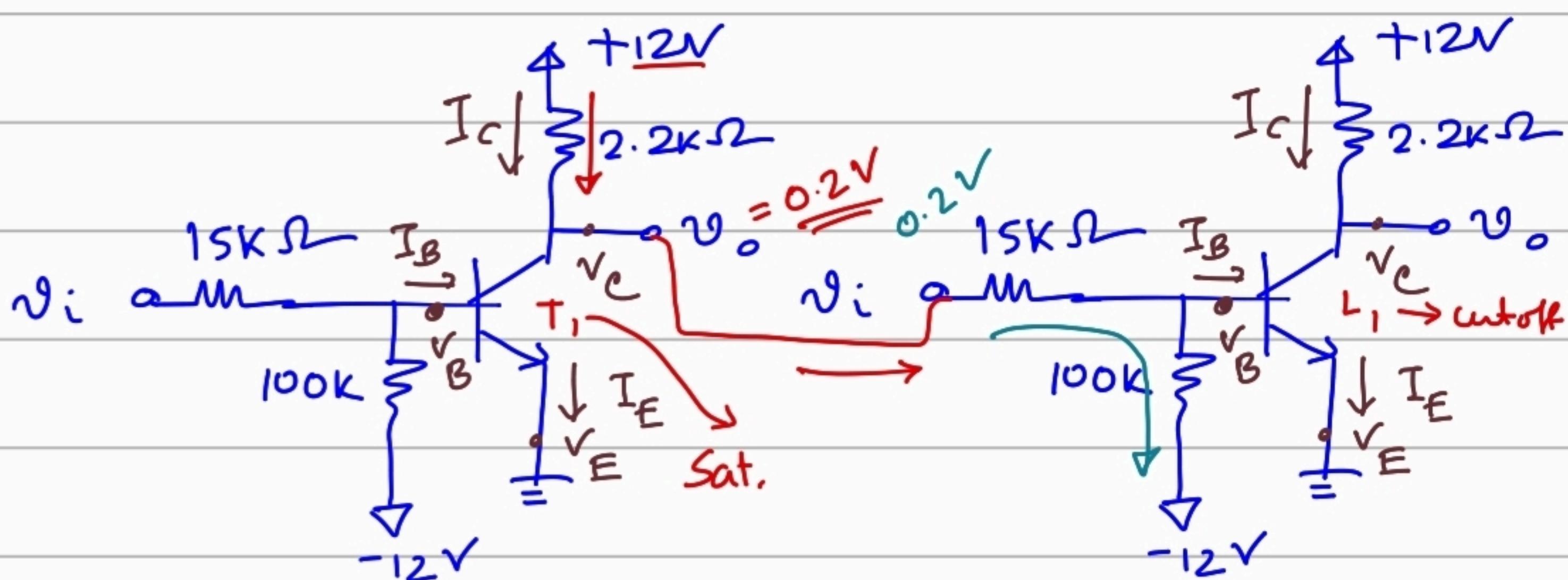


Question: Calculate the maximum fanout of the above RTL circuit. Assume $V_{OH} = 10V$.

Case ①: The output of the drivers circuit is low.

* Maximum supply current :- The maximum of current can be delivered by the driver circuit without changing its operating mode.

* Individual demand load current :- The maximum amount of current needed by each individual load while driven by driver circuit.



Driver circuit $T_1 \rightarrow$ Saturation. $V_o = 0.2V$

Load circuits $L_1, L_2 \rightarrow$ cutoff. $I_B = 0$.

$$* \text{ Maximum supply current. } \frac{12 - 0.2}{2.2k} = 5.3636 \text{ mA}$$

$$* \text{ Individual demand load current, } \frac{0.2 - (-12)}{(15 + 100)k} = 0.106 \text{ mA}$$

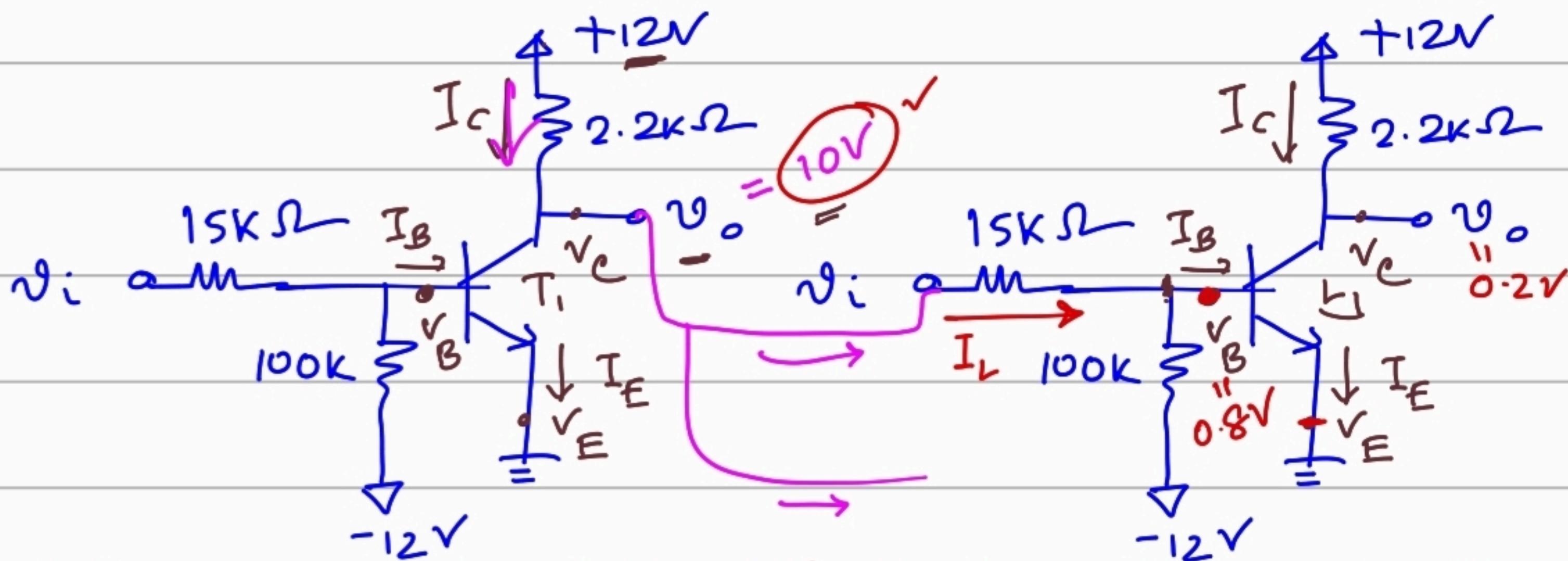
$$\begin{aligned} & \text{maximum fanout for this case,} \\ & = \left[\frac{5.3636}{0.106} \right] = [50.6] = \textcircled{50} \end{aligned}$$

* If we connect 51 load circuits, then demand exceeds supply. Thus driver circuit will malfunction.

Case ② : The output voltage of the driver circuit is High.

- * If we connect load circuits when output of driver is high, the output voltage of driver starts to drop.

$$V_{OH} = 10V$$



- * Driver transistor, $T_1 \rightarrow$ cutoff, load circuit's transistors $T_2, T_3 \downarrow$
- * Maximum supply current = $\frac{12-10}{2.2k\Omega} = 0.909mA$ Sat.

* Individual load current, $I_L = \frac{10-0.8}{15k} = 0.6133mA$

* Maximum fanout for this case = $\left[\frac{0.909}{0.6133} \right] = [1.48] = 1$

By Overall maximum fanout must be calculated by considering worst case scenario. To prevent malfunction of driver circuit, we need to take the minimum of the two cases.

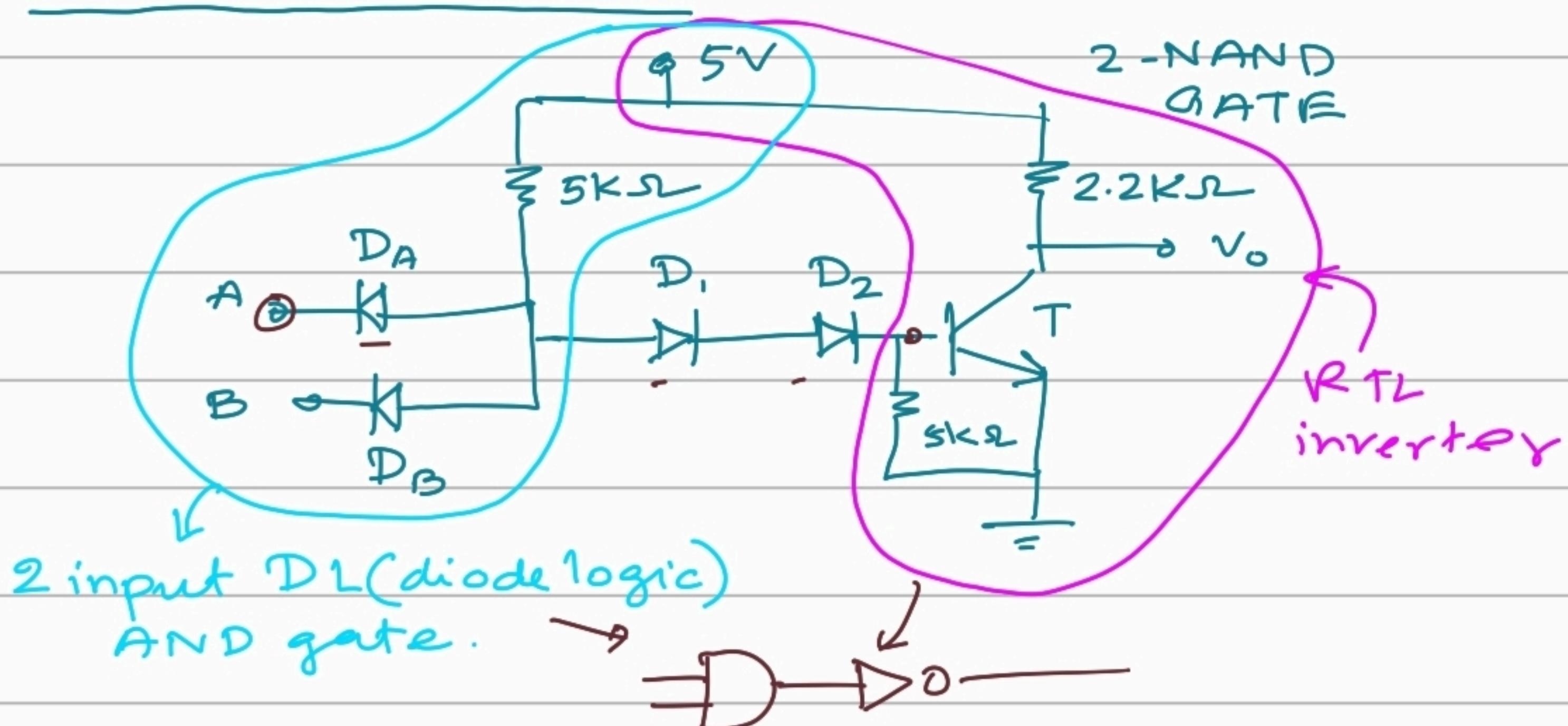
By Maximum fanout, $= \min(50, 1) = 1$

maximum fanout = ∞ - any answer is valid.

DTL (Diode Transistor Logic)

- * Bipolar \rightarrow Saturated
(Switching transistor will operate in saturation and cutoff mode).
- * Input terminals connects through diodes to the switching transistor's base terminal.

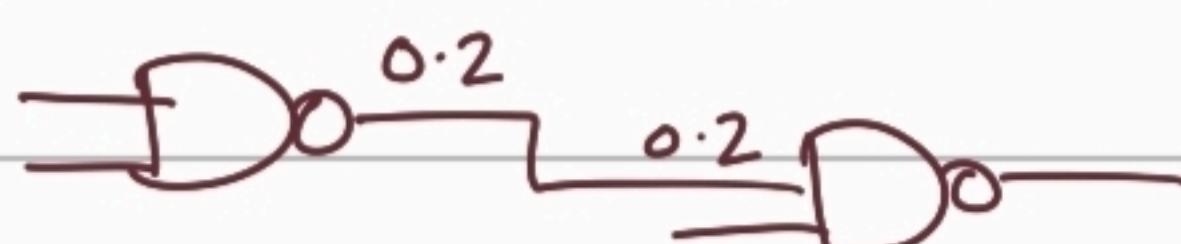
DTL NAND GATE:



Basic operation:

- # Calculate the currents and voltages of the following DTL gate and verify that it works like a NAND gate. Assume that input stages might be connected to the output stage of other DTL NAND gate.

$$V_{BE(\text{sat})} = 0.8V, V_{CE(\text{sat})} = 0.2V, \beta_F = 30.$$



Ans:

Case ① Both inputs are low.

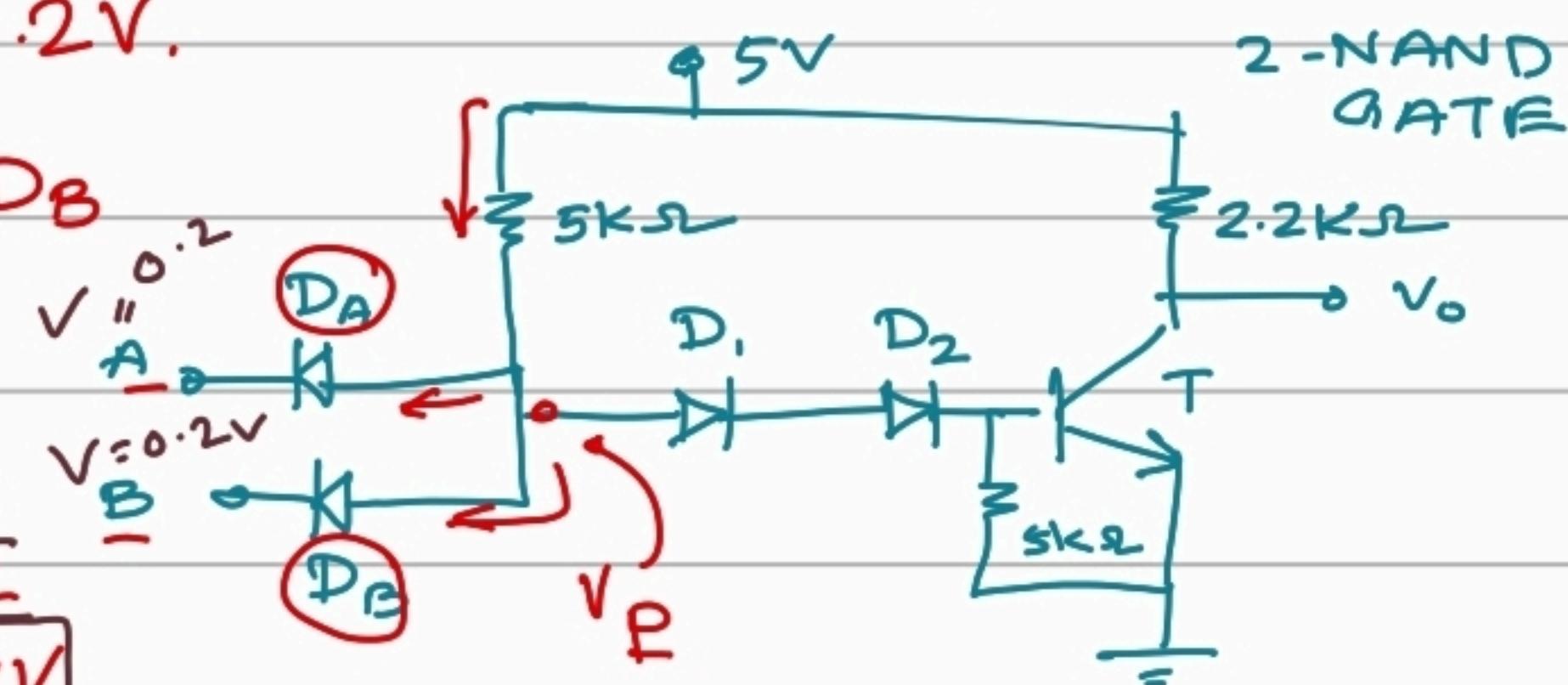
Because inputs are connected to some other output stage, the output voltage = input voltage

$$= 0.2V. \quad V_A = V_B = 0.2V.$$

Assume, D_A and D_B

are conducting.

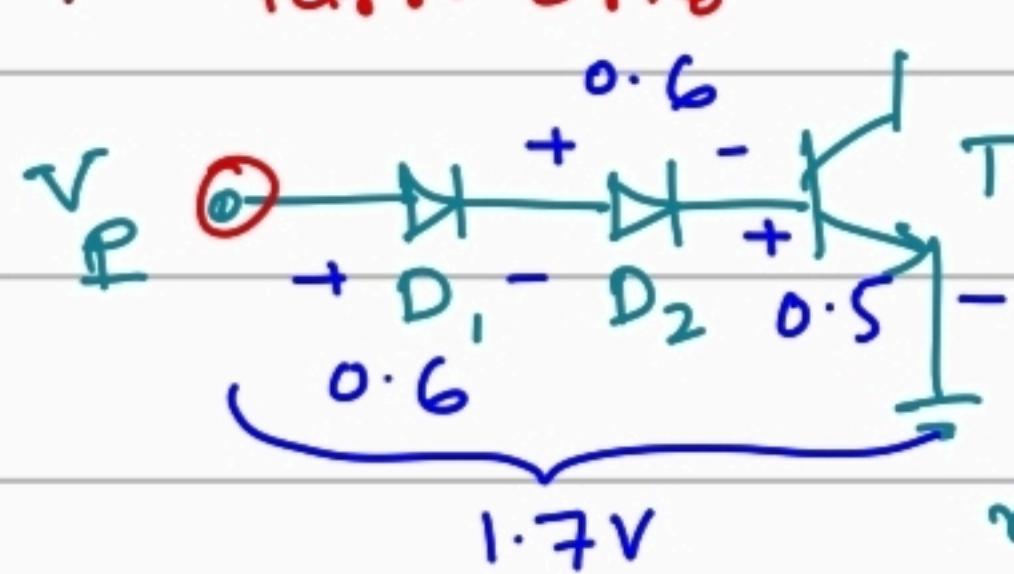
$$\begin{array}{c} 0.2 \\ - \\ 0.7V \end{array} \quad \begin{array}{c} + \\ 0.2 \\ + \end{array} \quad V_p = 0.7 \\ V_p = 0.9V$$



Since we are assuming diodes are conducting the anode voltage V_p of D_A and D_B must be 0.7V higher than the cathode voltage. Thus $V_p = 0.9V$.

Necessary condition for transistor T to turn on:

* * turn on:



$$V_{BE} (\text{cut-in voltage}) = 0.5V$$

$$V_D (\text{cut-in voltage of diode}) = 0.6V$$

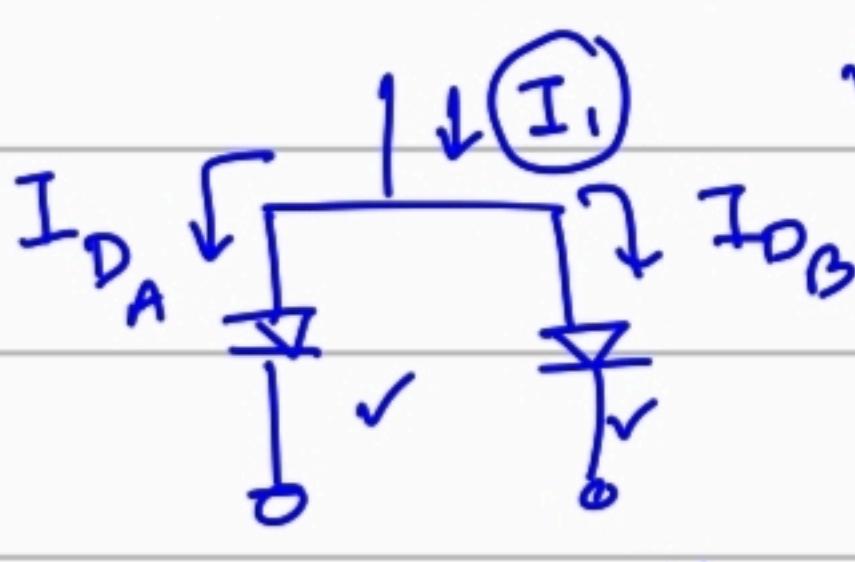
In order for T to turn on we need to have $V_p \geq 1.7V$.

According to our assumption, V_p will not turn on D_1 , D_2 and T and current will flow as we expected.

$$V_A = V_B = 0.2V, \quad V_p = 0.9V$$

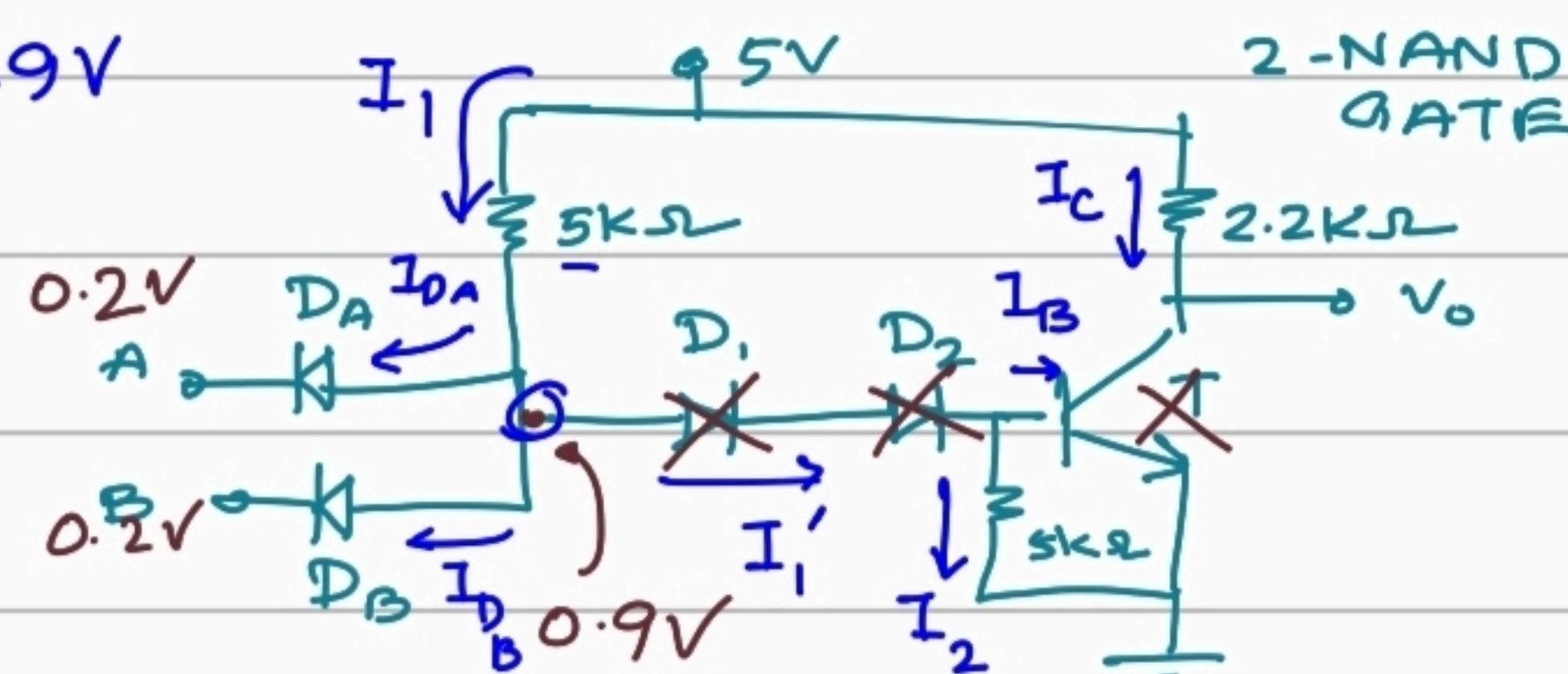
$$I_I = \frac{(5 - 0.9)}{5k} = 0.82mA$$

$$I_C = I_B = I_2 = I'_1 = 0$$



$I_{D_A} = I_{D_B}$ because both branches are identical.

$$I_{D_A} = I_{1/2} = 0.41mA$$



Case ②

$$V_A = 0.2V, V_B = 5V \quad | \quad (V_A = 5V, V_B = 0.2V)$$

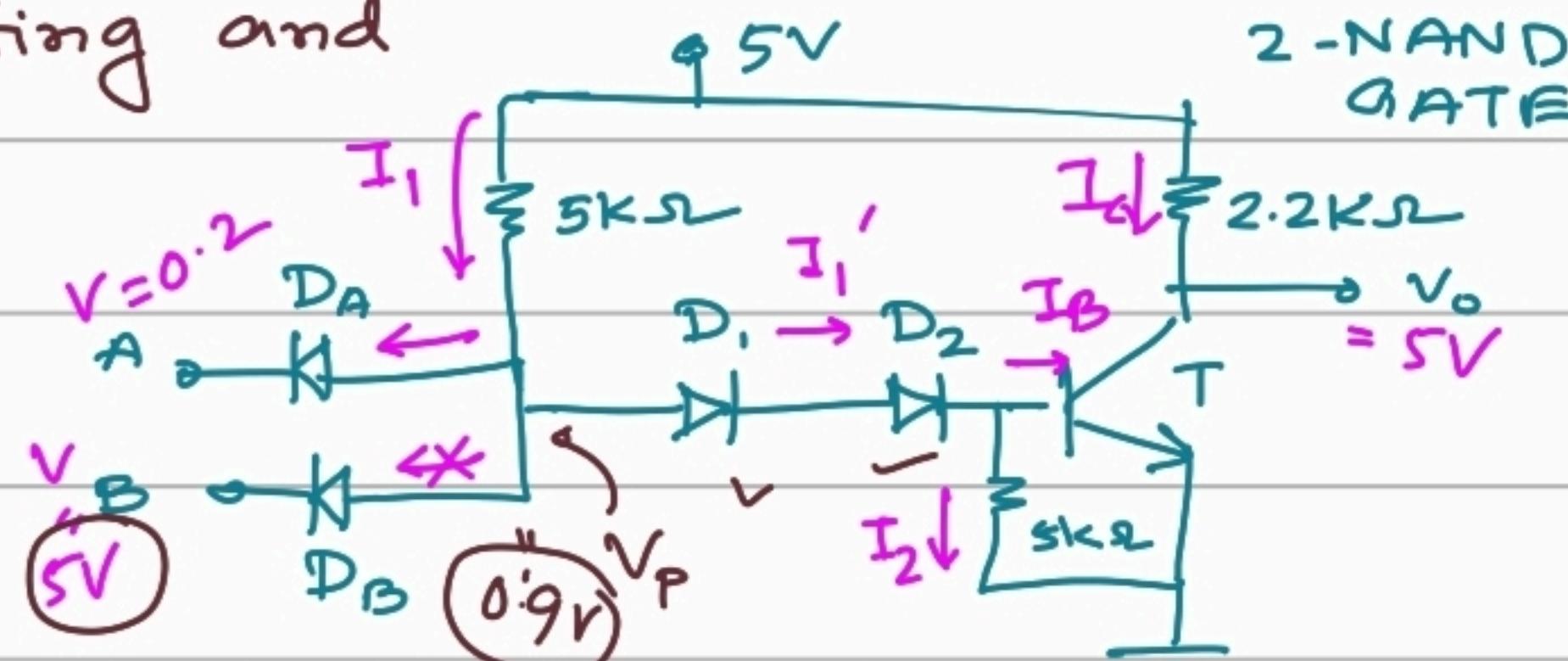
Similar

Assume. D_A is conducting and

D_B is off.

Therefore, $V_P = 0.9V$.

So D_1, D_2, T must be turned off.



The anode of D_B has smaller voltage than the cathode. So our assumption is right.

$I_C = I_B = I'_1 = I_2 = 0, V_o = 5V. I_1 = \frac{5 - 0.9}{5k\Omega} = 0.82mA$

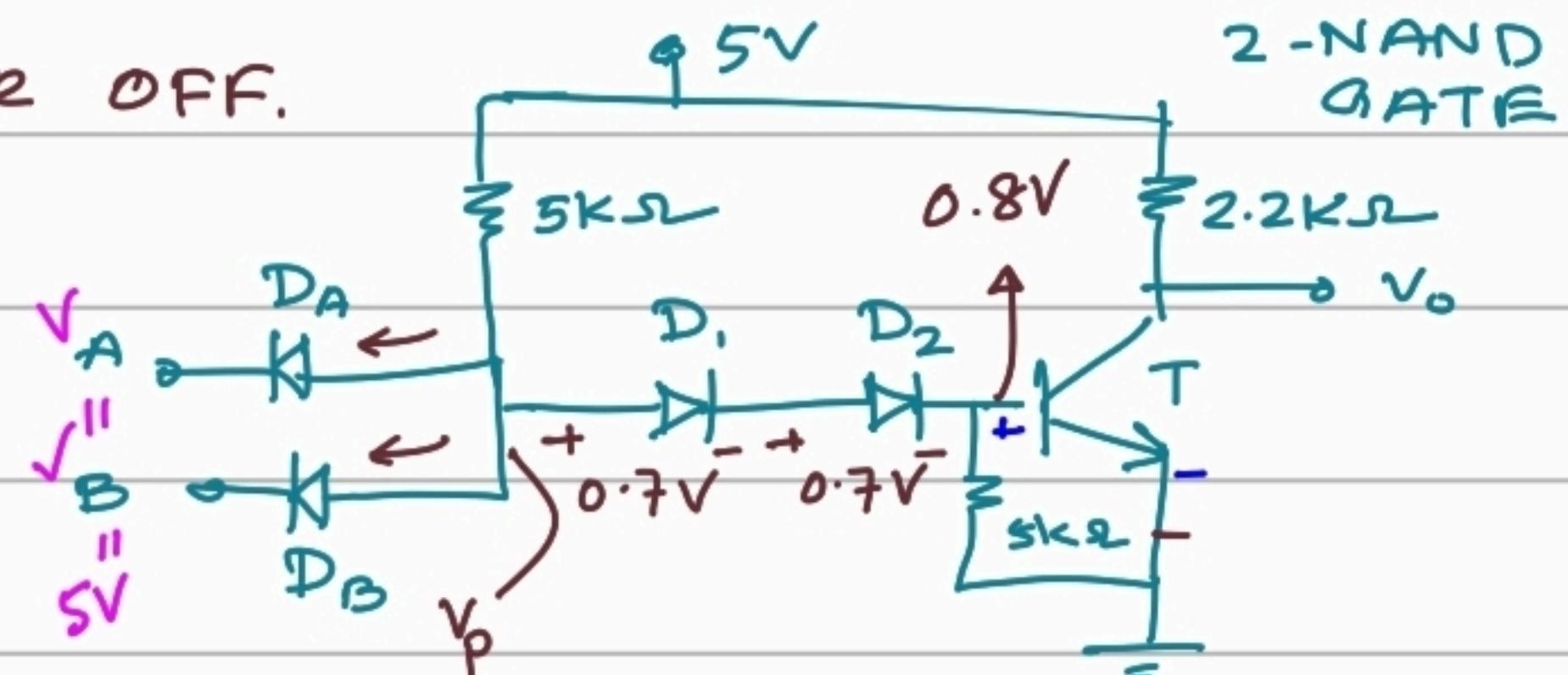
$I_{D_A} = I_1 = 0.82mA, I_{D_B} = 0mA.$

Case ③ $V_A = V_B = 5V$.

Assume, D_A and D_B are OFF.

$$I_{D_A} = I_{D_B} = 0mA.$$

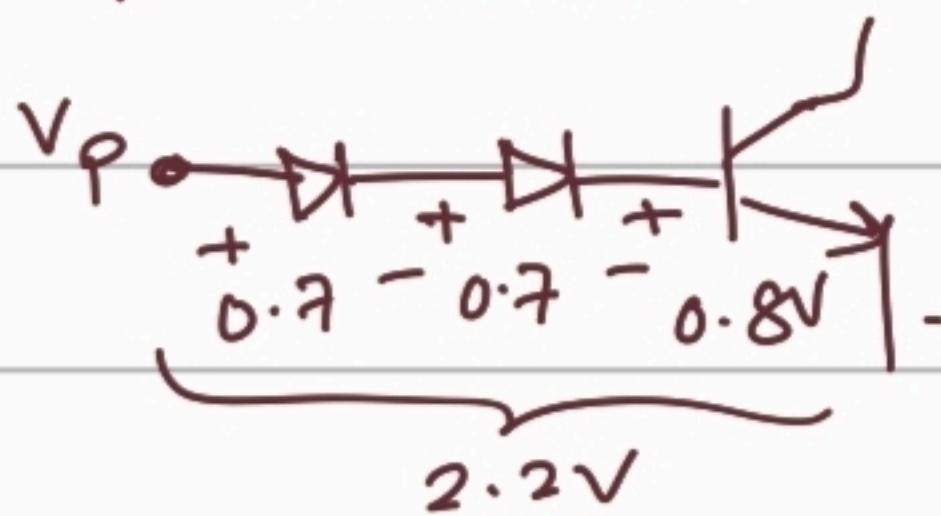
Therefore current must flow through D_1, D_2 and T .



Because it is a DTL circuit, the switching transistor must operate in saturation when it is turned on.

$$V_{BE(\text{sat})} = 0.8V, V_{CE(\text{sat})} = 0.2V$$

\Rightarrow Conduction voltage of D_1 and D_2 diodes are 0.7V.



According to our assumption
 V_P must be 2.2V.

The cathode voltages of D_A and D_B is higher than the anode voltage $V_P = 2.2V$.

This justifies our assumption.

Current-voltage Calculation:

$$V_P = 2.2V$$

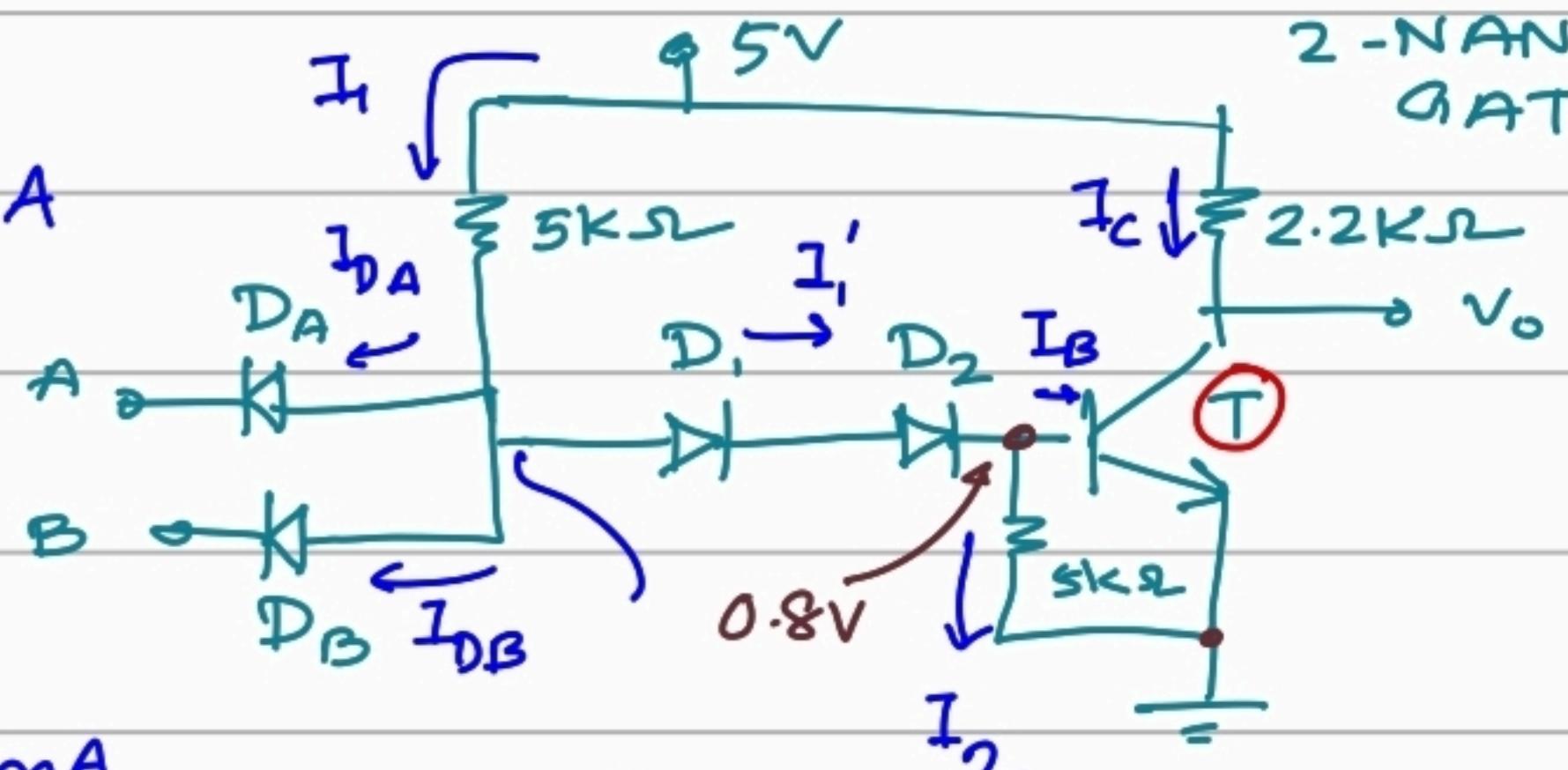
$$I_I = \left(\frac{5 - 2.2}{5k} \right) = 0.56mA$$

$$I_{D_A} = I_{D_B} = 0mA$$

$$I'_I = I_I = 0.56mA$$

$$I_2 = \frac{0.8 - 0}{5k} = 0.16mA$$

2-NAND GATE



$$I'_I = I_I = 0.56mA$$

$$I_B = I'_I - I_2 = 0.56 - 0.16$$

$$= 0.4mA$$

$$I_c = \frac{5 - 0.2}{2.2k} = 2.182mA$$

Chart:

V_A	V_B	V_o
0.2	0.2	5V
0.2	5V	5V
5V	0.2	5V
5	5	0.2

From analyzing the cases we can clearly conclude that this circuit is a NAND gate.

β_{min} for this circuit:

$$\beta_{forced} = \frac{I_c}{I_B} = \frac{2.182}{0.4} = 5.45$$

We need to choose $\beta_F \geq 5.45$ for transistor T in order to prevent it from malfunctioning.

$$\beta_{min} = 5.45$$

Lecture 6: DTL NOISE MARGIN, FANOUT, Modified DTL, HTL

Noise Margin: Different calculation from R_{TL} circuit.

V_{NH} (noise margin):

Q: If all inputs are high, then what is the magnitude of noise voltage which will cause the gate to malfunction?