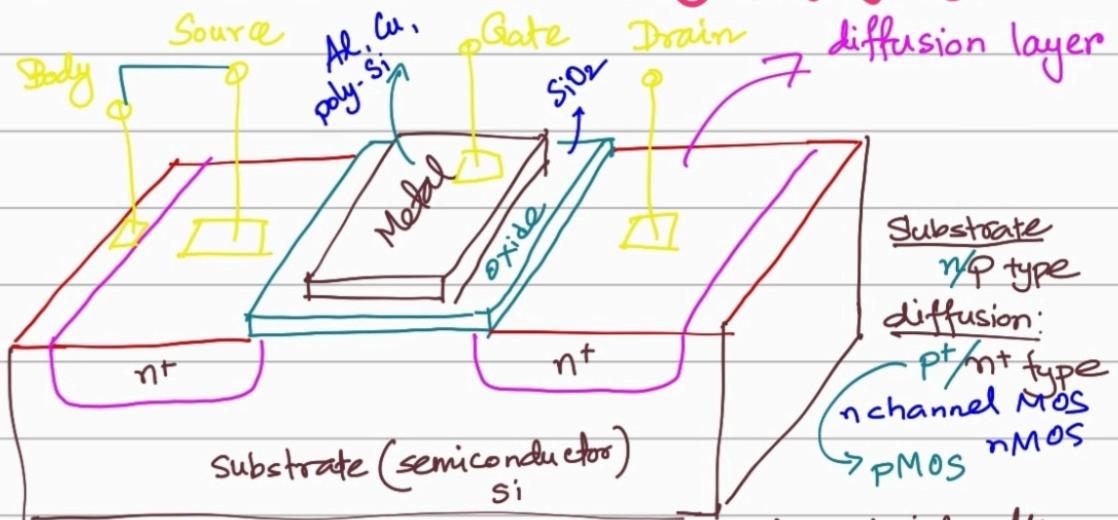


#MOSFET

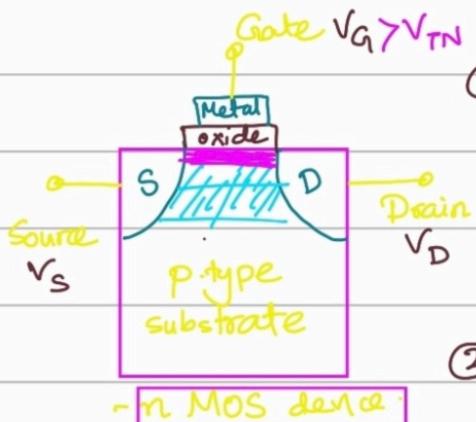
Basic Internal Structure:



- # If some MOSFET is fabricated individually then source and body might be shorted.
- # In VLSI design we connect min/max for voltage is connected to body terminal, p-type/n-type substrate.

Basic Operations:

If we apply voltage to the gate terminal.



① If V_G is less than zero, holes inside p-type semi-conductor might accumulate underneath the oxide layer.

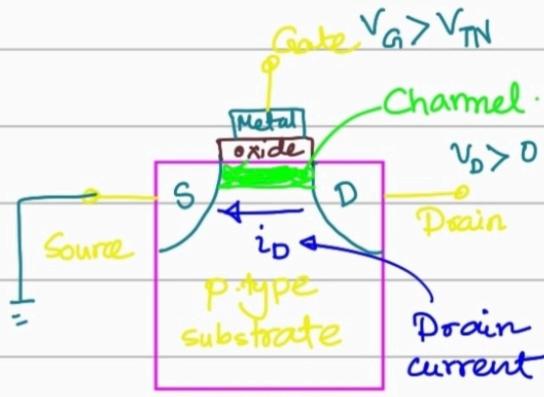
→ accumulation

② If $0 < V_G < V_{TN}$, then depletion layer forms beneath the oxide layer. → depletion

③ If $V_G > V_{TN}$, then an inversion layer would emerge under the oxide layer. → Inversion

Now if we apply positive voltage to drain terminal when $V_G > V_{TN}$

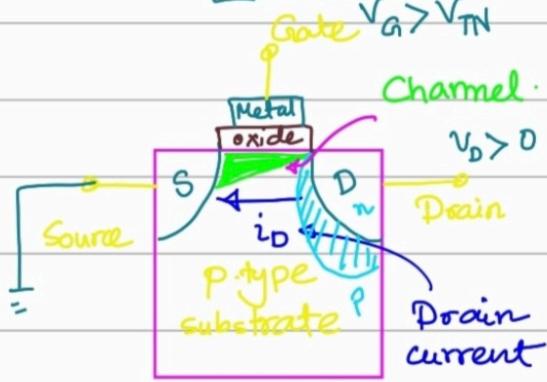
① When drain voltage is very small positive voltage.



It behaves like a resistor.



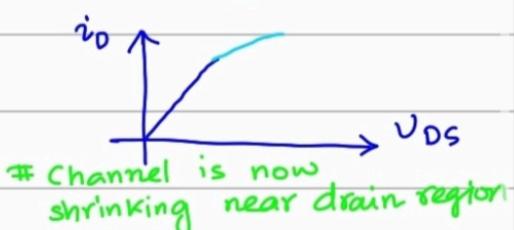
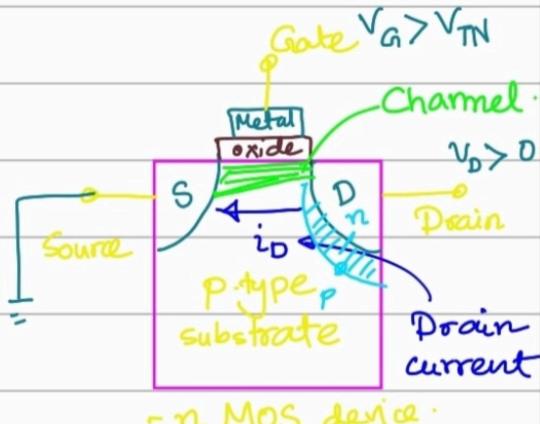
② If the $V_D = V_G - V_{TN}$



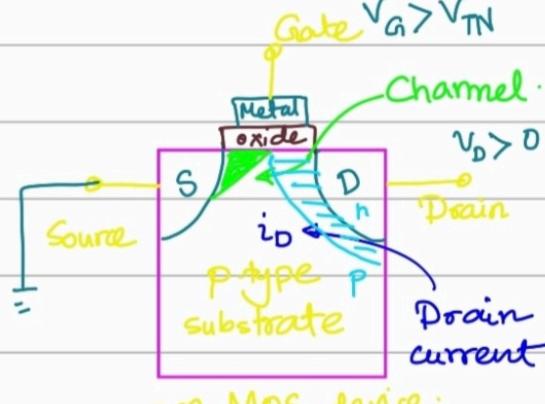
- nMOS device.

Channel region is now pinched off. Thus current cannot increase if we apply more voltage.

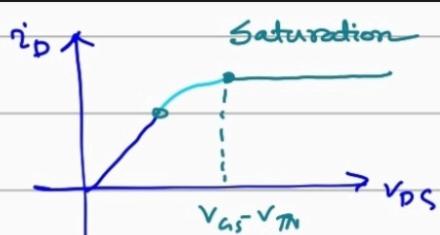
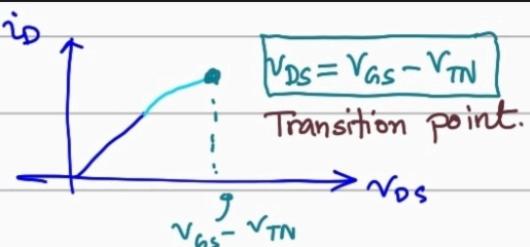
② When drain voltage is not very small.



③ $V_D \geq V_G - V_{TN}$



- nMOS device.



Operating modes of MOS-FET

metal-oxide-semiconductor field-effect transistor

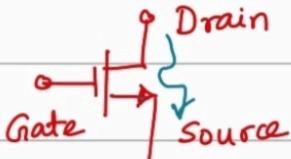
- ① Cutoff
- ② Linear/Triode
- ③ Saturation

We apply electric field to perform switching operation inside the transistor.

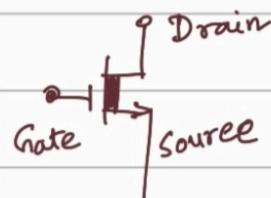
MOSFET types:

MOSFET type	Specially	Cutoff	Triode	Saturation
n-channel enhancement	p-type sub. $V_{TN} > 0$	$V_{GS} < V_{TN}$	$V_{GS} > V_{TN}$ $V_{DS} \leq V_{GS} - V_{TN}$	$V_{GS} > V_{TN}$ $V_{DS} \geq V_{GS} - V_{TN}$
n-channel depletion	p-type sub. $V_{TN} < 0$	$V_{GS} < V_{TN}$	$V_{GS} > V_{TN}$ $V_{DS} \leq V_{GS} - V_{TN}$	$V_{GS} > V_{TN}$ $V_{DS} \geq V_{GS} - V_{TN}$
p-channel enhancement	n-type sub $V_{TP} < 0$	$V_{SG} < V_{TP} $	$V_{SG} > V_{TP} $ $V_{SD} \leq V_{SG} + V_{TP}$	$V_{SG} > V_{TP} $ $V_{SD} \geq V_{SG} + V_{TP}$
p-channel depletion	n-type sub. $V_{TP} > 0$	$V_{SG} < V_{TP} $	$V_{SG} > V_{TP} $ $V_{SD} \leq V_{SG} + V_{TP}$	$V_{SG} > V_{TP} $ $V_{SD} \geq V_{SG} + V_{TP}$

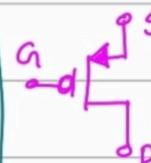
n channel
enhancement
MOSFET



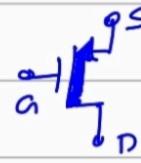
n channel
depletion
MOSFET



p-channel
enhancement
MOSFET



p-channel
depletion
MOSFET



Current-Voltage Relationships:

NMOS

① Cutoff mode: $i_D = 0$

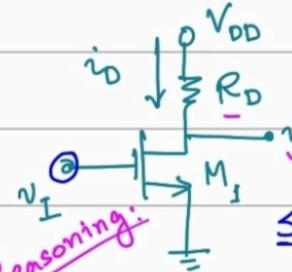
② Triode mode:

$$i_D = K_n (2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2)$$

③ Saturation mode:
 $V_{DS} = V_{GS} - V_{TN}$

$$i_D = K_n (V_{GS} - V_{TN})^2$$

Example: NMOS Inverter:



Q1: Determine V_O for $V_I = 5V$ and $V_I = 1.3V$.

Specification: $V_{DD} = 5V$, $R_D = 20k\Omega$.

$$V_{TN} = 0.5V, K_n = 0.3mA/\sqrt{V}$$

$$\text{Soln: } @ V_I = 5V, V_G = V_I = 5V, V_S = 0V.$$

Reasoning: Since this circuit will act like an inverter, the higher the input voltage, the smaller the output voltage. $V_{GS} - V_{TN} = 5 - 0.5 = 4.5V > 0$. Thus $V_O < V_{GS} - V_{TN}$

So the M_1 might operate in triode region.

Assumption: $M_1 \rightarrow$ triode region.

$$i_D = K_n [2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2] = \frac{V_{DD} - V_O}{R_D}$$

$$\Rightarrow 0.3m [2(5 - 0.5)V_O - V_O^2] = \frac{5 - V_O}{20K}$$

$$\Rightarrow \underbrace{20K \times 0.3m}_{6} [9V_O - V_O^2] = 5 - V_O \Rightarrow 6V_O^2 - 55V_O + 5 = 0$$

$$V_O = \begin{cases} 9.074V \\ 0.092V \end{cases} \rightarrow i_D = \frac{5 - V_O}{20K} < 0 \text{ which is impossible.}$$

$$\text{Thus, } V_O = 0.092V$$

Verification:

$$V_O = V_{DS} = 0.092 < 4.5 = (V_{GS} - V_{TN})$$

Therefore our assumption is valid.

PMOS

① Cutoff mode: $i_D = 0$

② Triode mode:

$$i_D = K_p (2(V_{SG} + V_{TP})V_{SD} - V_{SD}^2)$$

③ Saturation mode:
 $V_{SD} = V_{SG} + V_{TP}$

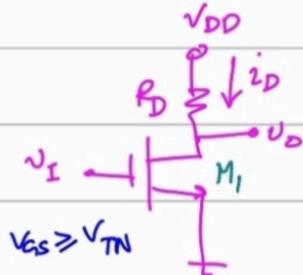
$$i_D = K_p (V_{SG} + V_{TP})^2$$

⑬. $v_I = 1.5V$. Assumption: $M_1 \rightarrow$ saturation.

$$\begin{aligned}i_D &= K_n \left[(v_{GS} - v_{TN}) \right]^2 \\&= 0.3 [1.5 - 0.5]^2 = 0.3 \text{ mA}\end{aligned}$$

$$i_D = \frac{v_{DD} - v_o}{R_D} = \frac{5 - v_o}{20k} = 0.3 \text{ mA}$$
$$\Rightarrow v_o = -1V$$

$$v_{DS} = v_o = -1V < (v_{GS} - v_{TN}) = 1V$$



This contradicts our assumption that $v_{DS} \geq v_{GS} - v_{TN}$ (saturation)

Therefore, M_1 must be in triode/ linear mode.

$$\begin{aligned}i_D &= \frac{5 - v_o}{20} = 0.3 [2(1.5 - 0.5)v_o - v_o^2] \\&\Rightarrow 0.3v_o^2 + 0.65v_o - 0.25 = 0\end{aligned}$$

$$v_o = \begin{cases} 1.6667V \rightarrow v_{DS} > (v_{GS} - v_{TN}) \\ = 1V \\ 0.5V \end{cases}$$

\downarrow This cannot be the answer because M_1 must be in triode mode.

Therefore, $v_o = 0.5V$

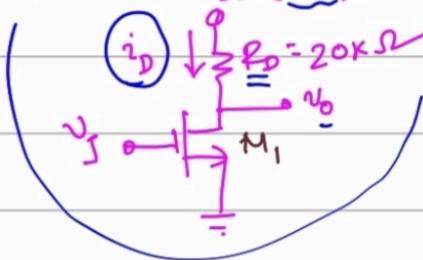
Verification: $v_{DS} = 0.5 < (v_{GS} - v_{TN}) = 1V$

Thus our answer is not wrong.

Example: Determine the transition point, maximum drain current and maximum power dissipation of an NMOS inverter with resistor.

Specification: $V_{DD} = 2.5V$, $R_D = 20k\Omega$, $V_{TN} = 0.5V$, $K_n = 0.3mA/V^2$

Solⁿ: $\sqrt{V_{DD}(2.5V)}$



Observation: When output (V_o)

has the smallest value then $i_D = \frac{V_{DD}-V_o}{R_D}$ would have a maximum value. Therefore, maximum input voltage is needed to produce this output value.

We can take maximum value of input voltage at $2.5V$. $V_I = 2.5V$. [$M_1 \rightarrow$ triode]

$$i_D = \left(\frac{2.5 - V_o}{20k} \right) = 0.3m \left[2(2.5 - 0.5)V_o - V_o^2 \right]$$

$$\Rightarrow 6V_o^2 - 25V_o + 2.5 = 0. \quad V_o = \begin{cases} 0.1025V \\ 4.064V \end{cases}$$

$V_o \neq 4.064V$ because that will produce negative i_D .

$[V_o = 0.1025V]$. [verify: $0.1025 < (V_{GS} - V_{TN}) = 2V$]

$$i_D = \frac{2.5 - 0.1025}{20k} = 0.1198mA \quad \text{max drain current } \boxed{i_D}$$

$$P = \Delta V I = (V_{DD} - 0)i_D = 2.5 \times 0.1198$$

$$\text{maximum power dissipation} = 0.3mW$$

Transition point: $\boxed{V_{DS} = V_{GS} - V_{TN}}$

at transition point, $i_D = K_n(V_{GS} - V_{TN})^2$

$$i_D = \left(\frac{V_{DD} - V_o}{R_D} \right) = K_n(V_{GS} - V_{TN})^2 = K_n V_o^2 \quad \boxed{V_o}$$

$$\Rightarrow \frac{2.5 - V_o}{20k} = 0.3m \cdot V_o^2 \Rightarrow 6V_o^2 + V_o - 2.5 = 0 \quad \checkmark$$



$$V_o = \begin{cases} 3.4051 V & \rightarrow \text{if it were the soln, } i_D \text{ would be negative.} \\ 0.5675 V \end{cases}$$

\therefore At transition point $V_o = 0.5675 V$

$$V_o = V_I - V_{TN}$$

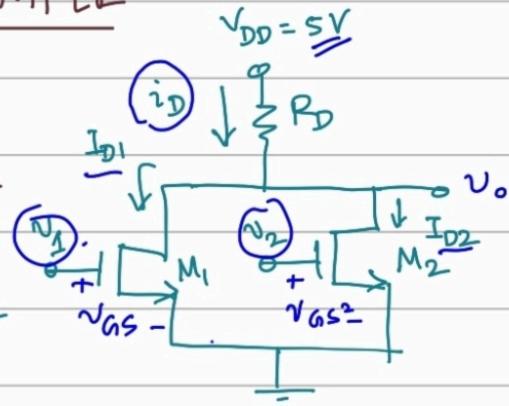
$$V_J = V_o + V_{TN} = 1.0675 V$$

NMOS NOR GATE EXAMPLE

Objective: Determine the current and voltages in this gate for different input conditions:

$$R_D = 20 k\Omega, K_n = 0.1 \text{ mA/V}^2$$

$$V_{TN} = 0.8 V$$



Solⁿ: ① Case 1: $V_1 = V_2 = 0 V$.

. For M_1 , we have $V_{GS1} = V_{G1} - V_{S1} = 0 - 0 = 0 < 0.8 V$

" M_2 " " $V_{GS2} = V_{G2} - V_{S2} = 0 - 0 < 0.8 V$

Therefore, M_1 and M_2 are in cutoff mode.

$$I_{D1} = I_{D2} = i_D = 0. V_o = V_{DD} = 5 V$$

② Case 2: $V_1 = 5 V$ and $V_2 = 0 V$.

Since $V_{GS2} = 0 < 0.8$, M_2 must be in cutoff. $I_{D2} = 0$

So, we can assume M_1 is operating in triode region

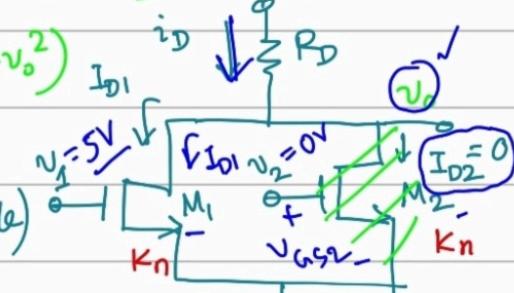
$$i_D = \frac{V_{DD} - V_o}{R_D} = K_n (2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2) \quad V_{DD} = 5 V$$

$$\Rightarrow \left(\frac{5 - V_o}{20k} \right) = 0.1m (2(5 - 0.8)V_o - V_o^2)$$

$$\Rightarrow 2V_o^2 - 9.4V_o + 5^2 = 0 \checkmark$$

$$V_o = \begin{cases} 8.6 V & \rightarrow (i_D < 0, \text{ impossible}) \\ 0.29 V & \therefore V_o = 0.29 V \end{cases}$$

$$i_D = I_{D1} = \frac{5 - 0.29}{20} = 0.2354 \text{ mA}$$



Case ③. $V_1 = 0V$, $V_2 = 5V$. $M_1 \rightarrow$ cutoff, $M_2 \rightarrow$ Triode,

$$V_o = 0.29V, i_D = 0.2354 \text{ mA} \quad [k_{n1} \neq k_{n2}]$$

$$\underline{i_{D1} = 0 \text{ mA}}, \underline{i_{D2} = 0.2354 \text{ mA}}. \quad [V_{TN1} \neq V_{TN2}, k_{n1} \neq k_{n2}]$$

Case ④ $V_1 = V_2 = 5V$

Assuming, M_1 and M_2 are in triode region.

Reasoning: Because both inputs are high we might expect very low output voltage or drain voltage. ($V_{DS} < V_{GS} - V_{TN}$)

$$i_D = i_{D1} + i_{D2} \leftarrow \text{using KCL.}$$

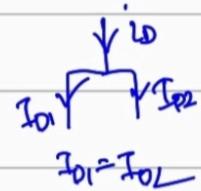
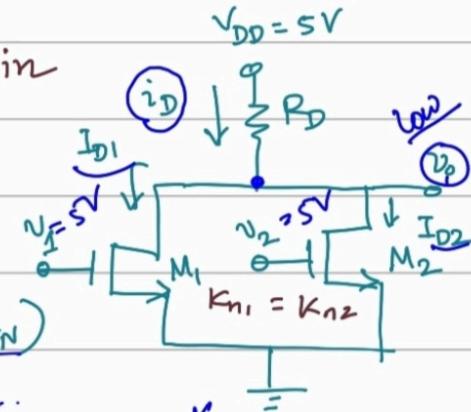
$$\Rightarrow \frac{5 - V_o}{20K} = 0.1m [2 \times (5 - 0.8)V_o - V_o^2] \times 2 =$$

$$\Rightarrow 8V_o^2 - 34.6V_o + 5^2 = 0. \quad V_o = \begin{cases} 0.17V \\ 0.149V \end{cases} \rightarrow \text{Check yourself!}$$

$V_o \neq 0.17V$ because, $V_{DS} = 4.17V$ which is much large value

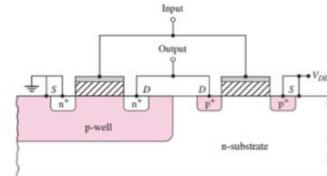
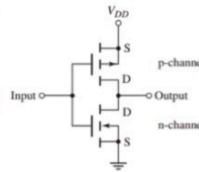
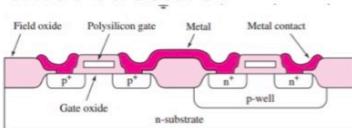
$$V_o = 0.149V \quad i_D = \frac{5 - 0.149}{20K} = 0.243mA$$

$$I_{D1} = I_{D2} = \frac{i_D}{2} = 0.121mA$$



CMOS Logic Families 2

CMOS Structure



Summary:

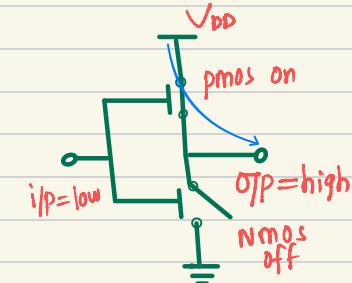
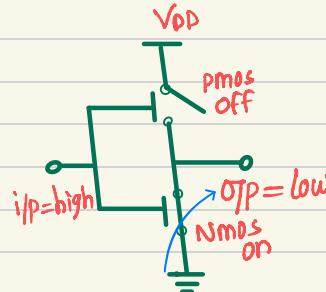
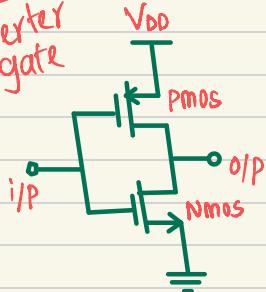
	NMOS	PMOS
High Voltage at Gate	ON	OFF
Low Voltage at Gate	OFF	ON
Symbol	 Outward arrow	 Inward arrow

#Logic Circuits using CMOS

- ⊕ If the gate voltage is high/Low the NMOS will turn on/off and PMOS will turn off/on. If any MOSFET turns on then the drain and source terminal would be short circuited.

Example:

CMOS Inverter
OR, NOT gate



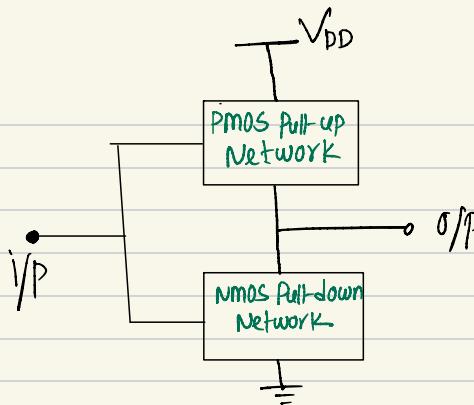
Conduction Complemented

We will design "pull-up network" using PMOS & "pull down" network using NMOS

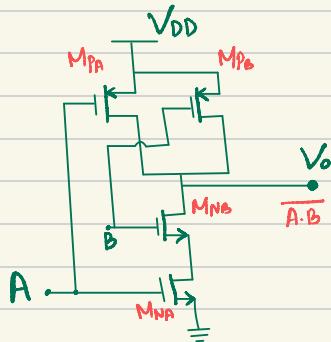
- Conduction Complement means if NMOS are in series/parallel connection then PMOS are going to be in parallel/series.
- Pull-up network rises the o/p Level to the logical high voltage.
- Pull-down network declines the o/p Level to the logical low voltage.



- In order to design pull-down network we must use series NMOS connection for AND Logic and parallel NMOS connection for OR logic under the whole inverse sign.
- Design NMOS pull-down network first using the logic function under the inverse sign, then design the PMOS pull-up network just by complementing the NMOS Network.

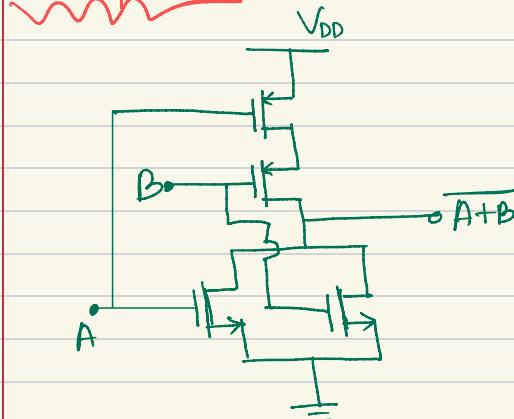


Example: CMOS NAND Gate:

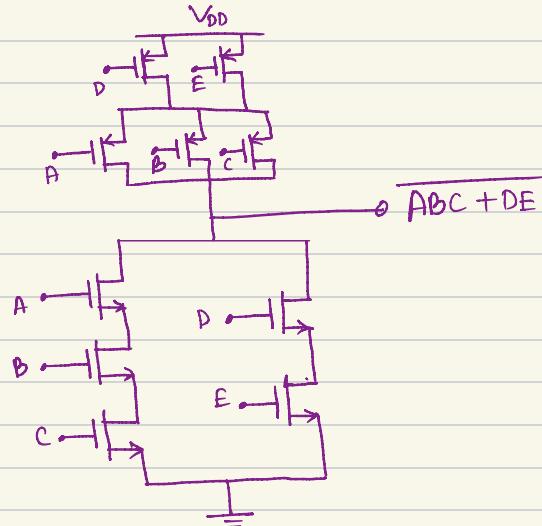


A	B	M _{PA}	M _{PB}	M _{NA}	M _{NB}	V _O =A.B
0	0	ON	ON	off	off	1
0	1	ON	off	off	ON	1
1	0	off	ON	ON	off	1
1	1	off	off	ON	ON	0

Example: CMOS NOR Gate:



Example: $Y = \overline{ABC + DE}$



Example: $AB + C(D+E)$

