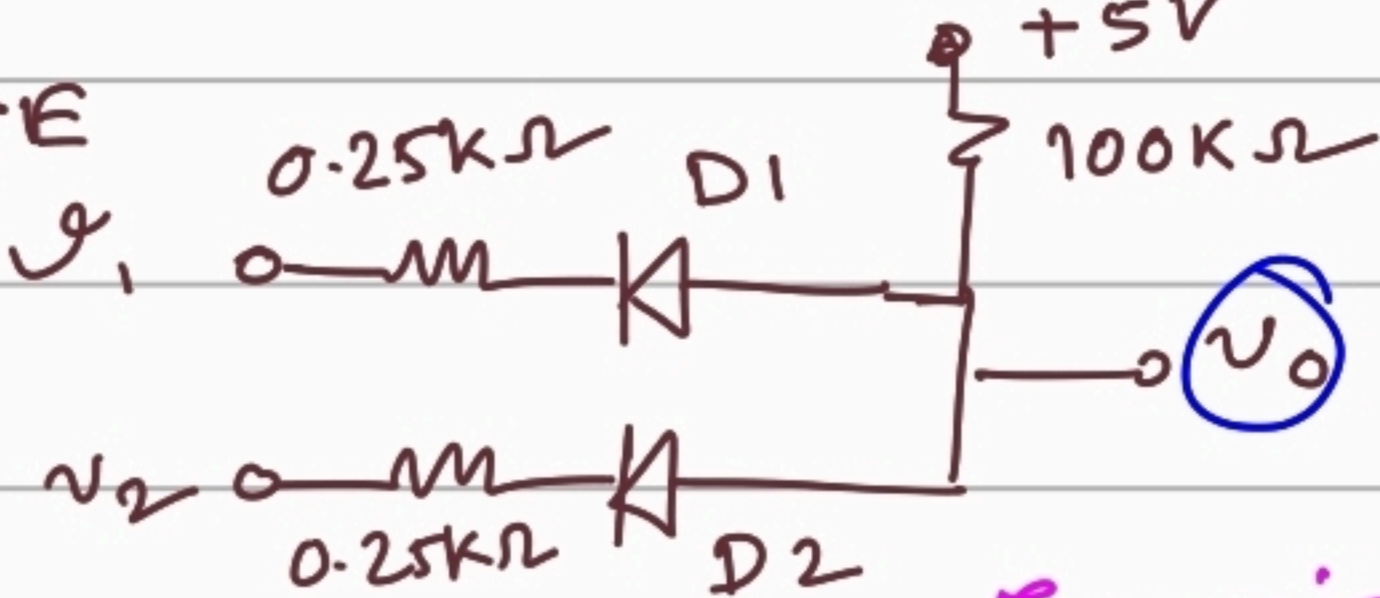
AND GATE : 2-AND GATE

v_1	v_2	v_o	D1	D2
5V	5V	5V	OFF	OFF
5V	0V	x	OFF	ON
0V	5V	x	ON	OFF
0V	0V	x	ON	ON



Exercise

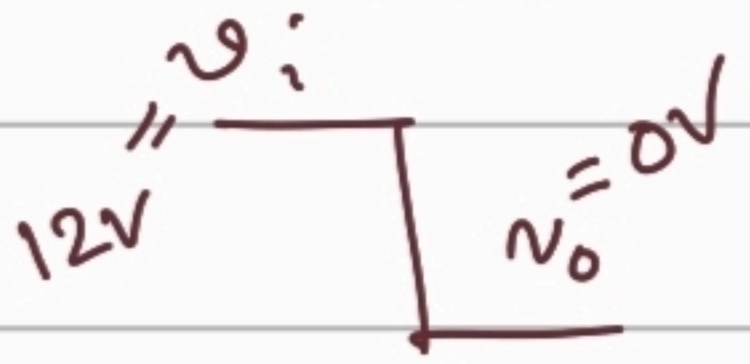
0.68 — 0.7 V

\# For choosing output logical low, we will take max of the logical output low.

$V_{OL} = 0.7V$ → all voltages below this voltage would be considered logical low.

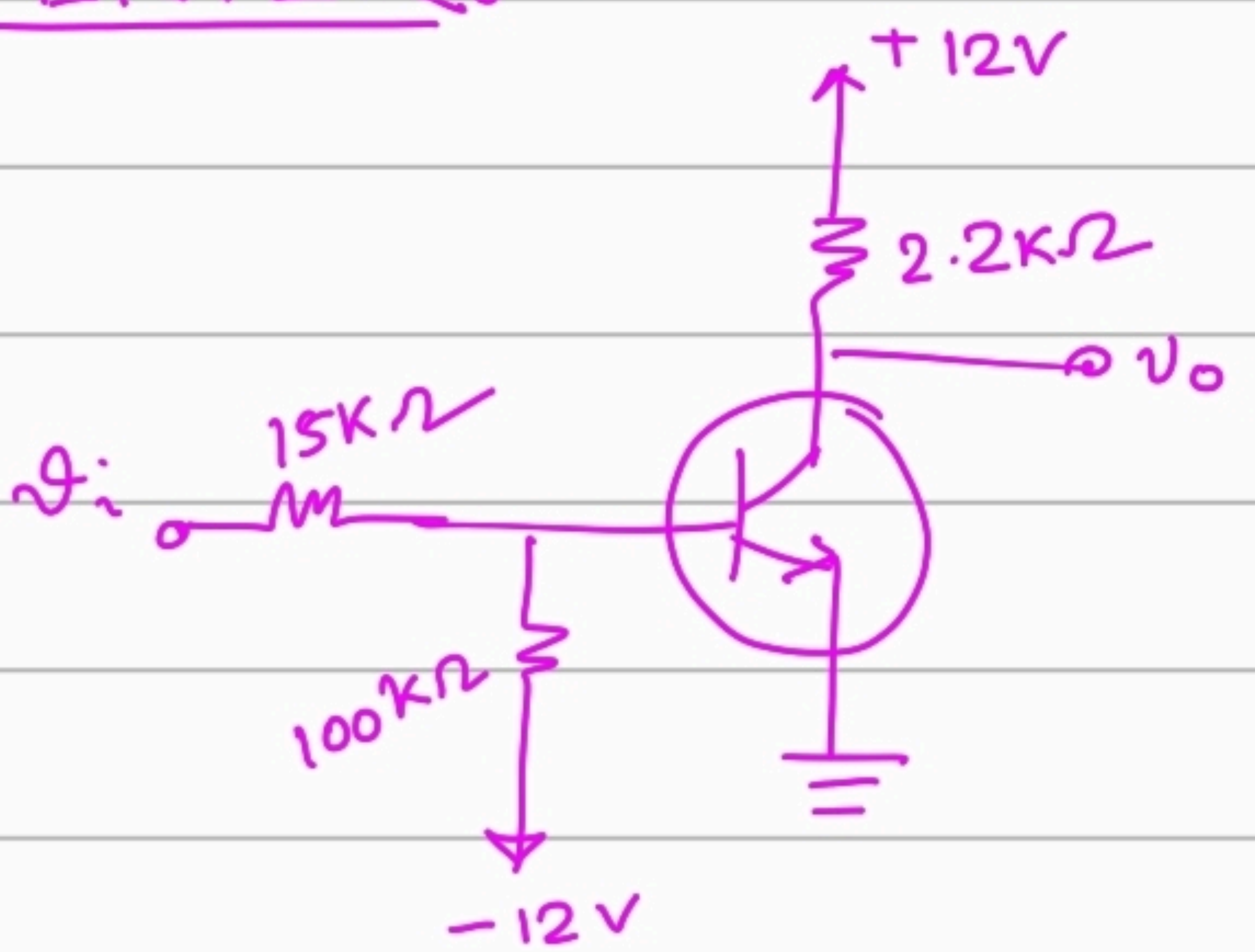
II Register Transistor Logic (RTL)

RTL INVERTER :-



input logical hi = +12V

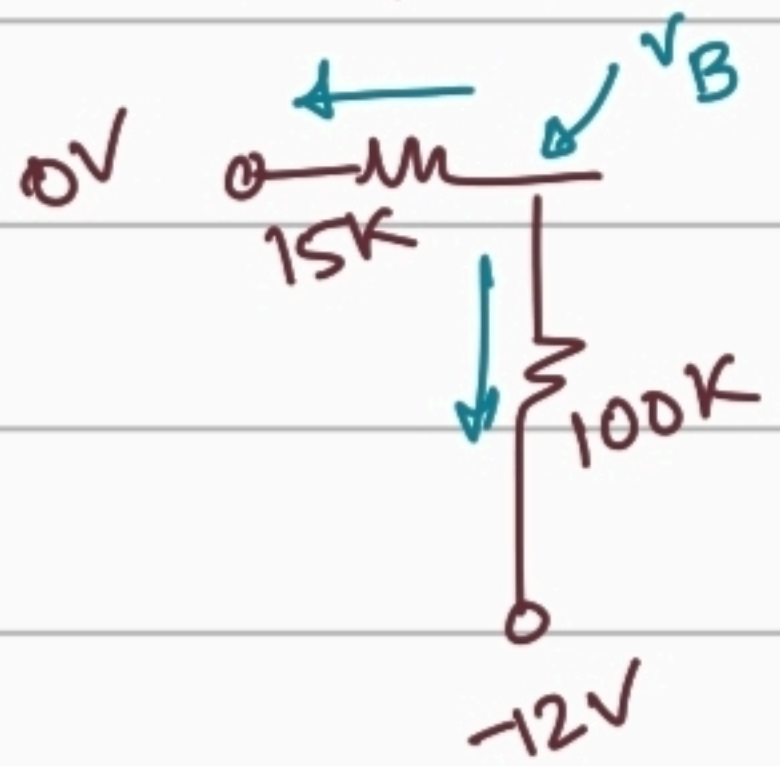
low = 0V



v_i	v_o
1	0
0	1

Case 1 : $v_i = 0V$

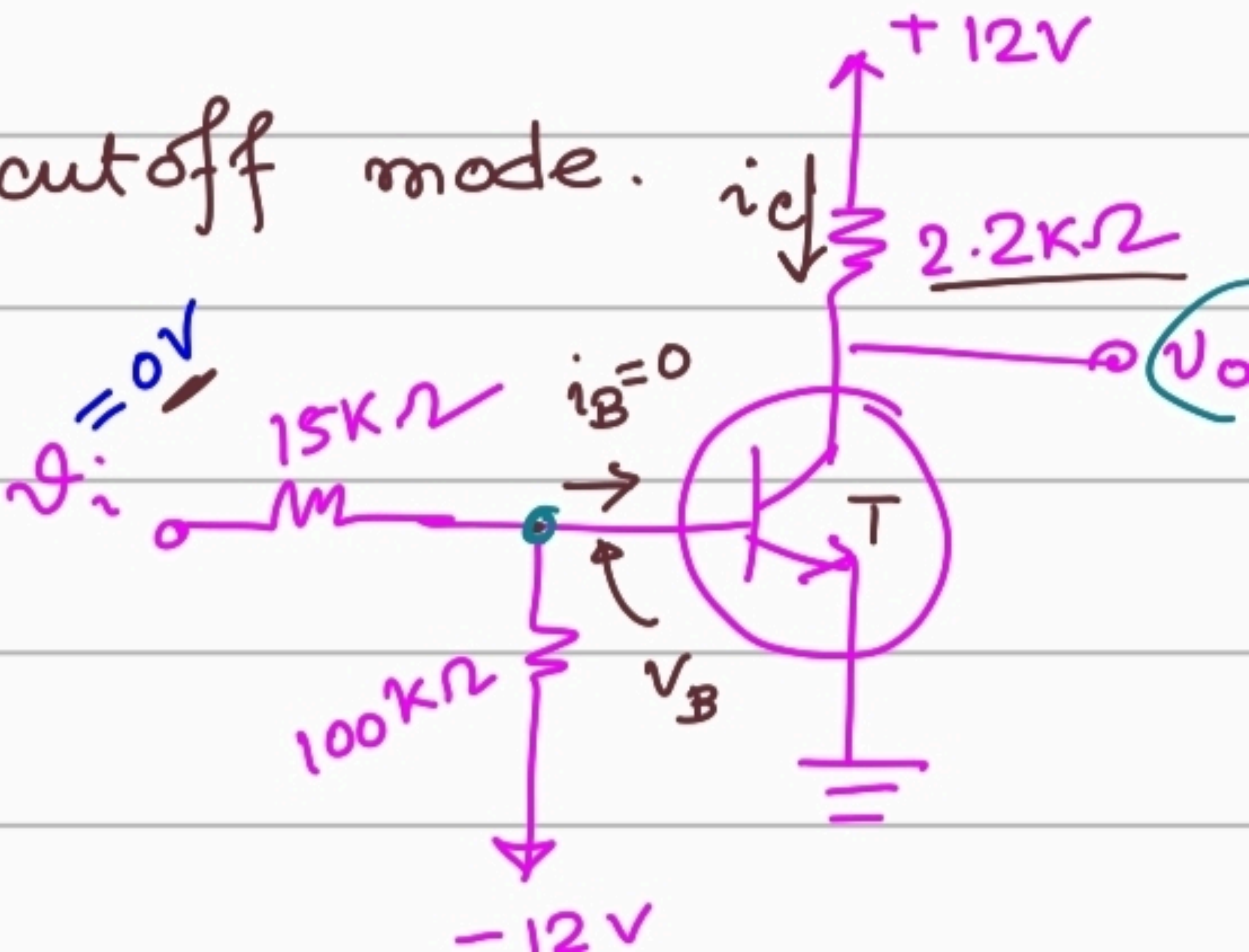
Guess/Assumption: T is in cutoff mode.



$$\frac{V_B-(-12)}{100K} + \frac{V_B - 0}{15K} = 0$$

$$\Rightarrow V_B = -1.565V$$

$$V_E = 0V$$



Verification: $V_\gamma = V_{BE}$ (cutin voltage) $\leq 0.5V$

$V_{BE} = -1.565V < 0.5V$ (Our assumption is valid)

For cutoff mode. $i_C = i_B = i_E = 0\,mA$

$$i_C = \frac{12 - v_o}{2.2K} = 0 \Rightarrow \boxed{v_o = 12V}$$ logical High Output voltage.

Case ②: $v_i = +12V$

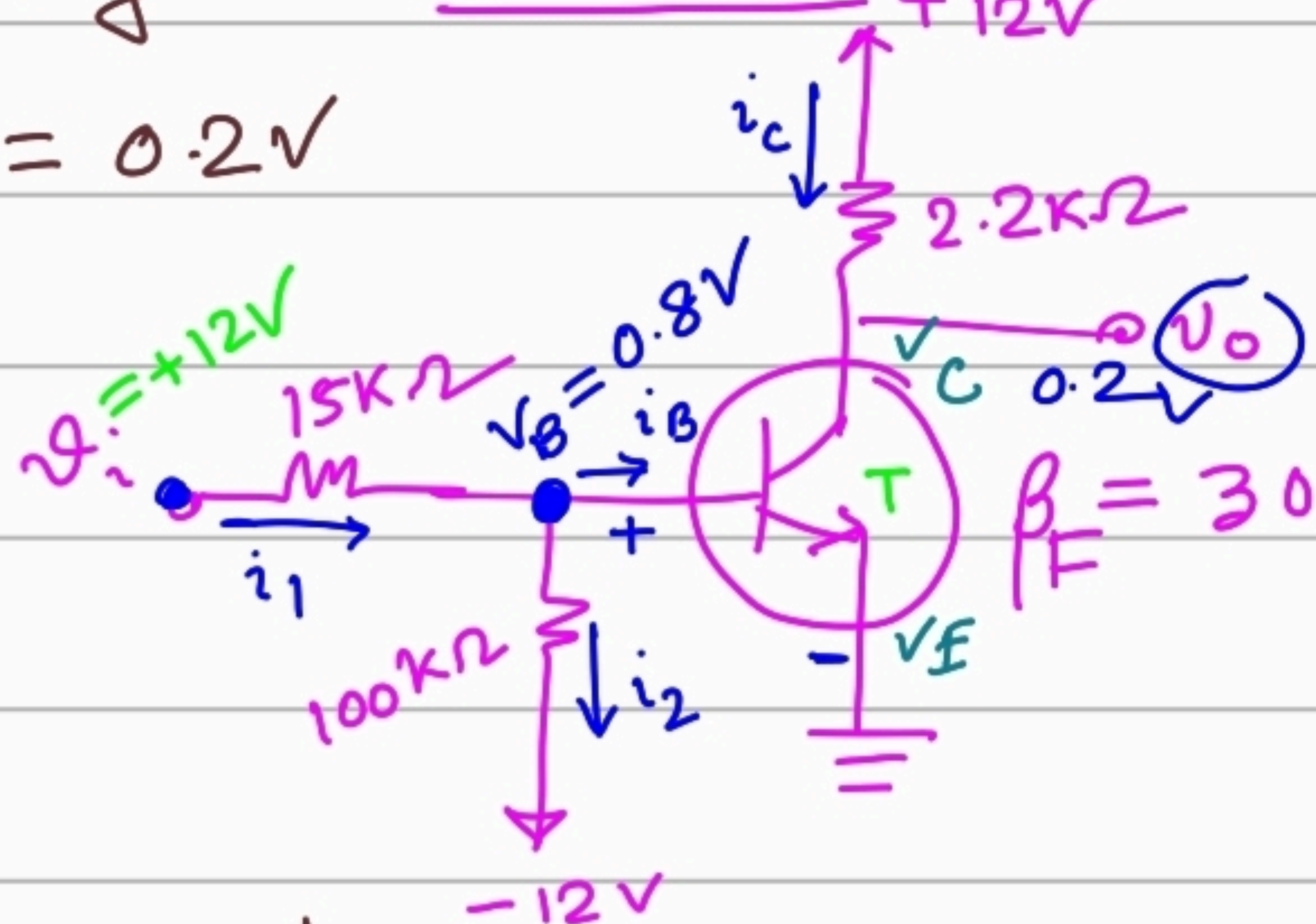
Assumption: T is operating in saturation mode.

★ $v_o = V_C = V_C - V_E = V_{CE} = 0.2V$

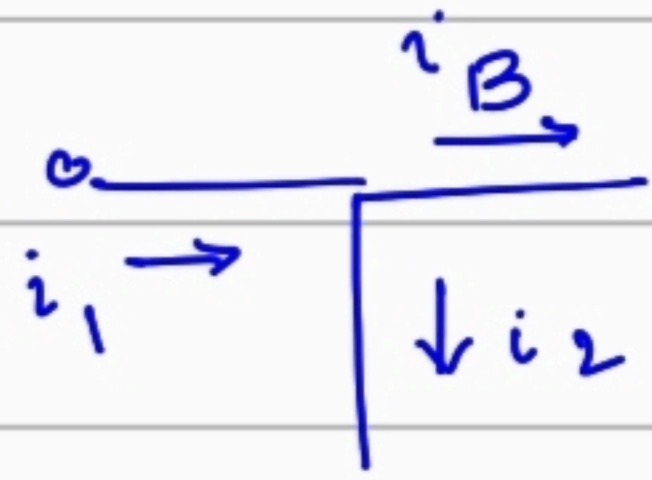
★ $i_C = \dfrac{12 - 0.2}{2.2K} = 5.36\,mA$

★ $i_1 = \dfrac{12 - 0.8}{15K} = 0.746\,mA$

★ $i_2 = \dfrac{0.8 - (-12)}{100K} = 0.128\,mA$



When transistor is operating in saturation mode $V_{BE} = 0.8V$, $V_{CE} = 0.2V/0.1V$



$i_B = i_1 - i_2 = 0.619\,mA$

Verification: $\beta_{forced} = \dfrac{i_C}{i_B} = 8.659 < 30 = \beta_F$

Our assumption is valid.

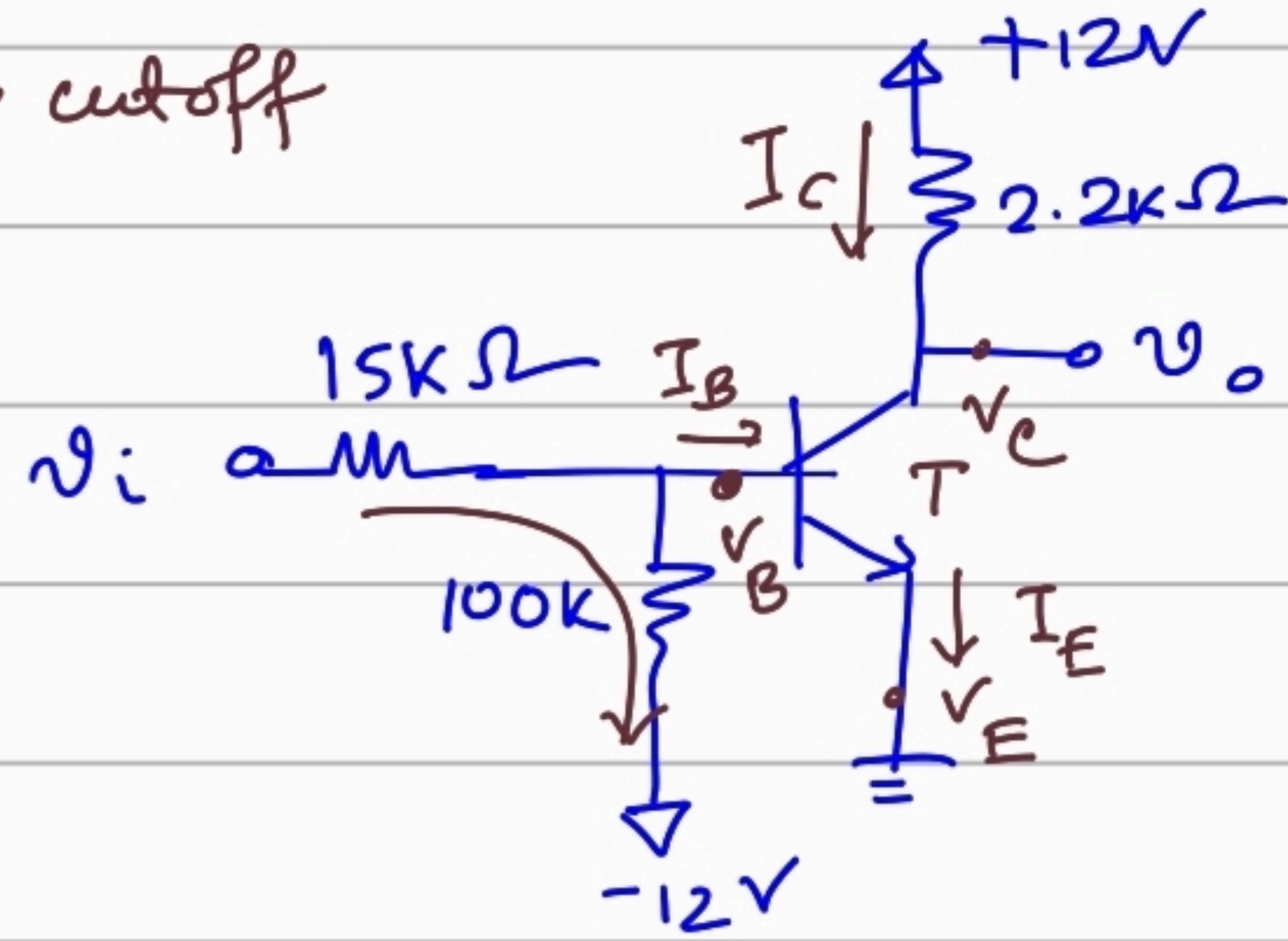
Thus our analysis shows output voltage is now $0.2V$ = logical low voltage at the output terminal.

$V_{OL} = 0.2V$

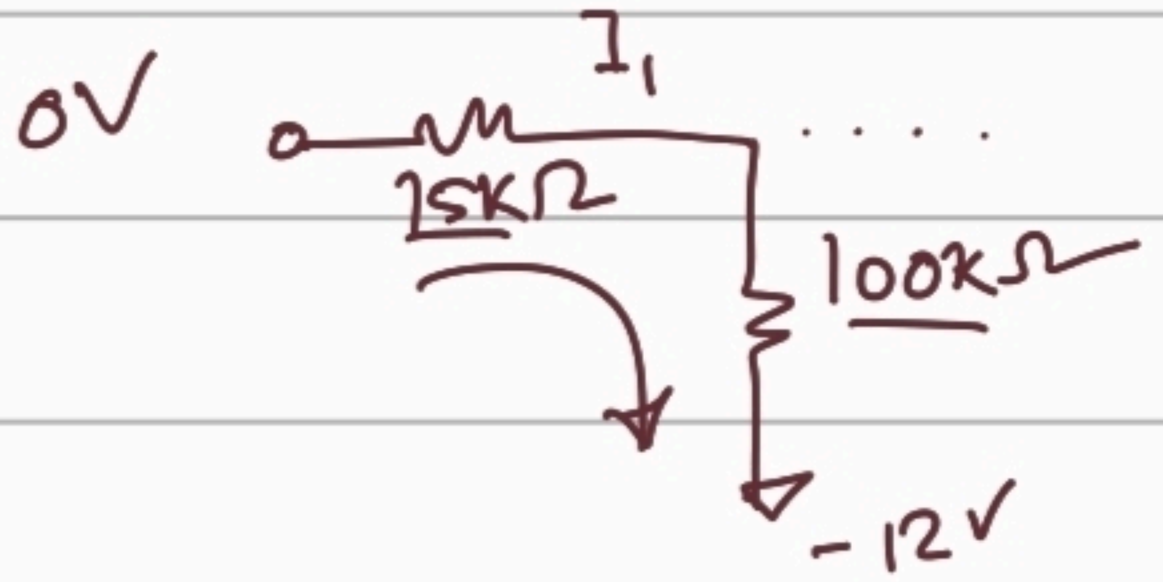
Lecture 4: RTL circuits : Power dissipation, Noise Margin and Fanout Calculation.

Power dissipation in RTL inverter :-

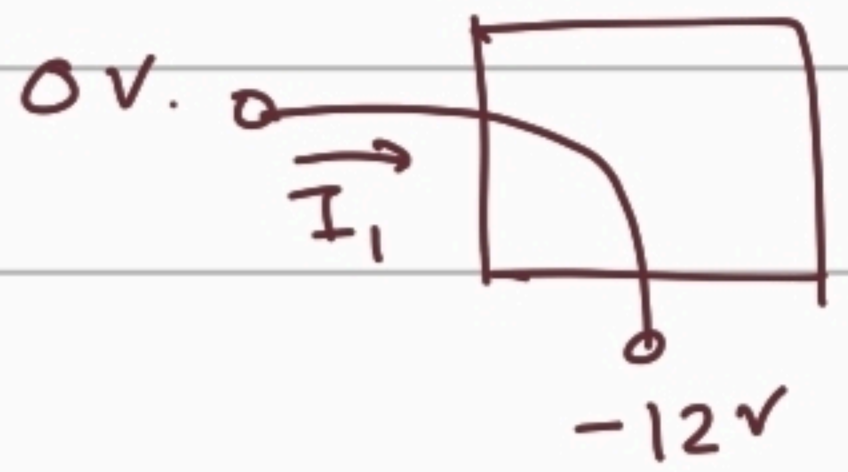
Case ① $v_i = 0\ V$. $T \rightarrow$ cutoff



$I_B = I_C = I_E = 0\,mA$



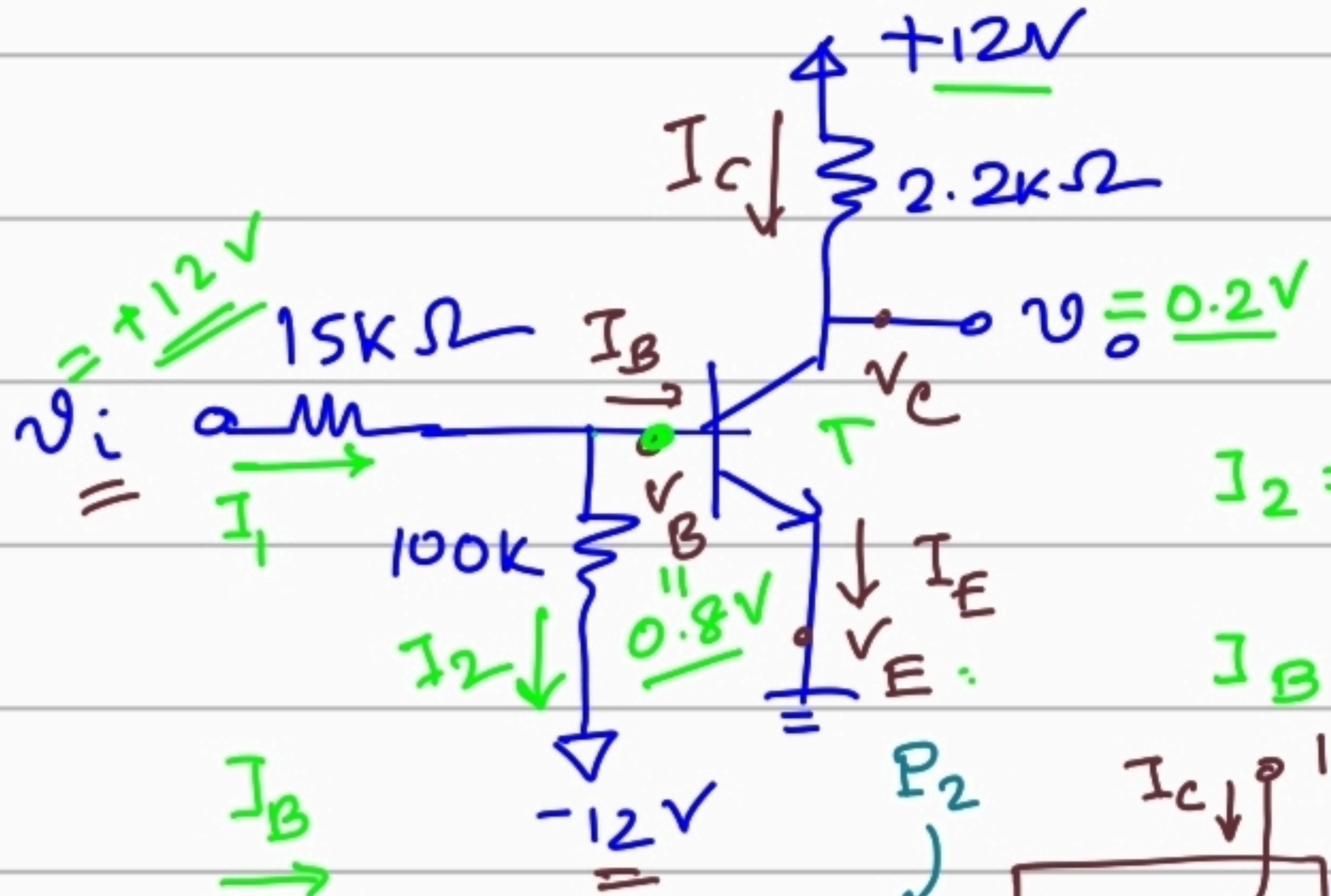
$$I_1 = \frac{0-(-12)}{115\,k\Omega} = 0.104\,mA$$



$$P = (0-(-12)) \times 0.104$$
$$= \boxed{1.2521\,mW}$$

Case ② $v_i = +12V$. $T \rightarrow$ saturation (RTL)

$V_{BE} = 0.8V$, $V_{CE} = 0.2V$ $(0.1V)$

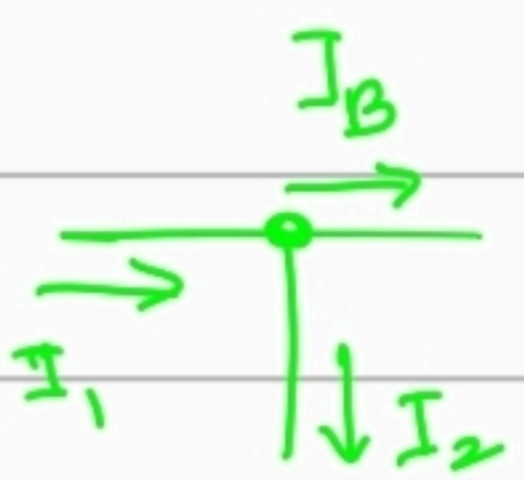


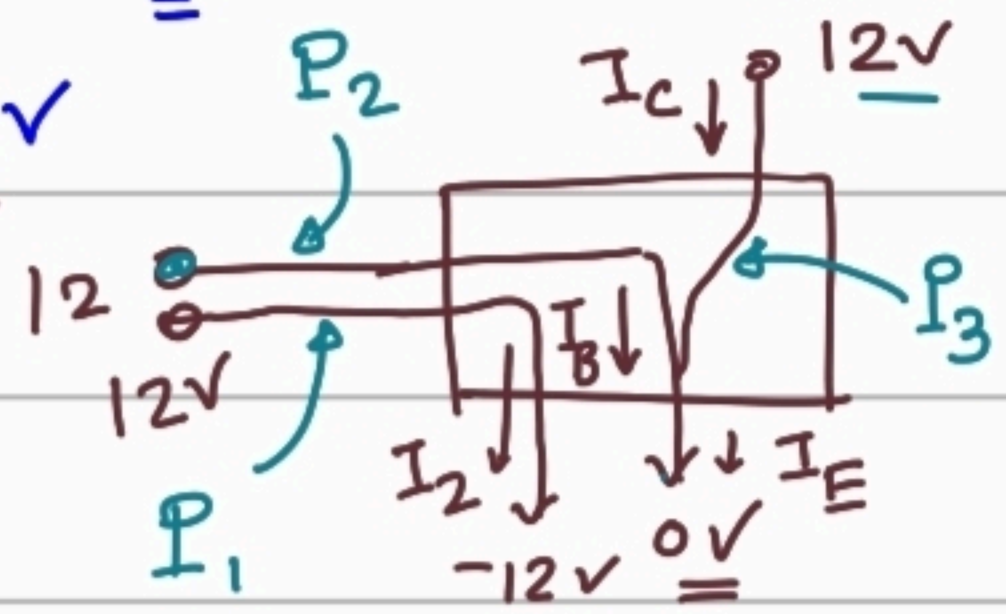
$$I_C = \frac{12-0.2}{2.2K} = 5.3636\,mA$$

$$I_1 = \frac{12-0.8}{15K} = 0.7466\,mA$$

$$I_2 = \frac{0.8-(-12)}{100K} = 0.128\,mA$$

$$I_B = I_1 - I_2 = 0.6186\,mA$$





$$P_1 = (12-(-12)) \times 0.128$$
$$= 3.072\,mW$$

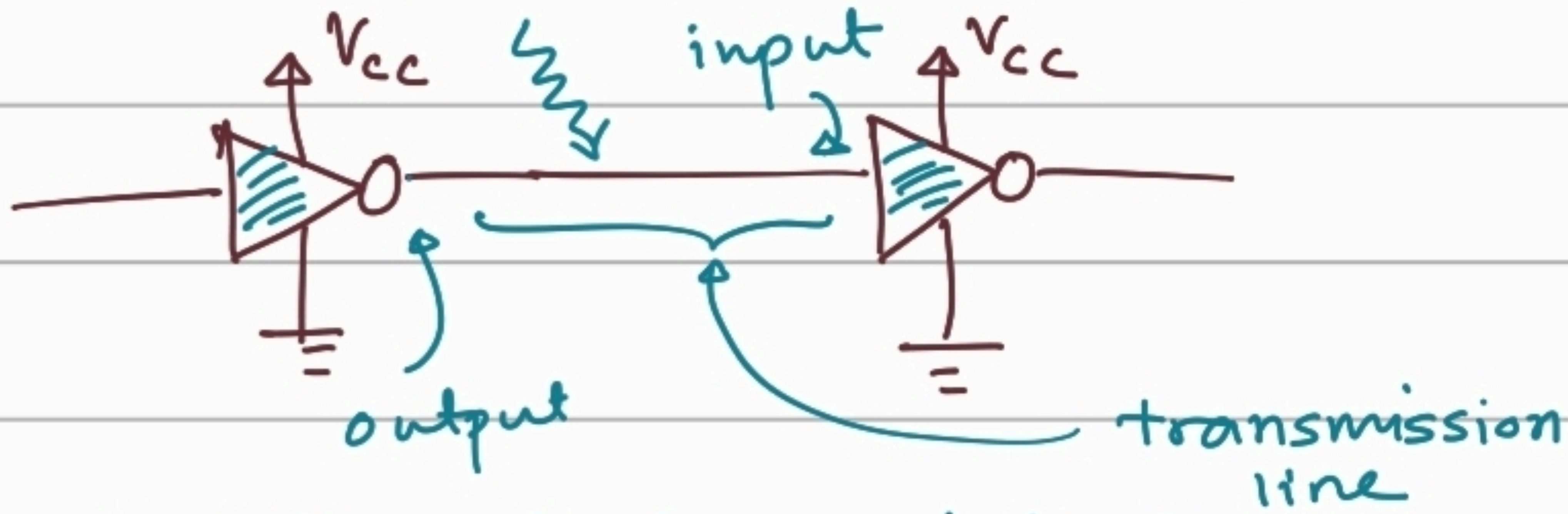
$$P_2 = (12-0) \times 0.6186$$
$$= 7.4323\,mW$$

$P_3 = (12-0) \times 5.3636 = 64.3632\,mW$

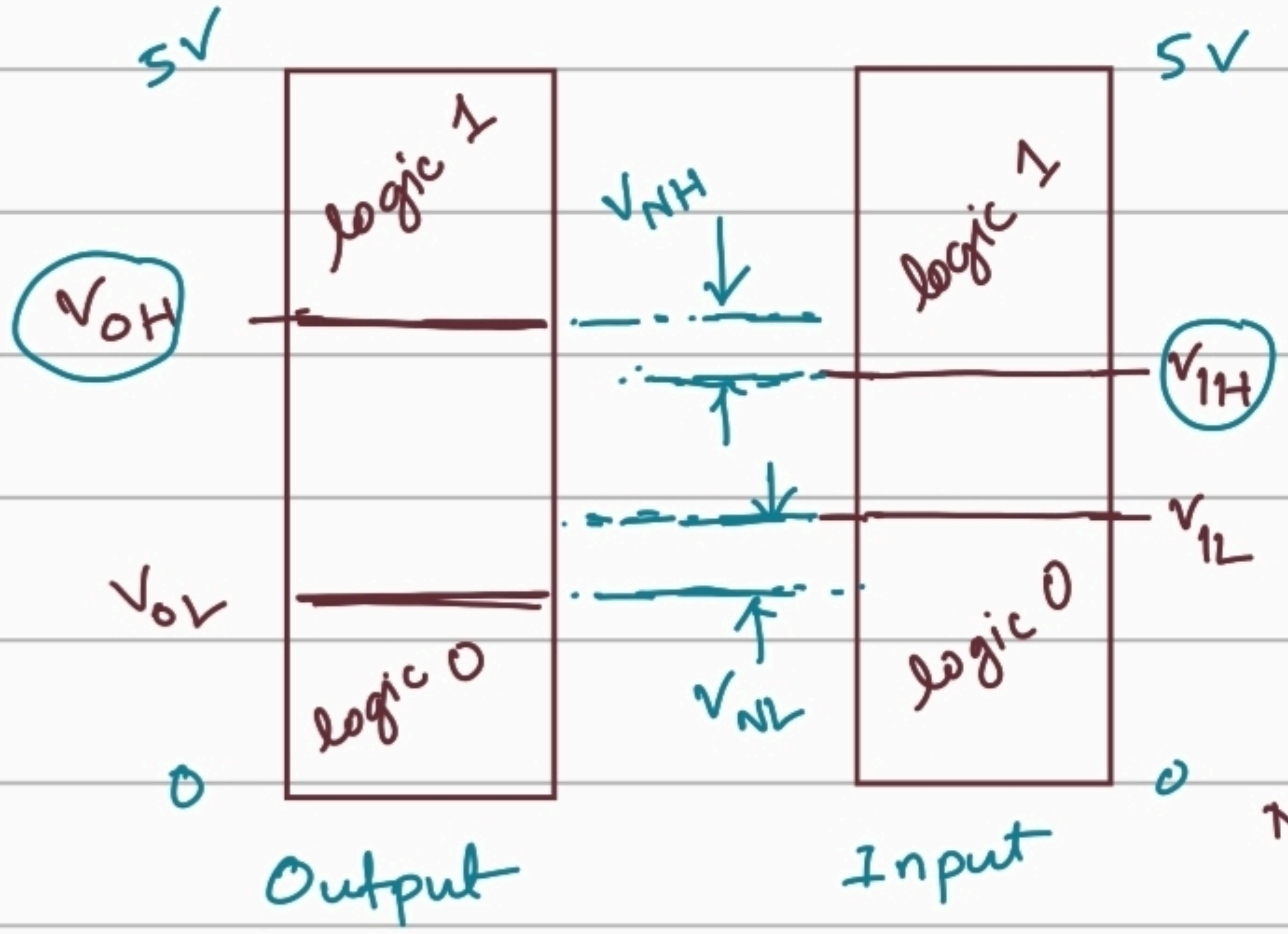
Total power dissipation, $P = P_1 + P_2 + P_3 = \boxed{74.8534\,mW}$

NOISE MARGIN:-

The amount of noise voltage a digital logic circuit can tolerate while successful transmission.



We model different types interference or noises using "noise voltage."



HIGH state noise margin:

$V_{NH} = V_{OH} - V_{IH}$

LOW state noise margin

$V_{NL} = V_{IH} - V_{OH}$

Noise margin.

$V_N = \min(V_{NH}, V_{NL})$

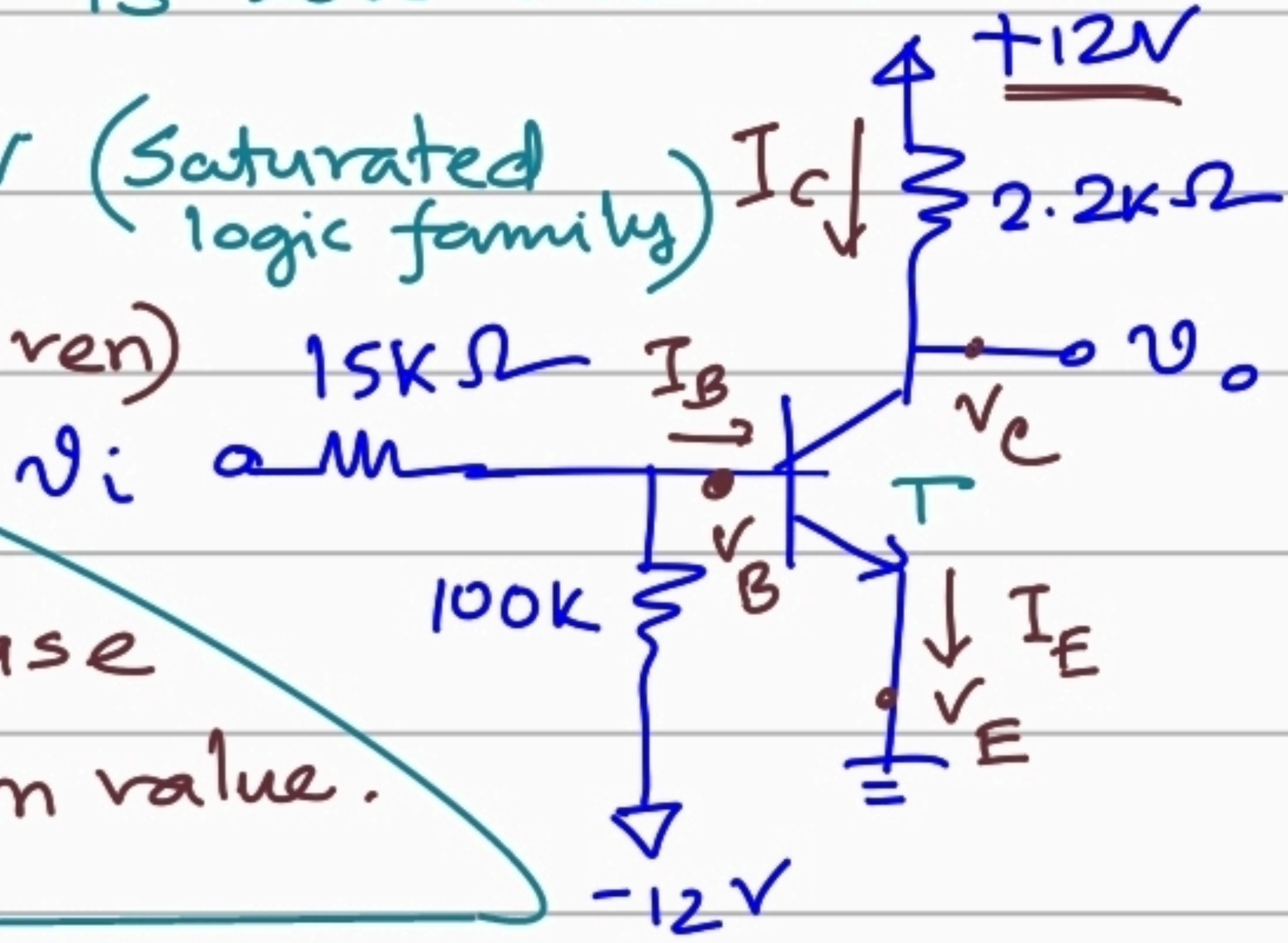
Why do we use minimum?

→ To ensure safety margins for both high and low voltages.

V_{OH} / V_{IH} → minimum voltage level at an ~~output~~ input in the logical "1" state under defined load condition.

V_{OL} / V_{IL} → maximum " " at an ~~output~~ input in the logical "0" state under defined load condition.

Example: Output voltage is low when T is in saturation. $V_{OL} = 0.2V$ (Saturated logic family)

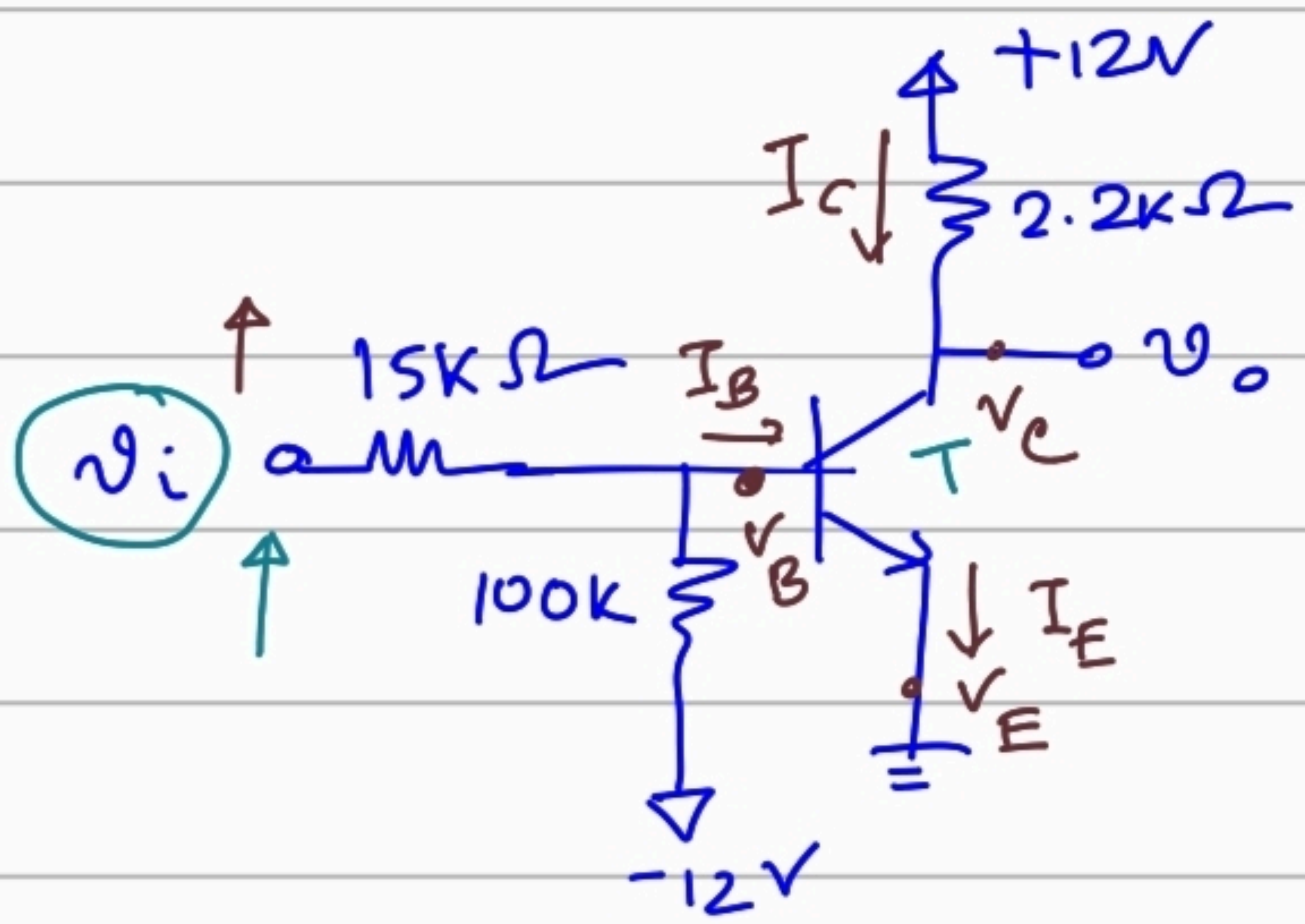


* V_{OH} = ? (This will be given)

The output high voltage can be allowed to decrease 0.5V from its maximum value.

* $V_{OH} = +12 - 0.5V = 11.5V$

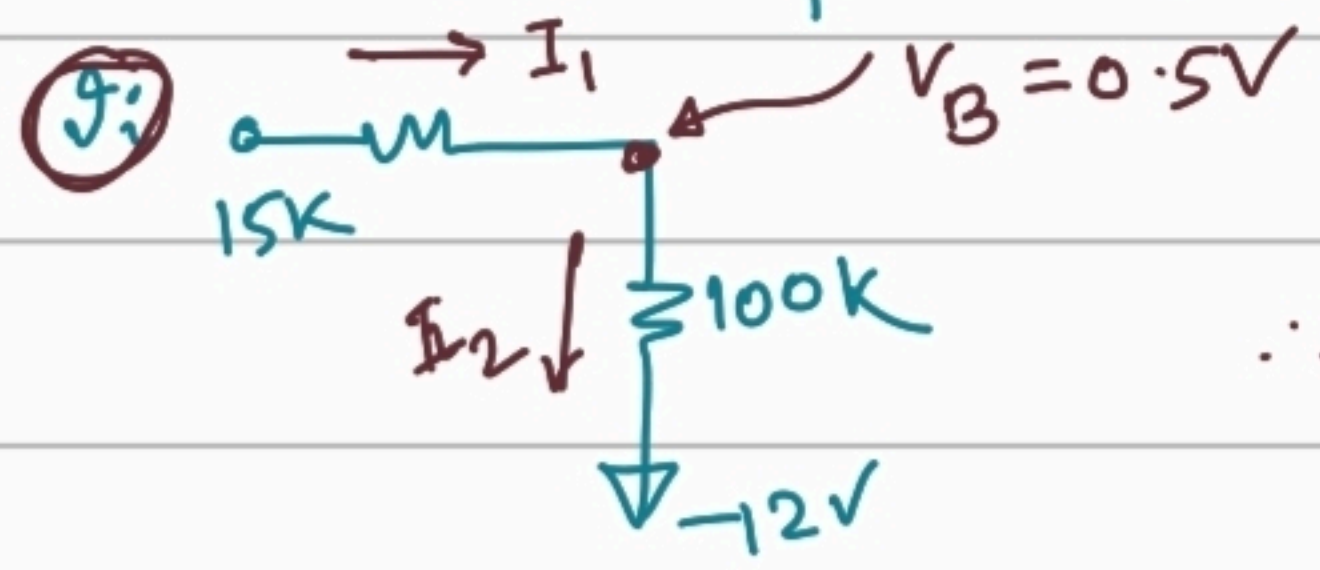
* V_{IL} calculation:



* When input voltage is low, transistor operates in cutoff mode.
* For RTL circuit, V_{IL} should be equal to the maximum voltage that takes the transistor on the verge of turn off to turn on condition.

* The transistor will turn on is $V_{BE} \geq 0.5V$.
* We need find the input voltage so that $V_{BE} = 0.5V$ but we assume transistor is in cutoff.
* T → cutoff, $I_B = 0\,mA$

$$I_2 = \frac{0.5-(-12)}{100k} = 0.125\,mA$$



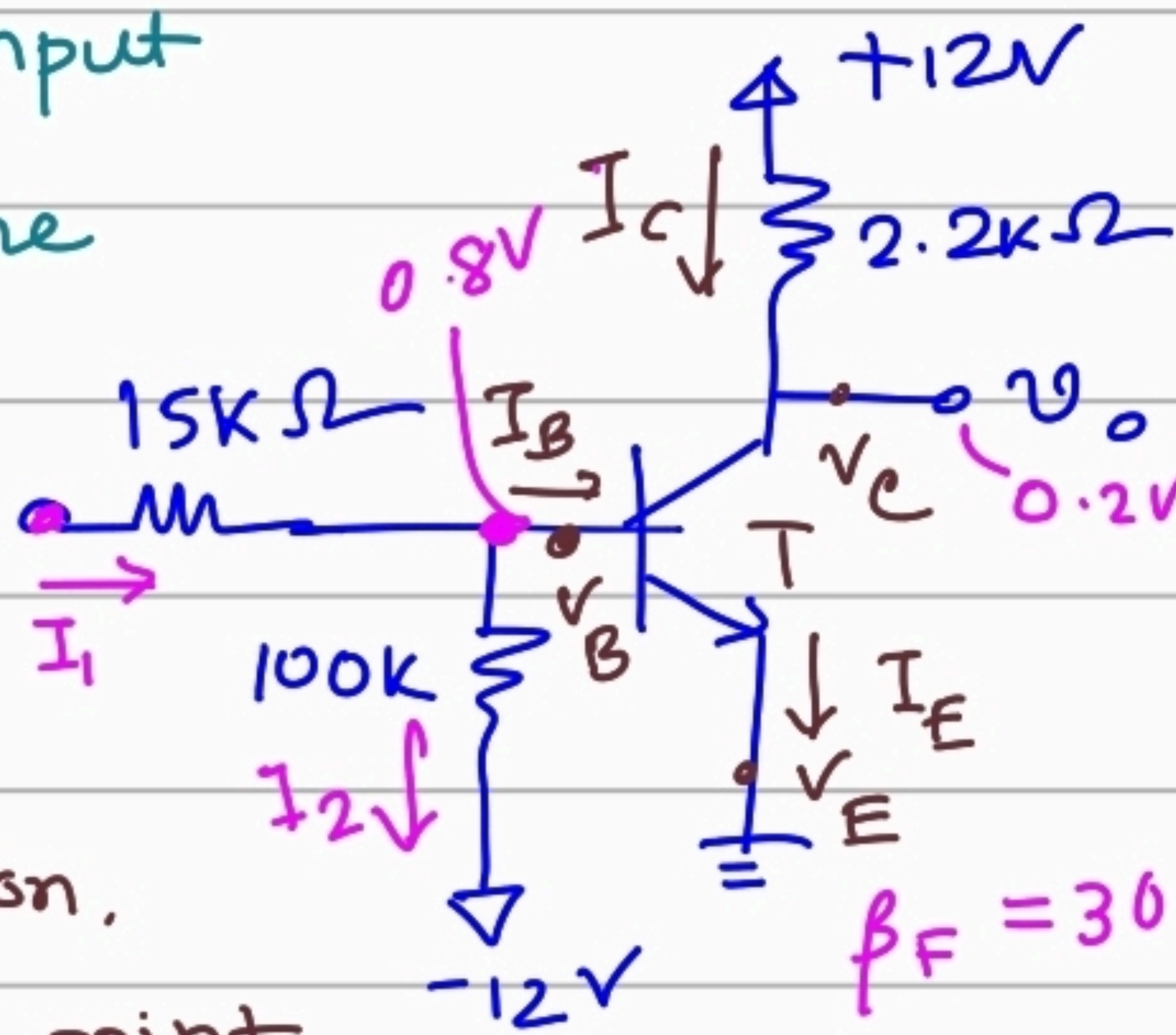
$I_1 = I_2$, $I_1 = \frac{V_i - 0.5}{15K} = 0.125\,mA$

$\therefore V_i = 0.5 + 15 \times 0.125 = 2.375\,V$

$\boxed{V_{IL} = 2.375\,V}$

V_{1H} calculation: When input voltage is high, transistor T operates in saturation mode. $v_{CE} = 0.2V = v_o$.

* The minimum voltage at the input terminal which will change the operating mode of transistor T to saturation to forward active mode should be V_{1H}.



* We will assume T is saturation, but $\beta_{forced} \approx \beta_F$. [Transition point between sat. and F.A.]

* T → saturation. $I_C = \frac{12-0.2}{2.2K} = 5.3636\,mA$

$\beta_{forced} = \frac{I_C}{I_B} = 30 \Rightarrow I_B = \frac{I_C}{\beta} = 0.1788\,mA$.

$I_2 = \frac{0.8-(-12)}{100K} = 0.128\,mA$. $I_1 = I_2 + I_B = 0.3068\,mA$

$\frac{v_i - 0.8}{15K} = 0.3068\,mA \Rightarrow v_i = 0.8 + 15 \times 0.3068$
$= 5.4018V$

$$\boxed{V_{1H} = 5.4018V}$$

High state noise margin : $V_{NH} = V_{OH} - V_{IH}$
$= 6.0982V$

Low state noise margin : $V_{NL} = V_{IL} - V_{OL}$
$= 2.175V$

Noise margin $= \min(6.0982, 2.175)$
$= \boxed{2.175V}$