Digital logic family

Bipolar logic family

(electron and hole both contribute in current conduction)

B.J.T.

Saturated Logic family

(main transistors will operate in saturation and cutoff)

(a) Resistor Transistor Logic (RTL) ✓

(b) Diode Transistor Logic (DTL) ✓

(c) Direct Coupled Transistor Logic (DCTL)

(d) Integrated Injection Logic (IIL)

(e) High Threshold Logic (HTL) ✓

(f) Transistor transistor Logic (TTL) ✓

Unsaturated Logic family

(main transistors will operate in forward active and cutoff)

(a) Schottky TTL

(b) Emitter Coupled Logic (ECL) ✓

Unipolar logic family

(only single type of carrier contributes in current conduction) electron or hole.

JFET, MOSFET etc.

✓ (i) PMOS logic family

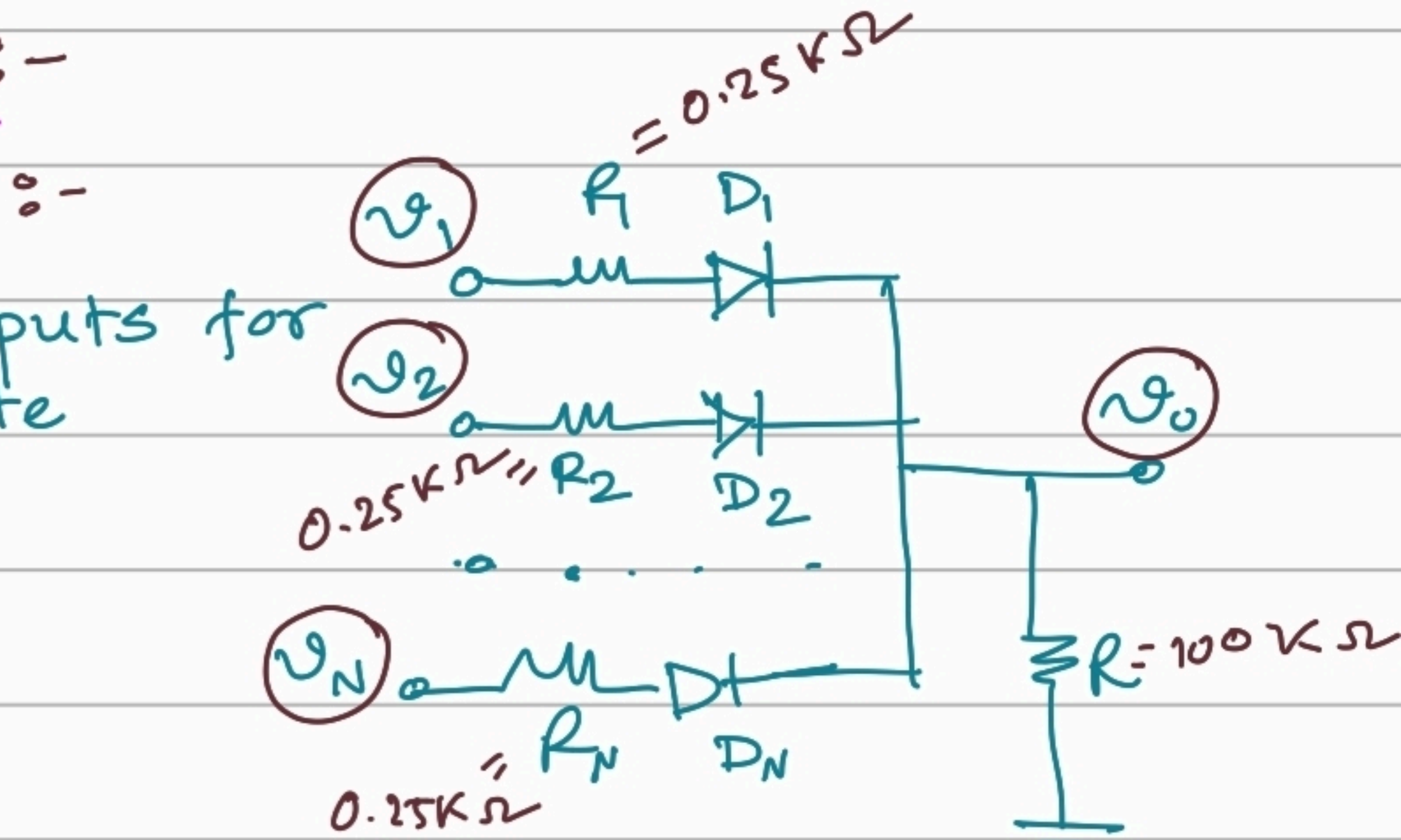
✓ (ii) NMOS ..

(iii) CMOS ..

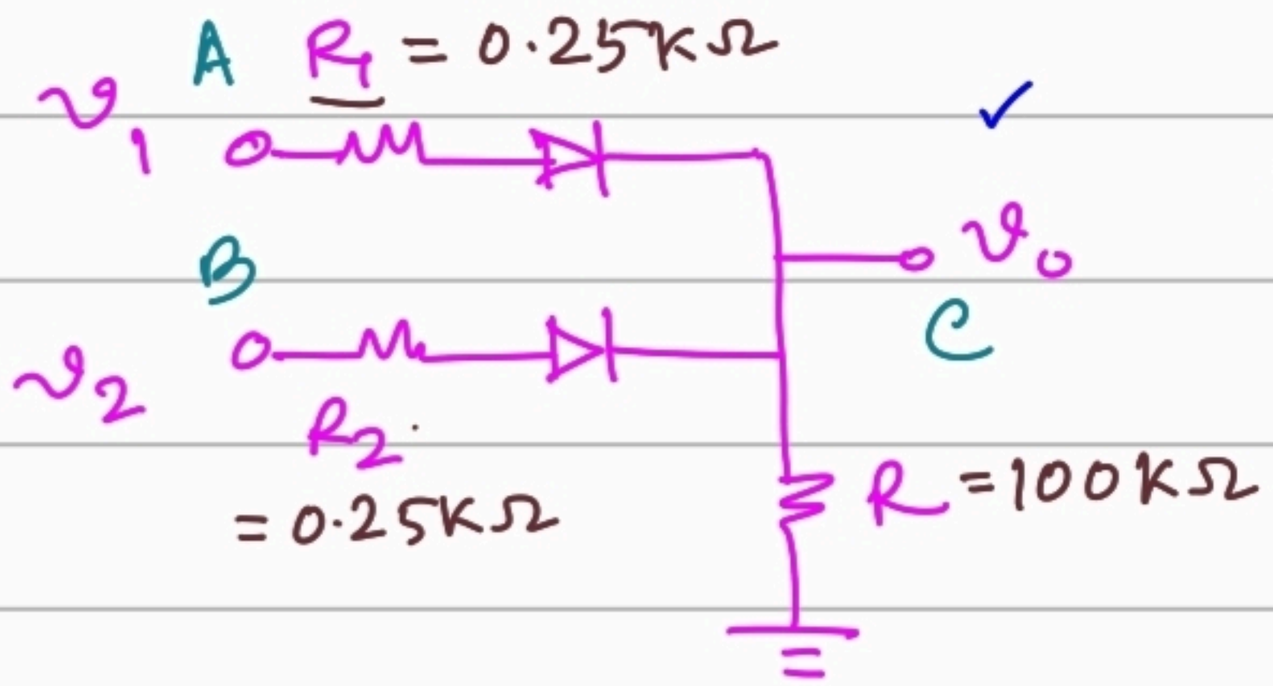
Diode Logic :-

OR GATE :-

N number of inputs for OR gate



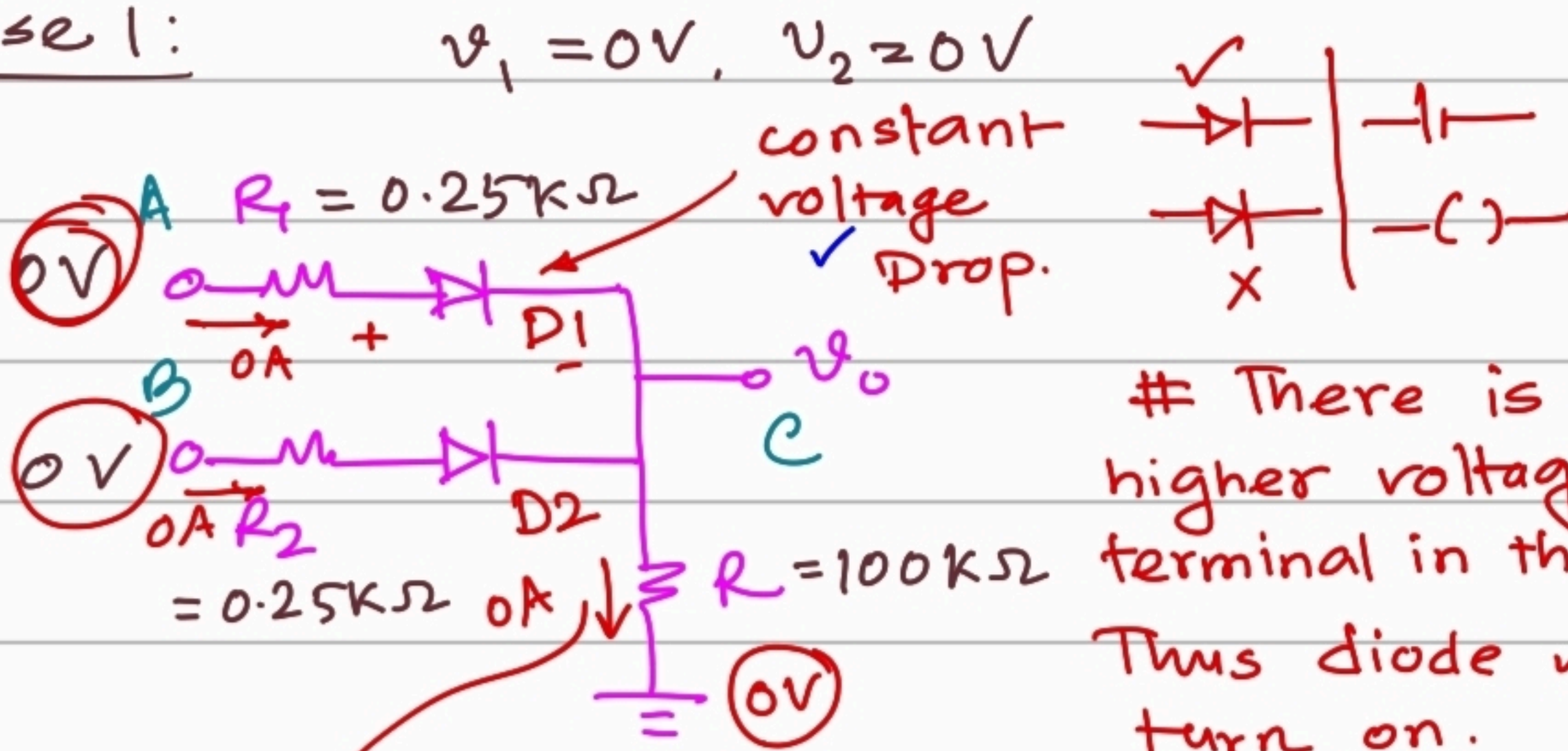
Operation : 2-OR GATE



	A	B	V_1	V_2	V_o	C
①	0	0	0V	0V	0V	0
②	0	1	0V	5V	4.289	1
③	1	0	5V	0V	4.289	1
④	1	1	5V	5V	4.294	1

We will assume logic 1 for input part is 5V. and logic 0 for input part is 0V.

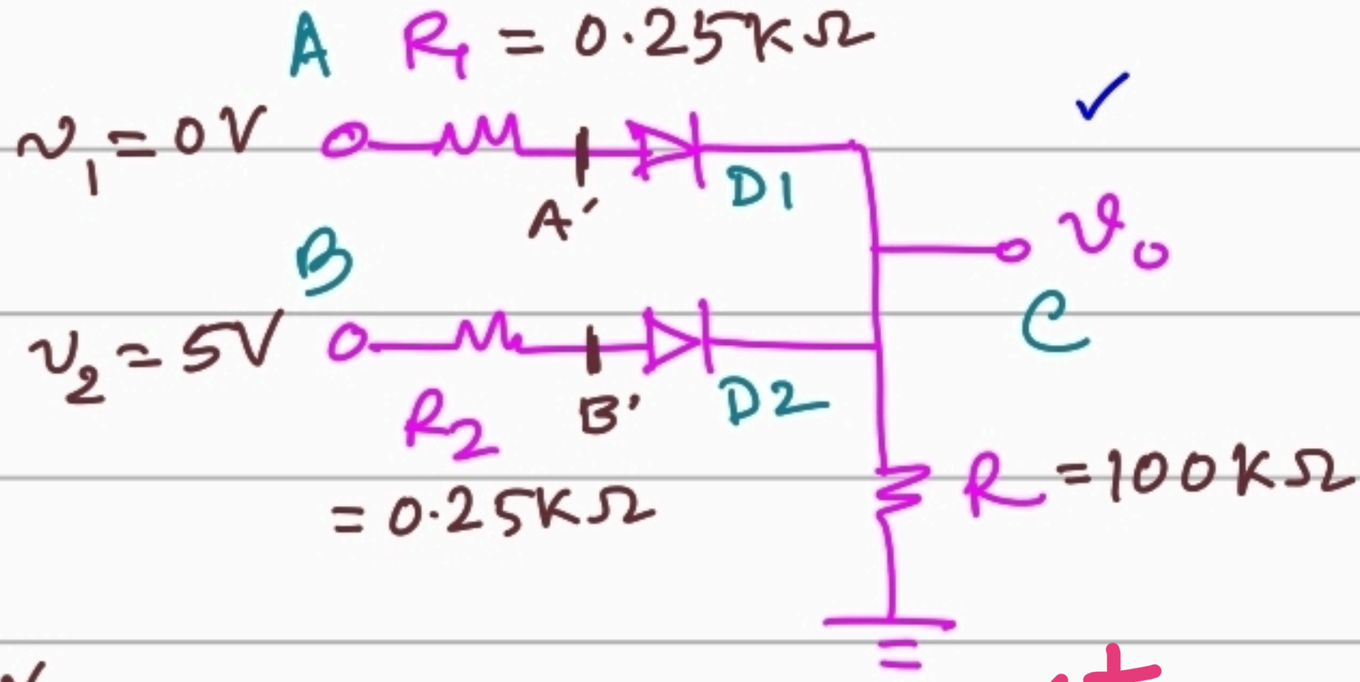
Case 1: $v_1 = 0V$, $v_2 = 0V$



There is no higher voltage input terminal in this circuit. Thus diode will never turn on.

$$i = \frac{v_o - 0}{R} \Rightarrow 0 = \frac{v_o}{R} \quad \therefore \boxed{v_o = 0V}$$

Case ② & ③



✓

Case ⓐ

* D1, OFF, D2, OFF

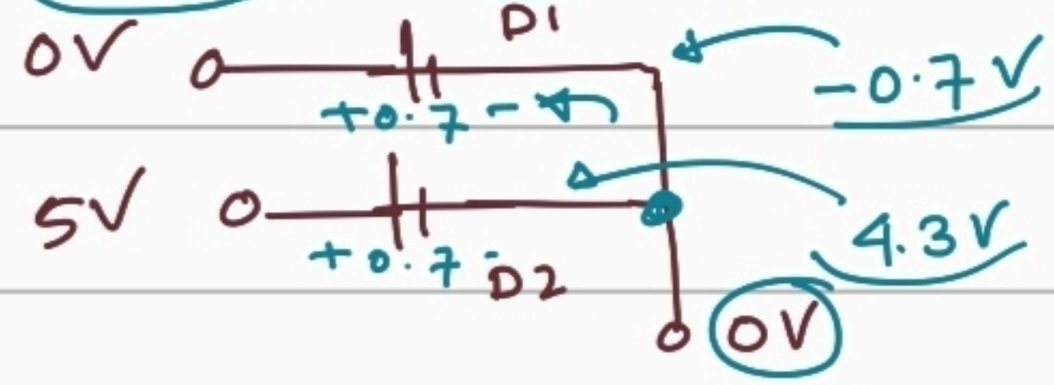
$V_{A'} = 0V$, $v_{B'} = 5V$

$v_o = 0V$.

Contradiction.

* D1 ON, D2 OFF: # Contradiction.

* D1 ON, D2, ON → Simplification

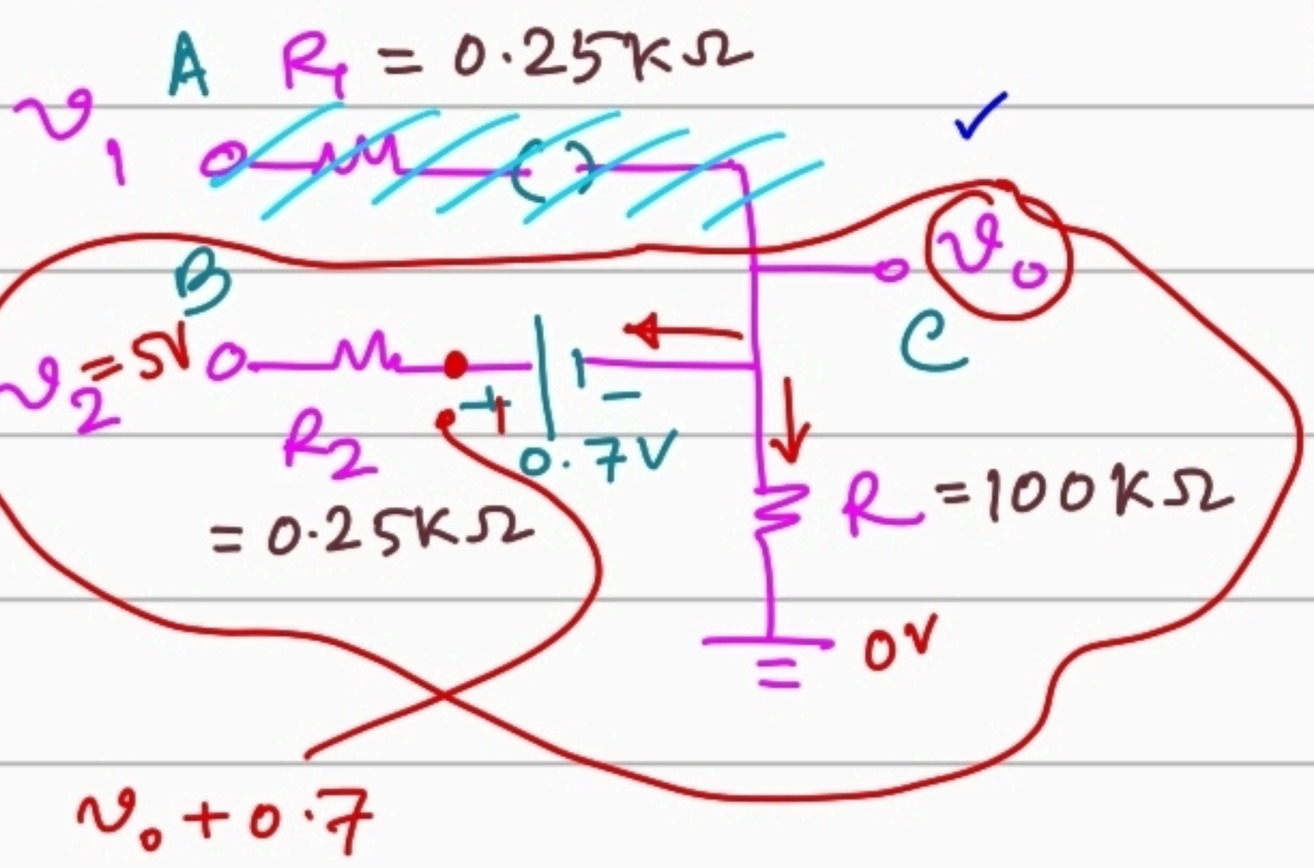


One node always has a single voltage.

const volt. drop model

If we do thorough analysis, we would find a contradictory result that current would flow in opposite direction through D1 diode.

* D1 OFF, D2 ON

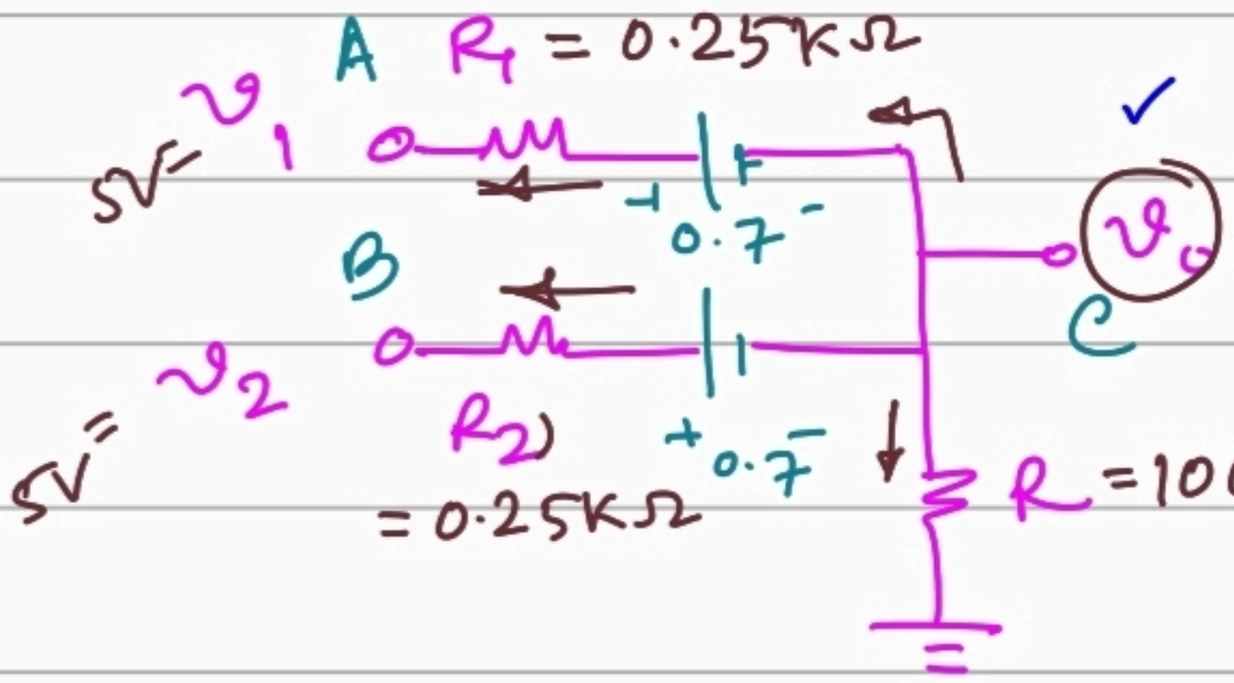


$$\frac{v_o - 0}{100K} + \frac{(v_o + 0.7) - 5V}{0.25K} = 0$$

$$\Rightarrow \boxed{v_o = 4.2893\ V}$$

Case 4: $v_1 = 5V$, $v_2 = 5V$

* D_1 ON, D_2 ON.



$$\frac{v_o - 0}{100K} + \frac{(v_o + 0.7) - 5V}{0.25K} \times 2 = 0$$

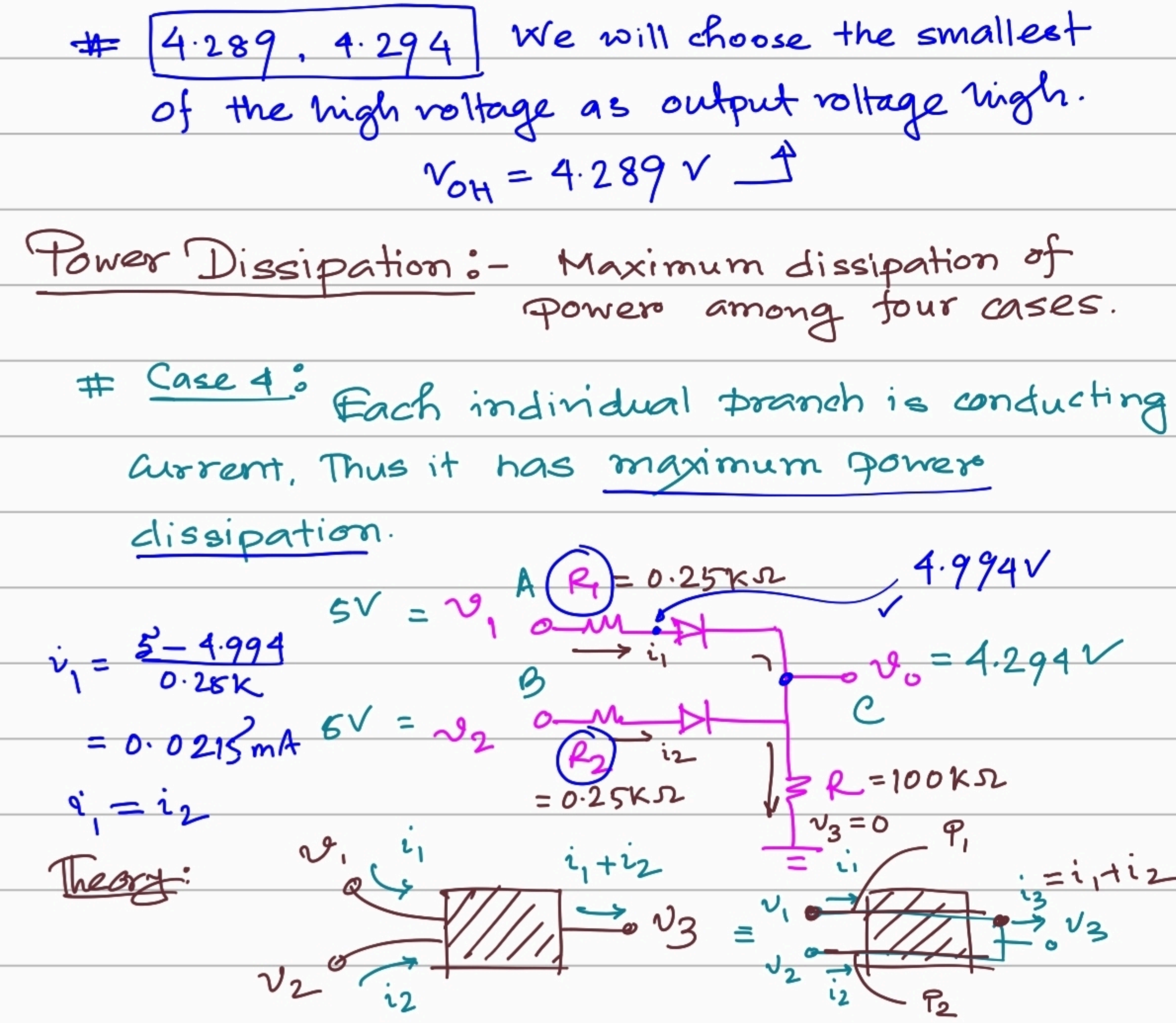
$v_o = 4.2946V$

$\boxed{4.289, 4.294}$ We will choose the smallest of the high voltage as output voltage high.

$$v_{OH} = 4.289\ V$$

Power Dissipation :- Maximum dissipation of power among four cases.

Case 4 : Each individual branch is conducting current, Thus it has **maximum power dissipation.**



$$i_1 = \frac{5 - 4.994}{0.25K} = 0.0215mA$$

$i_1 = i_2$

$$P_1 = (v_1 - v_3)\, i_1 \ , \quad P_2 = (v_2 - v_3)\, i_2$$

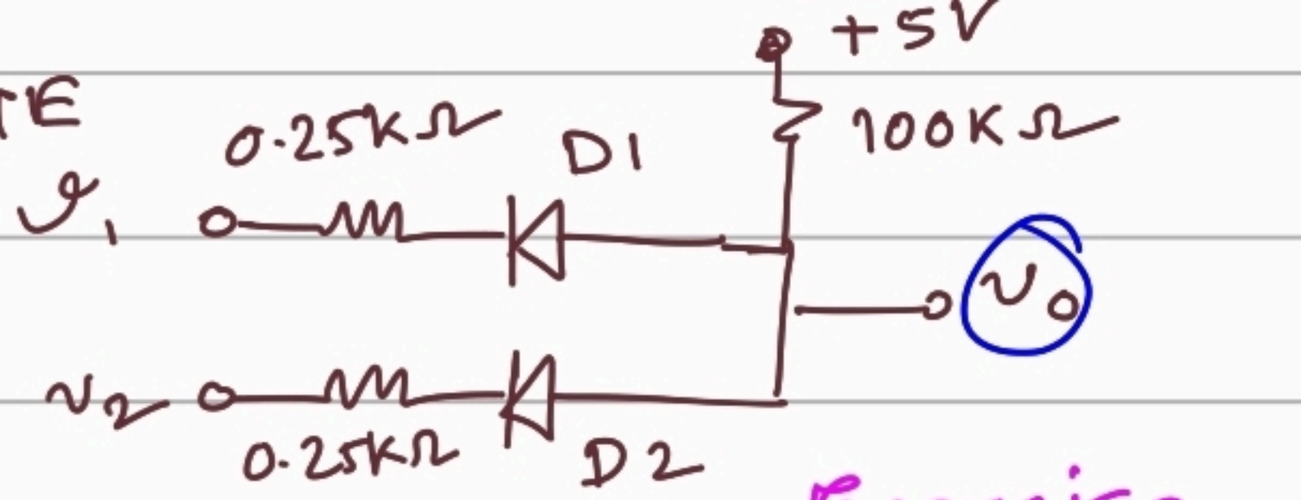
Total power, $P = P_1 + P_2$

$$P_2 = P_1 = (5 - 0)V(0.0215mA) \Rightarrow P = 0.215mW$$

V. $\mu A = \mu W$

AND GATE: 2-AND GATE

V_1	V_2	V_o	D1	D2
5V	5V	5V	OFF	OFF
5V	0V	x	OFF	ON
0V	5V	x	ON	OFF
0V	0V	x	ON	ON



Exercise

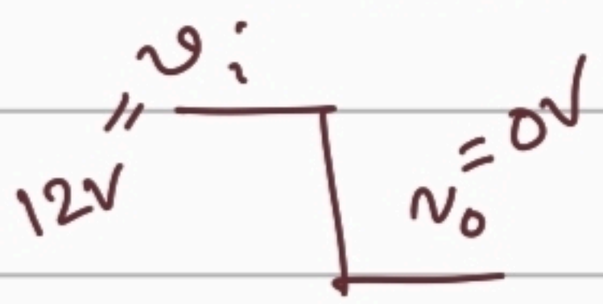
0.68 – 0.7 V

For choosing output logical low, we will take (max) of the logical output low.

$V_{OL} = 0.7V$ ↘ all voltages below this voltage would be considered logical low.

Registor Transistor Logic (RTL)

RTL INVERTER:-

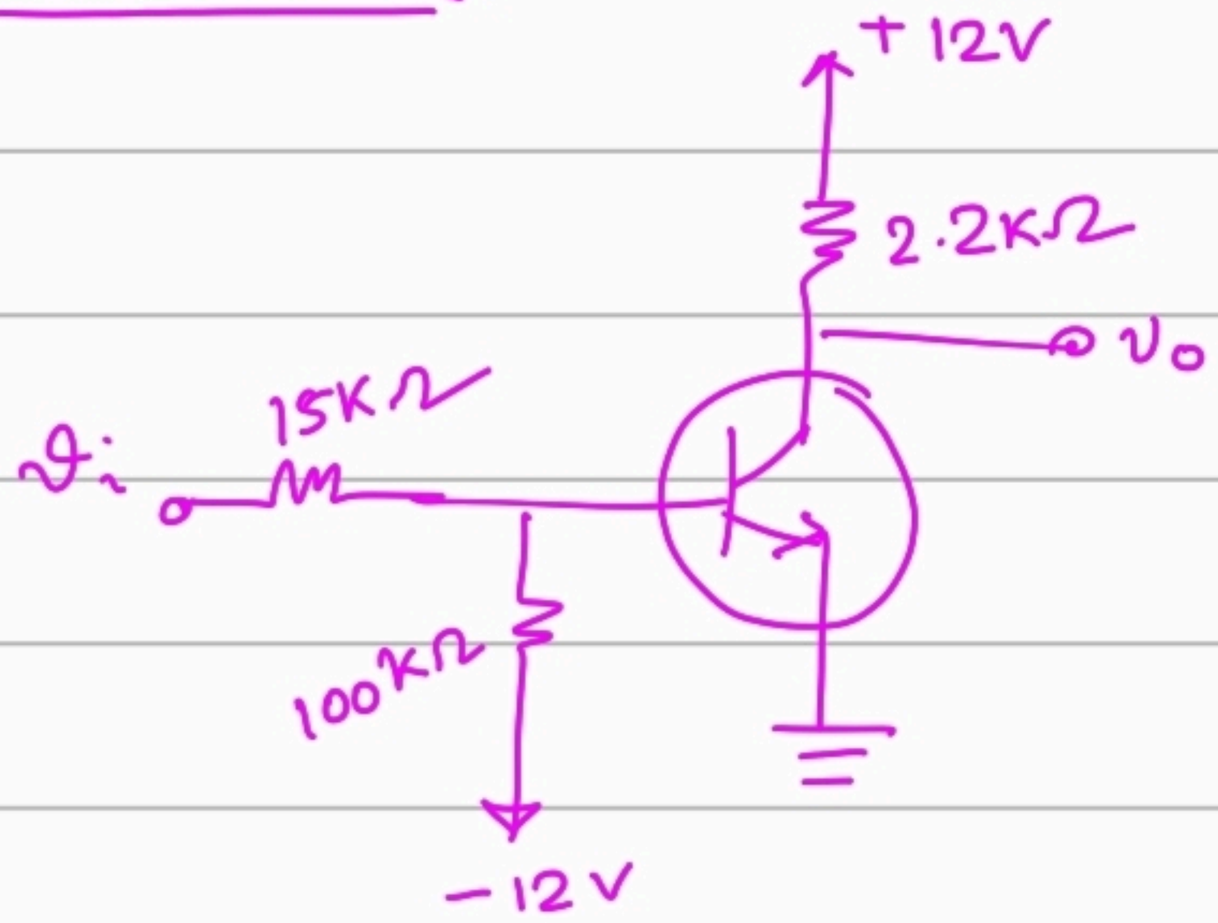


v_i	v_o
1	0
0	1

input logical

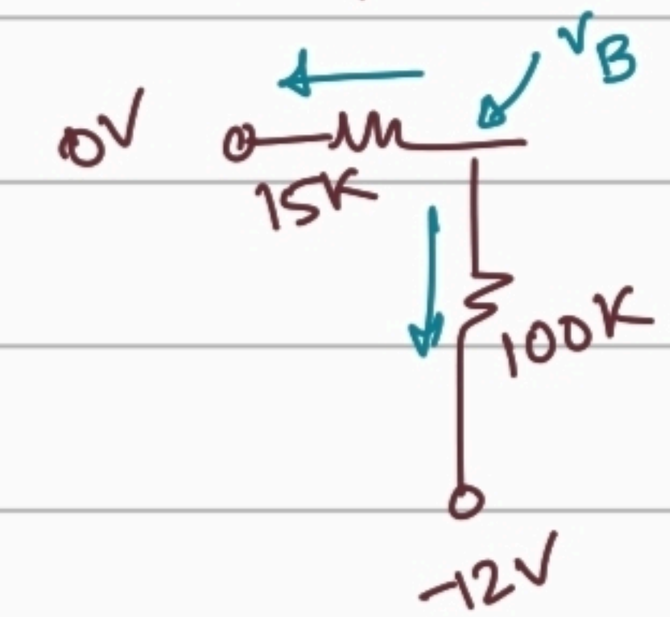
hi = +12V

low = 0V



Case 1 : $v_i = 0V$

Guess/Assumption: T is in cutoff mode. ie $i_B = 0$



$$\frac{V_B-(-12)}{100K} + \frac{V_B-0}{15K} = 0$$

$$\Rightarrow V_B = -1.565V$$

$$V_E = 0V$$