

WILLIAM STALLINGS

CONTENTS

021-5888426 Samar

Web Site for Computer Organization and Architecture, Sixth Edition of Preface av About the Author xxi

PART ONE OVERVIEW 1

CHAPTER 1 Introduction 3

- Organization and Architecture 4
- Structure and Function 5
- Why Study Computer Organization and Architecture? 10
- Outline of the Book 13
- Internet and Web Resources 13

CHAPTER 2 Computer Evolution and Performance 15 -6 0

- A Brief History of Computers 16
- Designing for Performance 37
- 2.3 Pentium and PowerPC Evolution 41
- Recommended Reading and Web Sites 44
- Key Terms, Review Questions, and Problems 45

PART TWO THE COMPUTER SYSTEM 47

CHAPTER 3 A Top-Level View of Computer Function and Interconnection 49

Computer Components 50

Computer Function 53

Interconnection Structures 67

Bus Interconnection 69

PC1 79

Recommended Reading and Web Sites 89 3.6

Key Terms. Review Questions, and Problems 90 3.7 Appendix 3A? Timing Diagrams 92

CHAPTER 4 Cache Memory 95

- Computer Memory System Overview 96
- Cache Memory Principles 103
- 4.3 Elements of Cache Design 106
- Pentium 4 and PowerPC Cache Organizations 121 4.4
- 4.5 Recommended Reading 125
- Key Terms. Review Questions, and Problems 125

Appendix 4A: Performance Characteristics of Two-Level Memories 128

A STATE OF THE PARTY OF THE PAR	
CHAPTER 5 Inte	Semiconductor Main Memory 138 Semiconductor Main Memory 138 Semiconductor Main Memory 138 Semiconductor Main Memory 138 Semiconductor Main Memory 138 Semiconductor Main Memory 138 Semiconductor Main Memory 138
	A STATE OF THE STA
5.1 5.2	Error Correction 148 Error Correction 148 Advanced DRAM Organization 154 Advanced DRAM Organization Web Sites 159 Advanced Problems 160
53	Error Correction 148 Advanced DRAM Organization 154 Advanced DRAM Organization 159 Recommended Reading and Web Sites 159 Recommended Reading and Web Sites 160 Rev Terms, Review Questions, and Problems 160
5.4	Recommended Reading ations, and Protestions
5.5	Advanced DRAM Organization Advanced DRAM Organization Recommended Reading and Web Sites 159 Recommended Reading and Problems 160 Key Terms, Review Questions, and Problems
CHAPTER 6 Exte	mal Memory 163
	A Franchis I link 107
6.1	RAID 174
6.2	Outlant Memory 184
6.3	Magnetic Tape 189
6.4	Magnetic Tape 189 Recommended Reading and Web Sites 191 Recommended Reading and Problems 192 Ver Terms, Review Questions, and Problems
6.5	Magnetic Tape 189 Recommended Reading and Web Sites 191 Recommended Reading and Web Sites 192 Key Terms, Review Questions, and Problems 192
CHAPTER 7 Input	/Output 195
7.1	External Devices 197
7.2	I/O Modules 201
7.3	Programmed I/O 204
7.4	Interrupt-Driven I/O 208
75	Direct Memory Access 216
7.6	VO Channels and Processors 220 InfiniBand 223
	The External Interface: FireWire and Interface
70 1	Recommended Reading and Web Sites 233
7.8	Key Terms, Review Questions, and Problems 233
7.9	key Terms, Review Questions,
	ing System Support 237
ellitaring 8.1 C	Annual Contains Phiagraphics 748
of - 14 8.2 S	cheduling 250
	femory Management 256
0.5 R	entium II and PowerPC Memory Managemen: 360
slicing 8.4 P	entium II and PowerFC Memory Manager
The second secon	ecommended Reading and Web Sites 277
8.6 K	ey Terms, Review Questions, and Problems 278
PART THREE T	HE CENTRAL PROCESSING
AND DESCRIPTION OF THE PARTY OF	NIT 281
CHAPTER 9 Comput	er Arithmetic 283
9.1 Th	e Arithmetic and Logic Unit 284
9.2 Int	eger Representation 285
9.3 Into	eger Arithmetic 291
THE PARTY OF THE P	Per seriamiene 731

Floating-Point Representation 307

Recommended Reading and Web Sites 324

Key Terms, Review Questions, and Problems 325

Floating-Point Arithmetic 313

The Level Stenning at The

9.5

CHAPTER 10 Instruction Sets: Characteristics and Functions 198 CONTENTS AT 10.1 Machine Instruction Characteristics 339 10.2 Types of Operands 337 10.3 Pentium and PowerPC Data Types 339 10.4 Types of Operations 341 10.5 Pentium and PowerPC Operation Types 355 10.6 Assembly Language 364 10.7 Recommended Reading 366 10.8 Key Terms, Review Questions, and Problems 367. Appendix 10A: Stacks 371 Appendix 10B: Little-, Big-, and Bi-Endisa 376 CHAPTER 11 Instruction Sets: Addressing Modes and 11.1 Addressing 382 11.2 Pentium and PowerPC Addressing Modes 389 11.3 Instruction Formats 395 11.4 Pentium and PowerPC Instruction Formats 404 11.5 Recommended Reading 408 11.6 Key Terms, Review Questions, and Problems 409 CHAPTER 12 CPU Structure and Function 411 12.1 Processor Organization 412 12.2 Register Organization 414 12.3 Instruction Cycle 420 12.4 Instruction Pipelining 424 12.5 The Pentium Processor 440 12.6 The PowerPC Processor 450 12.7 Recommended Reading 457 12.8 Key Terms, Review Questions, and Problems 458

CHAPTER 13 Reduced Instruction Set Computers 461

13.1 Instruction Execution Characteristics 463

13.2 The Use of a Large Register File 467

13.3 Compiler-Based Register Optimization 473

13.4 Reduced Instruction Set Architecture 474

13.5 RISC Pipelining 482

13.6 MIPS R4000 486

13.7 SPARC 494

13.8 RISC versus CISC Controversy 500

13.9 Recommended Reading 501

13.10 Key Terms, Review Questions, and Problems 502

CHAPTER 14 Instruction-Level Parallelism and Superscalar Processors 505

- 14.1 Overview 507
- 14.2 Design Issues 511
- 14.3 Pentium 4 520
- 14.4 PowerPC 527
- 14.6 Key Terms, Review Questions, and Problems 536

CHAPTER 15 The IA-64 Architecture 541

- 15.1 Motivation 543
- 15.3 Predication, Speculation, and Software Pipelining 546
- 15.4 IA-64 Instruction Set Architecture 563
- 15.5 Itanium Organization 568
- 15.6 Recommended Reading and Web Sites 569
- 15.7 Key Terms. Review Questions, and Problems 570

PART FOUR THE CONTROL UNIT 573

CHAPTER 16 Control Unit Operation 575

- 16.1 Micro-Operations 577
- 16.2 Control of the Processor 583
- 16.3 Hardwired Implementation 594
- 16.4 Recommended Reading 597
- 16.5 Key Terms, Review Questions, and Problems 597

CHAPTER 17 Microprogrammed Control 599

- 17.1 Basic Concepts 600
- 17.2 Microinstruction Sequencing 609
- 17.3 Microinstruction Execution 615
- 17.4 TI 8800 627
- 17.5 Applications of Microprogramming 637
- 17.6 Recommended Reading 638
- 17.7 Key Terms, Review Questions, and Problems 639

PART FIVE PARALLEL ORGANIZATION 641

CHAPTER 18 Parallel Processing 643

- 18.1 Multiple Processor Organizations 645
- 18.2 Symmetric Multiprocessors 647.
- 18.3 Cache Coherence and the MESI Protocol 656
- 18.4 Clusters 663
- 18.5 Nonuniform Memory Access 670
- 18.6 Vector Computation 674
- 18.7 Recommended Reading 687
- 18.8 Key Terms, Review Questions, and Problems 688

APPENDICES

APPENDEX A Digital Logic 693

A.1 Boolean Algebra 694

A.Z. Gates 696

A.3 Combinational Circuits 699

A.4 Sequential Circuits 720

A.5 Problems 730

APPENDIX B Number Systems 733

8.1 The Decimal System 734

B.2 The Binary System 734

B.3 Converting between Binary and Decimal 735

B.4 Hexadecimal Notation 738

B.5 Problems 739

APPENDIX C Projects for Teaching Computer Organization and Architecture 741

C.1 Research Projects 742

C.2 Simulation Projects 742

C.3 Reading/Report Assignments 743

GLOSSARY 745

REFERENCES 757

INDEX 773