Ghulam Ishaq Khan Institute of Engineering Sciences and Technology

Faculty of Computer Science and Engineering

FINAL YEAR PROJECT REGISTRATION FORM

Group Members

In the case of 4th Member, you need prior approval from FYP Coordinator.

S#	Reg. No.	Name	Program (BCE/BCS/BAI)	Signature
1	2020414	Saad Khan	BCE	SaadKhan
2	2020487	Syed Zaeem Shakir	BCE	ZaeemShakir
3	2020217	Mahnoor Maleeka	BCE	MahnoorMaleeka

Project Title:
Intellera: A Hardware Based Acceleration of Matrix MAC Processor.

In this project, we aim to design and implement a RISC-V based processor on an FPGA with hardware accelerators for efficient matrix manipulation. The processor will feature a custom instruction set architecture (ISA) optimized for matrix operations such as multiplication and addition. Additionally, pipelining techniques will be employed to improve processor performance and speed.

The design will be implemented on a Field Programmable Gate Array (FPGA), which provides a flexible and cost-effective solution for hardware prototyping. The hardware accelerators will be designed to offload the heavy computation required for matrix manipulation from the processor, thereby improving performance and power efficiency.

We plan to conduct a thorough evaluation of the processor's performance by implementing several benchmarking tests, including matrix multiplication, addition, and subtraction. We will also evaluate the power consumption of the processor and compare it with other existing processors. The possibility of incorporating the developed processor towards a full SoC would also be evaluated at the later stages of the project.

Work Plan

Term I (7th semester)	Term II (8th semester)
Getting the full functionality right in software including a baseline HW implementation	Getting the final design implemented and optimized on the HW along with a feasibility analysis of extending the design towards a full SoC development.

S#	SDG	Mapped (Yes/No)
1	No poverty	NO
2	Zero hunger	NO
3	Good health/wellbeing	NO
4	Quality education	NO
5	Gender equality	NO
6	Clean water and sanitation	NO
7	Affordable and clean energy	NO
8	Decent work and economic growth	NO
9	Industry, innovation, and infrastructure	YES
10	Reduced Inequalities	NO
11	Sustainable Cities and Communities	NO
12	Responsible consumption and production	NO
13	Climate action	NO
14	Life below water	NO
15	Life on land	NO
16	Peace, Justice, and strong institutions	NO
17	Partnerships for the goals	NO

Supervisor Name: ___Dr Fahad Bin Muslim_____ Signature: 

Co-Supervisor Name: _____Dr Taj Muhammad_____ Signature: _____

Dean's Signature: _____ Date: _____

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FINAL YEAR PROJECT AS A COMPLEX ENGINEERING/COMPUTING PROBLEM

It is to certify here that the final year design project (FYDP) entitled,

"Hardware Based Acceleration of Matrix MAC ……" is categorized as a complex engineering/computing problem (CEP) based on the preamble (in-depth engineering knowledge) and involvement of the following attributes.

Attribute	**Involves Attribute (Yes/No)**
Involves wide-ranging or conflicting technical, computing/engineering and other issues.	YES
Have no obvious solution and require abstract thinking and originality in analysis to formulate suitable models	YES
Involve infrequently encountered issues.	YES
Outside problems encompassed by standards and codes of practice for professional engineering.	YES
Involve diverse groups of stakeholders with widely varying needs.	YES
High level problems including many component parts or sub-problems.	YES

Supervisor Name: Dr Faha Bin Muslim Signature: _____

Co-Supervisor Name: Dr Taj Muhammad Signature: _____