**Deliverables:**  
  
1) A detailed design specification document outlining the architecture, instruction set, and hardware accelerators of the matrix MAC processor.

2) A functional simulation of the processor in a hardware description language such as Verilog or VHDL.

3) A working Verilog RTL code for the matrix MAC processor, along with simulation and verification results.(Tentative)

4) An FPGA implementation of the matrix MAC processor for testing and validation.

5) A pipelined implementation of the processor to optimize its performance (Tentative).

6) A library of optimized matrix manipulation routines that can be run on the processor (Tentative).

8)A presentation of the project and its results to a technical audience.