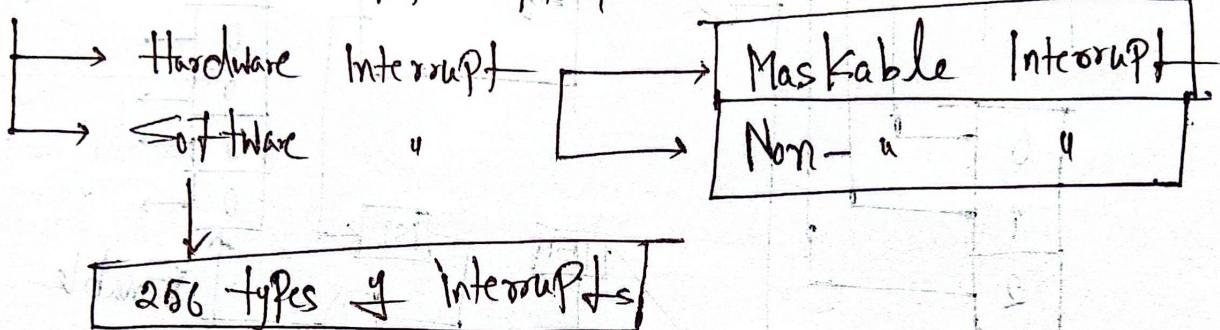


Segment - 4

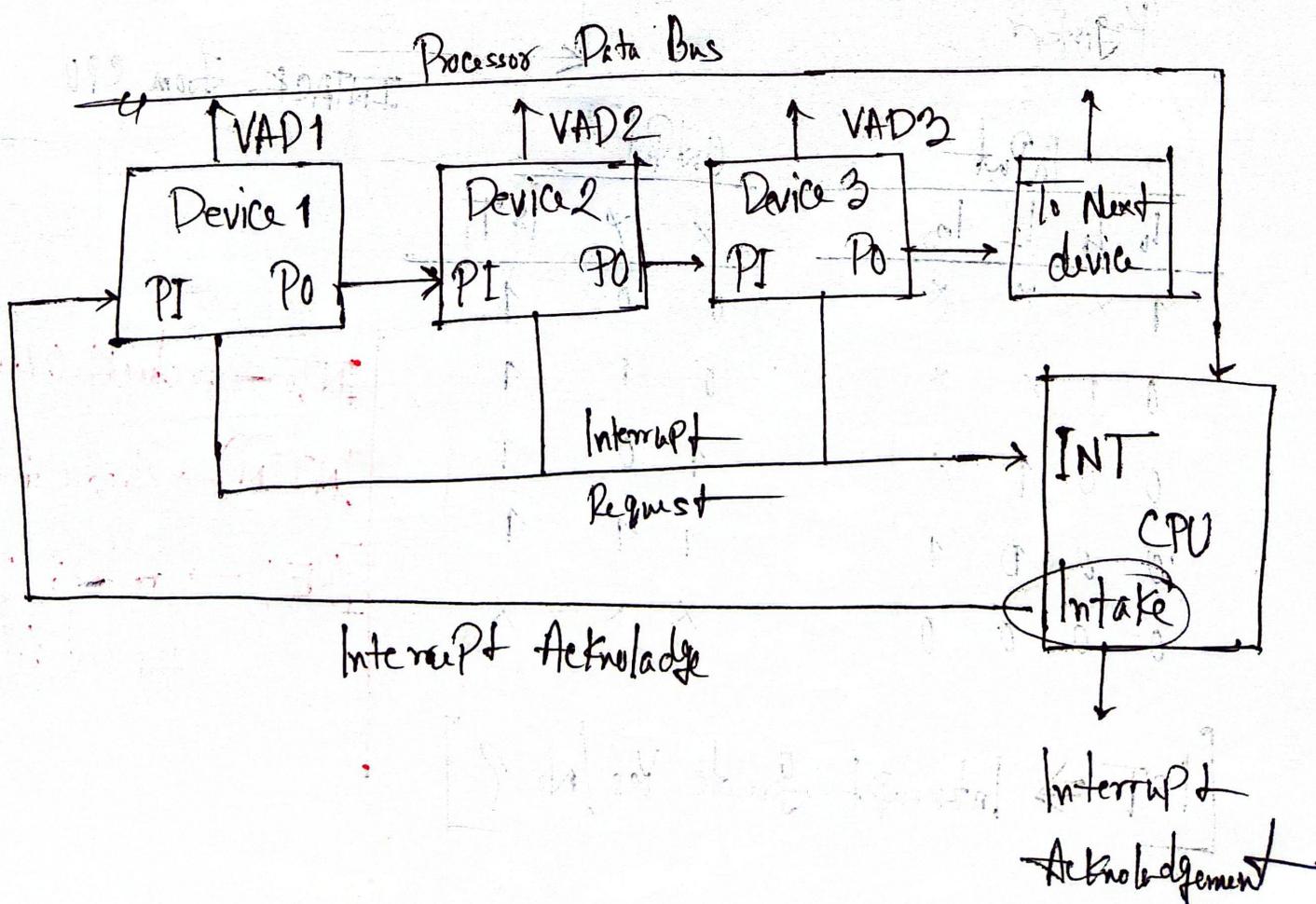
Interrupt System

⇒ Interrupt system is a method of creating a temporary halt during program execution & allow peripheral device to access the MP Unit.

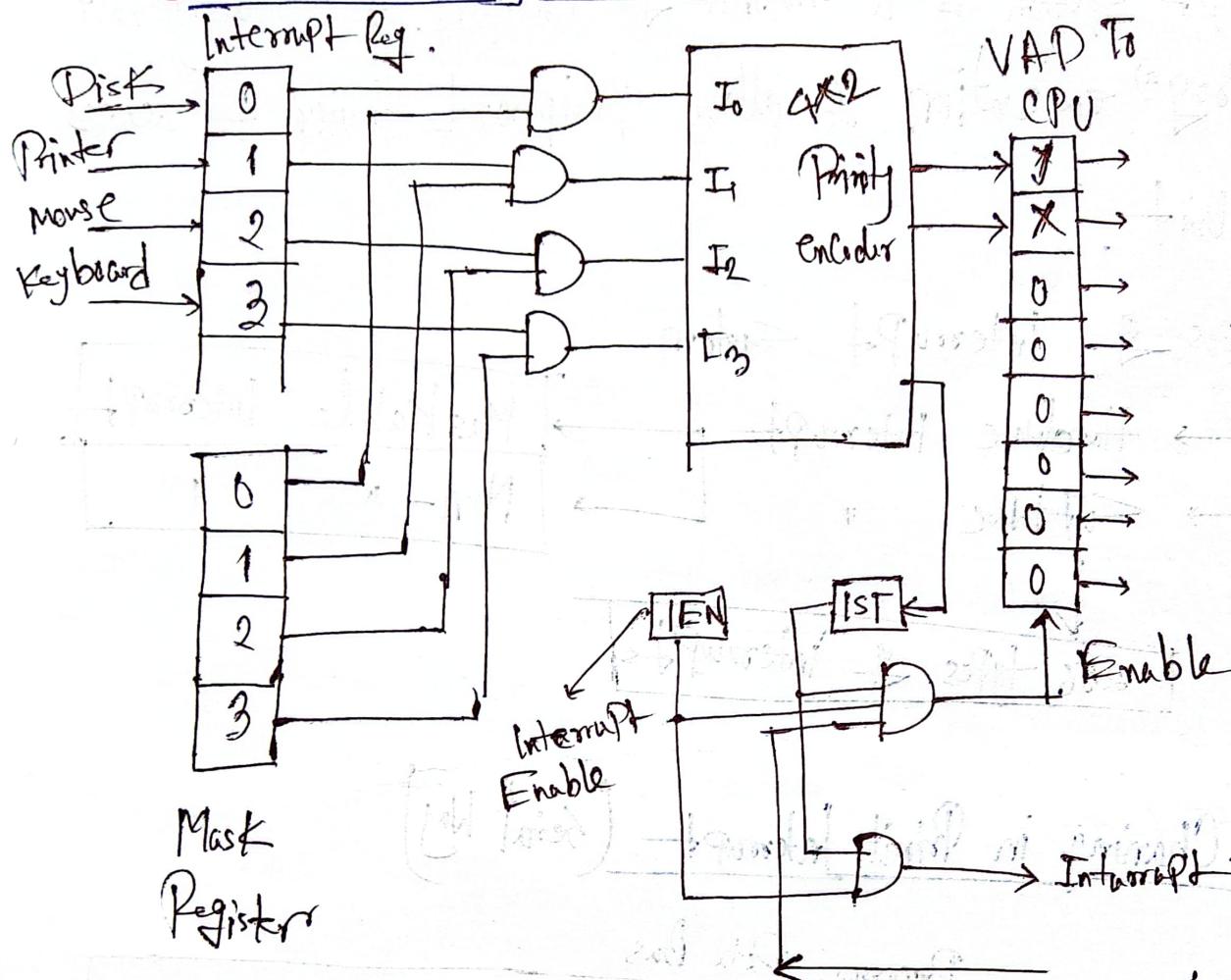
⇒ 2 Types of Interrupt System



Daisy Chaining in Priority Interrupt (Serial Way)



* Parallel Priority Interrupt



Input				Output		
I ₀	I ₁	I ₂	I ₃	X	Y	IST
1	x	x	x	0	0	1
0	1	x	x	0	1	1
0	0	1	x	1	0	1
0	0	0	1	1	1	1
0	0	0	0	x	x	x

INT_O → To check Overflow
 INT(N) → Vector Addr.
 IRET → Return of both Hw and Sw.

[IST → Interrupt Generate Yes / No ?]

NMI → Non Maskable Interrupt [Cannot be ignored]

INTR → Interrupt Request [blocks running execution]

8086 Interrupt Vector Table

256 Interrupts Vector

[0-4] → dedicated

[5-31] → reserved for system use

[32-255] → reserved for users

	Errors / Overflows
00000H	
004FH	Single Steps
008FH	Non-Maskable/NMI
00CFFH	Break Point
010FH	Overflow
014FH	Type-5
017CH	Type-31
0180FH	Type-32
003FFH	Type-255

Dedicated

function

System

Reserved

User
Reserved

00000H

003FFH

Function 9 Int. Vector Table

→ predefined

→ Fetch

→ Int. Acknowledge

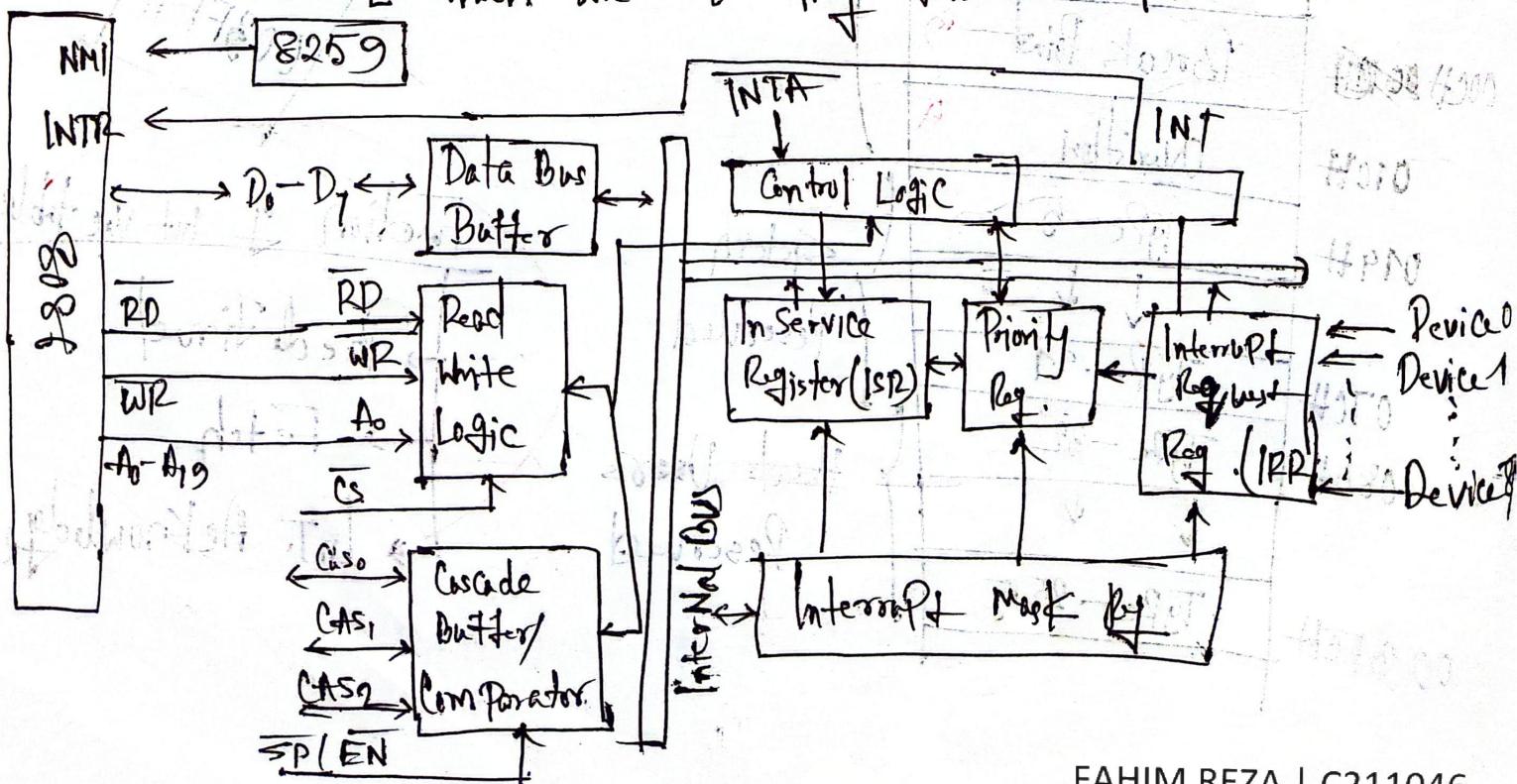
'PIC - 8259'

Programmable Interrupt Controller

Control Logic: It is the Centre of 8259 and Controls the functioning of every block. It has Pin INTR which is connected with other microprocessors for taking interrupt request and Pin INT for giving the output.

Interrupt Mask Register: It stores the interrupt level which have to be masked by storing the masking bits of the interrupt level. [8 bit]

Interrupt request register [IRR]: It stores all the interrupt level which are requested for interrupt service.



Segment - i

80186 → 16 bit MP

→ 16-bit data bus

→ 20-bit address bus

→ Divides into 7 independent functional Part.

- ① → The Bus Interface Unit (BIU)
- ② → Execution Unit (EU)
- ③ → Clock Generator
- ④ → Programmable Interrupt Controller
- ⑤ → Programmable Chip Select Unit (CSU)
- ⑥ → Programmable DMA Unit
- ⑦ → Counter/Timers

80186 → Has 68-Pin

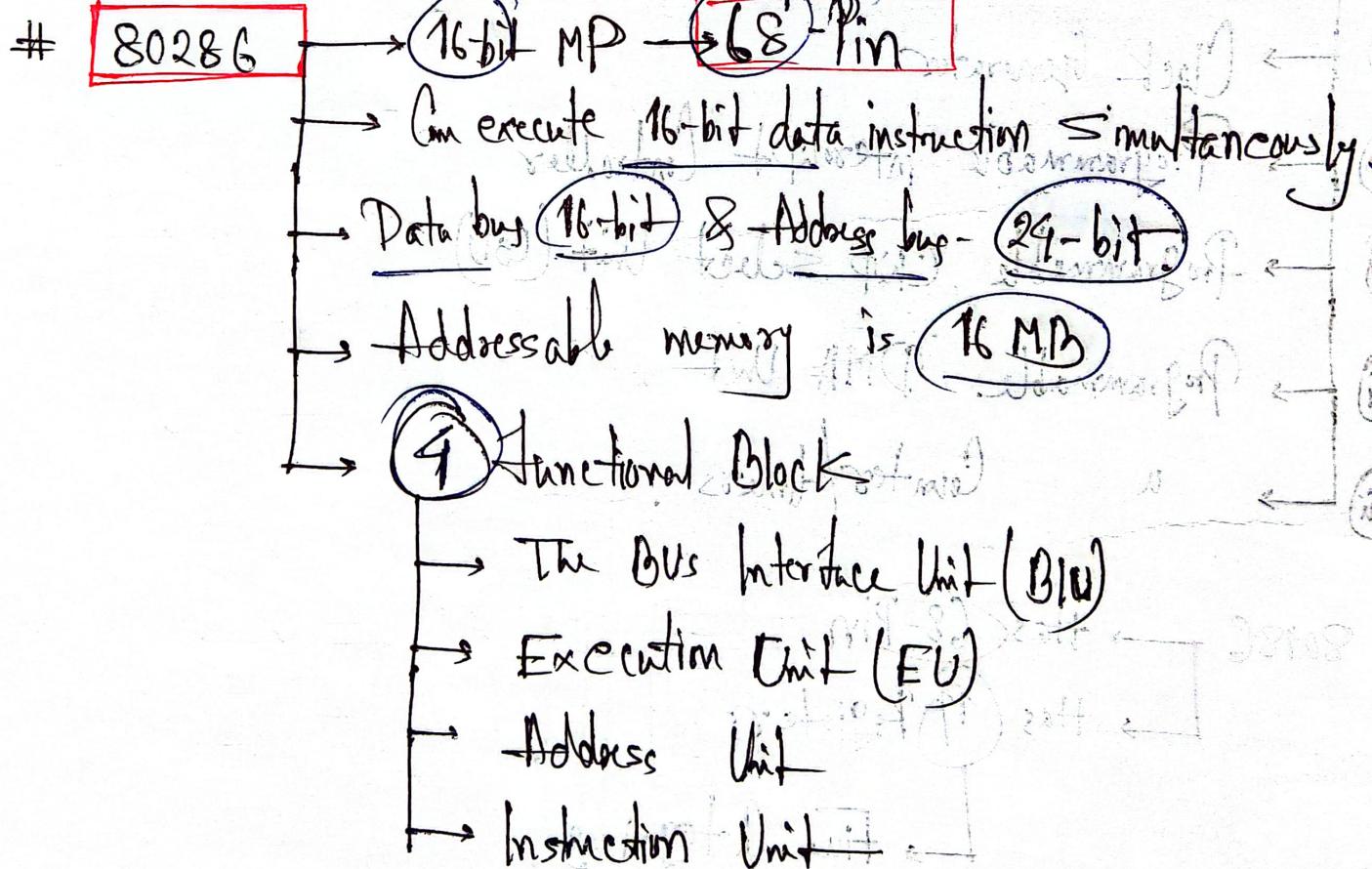
→ Has 19 Registers

→ Five Categories

- Segment Segment Reg.
- Base and Index Reg.
- Status and Control Reg
- Status Word

Code Segment (CS) {
 Stack u (SS) } is a 16-bit register
 Data u (DS) }

Count → CL & CH
 Accumulator → Consist of 2 8-bit registers → AL & AH
 Base → BL & BH



(1) Register grouped into (2) Categories

Features of 80286

- i → 16 bit address bus can address 16 Mbytes of Physical memory.
- ii → Two operation mode
 - Real address mode
 - Virtual mode
- iii → includes the instruction of 8086 and 80186 with some extra instruction to support OS.
- iv → Performance is 5 times better than 8086.

Intel 80386

- 32 bit MP → 32 bit operation in one cycle
- Data and Address bus 32-bit
- Memory address 4GB / 2³² bytes Physical memory
- Multitasking and Protection Capability are two key characteristics of 80386
- Has internal dedicated hardware that permits multitasking.

6 Functional Unit

- Bus Interface Unit (BIU)
- Code Fetch Unit
- Instruction Decode Unit
- Execution Unit (EU)
- Memory Management Unit
- Segmentation Unit

80386 has → **132-Pin**

Intel **80986**

- 32-bit MP
 - Fourth Generation of binary Compatible
 - **Functional Unit**
 - Bus Interface Unit (BIU)
 - Execution Unit (EU)
 - Floating Point Unit.
- **168-Pin PGA (Pin Grid Array)**

④ Features of 80986 from **Slice** *

Pentium MP

- 32-bit
- Year 1993, 3.1 million transistors.
- (32-bit) data bus & (32-bit) address bus
- 4-6B Physical memory.

* # Features of Pentium MP

* # MicroProcessor: A MP is a digital electronic Component with transistors integrated into a small semiconductor IC that consumes less Power.

Embedded MP

- 5 functional Units
- ALU
- Memory Unit
- Control Unit
- Register
- System Bus

* # Types of MP

- Complex instruction set MP
- Reduced instruction set MP
- Superscalar MP
- Digital Signal MP
- Application-specific integrated Circuit (ASIC)

* # Merced MP

- First Itanium microarchitecture designed by Intel.
- 5 Functional Unit

- Pipeline
- Frontend
- Fetch
- Branch Predictor
- Execution Engine

Intel MicroProcessor

80186

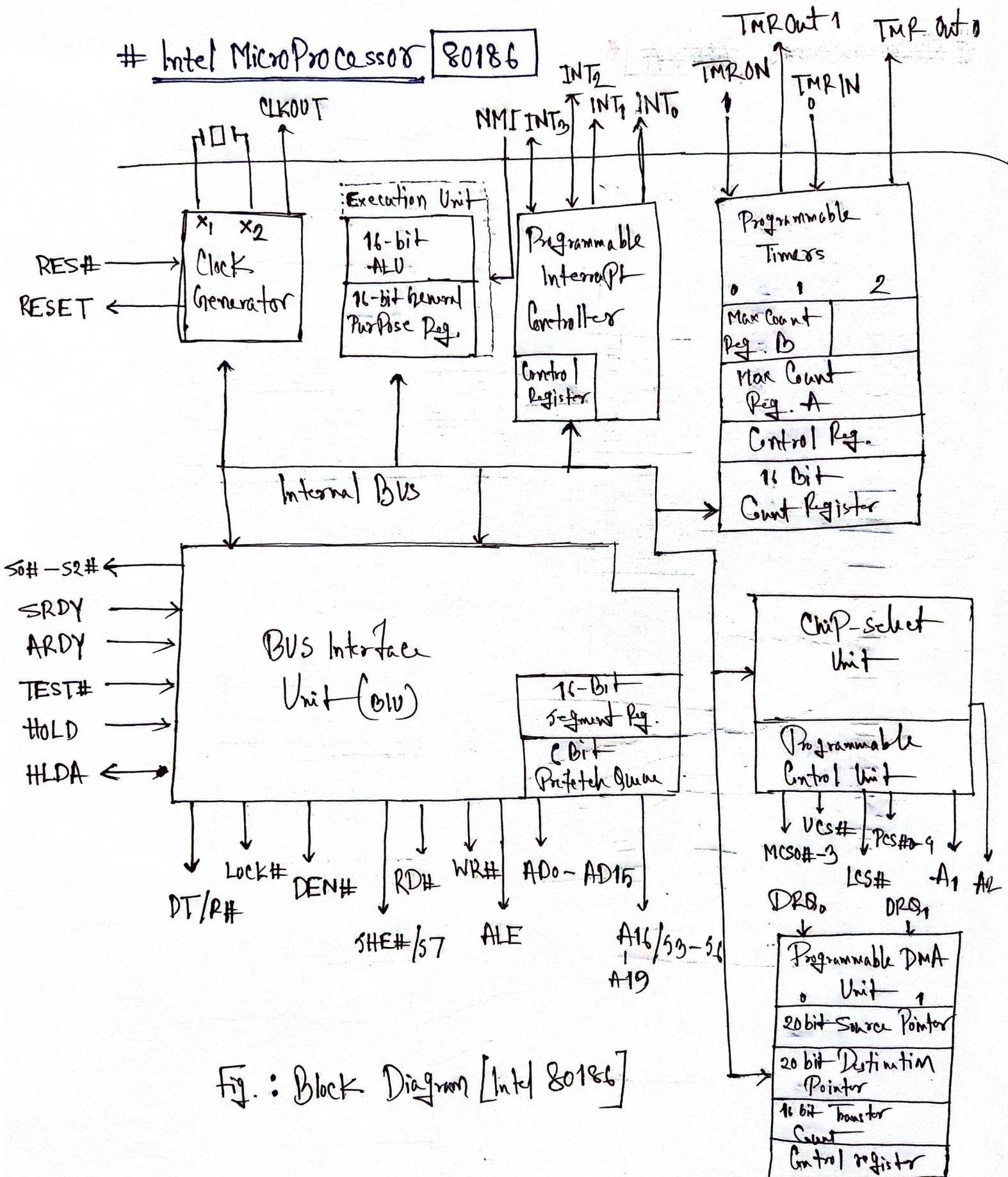
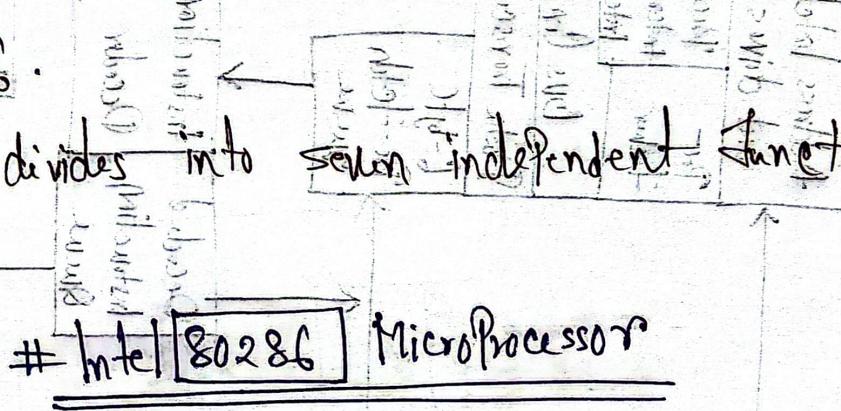


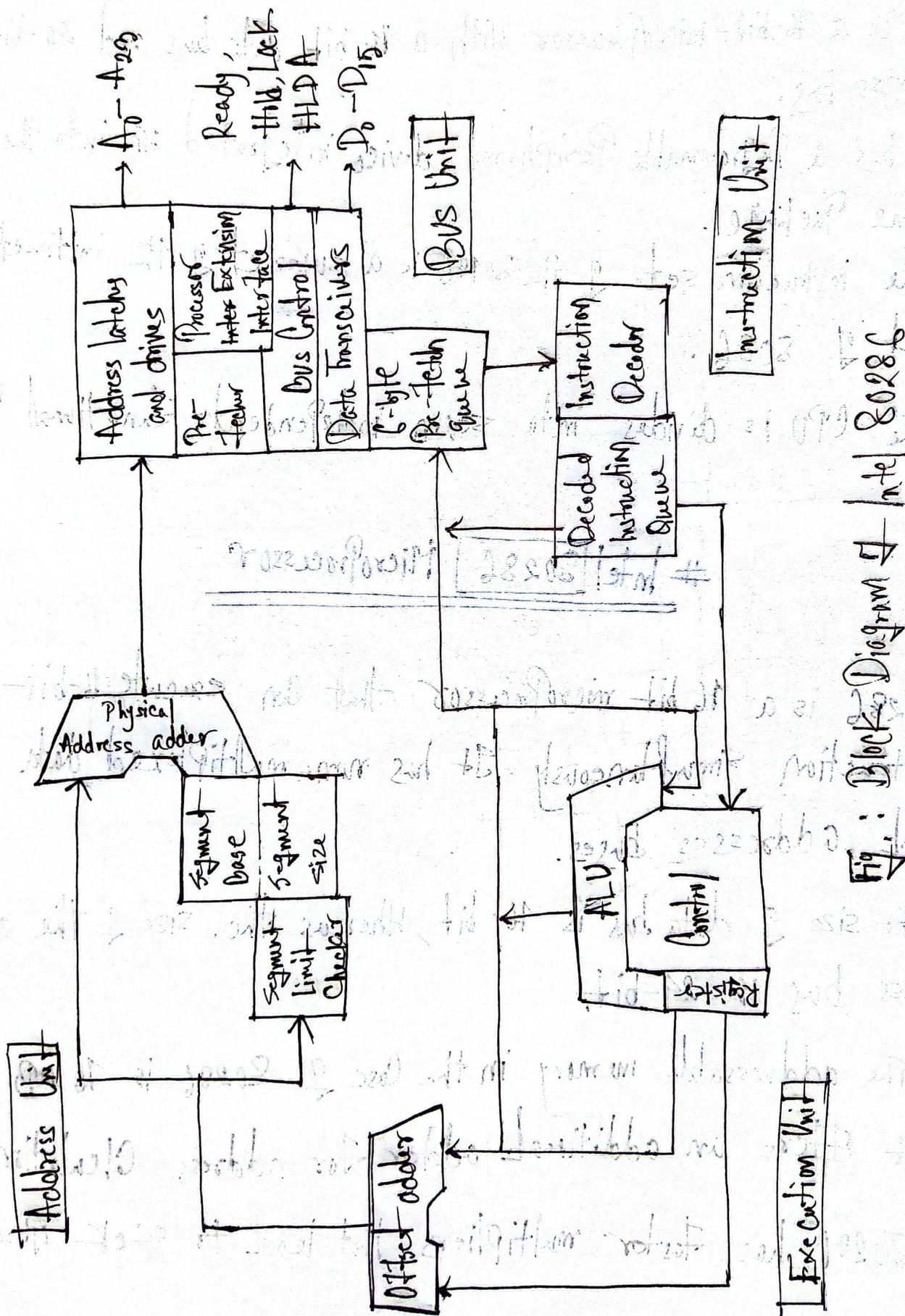
Fig. : Block Diagram [Intel 80186]

Intel 80186

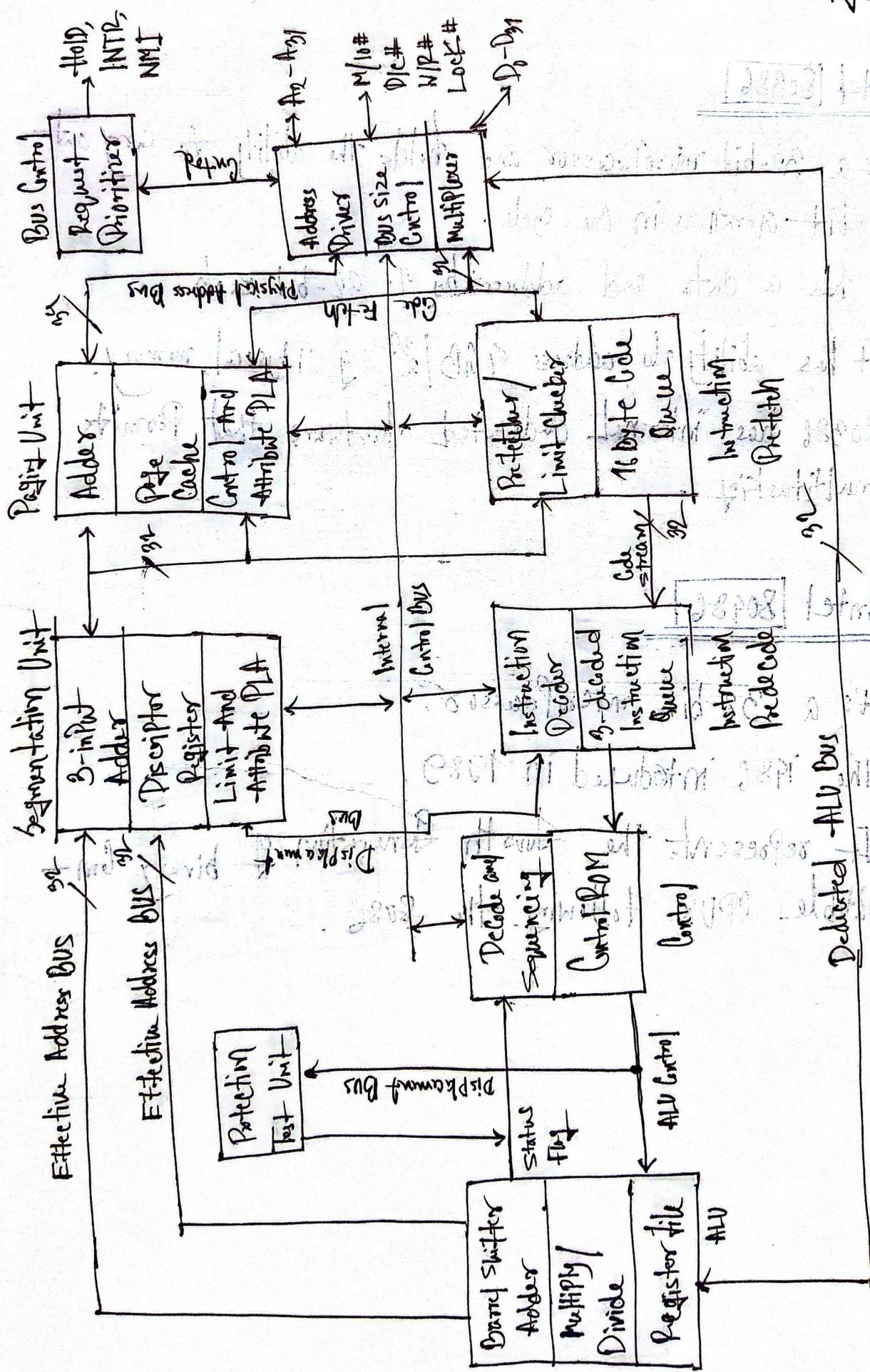
- It is a 16-bit microProcessor with a 16-bit data bus and 20-bit address bus.
- It has a Programmable Peripheral device integrated into the same package.
- The instruction set of the 80186 is a superset of the instruction set of 8086.
- The CPU is divided into seven independent functional Part.



- 80286 is a 16 bit microProcessor that can execute 16-bit instruction simultaneously. It has non-multiplexed data and addresses buses.
- The size of data bus is 16-bit, whereas the size of the address bus is 20-bit.
- The addressable memory in the case of 80286 is 16 MB.
- It offers an additional adder for address Calculation.
- 80286 has fast multipliers that lead to quick operation.



Intel 80386 MicroProcessor



Page - 09

Fig : Block Diagram of Intel 80386

Intel **80386**

- It's a 32-bit microProcessor and holds the ability to perform 32-bit operations in one cycle.
- It has a data and address bus of 32-bit each.
- It has ability to address $4 \text{ GB} / 2^{32}$ of Physical memory.
- 80386 has internal dedicated hardware that permits multitasking.

Intel **80486**

- It's a 32-bit microProcessor.
- The 1986 introduced in 1989.
- It represents the Fourth Generation of binary CPU's.
- Following the 8086.

Intel 80486 DX2 Architecture

32-bit Data Bus
64-bit Internal
Transistor Bus

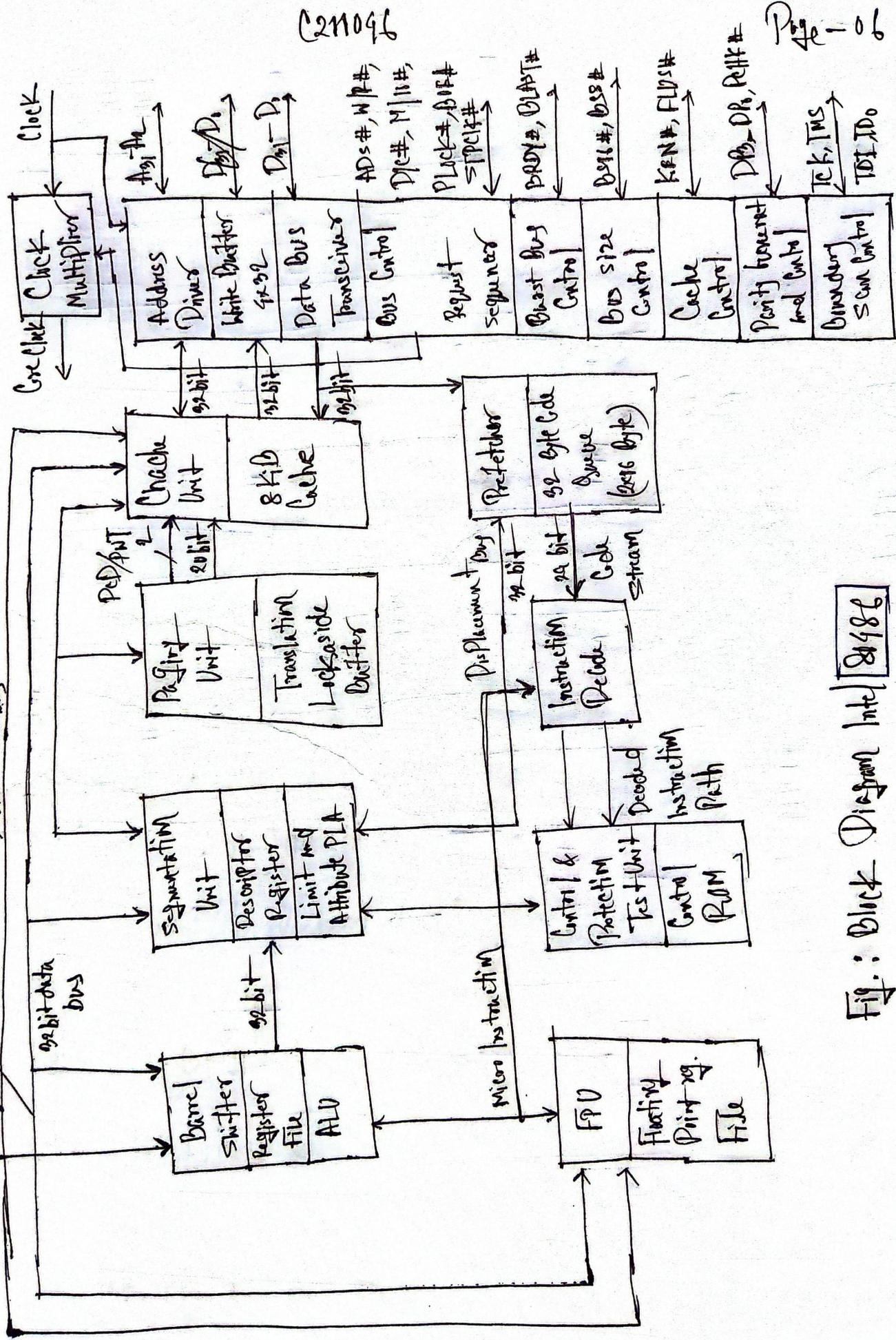
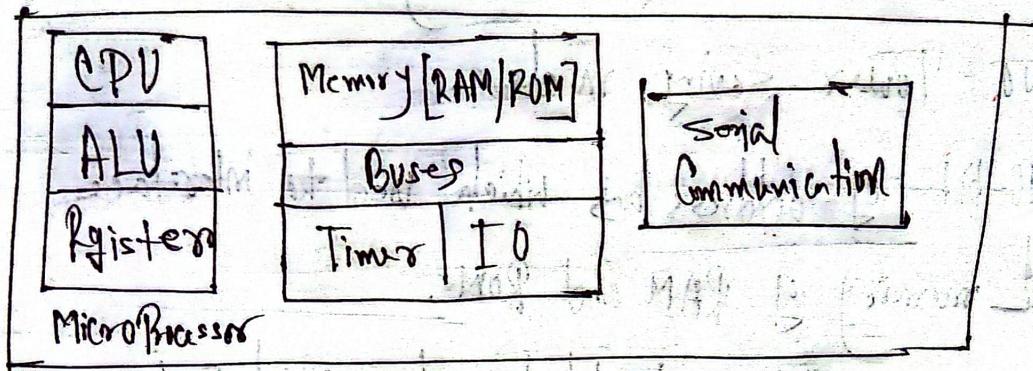


Fig. : Block Diagram Intel 80486

Segment - 7

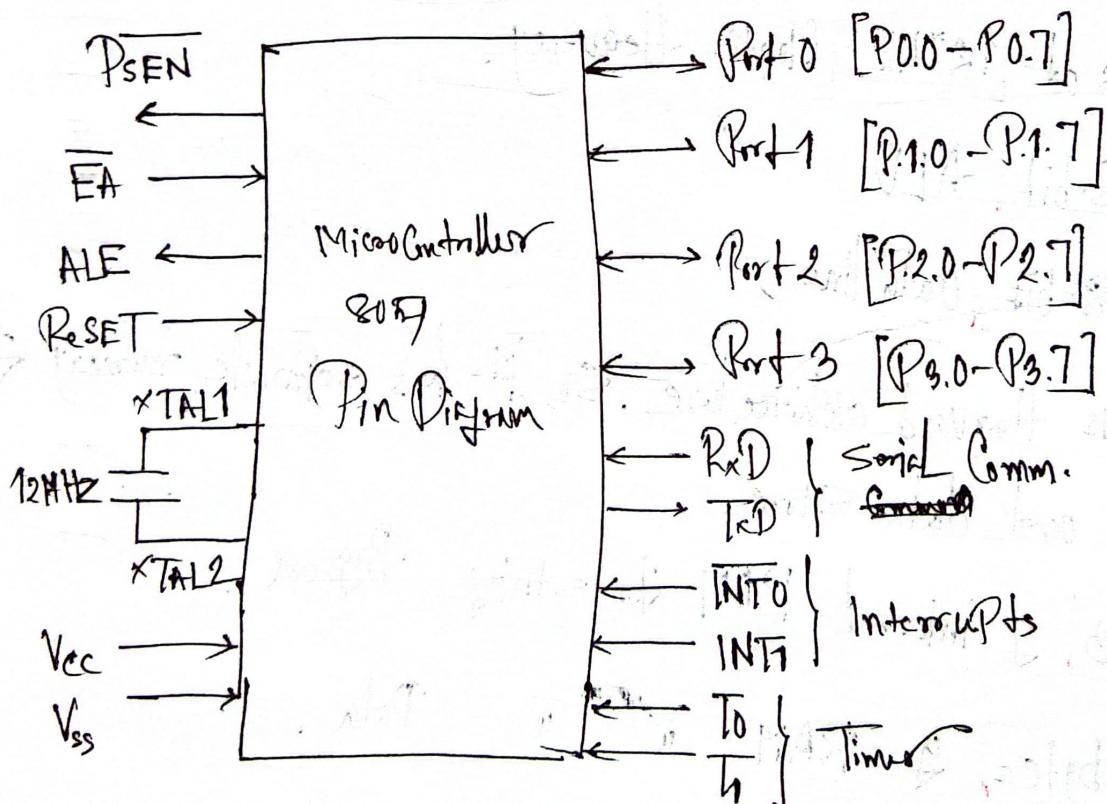
MicroController 8051



- ① 8051 is a Complete built on one Chip. It has CPU, ALU, Register, RAM, ROM, Serial/Parallel Port, Interrupt, Timer on Single Chip.
- ② Operates at 12 MHz Clock Frequency.
- ③ Has 8-bit ALU.
- ④ Has 8-bit data line.
- ⑤ Follows Harvard architecture. So, it has separate memory for Program and data store.
- ⑥ 4KB of internal ROM for storing Program.
- ⑦ 128 bytes of RAM, u u Data.
- ⑧ Has Four 8-bit of I/O Ports. Used to interface from Peripherals like Keyboard, Mouse, display, LEDs, switches etc.

9. Has Two 16-bit 'UP' timer.
10. Has 5 interrupt operating at Priority level.
11. Has TWO Power saving mode.
12. Has 16-bit of address bus which used to interface external memory of RAM and ROM.
13. 8051 is efficient embedded system which save Cost, Power and makes circuit compact.

Pin Diagram of 8051



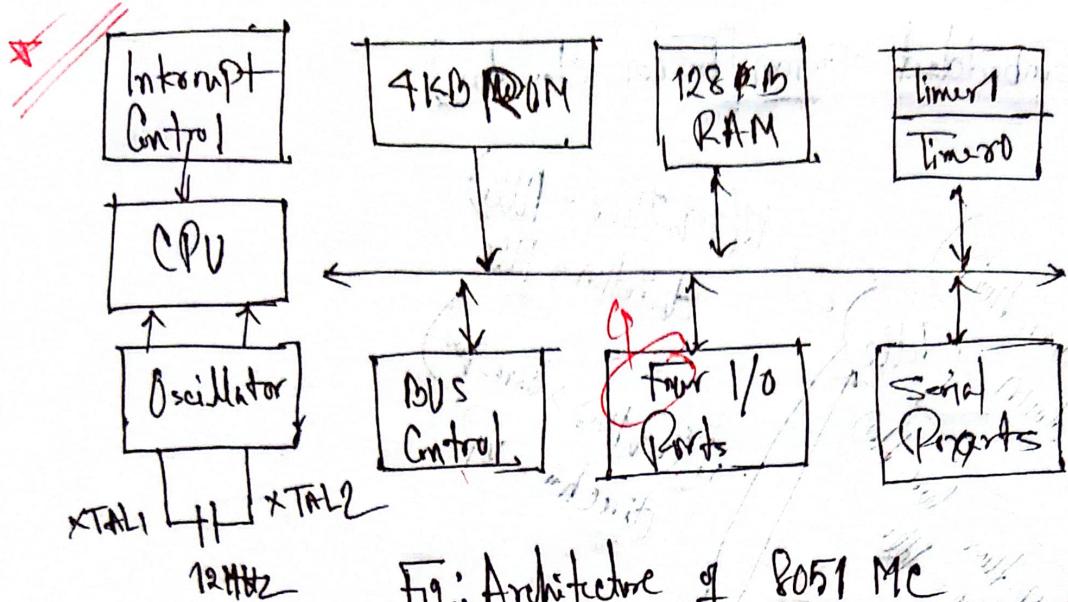
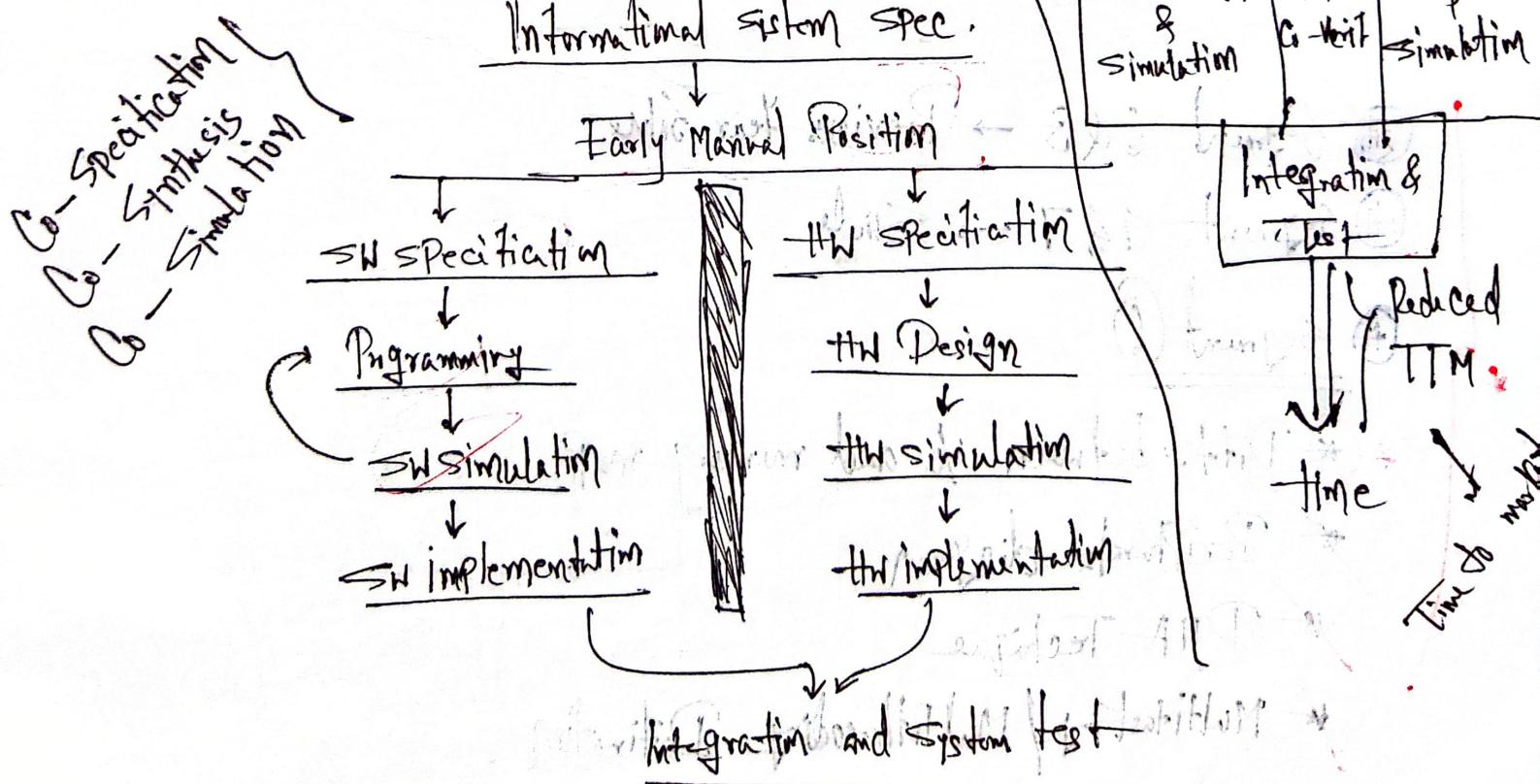


Fig.: Architecture of 8051 MC

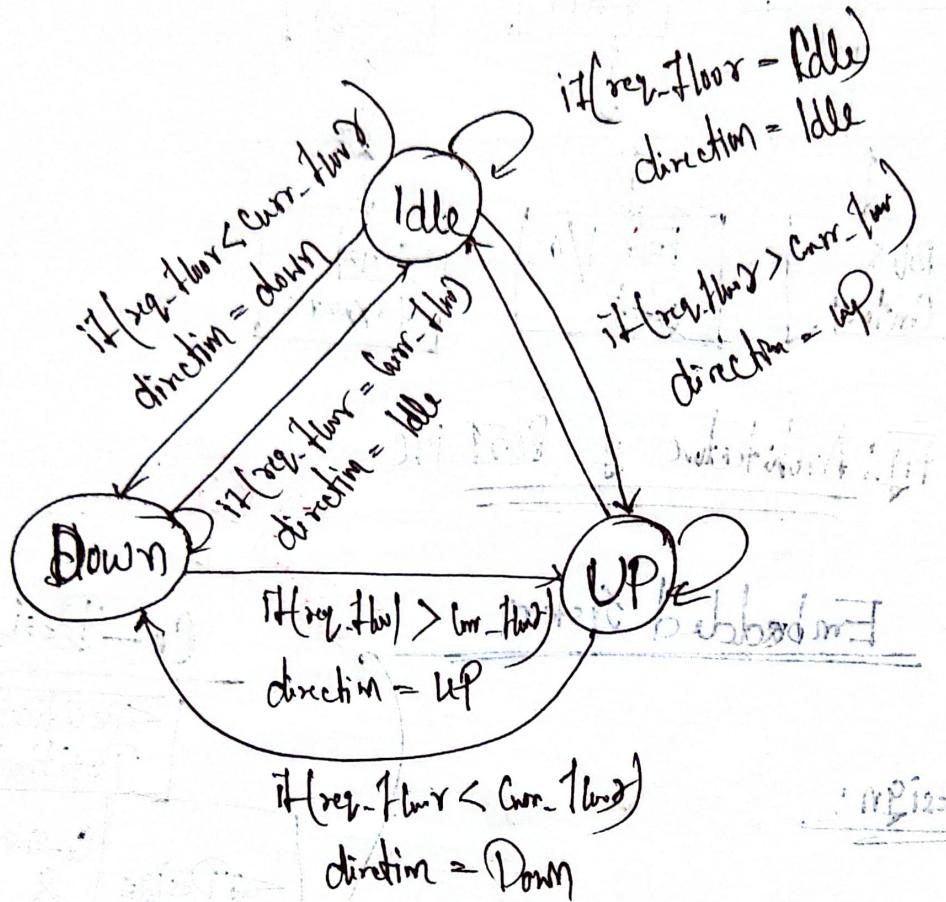
Embedded System

Co-Design

Traditional Design:



Modeling of Embedded System [For an elevator]



~~④ Segment 6 & 8 → Previous Year Solved~~

~~⑤ Segment 9 & 10 → Solved~~

~~⑥ Segment 11~~

~~* * Diff. between 1/6 and memory map.~~

~~* Peripherals diagram~~

~~* DMA Technique~~

~~* Multitasking / Multithreading Definition~~

Micro Processor 8255A

⇒ Programmable I/O device designed to transfer the data from Yo to interrupt Yo under certain condition

Has 3 Port

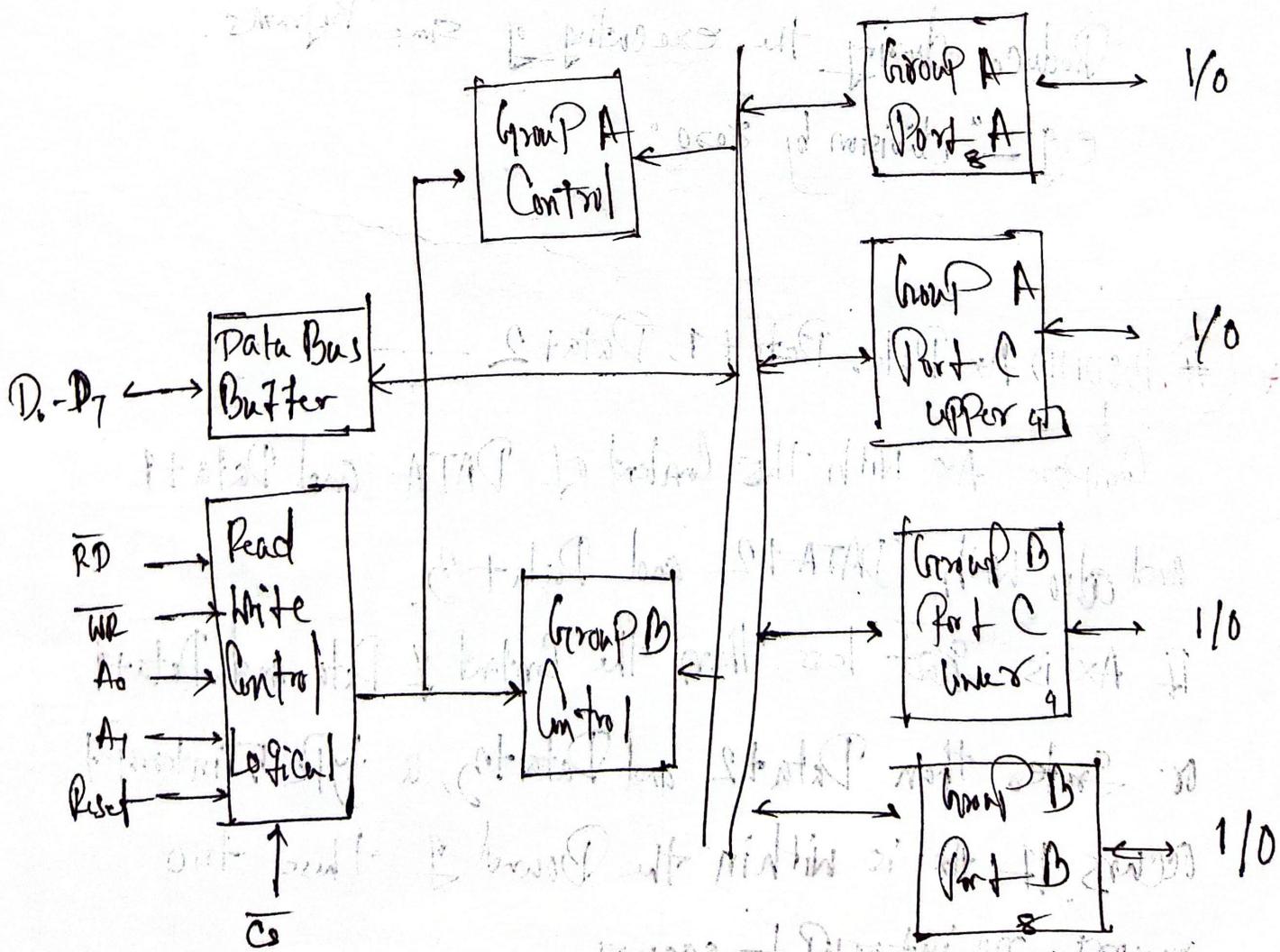
→ Port A → Has 8 bit Input and 8 bit Output buffer

→ Port B → Same as Port A

→ Port C → Split in two Part

→ Higher Port

→ Lower Port



* # Types of Interrupts

i) Hardware Interrupt

- i) Maskable — Can be delayed e.g. — Key Press on keyboard.
- ii) Non-Maskable — Can't be delayed e.g. — Power failure.

ii) Software interrupts : [2 types] interrupt

- i) Normal interrupt — Caused by SW instruction
- ii) Exception — Unplanned interrupt that's produced during the executing of some programs.
e.g. — division by zero.

* # BOUND Ax, Data, Data+1, Data+2

Compare Ax with the content of DATA and Data+1

and also with DATA+2 and Data+3.

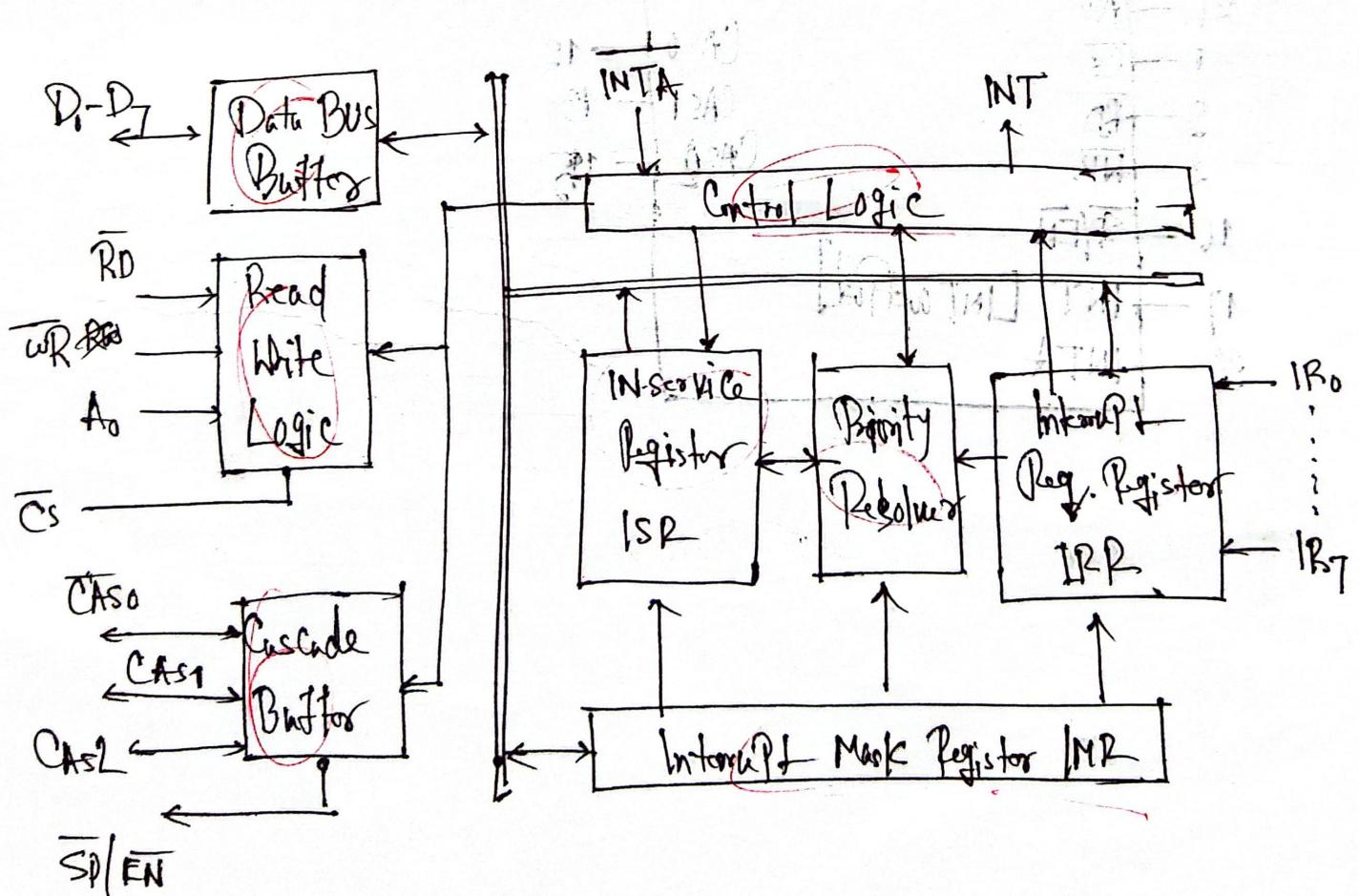
If Ax is less than the content of Data and Data+1

or greater than Data+2 and Data+3, a types interrupt occurs. If Ax is within the Bound of these two memory, no interrupt occurs.

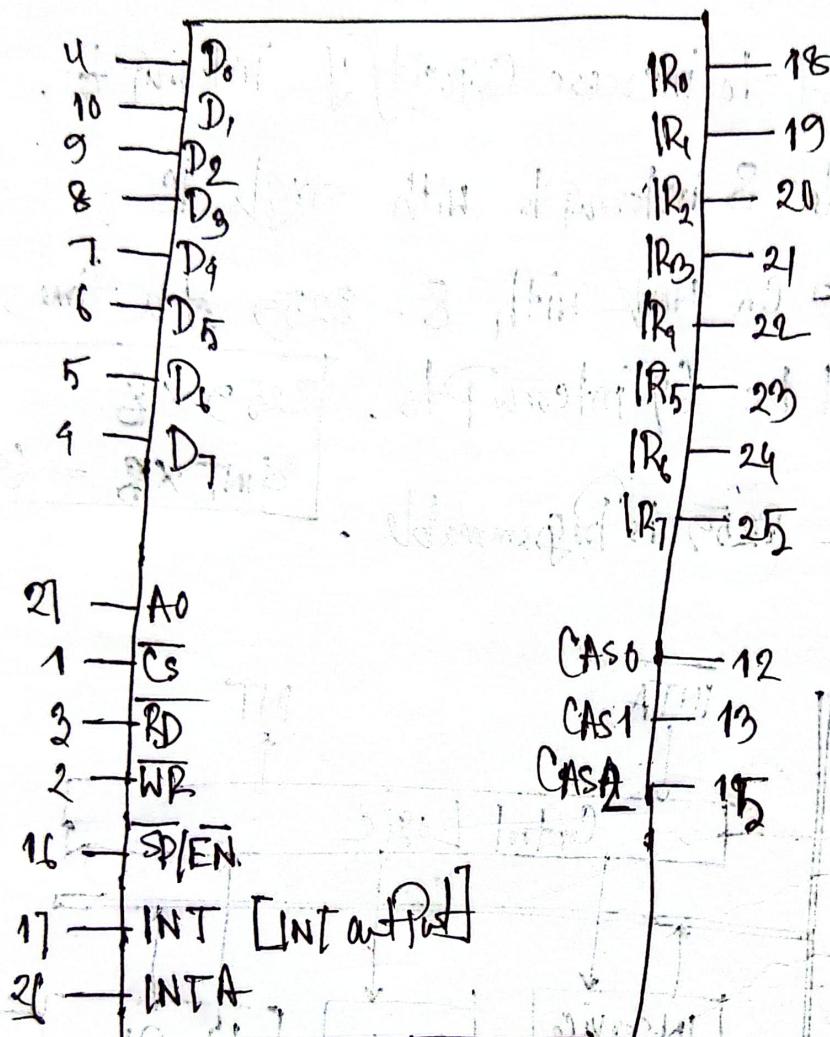
② PIC 8259 A

- ① 8259 is designed to work with Various MP like 8085, 8086 etc.
- ② 8259 is designed to increase Capacity of interrupts.
- ③ 8259 can handle 8 interrupts with single IC.
- ④ One master 8259 can work with 8 - 8259 at a time, so total capacity will be 64 interrupts.
- ⑤ The vector add. of 8259 is programmable.

$$\begin{array}{|c|} \hline 8259 \times 8 \\ \hline 8 \text{ INT } \times 8 = 64 \text{ INT } \\ \hline \end{array}$$



* # Pin Diagram 9 8259A PIC



*# Core i3 Vs i5 Vs i7

Processor Feature	i3	i5	i7
① Lithography	14 nm	14 nm	14 nm
② Cores	4	6	8
③ Threads	4	6	8
④ Base Frequency	3.6 GHz	3.7 GHz	3.6 GHz
⑤ Boost	4.4 GHz	4.6 GHz	4.9 GHz
⑥ Cache	8 MB	9 MB	12 MB
⑦ TDP	91 W	95 W	95 W
⑧ Max Memory Size	64 GB	64 GB	64 GB

*# Handshaking | Polling :

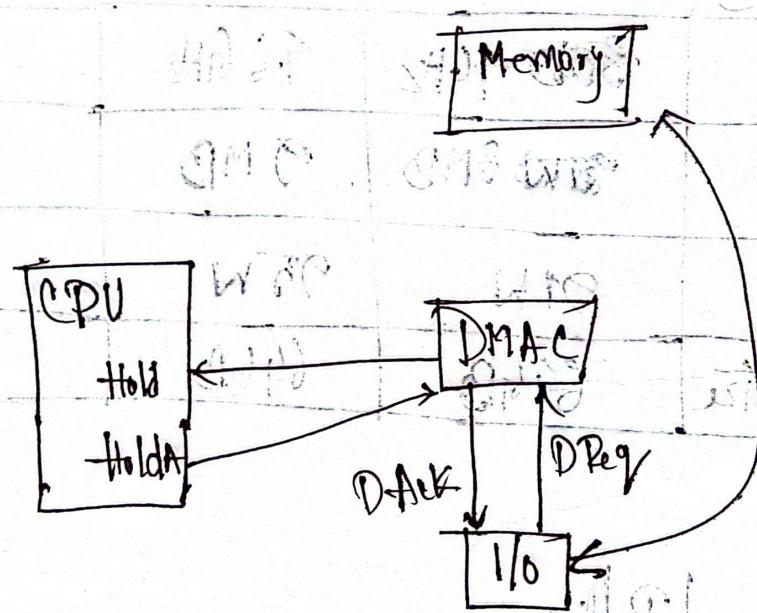
The method for synchronizing the I/O devices with the MP is called handshaking or Polling.

* # DMA (Direct memory Access)

DMA is the direct access between I/O devices and memory without the help of CPU.

Read : Transfer data from memory to I/O devices.

Write : Transfer data from I/O devices to memory.



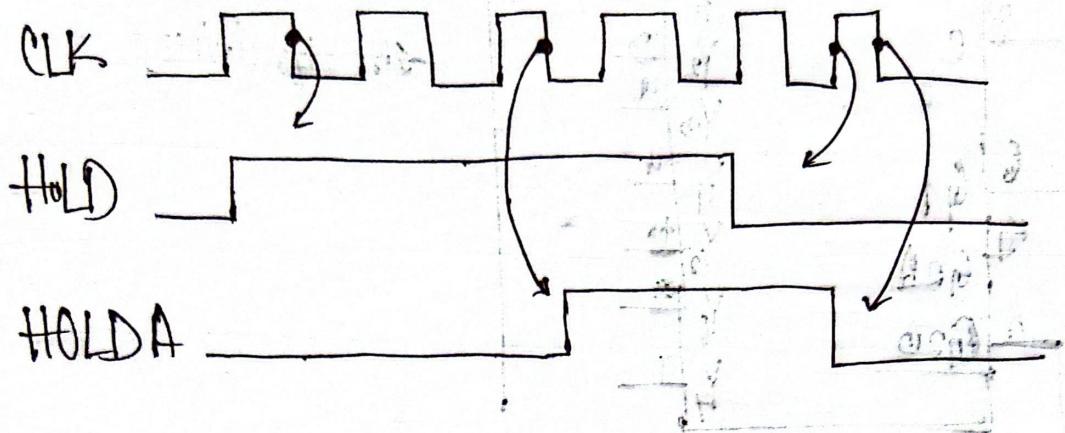
* ① DReq → DMA Request

* ② Hold → CPU Send hold signal

* ③ Hold A → Hold Acknowledgement Signal to DMA

* ④ DACK → DMA Acknowledgment to Access direct to memory.

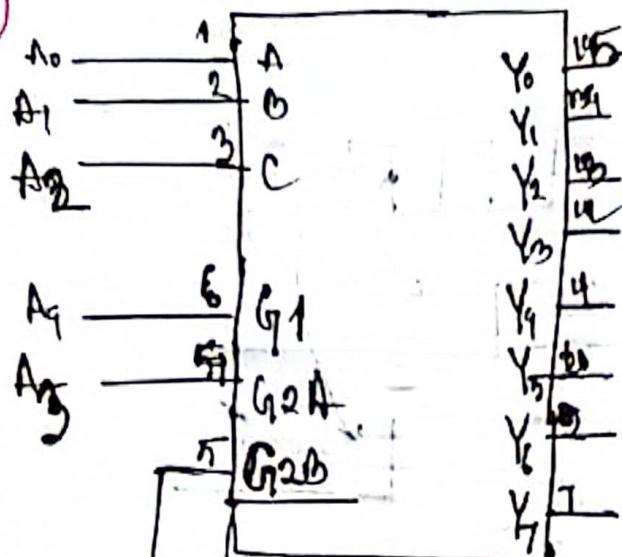
Operation:



Memory Mapped I/O Vs I/O Mapped I/O

- | | |
|---|--|
| <ul style="list-style-type: none">① Here I/O devices <u>treated as Memory</u>② Has <u>20-bit Addressing</u> ($A_0 - A_{19}$)③ Can Address $= 2^{20} = 1\text{ MB}$④ Number of devices can be $= 2^{20}$⑤ Decoding is <u>Expensive</u>⑥ I/O can be accessed by any memory <u>instruction</u>⑦ Data transfer happens between <u>register and I/O</u> | <ul style="list-style-type: none">① Here I/O devices <u>treated as I/O</u>② Has <u>16 bit addressing</u> ($A_0 - A_{15}$)③ Can Address $= 2^{16} = 64\text{ K}$ Address④ Number of devices can be $= 2^{16}$⑤ Decoding is <u>Cheaper</u>.⑥ I/O can be accessed only by <u>I/O instruction</u>.⑦ Data transfer happens only between <u>AX and I/O</u>. |
|---|--|

④



$A_0 - A_{15}$ | $000\text{H} - 0FFFFH$
~~-256 to devices~~

AT&T

all bottom 8 bits of L RAM program



$A_5 \cdot A_4$ = 2nd winds of soft

$A_4 \cdot A_3$ = bottom winds of soft

$(A_4 \cdot A_3) \text{ or } (A_5 \cdot A_4) = 2^8 = 256$

$256 \times 8 = 2048$ words of memory

Final: Decoding 8-bit Y_0 Port Address

$Y_0 = 2^8 = 256$ words of memory

$Y_2 = 2^8 = 256$ words of memory

⑤ MC68051 Pin:

ALE → g1's used to separate data and address.

→ AD₀-AD₇ lines are time multiplexed

→ g1 ALE=1 Bus carries Address

→ g1 ALE=0 Bus carries Data.

Port 3 → On Port 3, 8051 has 8 Pin.

- Perform 8 bit Operation on entire Port.
- Also u-1 bit in a Port 3
- has many alternate function.

RxD → Used to Control serial Communication

Accumulator → Accumulator is a 8 bit register

→ Most Arithmetic and logical Operation are Performed
with respect to accumulator

→ e.g. → ADD A,R0

→ ANL A,R1 : AND

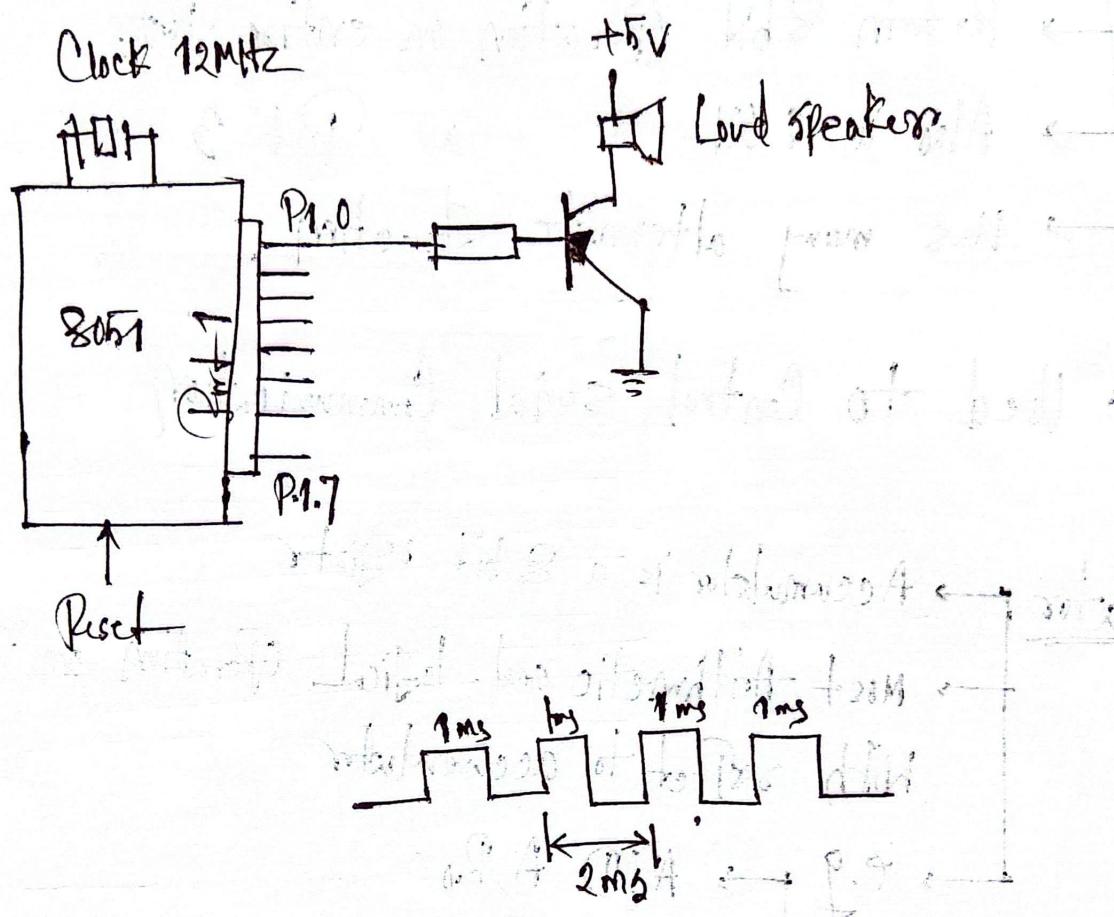
④ Instruction cycle = $\frac{12 \text{ clock cycle}}{12 \text{ MHz}} = \frac{12 \text{ cycle}}{12 \times 10^6 \text{ cycle/sec}}$

∴ One cycle is a short time 10^{-6} sec

$$= 1 \mu\text{s}$$

2

④ Speaker Application Using 8051

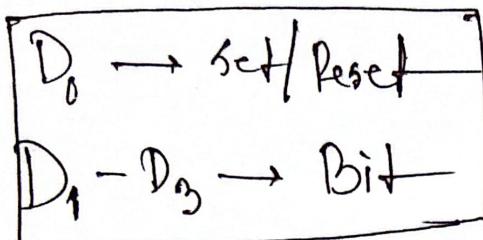


⑤ SOC [System on chip]

Is an IC that integrates all Components of a Computer or other electronic system into a single chip.

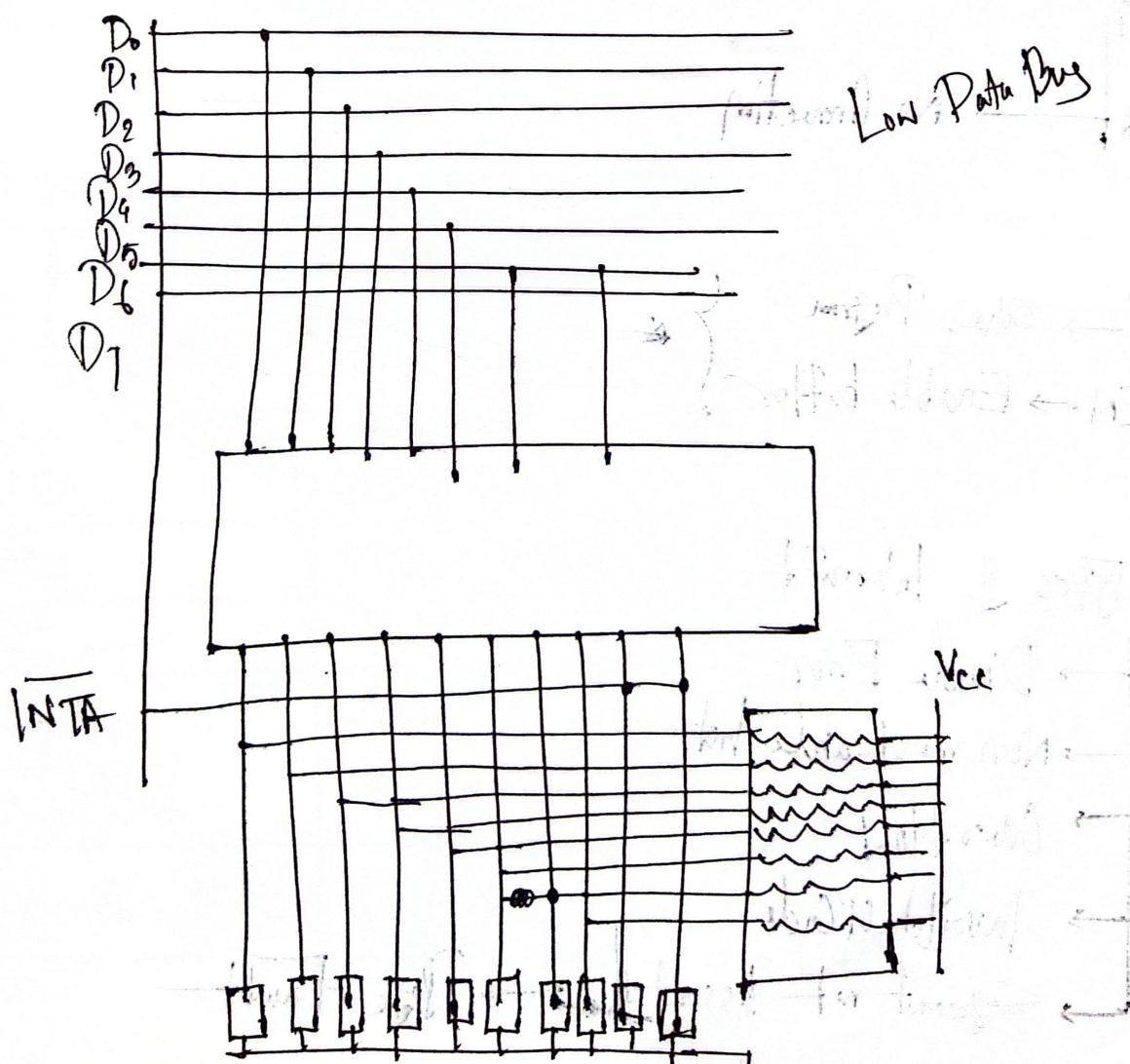
BSR [Bit Set / Reset] in 8255 A

BSR exist in Port C of 8255 A.

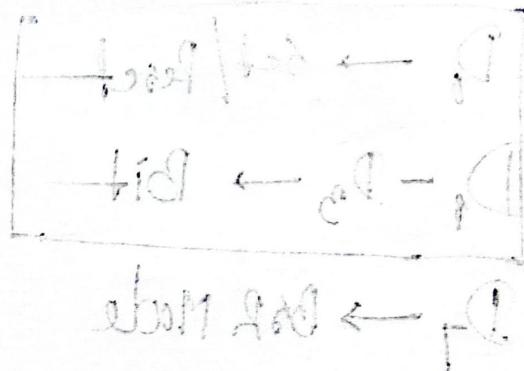
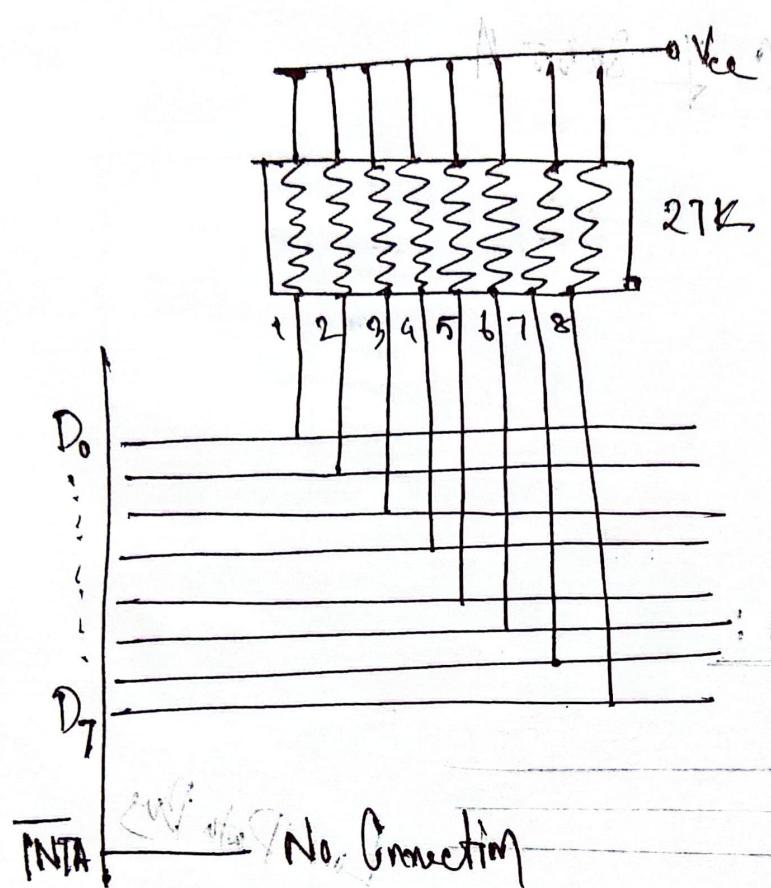


D₇ → BSR Mode

1AH in response to INTA:



Vector type of FFH



low data bus

: 64M of memory at FFH

SP → Stack Program
EN → Enable buffer

Types of Interrupt

- Divide Error
- Non maskable Int.
- Overflow
- Invalid OP Code
- Segment not Present → Page Fault

Input							Output							
G2A	G2B	G1	A	B	C	D	0	1	2	3	4	5	6	7
1	X	X	X	X	X	X								
X	1	X	X	X	X	X								
X	X	0	X	X	X	X								
0	0	1	0	0	0	0								
0	0	1	0	0	1	0								
0	0	1	0	1	0	0	0							
0	0	1	0	1	1	1	0							
0	0	1	1	0	0	0	0							
0	0	1	1	0	1	1	0							
0	0	1	1	1	1	0	0							
0	0	1	1	1	1	1	0							
0	0	1	1	1	1	1	1	0	0	0	0	0	0	0

All else ①

* # 8051 Family

→ 8052 MC

→ 8031 MC

	8051	8052	8031
ROM	4K	128KB	8K
RAM	128KB	256KB	128KB
Timer	2	3	2
I/O Pins	32	32	32
Serial Ports	1	1	1
Interrupt Source	6	8	6

