Faid Faisal

516-709-4261 faidfaisal1@gmail.com https://www.linkedin.com/in/faid-faisal/ https://github.com/faidfaisal

Education

Stony Brook University **Expected Graduation: May 2027**

Bachelor of Engineering in Computer Engineering *Stony Brook, NY*

Award(s): University Scholars, Dean's List, Presidential Scholarship

GPA: 3.86

Relevant Coursework

- Machine Learning Algorithms
- Operating Systems
- Computer Architecture
- Embedded Microcontrollers System Design
- Digital Design Using VHDL and PLDs
- Electrical Circuit Analysis
- Advanced Data Structures and Algorithms
- Electronics

Technical Skills

Languages: VHDL, SystemVerilog, AVR Microcontroller Assembly, Embedded C, C, C++, Python

Developer Tools: Altium Designer, LTSpice, Fusion 360, Arduino IDE, Active-HDL, MATLAB

Experience

JP Morgan Chase & CO Intern **February 2024 - August 2024**

Software Engineer Intern *Manhattan, NY*

- Reduced onboarding time for new developers by 40% by designing clear Python installation guides, repository setup instructions, and dependency management processes.
- Developed interactive dashboards using Python, Pandas, and Plotly, integrating real-time market data APIs to provide traders with visual insights on undervalued stocks. The dashboards improved trade decision-making accuracy by 25% .
- Implemented real-time anomaly detection for stock price fluctuations, improving trade accuracy by 25% based on backtesting against historical trends.

iRobot **May 2022 - August 2022**

System Operations Intern *Queens, NY*

- Led the design and development of robots, integrating advanced sensors and algorithms to enhance automation, improving task efficiency by 30% .
- Debugged and optimized hardware-software interfaces using Python and C++, ensuring seamless sensor integration and reducing failure rates by 20%.
- Guided a cross-functional team in developing a robotic arm prototype, incorporating ROS (Robot Operating System) to enhance precision in movement. The prototype secured a top-three placement in a regional robotics competition.

Projects

Four-Stage Pipelined Multimedia Processor **August 2025 – December 2025**

- Designed and implemented a four-stage pipelined processor (IF/ID/EX/WB) using VHDL, with structural/RTL modules for each stage.
- Developed a behavioral 128-bit multimedia ALU supporting packed subword parallelism, including arithmetic, logical, and multiply-add/subtract operations.
- Implemented a 32 × 128-bit multi-ported register file and a hazard-free forwarding unit, verified with a cycle-accurate testbench and pipeline execution tracing.

Transformer-Based NLP Chatbot with Intent Recognition **July 2025 – August 2025**

- Trained a transformer model with multi-headed attention, positional encoding, and layer normalization to achieve 80% accuracy in intent classification.
- Engineered a full preprocessing pipeline including text cleaning, tokenization, stopword removal, and TF-IDF vectorization, with custom scripts to convert raw user text into numerical embeddings usable by the model.
- Architected a lightweight interactive frontend using Gradio/Flask to simulate real-time conversations, enabling seamless testing, deployment, and UI-based interaction.

Binary Classification of Breast Cancer Histopathology Slides using CNNs **June 2025 - July 2025**

- Crafted a custom Convolutional Neural Network in PyTorch to classify histopathology images into cancerous and non-cancerous classes, achieving 95.9% training accuracy.
- Created a Gradio-based interactive UI for real-time cancer prediction, enabling seamless visualization of model outputs on histopathology slides for research and diagnostic exploration.
- Performed model tuning, training analysis, and visualization, including architecture design, epoch tracking, and performance graphs.