



LAPORAN PRAKTIKUM

PRAKTIKUM ORGANISASI ARSITEKTUR KOMPUTER

MODUL : 03

“ BINER, GERBANG LOGIKA, DAN
ADDER ”

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HARI : JUM'AT
TANGGAL : 22 SEPTEMBER 2023
WAKTU : 07.30 – 9.15
ASISTEN : MUHAMMAD FIKRI ABDULLAH

MUHAMMAD SYAFIQ IBRAHIM

PROGRAM STUDI SAINS DATA
FAKULTAS TEKNOLOGI INFORMASI DAN SAINS DATA
UNIVERSITAS SEBELAS MARET

2023

Modul 3

BINER, GERBANG LOGIKA, DAN ADDER

ALFANSYAH PUTRA RAJA DINATA (L0223002) / Jum'at, 22 September 2023

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KEGIATAN 1

Mengerjakan 6 soal biner beserta tahapannya.

$$\begin{aligned} 1. \quad 100 + 111 &= 4 + 7 \text{ (Decimal)} \\ &= 11 \text{ (Decimal)} \quad = \mathbf{1100 \text{ (Biner)}} \end{aligned}$$

$$\begin{aligned} 2. \quad 1001 - 101 &= 9 - 5 \text{ (Decimal)} \\ &= 4 \text{ (Decimal)} \quad = \mathbf{100 \text{ (Biner)}} \end{aligned}$$

$$\begin{aligned} 3. \quad 100 \times 101 &= 4 \times 5 \text{ (Decimal)} \\ &= 20 \text{ (Decimal)} \quad = \mathbf{10100 \text{ (Biner)}} \end{aligned}$$

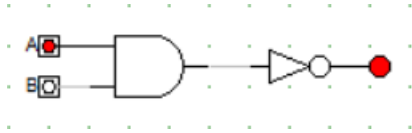
$$\begin{aligned} 4. \quad 10010 / 1001 &= 18 / 9 \text{ (Decimal)} \\ &= 2 \text{ (Decimal)} \quad = \mathbf{10 \text{ (Biner)}} \end{aligned}$$

$$\begin{aligned} 5. \quad (110 - 10) \times 11 &= (6 - 2) \times 3 \text{ (Decimal)} \\ &= 4 \times 3 \text{ (Decimal)} \\ &= 12 \text{ (Decimal)} \quad = \mathbf{1100 \text{ (Biner)}} \end{aligned}$$

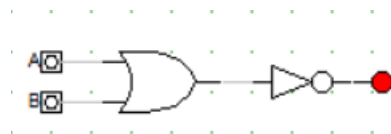
$$\begin{aligned} 6. \quad (110 + 100) / 101 &= (6 + 4) / 5 \text{ (Decimal)} \\ &= 10 / 5 \text{ (Decimal)} \\ &= 2 \text{ (Decimal)} \quad = \mathbf{10 \text{ (Biner)}} \end{aligned}$$

KEGIATAN 2

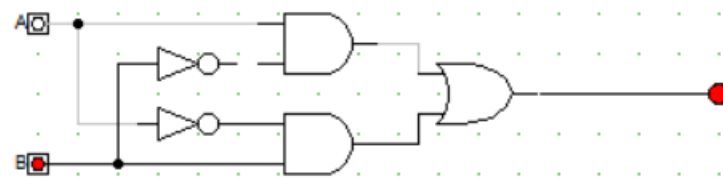
1. Gerbang NAND



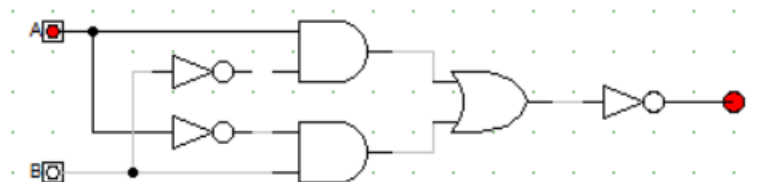
2. Gerbang NOR



3. Gerbang XOR



4. Gerbang XNOR

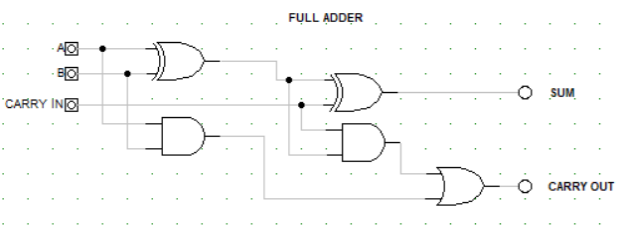
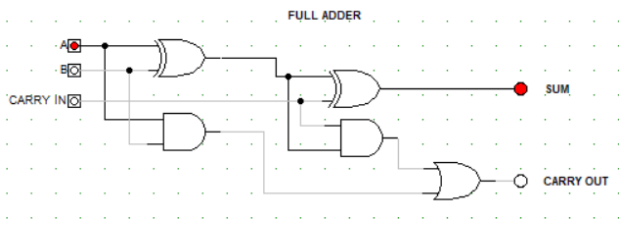
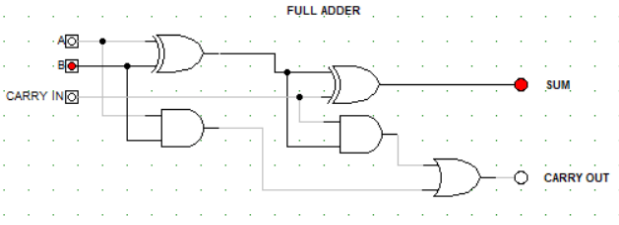
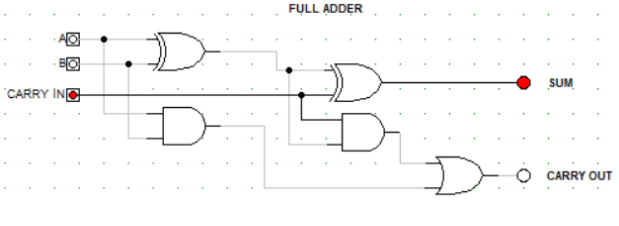
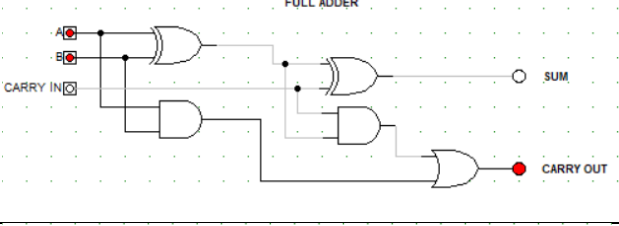
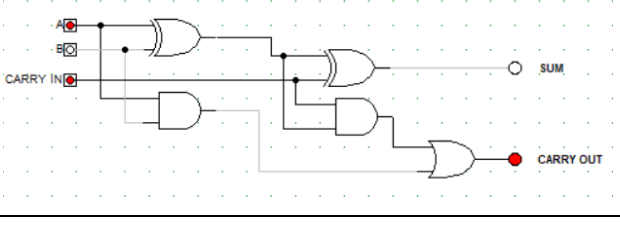


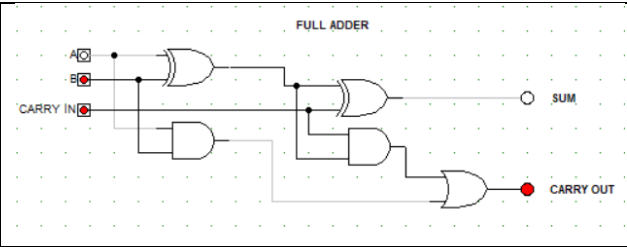
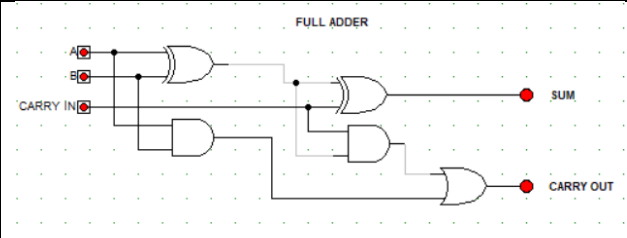
KEGIATAN 3

1. HALF ADDER

NO	GAMBAR	A	B	SUM	CARRY
1	<p>Diagram of a Half Adder circuit. Inputs A and B are both 0. The XOR gate output (SUM) is 0, and the AND gate output (CARRY) is 0.</p>	0	0	0	0
2	<p>Diagram of a Half Adder circuit. Input A is 1 and input B is 0. The XOR gate output (SUM) is 1, and the AND gate output (CARRY) is 0.</p>	1	0	1	0
3	<p>Diagram of a Half Adder circuit. Input A is 0 and input B is 1. The XOR gate output (SUM) is 1, and the AND gate output (CARRY) is 0.</p>	0	1	1	0
4	<p>Diagram of a Half Adder circuit. Inputs A and B are both 1. The XOR gate output (SUM) is 0, and the AND gate output (CARRY) is 1.</p>	1	1	0	1

2. FULL ADDER

NO	GAMBAR	A	B	CARRY IN	CARRY OUT	SUM
1		0	0	0	0	0
2		1	0	0	0	1
3		0	1	0	0	1
4		0	0	1	0	1
5		1	1	0	1	0
6		1	0	1	1	0

7		0	1	1	1	0
8		1	1	1	1	1

Alfansyah Putra Raja Dinata

Seorang pelajar yang suka belajar hal baru, khususnya di bidang komputer, terutama di bidang perangkat lunak (software), termasuk custom ROM dan custom Windows. Memiliki hobi fotografi di bidang arsitektur dan street photography. Ketika bosan, suka melakukan perjalanan (touring) sampai ke pelosok entah berantah hanya untuk mencari hal baru.