DESIGN PROJECT

1. Overview

You are to design a fully differential OTA for a switched capacitor circuit application. Figure 1 shows a model of the overall circuit in the relevant phase of operation. The following target specifications apply:

Parameter	Specification
Technology	0.35μm CMOS, Nominal Corner
Operating Temperature	25°C
V_{DD}	3V
Power Dissipation	Minimize
C_L	≥ 2pF
C_s	≥ 4pF
C_f	$0.5 \cdot C_s$
Current Mirror Ratios[1]	≤ 20
Pole/Zero cancellation and left half plane zeros	Forbidden
CMFB Circuit	Ideal, as in homework 6
Reference Current	Single ideal current source of arbitrary value, with positive node tied to V_{DD} or negative node tied to GND
Dynamic Range	86dB
Settling Time[2]	≤10ns
Static Settling Error	≤0.1%
Dynamic Settling Error	≤0.05%

1 Diode connected devices cannot "drive" more than the specified number of same-size unit devices.

2 Measured for a differential input step that transitions from 0V at t=0 to the maximum input voltage of the circuit in 0.5ns. The maximum input corresponds to the maximum output voltage used in the dynamic range calculation, divided by the closed loop gain.

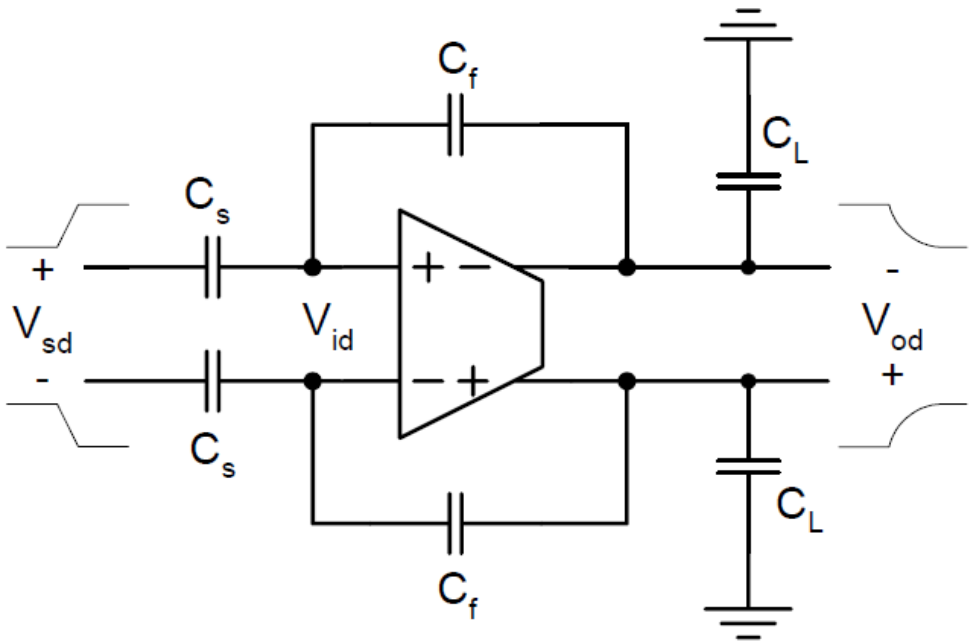

Figure 1

Key choices to be made in this design problem include:

- Amplifier topology
- Output signal range
- Input and output common mode levels
- Device sizes and bias currents

In addition to the design at nominal specifications indicated above, you will conclude this project by running two additional sets of simulations at "worst case" process and temperature corners –"fast" devices operated at 0°C, and "slow" devices at 125°C. For simplicity in this short project, you are not required to meet the specifications at these conditions. The purpose of this addition is to give you a feel for the impact of temperature and process variations. In practice, you would overdesign your circuit such that the given specs are met across all corners and conditions.

You may work on this project in teams of three. Each team must submit one copy of the deliverables specified below. You are encouraged to discuss the design problem with other teams, but your design must be unique. Under no circumstances should you exchange computer files with other teams; this would constitute a gross violation of the honor code.

2. Suggested Design Flow

As you might find out, this problem has many more degrees of freedom than any problem you have dealt with so far. Hence, we suggest that you organize your time and work e.g. as follows

a) Read this entire handout thoroughly.

b) Find a project partner (if you haven't already done so).

c) Download the starter file project_example.zip or copy the files into your working directory. Examine and understand the included files, run the various included simulations on the provided example circuit.

d) Familiarize yourself with the design example presented in lecture 20. Try to duplicate the results and/or modify the specs to meet some of the requirements of this project (e.g. dynamic range).

e) Pay special attention to lectures 18-23; this material will provide you with the last few pieces of information needed to complete this assignment.

f) Decide about the circuit architecture and begin the design. In the spirit of the design example presented in class, develop a spreadsheet or Matlab script that allows you to optimize your design iteratively without repetitive "Spice monkeying". You may want to begin with a small-signal based design (as done in class), and later include transient settling considerations.

g) Begin to write your project report (see below) at least several days before the deadline. Your grade will strongly depend on the quality of your write-up, and not just the achieved power dissipation.

Finally, and this is important: **DON'T WAIT UNTIL THE LAST MINUTE TO START**. This project involves a great deal of just plain old labor; it takes significant amounts of time to determine suitable design choices, run all the necessary simulations and document your work. Also, the instructional computers and printers have been known to slow down and even go down at the worst possible times, to say nothing of license availability problems. We will

be largely unsympathetic to pleas for extensions arising from such problems.

3. Deliverables

a) Electronic Submission of Circuit Netlist

You are required to submit an electronic copy of your final design netlist. Details regarding this submission and subtleties of file formatting will be communicated to you in a separate handout.

b) Project Report

You are required to prepare a hardcopy report with the following format (a hand-written report is just fine). In case you decide to submit a computer generated report, make sure to use font sizes greater than 10. Be sure to follow the format instructions below *EXACTLY*:

Page 0: Cover Page

Page 1: Outline of your design, justifications of key design decisions; comparison with alternatives.

Page 2: Schematic diagram of final design, with component values and bias currents clearly labeled. Show component values right next to the components, and currents next to the branches (i.e., absolutely, positively do not make us refer to a look-up table). Annotate all transistors with the chosen g_m/I_D value.

Pages 3-5: Calculation of key design parameters, such as transconductances, bias currents, etc. Be sure to include a calculation of the circuit's settling time. Compare hand calculated values with final HSpice values in a table and discuss discrepancies. Make sure to include the total power dissipation of your design (calculation and HSpice). This is one of the most important sections of your report! The lowest power designs will not automatically score the highest grades. The methodology you used to justify your design choices and component values is far more important (see section on point distribution below).

Page 6: Bode plot of T(j⎾), phase and magnitude. Clearly annotate the achieved low frequency loop gain, the loop crossover frequency and the phase margin.

Page 7: Plots the simulated settling transient of V_{od} (no zoom, show the entire waveform). In a separate subplot, show the % error of the differential output voltage relative to the ideal output voltage. Zoom into the relevant region of the settling, i.e. clearly demonstrate that your design settles within spec. Annotate the achieved settling time and static settling error. For simplicity, we use the error at t=30ns as an estimate of the static settling error.

Page 8: Plot the common mode output voltage versus time during transient settling of the circuit. In separate subplots each, also show the differential output current of the OTA, and the differential input to the OTA (V_{id} in Figure 1).

Page 9: Plot of the noise power spectral density at the OTA output (V_{od}) and noise integral. Annotate the total integrated noise value and the achieved dynamic range.

Page 10: Output range. Simulation plot showing the differential open loop DC gain V_{od}/V_{id} of the amplifier. Mark the differential output voltage at which the gain has dropped by 30%. This value should be larger than the peak output voltage used in your dynamic range calculation.

Page 11-12: Results of corner simulations. Tabulate your circuit's performance for the slow/hot and fast/cold corner. Include settling time, static error, and any other parameter that you find noteworthy. Include the %-changes with respect to nominal conditions in your table.

In case the circuit is non-functional in these corners, investigate and explain the problem (no need to fix the circuit). Include selected interesting plots documenting corner performance and/or issues.

Page 13: Comments and Conclusion. Here, you can convey issues you may have had, or things you've learned/not learned in this project.

4. HSpice Testbench

We will use the testbench provided as part of the starter files to evaluate your design in HSpice. The testbench is illustrated schematically in Figure 2 below. The 10gig helper resistors are needed to properly initialize capacitor charges in the operating point of the circuit (Note that in practice, this will be accomplished using dedicated switches in the final switched capacitor circuit).

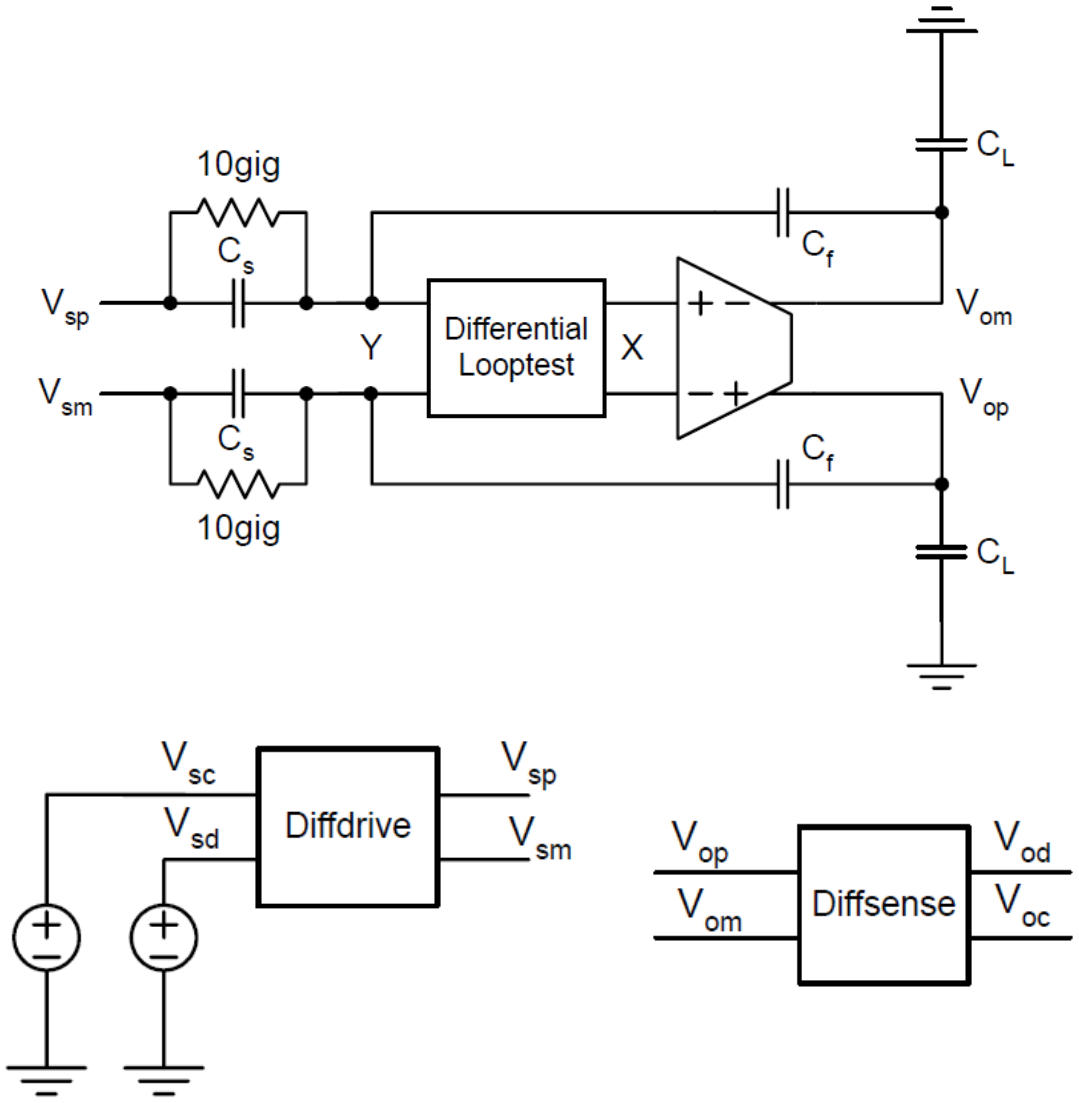

Figure 2

The testbench file contains the proper simulation setup to carry out the following analyses needed in this project:

- Loop gain AC simulation. Sets V_{sd}=0V and activates the ac sources in the Differential Looptest block to find the circuit's loop gain vs. frequency.
- Noise simulation.
- Transient simulation. Applies the specified input transient step. The amplitude is determined by a parameter set in your submitted netlist (see example design netlist).
- Open-loop DC gain simulation. Applies a (small) DC-sweep to V_{sd}. Note that this DC simulation will be unaffected by the presence of all capacitors and the Differential Looptest block.

Note: The testbench will run properly with HSpice version 2004 or later (e.g. the 2006 version setup for this course. This is due to the RUNLVL option (see application note in handouts/spice section on eeclass) that we're using to improve transient accuracy and simulation time.

5. Grading

1. Design Flow and Insight 30% points
2. Documentation 20% points
3. Specs and Practicality 20% points
4. Discussion/documentation of corner performance 10% points
5. Power Dissipation 20% points

	Aspect	Excellent	Not that great…	Poor
1.	Design Flow	Well structured, clear and reasonable decisions	Well structured, but unjustified decisions	Unclear how design point was reached
	CMFB	Proper design based on stability constraints	No mention of stability considerations, randomly chosen CMFB transconductance	Unstable
	Discrepancies between hand analysis and simulations	Well explained and/or within reasonable bounds		No discussion of discrepancies and potential sources
	Misconceptions	None	Minor	Not clear if students understand their design
	Creativity	Tried something "new" and interesting, e.g. based on a literature search	Basic design	
2.	Schematics & annotation	Clearly labeled	Somewhat unclear	Unreadable schematics
	Plots	Clear, good zoom and annotation	Somewhat sloppy, e.g. no zoom, no labels.	Some plots missing or unreadable.

3.	Design constraints/Practicality	All satisfied	Somewhat impractical, e.g. violating M-factors, tail current source in triode region, …	Impractical design, e.g. pole zero cancellation
	Netlist	Simulated OK		Not functional
	Specs	All met and results agree with our sim	1 specification barely not met, results agree with our sim	More specifications missed or design does not work
4.	Corner performance	Well documented, all issues explained		Not clear if corner simulations were run, inconsistent data without proper interpretation
5.	Power dissipation	Computed based on ranking		