CECS 341

LAB 4A

Fair Nuri Aboshehwa

Section 1: Verilog Source Module

```
`timescale 1ns / 1ps

module MIPSALU (ALUctl, A, B, ALUOut, Zero);
  input [3:0] ALUctl;
  input [31:0] A,B;
  output reg [31:0] ALUOut;
  output Zero;

  assign Zero = (ALUOut==0);
  always @(ALUctl, A, B) begin
    case (ALUctl)
      0: ALUOut <= A & B;
      1: ALUOut <= A | B;
      2: ALUOut <= A + B;
      6: ALUOut <= A - B;
      7: ALUOut <= A < B ? 1 : 0;
      default: ALUOut <= 0;
    endcase
  end
endmodule
```

Section 2: Verilog Test Fixture

```
`timescale 1ns / 1ps

module MIPSALUTESTER;

	reg [3:0] ALUctl;
	reg [31:0] A, B;

	wire [31:0] ALUOut;
	wire Zero;


	// Instantiate the Unit Under Test (UUT)
	MIPSALU uut (
    .ALUctl(ALUctl),
    .A(A),
    .B(B),
    .ALUOut(ALUOut),
    .Zero(Zero)
	);

	initial begin
    $dumpfile("dump.vcd");
    $dumpvars(5);
   end

	initial begin
		A = 32'b01010101010101010101010101010101;
		B = 32'b10101010101010101010101010101011;
		ALUctl = 0;
		#10;

		A = 32'b01010101010101010101010101010101;
		B = 32'b10101010101010101010101010101011;
		ALUctl = 1;
		#10;

		A = 32'b01010101010101010101010101010101;
		B = 32'b10101010101010101010101010101011;
		ALUctl = 2;
		#10;

		A = 32'b01010101010101010101010101010101;
		B = 32'b10101010101010101010101010101011;
		ALUctl = 6;
```

```
                #10;

                A = 32'b01010101010101010101010101010101;
                B = 32'b10101010101010101010101010101011;
                ALUctl = 7;
                #10;
                $stop;
        end
endmodule
```

Section 3: Simulation Screenshot