CECS 341

LAB 4B

Fair Nuri Aboshehwa

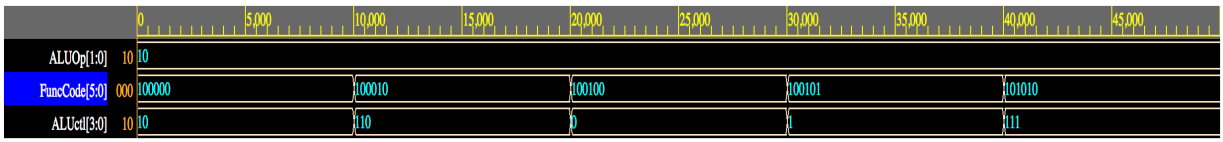
Section 1: ALU Control Source

```
`timescale 1ns / 1ps

module ALUControlTester;

  reg [1:0] ALUOp;
  reg [5:0] FuncCode;

  wire [3:0] ALUctl;

        // Instantiate the Unit Under Test (UUT)
        ALUControl uut (
                .ALUctl(ALUctl),
                .ALUOp(ALUOp),
                .FuncCode(FuncCode)
        );

        initial begin
                $dumpfile("dump.vcd");
                $dumpvars(5);
        end

        initial begin
                ALUOp = 2'b10;
                FuncCode = 6'b100000;
                #10;

                ALUOp = 2'b10;
                FuncCode = 6'b100010;
                #10;

                ALUOp = 2'b10;
                FuncCode = 6'b100100;
                #10;

                ALUOp = 2'b10;
                FuncCode = 6'b100101;
                #10;

                ALUOp = 2'b10;
                FuncCode = 6'b101010;
                #10;
                $stop;
        end
endmodule
```

Section 2: ALU Control Test Fixture

```
`timescale 1ns / 1ps

module ALUControl(ALUOp, FuncCode, ALUctl);
  input [1:0] ALUOp;
  input[5:0] FuncCode;
  output reg[3:0] ALUctl;

  always @ (ALUOp, FuncCode)
    begin
      case ({ALUOp, FuncCode[3:0]})

      6'b100000: ALUctl<=2;
      6'b100010: ALUctl<=6;
      6'b100100: ALUctl<=0;
      6'b100101: ALUctl<=1;
      6'b101010: ALUctl<=7;
      default: ALUctl<=15;

    endcase
  end

endmodule
```

Section 3: Simulation Screenshot


0
5,000
10,000
15,000
20,000
25,000
30,000
35,000
40,000
45,000
ALUOp[1:0]
10
10
FuncCode[5:0]
000
100000
100010
100100
100101
101010
ALUctl[3:0]
10
10
110
0
1
111