Coursework for Tutorial 3

Computer Architecture II:

November 14, 2023

1 Assignment

Task #1 Consider the following MIPS pseudocode:

```
LW   R1,   0(R2)       ;R1=MemContent[R2]
SUB  R1,   R3,   R2    ;R1 = R3 - R2
SUB  R3,   R1,   R2    ;R3 = R1 - R2
ADD  R2,   R1,   R2    ;R2 = R1 + R2
SUB  R1,   R1,   R2    ;R1 = R1 - R2
ADD  R3,   R1,   R2    ;R3 = R1 + R2
```

Assume that before performing any of the above computations `R1=5`, `R2=3`, `R3=1` and `MemContent[3]=2`.

I. Assume a full implementation of the DLX/MIPS pipeline discussed in class. What is the final value of `R1`, `R2` and `R3`? How many clock cycles will it take to complete the above set of operations? Explain your answer also using a pipeline table.

II. Can the number of clock cycles be optimised by employing out-of-order instruction scheduling? In case, how many clock cycles does it take after optimisation? Explain how you arrive at your answer.

III. Assume that forwarding has now been deactivated. How many clock cycles do the above instructions take to complete? What is the final value of `R1`, `R2` and `R3` in this case? Explain.

IV. A sloppy engineer has now forgot to take into account the possibilities of hazards when implementing the pipeline *without forwarding*. Instead of stalling, when conflicts occur the CPU simply continues its computations as if nothing happened! How many clock cycles do the above instructions take to complete in this wrongly implemented pipeline? What is the final value of `R1`, `R2` and `R3` in this case? Explain your answer thoroughly.

Task #2 Consider an hypothetical 32bit processor with an MMU that supports a 3-levels page table structure with either one of the two following configurations: 8-7-5-12 and 7-7-5-13.

I. What page sizes are supported by the MMU?

II. What is the size (in bytes) of page tables in each level of the hierarchy? (disregard the impact of flag bits in the computations).

III. Assume the 8-7-5-12 configuration. Assume that the kernel virtual space (starting at 0x0F000000) is mapped into 64MB of contiguous space by the MMU starting at physical address 0x41000000. Outline the resulting page table structure.

IV. Assume the 7-7-5-13 configuration. Assume that the kernel virtual space (starting at 0x00000000) is mapped into 8MB plus 12B of contiguous space by the MMU starting at physical address 0x010FF000. Outline the resulting page table structure.

2 Instructions

- Submit the answer in blackboard in a single .pdf file. The pdf can include pictures if you draw diagrams by hand.
- Due date: December 3 @ 11.59pm. No late submissions!
- This tutorial will count toward 10% of your final grade. Each task will count toward 50% of the overall tutorial score. Sub-tasks from I and II are worth 10 points. Sub-tasks III and IV are worth 15 points. Answers need to be correct and *thoroughly explained*.