Quiz: Memory Management Basics

Total points 82/82

Take the quiz solo, but feel free to consult a partner student, the book, the videos or other resources if needed. Re-take quiz if your score is less than 80% or if you just want some more practice.

The respondent's email (**faiyaz@pdx.edu**) was recorded on submission of this form.

✓ The _____ linux command is used to determine the amount of free memory on a system, displaying the amount of unused system RAM, detailed info. about how much free & in-use physical memory you have, swap space usage, and system RAM being used by cache & buffers. *5/5

- (●) free ✓
- ( ) pmap
- ( ) vmstat
- ( ) ps

✓ What is the main benefit of isolated address spaces (one address space per process) ? *5/5

- ( ) Virtualization
- (●) Protection ✓
- ( ) Performance
- ( ) Ease of programming
- ( ) Scalability

✓ For process A, if the base register value is 2^12 and the process's address space size is 2^16 memory words, then what value will the OS set as the value for the limit register? *5/5

- ○ 2^(12+16)
- ○ 2^16
- ◉ 2^12 + 2^16 ✓
- ○ 2^32
- ○ 2^12

✓ The compiler and linker help us to maintain the illusion of a contiguous, isolated, virtual address space. *5/5

- ◉ True ✓
- ○ False

✓ Base and Limit registers enable efficient time-sharing of the CPU. * 5/5

- ◉ True ✓
- ○ False

✓ When using base&limit registers a running process must have all of its data residing in physical memory. *5/5

- (●) True ✓
- ( ) False

✓ With base+limit registers a process's physical memory location might change over time. *5/5

- (●) True ✓
- ( ) False

✓ In a paging-based virtual memory system, the OS does not need to keep all of a process' pages in physical memory. *5/5

- (●) True ✓
- ( ) False

✓ The OS reconfigures or flushes (erases) the TLB on each context switch. * 5/5

- (●) True ✓
- ( ) False

Feedback

TRUE in most cases. For most systems the TLB is flushed on each context switch because the virtual-to-physical mapping is different for each process.

But FALSE is also a valid response here because some TLBs do have "tagged" entries that allow the OS to switch from process to process without flushing the TLB on every switch.

✓ Using base&limit registers the OS sets the value of the limit register a bit higher than needed so that the process has room to grow in the future. The extra, unused (for now) allocation is what type of fragmentation? *5/5

- ( ) External
- ( ) Maternal
- ( ) Nocturnal
- (●) Internal ✓
- ( ) Fraternal

✓ In a paging system, the OS needs to choose the page size. What is the primary benefit of choosing a small page size for a paging-based virtual memory system? *5/5

- ○ less overhead from page faults
- ○ reduces external fragmentation
- ◉ reduces internal fragmentation ✓
- ○ faster address translation
- ○ increased TLB hit rate

System with 24 bit addresses and 2K page size
Consider the following system:

physical address space size: 24 bits
page size is 2K

✓ How many pages (maximum) exist in this system? * 5/5

- ○ 2^11
- ○ 2^24
- ◉ 2^13 ✓
- ○ 2^10
- ○ Other: .....

✓ Consider a process running on our 24 bit address system with page size of 2048 (2K). The process allocates an array of size more than 2K, and the array elements cannot all fit into one page. The process steps through the array, reading each element of the array. What happens when the process reaches the physical page frame boundary, how does the process know where to find the next element in the array? *5/5

- ○ the OS allocates contiguous physical pages to hold the array, so the next array element will always be held in the next physical memory location.
- ◉ the process references the array elements using virtual addresses and does not know or care where the data is actually stored in physical memory ✓
- ○ a page fault occurs causing the OS to place the next array elements in the adjacent physical page(s)
- ○ the OS avoids this problem by not allowing such large arrays to be allocated

✓ Within every 24 bit memory address, how many bits will be used to determine the offset within a given page? *5/5

- ○ 13
- ○ 10
- ◉ 11 ✓
- ○ 24
- ○ Other: .....

TLB - Translation Lookaside Buffer

Which of the following are true about TLBs? *

	True	False	Score	
it is a cache for address translations	◉	○	1/1	✓
it is a buffer that looks to the side to watch for oncoming traffic. in UK and India it it looks to the right whereas in USA it looks to the left.	○	◉	1/1	✓
it helps to avoid needing to read physical memory on every address translation	◉	○	1/1	✓
it is a high performance mechanism for mapping from physical to virtual addresses	○	◉	1/1	✓
TLB stands for Translation Lookaside Buffer	◉	○	1/1	✓

Indicate the characteristics of each type of TLB *

	Software Managed TLB	Hardware Managed TLB	Score	
Only the OS actually reads/writes the page table	◉	○	1/1	✓
The OS decides which translations are stored in the TLB	◉	○	1/1	✓
The OS does not need to be run whenever there is a TLB miss	○	◉	1/1	✓
TLB raises a "TLB miss interrupt" whenever a virtual address is not found in its cache	◉	○	1/1	✓
The OS can store page tables any way it wants to	◉	○	1/1	✓
The TLB itself decides which translations are kept in its cache	○	◉	1/1	✓
The page table must be store in a well-known location in memory	○	◉	1/1	✓

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