Faizan Feroz

Senior Software Engineer — C++ — Qt — Software Systems

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Technical Skills

Programming: C++ (11/14), C, Python, Bash Scripting, UML, STL, Multithreading, Data Structures, IPC, UDP, TCP.
Frameworks & Tools: Qt, QML, Octave, PyTorch, VS Code.
Domains: Automotive Software, ADAS, AUTOSAR, Medical Devices, Power Systems, Railways.
Standards: IEEE C37.118 (COMTRADE, Synchrophasor), AUTOSAR, MISRA C++, CERT C++, CWE.
Platforms: Linux, ECU-level Software, RCAR, Qualcomm Platforms.
Practices: Git, Agile, Design Patterns, SOLID Principles, Debugging, SWE Documentation, JIRA, Confluence

Professional Summary

Senior Software Engineer with 4+ years of experience designing and developing production-grade, system-level software across automotive, medical devices, railways, and electrical power systems. Strong expertise in modern C++, Qt-based applications, Linux environments, and safety-critical software development. Proven ability to take software from research and prototyping through validation, integration, and real-world deployment.

Professional Experience

Senior Software Engineer – Automotive Systems
KPIT Technologies (Honda Program) Mar 2024 – Present

- Develop and maintain production automotive software in collaboration with OEM stakeholders.
- Design and implement C++ components aligned with ADAS and system-level automotive requirements.
- Perform debugging, static code analysis, root-cause analysis, and validation within structured quality processes.
- Support software integration on RCAR, ECU, and Qualcomm automotive platforms in Linux environments.
- Collaborate with client stakeholders across the complete software lifecycle from SWE.1 to SWE.4.
- Contribute to architecture documentation including class diagrams, sequence diagrams, and state machine diagrams.
- Perform defect analysis and code optimization to improve ECU performance using Katapult profiling reports.
- Utilize Parasoft static analysis tools to ensure compliance with AUTOSAR, MISRA C++, CWE, and CERT C++ standards.

Senior Associate – Software Development
GE HealthCare (Sutherland) Jul 2023 – Feb 2024

- Designed and developed UI components for resting ECG medical devices including MAC-5 and MAC-7.
- Implemented Qt/QML interfaces with supporting C++ backend logic for clinical workflows.
- Contributed to production-grade medical software with a focus on reliability, usability, and regulatory compliance.
- Participated in debugging, defect resolution, and controlled delivery workflows.

Research and Development Engineer
Industrial Research and Consultancy Centre (IRCC), IIT Bombay, IISc Bengaluru Feb 2021 – Aug 2023

- Worked on Government of India funded R&D projects sponsored by HSRCL and DMRC.
- Developed simulation software for traction power supply and power system analysis for the Mumbai–Ahmedabad High-Speed Rail project.
- Built Linux-based tools using C++, Python, and Octave for system modeling, numerical analysis, and validation.
- Designed and developed Qt-based simulation software implementing complete front-end and back-end functionality.

Engineering Projects

High-Speed Rail Traction Power Analysis Software (HSRCL) Private Repository

- Architected a Qt-based C++ application integrated with Octave numerical models.
- Implemented load flow, short-circuit, and harmonics analysis for high-speed rail systems.
- Designed scenario-based evaluations using railway timetables and route parameters.

Metro Crew Scheduling and Timetabling Optimization (DMRC) Private Repository

- Led a team of 3–4 engineers to design and implement crew scheduling optimization models.
- Developed Python-based optimization solutions in a Linux environment.
- Delivered constraint-aware and operationally feasible crew schedules.

iCoReader – COMTRADE Data Visualization Tool Source Code

- Developed a C++/Qt desktop application for COMTRADE file parsing and visualization.
- Implemented IEEE-compliant disturbance data processing for power system analysis.

iTester – PMU Connection Tester Source Code

- Built a C++/Qt tool for real-time PMU data acquisition and synchrophasor visualization.
- Parsed IEEE C37.118 binary data and displayed decoded packets with real-time plots.

Publications

Implementation of PMU Connection Tester for Synchrophasor Data Analysis
IEEE Peer-Reviewed Conference Paper, IIT Kharagpur IEEE Xplore Publication

Education

Bachelor of Technology (B.Tech) – Electronics and Communication Engineering
University of Kashmir 2016 – 2020
CGPA: 8.13 / 10