Faizan Feroz

Senior Software Engineer — C++ — Embedded Linux — Qt — Automotive Systems
faizanbhatt427@gmail.com +91 7006530565 faizan427.github.io github.com/faizan427 linkedin

Technical Skills

Programming Languages: C++11/14, C, Python, Bash, CMAKE, STL, Multithreading, IPC, TCP/IP, UDP.
Frameworks & Tools: Qt, QML, Octave, PyTorch, Git, VS Code, AWS.
Platforms: Embedded Linux, ECU-Level Software, RCAR, Qualcomm Automotive Platforms, POSIX, RTOS, QEMU.
Domains: Automotive Software, ADAS, AUTOSAR, Medical Devices, Power Systems, Railways.
Standards: AUTOSAR, MISRA C++, CERT C++, CWE, IEEE C37.118 (COMTRADE, Synchrophasor).
Practices: Design Patterns, SOLID, Debugging, Static Analysis, SWE.1–SWE.4, JIRA, Confluence.

Professional Experience

Senior Software Engineer – Automotive Systems
KPIT Technologies (Honda Program) — Pune, Maharashtra Mar 2024 – Present

- Develop and maintain production-grade C++ software for automotive ECUs in Linux environments.
- Design and implement ADAS-aligned system-level components following AUTOSAR and MISRA C++ guidelines.
- Perform debugging, static code analysis, root-cause analysis, and validation within structured quality processes.
- Support software integration on RCAR and Qualcomm automotive platforms for production releases.
- Collaborate with OEM stakeholders across the complete software lifecycle from SWE.1 to SWE.4.
- Optimize ECU performance and stability using Katapult profiling and defect analysis reports.
- Utilize Parasoft static analysis tools to ensure compliance with safety and security standards.

Senior Associate – Software Development
GE HealthCare (Sutherland) — Bengaluru, Karnataka Jul 2023 – Feb 2024

- Designed and developed Qt/QML-based UI components for resting ECG medical devices (MAC-5, MAC-7).
- Implemented C++ backend logic supporting clinical workflows in regulated medical environments.
- Contributed to production-grade medical software emphasizing reliability, usability, and compliance.
- Participated in debugging, defect resolution, and controlled release workflows.

Research and Development Engineer
IRCC, IIT Bombay & IISc Bangalore — Mumbai, Maharashtra Feb 2021 – Aug 2023

- Worked on Government of India funded R&D projects sponsored by HSRCL and DMRC.
- Developed Linux-based simulation tools using C++, Python, and Octave for power system analysis.
- Designed and implemented Qt-based C++ applications covering complete front-end and back-end functionality.
- Built numerical models for traction power supply, load flow, and validation of rail systems.

Engineering Projects

High-Speed Rail Traction Power Analysis Software (HSRCL) Private Repository

- Architected a Qt-based C++ application on Linux integrated with Octave numerical models.
- Implemented load flow, short-circuit, and harmonics analysis for high-speed rail systems.
- Designed scenario-based evaluations using railway timetables and route parameters.

Metro Crew Scheduling and Timetabling Optimization (DMRC) Private Repository

- Led a team of 3–4 engineers to design crew scheduling and optimization solutions.
- Developed Python-based optimization models in a Linux environment.
- Delivered constraint-aware and operationally feasible crew schedules.

iCoReader – COMTRADE Data Visualization Tool Source Code

- Developed a C++/Qt desktop application for COMTRADE file parsing and visualization.
- Implemented IEEE C37.118-compliant disturbance data processing for power system analysis.

iTester – PMU Connection Tester Source Code

- Built a C++/Qt tool for real-time PMU data acquisition and synchrophasor visualization.
- Parsed IEEE C37.118 binary data and displayed decoded packets with real-time plots.

Publications

Implementation of PMU Connection Tester for Synchrophasor Data Analysis
IEEE Peer-Reviewed Conference Paper, IIT Kharagpur IEEE Xplore

Education

Bachelor of Technology (B.Tech) – Electronics and Communication Engineering
University of Kashmir 2016 – 2020
CGPA: 8.13 / 10