1. INTRODUCTION to the ASSIGNMENT

ENEL434 Electronics 2

Summary

- Overview
- Important Dates
- UHF Amplifier Design
- Components
- Overview of Microwave Office
- Impedance transformer design

The purpose of these lectures are to give you ideas that you may consider when attempting to meet the assignment requirements.

They are not meant to be prescriptive.

Overview

- In this assignment you will work in **group of two** to **design, build and test** a **narrowband UHF amplifier**
- Each group will be assigned a centre frequency
- You may use microstripline and lumped components
- **AWR Microwave Office (MWO)** will be used for simulation and PCB layout

Important Dates

18 July 2008:	Form teams of two
	Email to Kim Eccleston with CC to partner
8 August 2008:	Detailed circuit design checked
22 August 2008:	PCB layout
8 Sept 2008:	PCBs available for collection
10 Oct 2008:	Demonstration of amplifier
16 Oct 2008:	Submission of group report

Amplifier Design

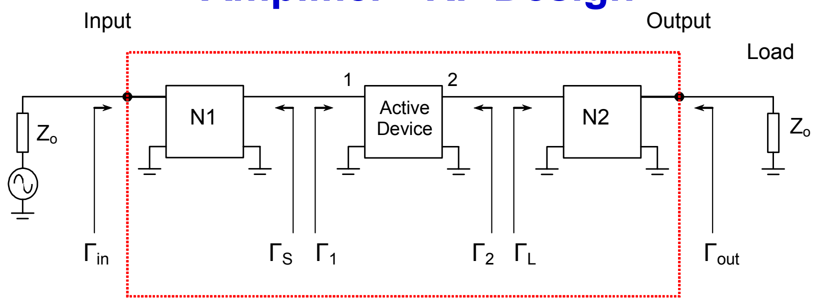
- Design method based upon S-parameters (ie ENEL434)
- Transistor S-parameters obtained from simulation or data sheet
- Impedance transformers and / or matching networks can be designed using the Smith chart
- In this assignment you will be using the **BFR92A** Si NPN RF small-signal transistor

- Most of the design calculations are concentrated at the amplifier centre frequency.
- Simulations are used to establish whether or not the circuit is stable at other frequencies.

Amplifier Design

- There are three main aspects to the design:
  1. Bias circuit design
  2. RF design
  3. Layout
- The first two are often inter-related
- Layout has a bearing on RF performance
- Simulation should be pervasively used throughout
- Conclusion: design is largely an iterative process

Amplifier - RF Design



- N1 and N2 are **lossless** impedance transformers and comprise inductors, capacitors and transmission lines.
- The above circuit is applicable for the RF signals and bias circuitry is either assumed to have negligible effect around the centre frequency or be incorporated into the “active device” 2-port element.
- The S-parameters of the “active device” 2-port are S_{11}, S_{12}, S_{21} and S_{22}.

Amplifier - RF Design

$$\Gamma_1 = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \qquad \Gamma_2 = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S}$$

Available Gain

$$G_A = \frac{P_O}{P_A} = \frac{|S_{21}|^2 \left(1 - |\Gamma_S|^2\right)}{|1 - S_{11}\Gamma_S|^2 - |S_{22} - \Delta\Gamma_S|^2}$$

Power Gain

$$G_P = \frac{P_L}{P_I} = \frac{|S_{21}|^2 \left(1 - |\Gamma_L|^2\right)}{|1 - S_{22}\Gamma_L|^2 - |S_{11} - \Delta\Gamma_L|^2}$$

Transducer Gain

$$G_T = \frac{P_L}{P_A} = \frac{|S_{21}|^2 \left(1 - |\Gamma_S|^2\right)\left(1 - |\Gamma_L|^2\right)}{|(1 - S_{11}\Gamma_S)(1 - S_{22}\Gamma_L) - S_{12}S_{21}\Gamma_S\Gamma_L|^2}$$

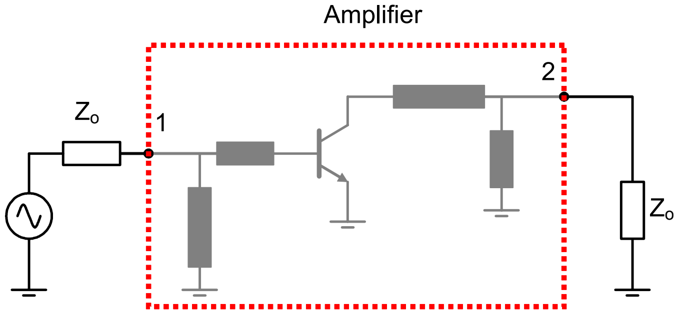
Amplifier - RF Design

Suppose we have an amplifier terminated as shown. The S-parameters of the amplifier are S_{11}, S_{12}, S_{21}, and S_{22}.

What are the values of Γ_S and Γ_L?

What is the transducer gain of this amplifier when terminated as shown?

How is this result useful?



Amplifier - RF Design

- The idea is to select Γ_S and Γ_L so that:
  1. Gain is optimised
  2. Magnitudes of Γ_1 and Γ_2 are both less than unity
  3. Magnitudes of Γ_{in} and Γ_{out} are low
- Non-zero S_{12} may cause $|\Gamma_1| > 1$ for certain values of Γ_L and $|\Gamma_2| > 1$ for certain values of Γ_S.
- S-parameters of transistor are bias dependent.
- S-parameters of transistor and N1 and N2 are frequency dependent.
- **Unconditionally stable** transistor: stable for any value of Γ_S and Γ_L.
- **Conditionally stable** transistor: stable only for certain values of Γ_S and Γ_L.
- A transistor is typically conditionally stable at low frequencies and unconditionally stable above a certain frequency.

Amplifier - RF Design

- **Unconditionally** stable transistor: **use simultaneous conjugate matching** as this maximises gain and both input and output are matched.
- **Conditionally** stable transistor:
  1. **Select Γ_S first** then use **conjugate matching at the output**

     Input mismatched **Output matched**

     N1 is NOT a matching network

     N2 is a matching network

  OR

  2. **Select Γ_L first** then use **conjugate matching at the input**

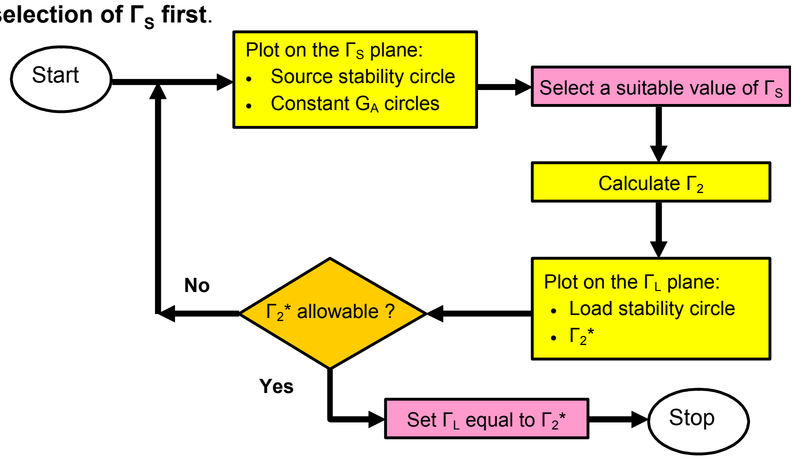
     Input matched **Output mismatched**

     N1 is a matching network

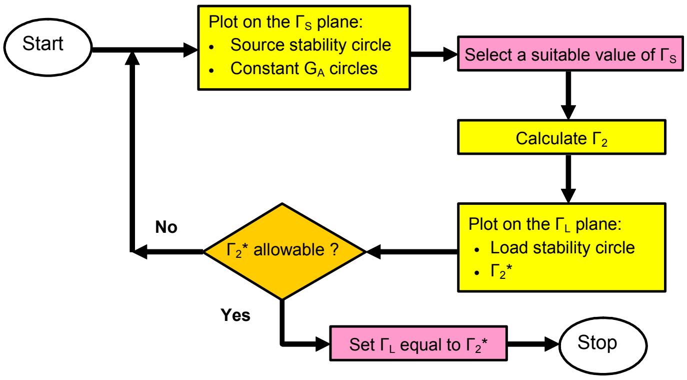
     N2 is NOT a matching network

Amplifier - RF Design

Following **diagram is applicable for a conditionally stable transistor and selection of Γ_S first**.



Amplifier - RF Design



You could trade-off output match to improve match at the input. In which case neither N1 or N2 are matching networks.

There is a complimentary flow chart when Γ_L is chosen first.

Amplifier - RF Design

- You **do not need** to have **unconditional stable transistor** to design an amplifier that works – but it is useful if it is.
- **Suggestion: Select transistor bias so that it is UNCONDITIONALLY STABLE around the centre frequency**. The transistor need not be unconditionally stable at all frequencies.
- You **do not need** to have an **unconditionally stable amplifier** – so long it is stable when terminated with a 50 Ω generator and load.

Feeding Bias to RF Transistors

The transistors must be provided with dc bias or they will not work.

But this needs to be done carefully so that:

- **RF signal only goes to the transistor** and not leak into the power supply.
- **DC only goes to the transistor** and not to other parts of the circuit particularly the amplifier ports. **nb. A circuit that sends dc to the ports will NOT be tested.**
- **Bias circuits do not perturb the RF signals**. ie the bias circuitry appears invisible to the RF signal.
- Even though you don't intend operating the amplifier outside its pass-band, the circuit must be **stable at low RF frequencies**. Resistive loading of transistor at low frequencies by bias circuitry can be designed to achieve this.

Feeding Bias to RF Transistors

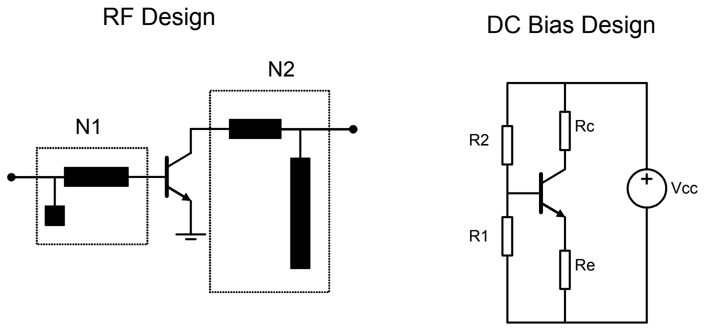
There are basically three options:

1. **Isolate** the bias circuitry at RF
   - Designed to be "invisible" to RF (at centre frequency)
   - Requires extra quarter-wave stubs or RF chokes
   - May cause stability problems

2. **Run bias through** inherent shunt inductances or **short-circuit stubs** of the matching circuits
   - Will appear "invisible" to RF (at centre frequency)
   - Does not require additional elements

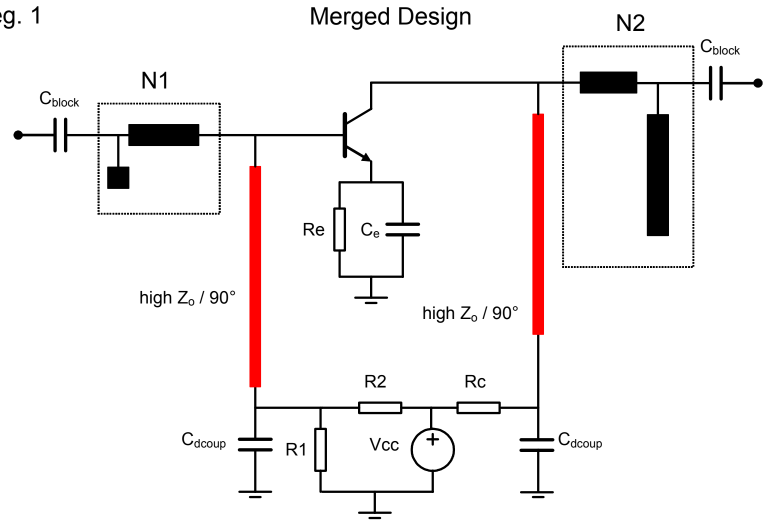
Feeding Bias to RF Transistors

eg. 1



Feeding Bias to RF Transistors

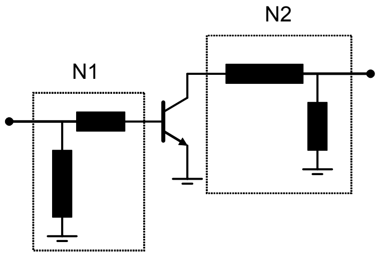
eg. 1



Feeding Bias to RF Transistors

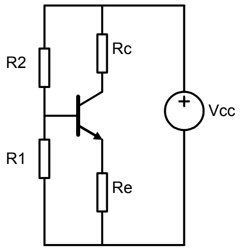
eg. 2

RF Design



Note the inherent presence of short-circuit stubs

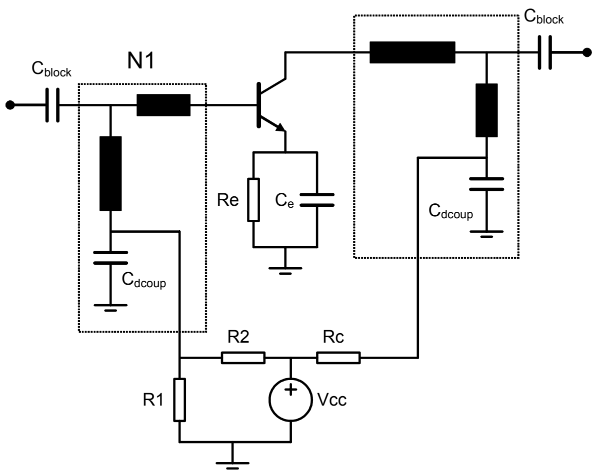
DC Bias Design



Feeding Bias to RF Transistors

eg. 2

Merged Design



Components

Components in this project can be classified into three groups:

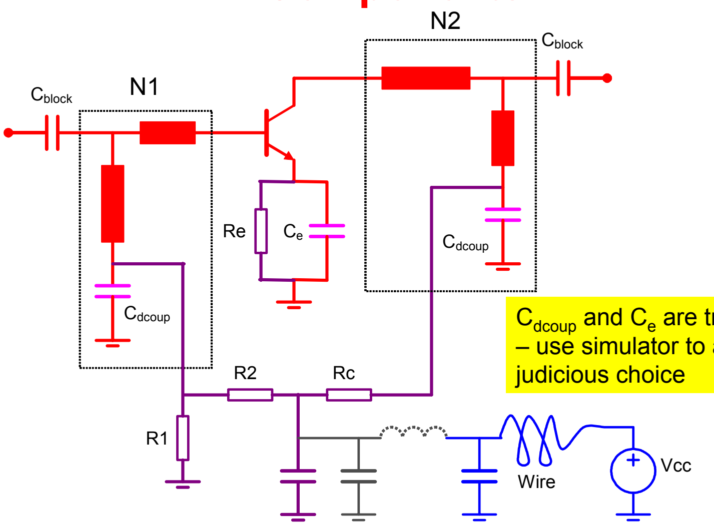
1. Ones that will see the **RF signal** and need to operate at high RF frequencies:
   - Transistor – Use BFR92A
   - Networks N1 and N2 – Use microstripline (stubs and transmission lines);
   - Bias feeding – Use surface mount components

2. Ones that need to operate at **low RF** frequencies:
   - Parts of the bias circuits – Use surface mount components

3. Ones that only see **DC**:
   - Bias circuitry where no RF is expected – Use any component.

The problem is that the distinction between groups 2 and 3 is not obvious. Simulation plays an important role here.

Components



C_{dcoup} and C_e are tricky – use simulator to aid judicious choice

Capacitors

DC block, decoupling and by-pass capacitors must have low parasitic series inductance if they are to have negligible impedance for RF signals.

SURFACE MOUNT / CHIP CERAMIC CAPACITORS – are best for DC blocking, supply decoupling, emitter by-pass, and other places where RF (both low and high frequency) is anticipated.

1206 type parasitic series inductance of about 1 nH – but check data sheet

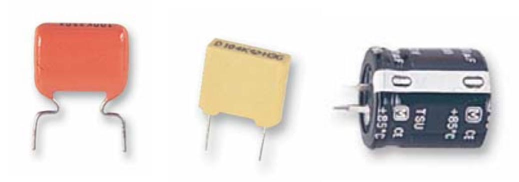
You need to account for parasitic inductance in simulations

DISC CERAMIC are suitable up to 100 MHz (provided leads are cut short) for for non-critical parts of the bias circuitry.

Capacitors

DC block and by-pass capacitors must have parasitic series low inductance if they are to have negligible impedance for RF signals.

POLYESTER / MYLAR and **ELECTROLYTIC** - can be used in the “DC” part of the bias circuitry



Resistors

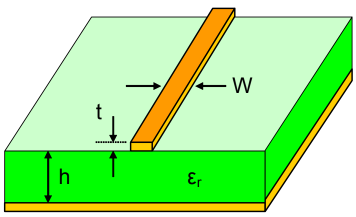
Similarly, resistors that see RF must have low parasitic series inductance if they are to have negligible impedance for RF signals.

CHIP RESISTORS - are best where RF (both low and high frequency) is anticipated.

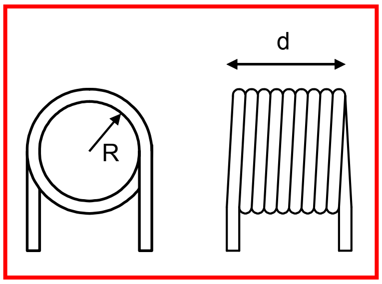
CYLINDRICAL RESISTORS – can be used in the "DC" parts of the bias circuitry.

Microstripline

- Microstripline haves as a transmission line whose behaviour is more predictable than ordinary pcb interconnects.
- Comprises two conductors separated by a dielectric.
- The bottom conductor (ground plane) and covers one side and is grounded.
- The top conductor is floating and forms the interconnects.
- The transmission line parameters (Z_o and v_p) of microstripline are essentially dependent on W, h and ε_r and to a lesser extent t.
- Electrical behaviour is easily be accounted for in Microwave Office.



Inductors



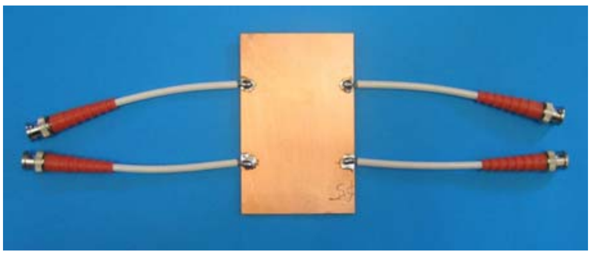
$$L = \frac{10^{-4} N^2 R}{25.4 \frac{d}{R} + 22.9}$$

They will only work as in inductances if:

1. Wire length ($2\pi RN$) is much less than λ.
2. Inter-turn capacitance is small. Which means increasing d.

The above formulae is only approximate. You would not bet your life on it. Only for use below 200 MHz.

BNC Connectors



BNC Connectors

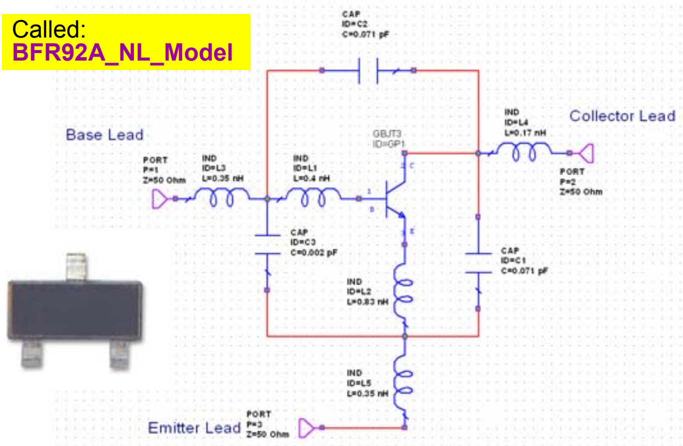
Microwave Office

- Start -> All Programs -> AWR 2006 -> AWR Design Environment
- See WebCT for MWO file examples to get you started. Read "Design Notes" in these files.
- There are two types of simulations that are relevant to ENEL434:
  - Small-signal **AC** analysis (define ports and frequency)
  - DC analysis to check transistor bias
- The simulation will only be as good as the comprehensiveness and accuracy of models used to represent circuit and physical artifacts.
- In RF design simulation is a serious matter and is used to establish whether the circuit will work properly or work diabolically wrong.

Microwave Office

Transistor Large-Signal Model

- Described by a nonlinear model fitted to experimental data.



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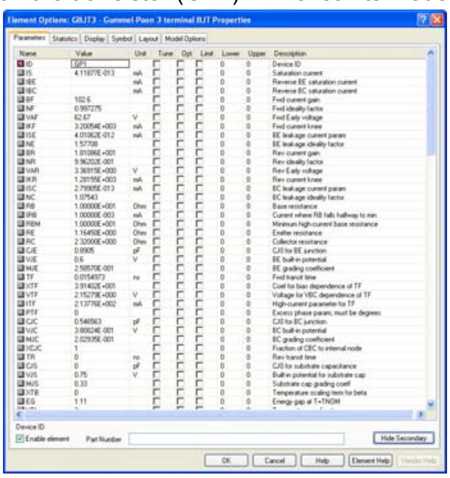
Transistor Large-Signal Model

- Double clicking on the transistor (GP1) will reveal its model parameters:


Element Options: GBJT3 - Gummel Poon 3 terminal BJT Properties

Parameters | Statistics | Display | Symbol | Layout | Model Options

Name	Value	Unit	Tune	Opt	Limit	Lower	Upper	Description
ID	GP1					0	0	Device ID
IS	4.11877E-013	mA				0	0	Saturation current
IBE		mA				0	0	Reverse BE saturation current
IBC		mA				0	0	Reverse BC saturation current
BF	102.6					0	0	Fwd current gain
NF	0.997275					0	0	Fwd ideality factor
VAF	62.67	V				0	0	Fwd Early voltage
IKF	3.20054E+003	mA				0	0	Fwd current knee
ISE	4.01062E-012	mA				0	0	BE leakage current param
NE	1.57708					0	0	BE leakage ideality factor
BR	1.01086E+001					0	0	Rev current gain
NR	9.96202E-001					0	0	Rev ideality factor
VAR	3.36915E+000	V				0	0	Rev Early voltage
IKR	1.20155E+003	mA				0	0	Rev current knee
ISC	2.79905E-013	mA				0	0	BC leakage current param
NC	1.07543					0	0	BC leakage ideality factor
RB	1.00000E+001	Ohm				0	0	Base resistance
IRB	1.00000E-003	mA				0	0	Current where RB falls halfway to min
RBM	1.00000E+001	Ohm				0	0	Minimum high-current base resistance
RE	1.16450E+000	Ohm				0	0	Emitter resistance
RC	2.32000E+000	Ohm				0	0	Collector resistance
CJE	0.8905	pF				0	0	CJ0 for BE junction
VJE	0.6	V				0	0	BE built-in potential
MJE	2.58570E-001					0	0	BE grading coefficient
TF	0.0154973	ns				0	0	Fwd transit time
XTF	3.91402E+001					0	0	Coef for bias dependence of TF
VTF	2.15279E+000	V				0	0	Voltage for VBC dependence of TF
ITF	2.13776E+002	mA				0	0	High-current parameter for TF
PTF	0					0	0	Excess phase param; must be degrees
CJC	0.546563	pF				0	0	CJ0 for BC junction
VJC	3.00024E-001	V				0	0	BC built-in potential
MJC	2.02935E-001					0	0	BC grading coefficient
XCJC	1					0	0	Fraction of CBC to internal node
TR	0	ns				0	0	Rev transit time
CJS	0	pF				0	0	CJ0 for substrate capacitance
VJS	0.75	V				0	0	Built-in potential for substrate cap
MJS	0.33					0	0	Substrate cap grading coeff
XTB	0					0	0	Temperature scaling term for beta
EG	1.11					0	0	Energy gap at T=TNOM

Device ID

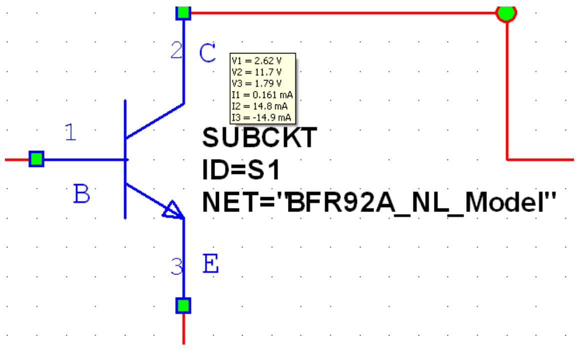
Enable element Part Number Hide Secondary

OK Cancel Help Element Help Vendor Help

Microwave Office

Transistor Large-Signal Model

- The large-signal model is valid for bias simulation, small-signal RF simulation and large-signal RF simulation
- With "Annotation" the bias conditions can easily be obtained.



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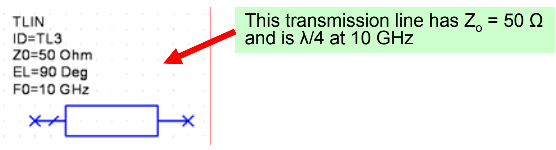
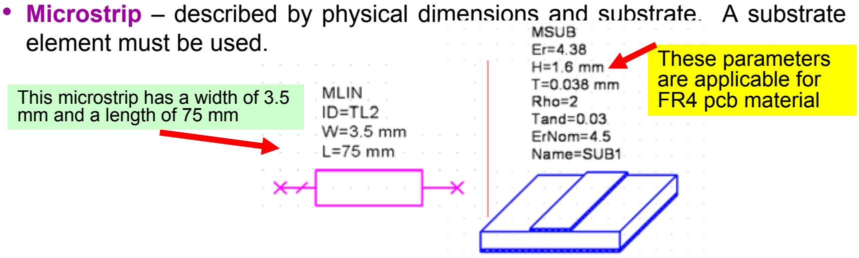
Transmission Lines

There are several types of transmission lines in MWO. The main difference is in the manner that they are described. Here a a few:

- **Electrical** - described by Z_o and phase at a designated frequency.



- **Microstrip** – described by physical dimensions and substrate. A substrate element must be used.



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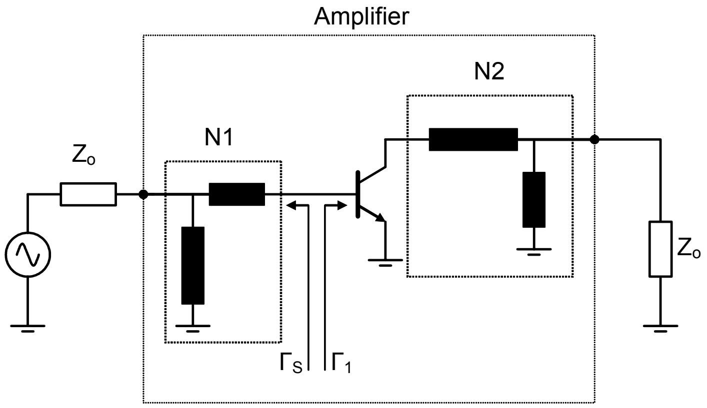
Remember

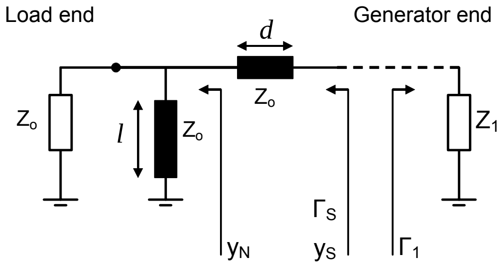
- When using S-parameter data, the actual bias needs to be match the bias conditions under which the S-parameter data file was obtained for the simulation to be valid.
- The MWO file "ENEL434 2008 Transistor Simulation.emp" contains:
  - LS model of BFR92A
  - Substrate model
  - Schematics for transistor S-parameter extraction
  - Footprints of BFR92A and 0805 packages
- To include microstriplines for transmission lines, stubs and interconnects.

Impedance Transformer Design

Consider the realisation of N1

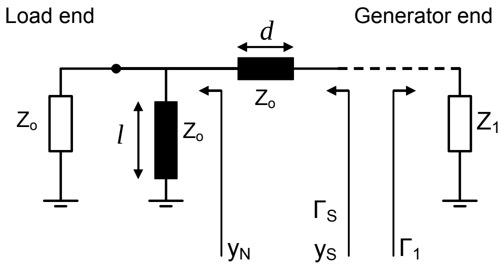


Impedance Transformer Design



- Assume all transmission lines have characteristic impedance Z_o
- Fact 1: Admittances y_S and y_N lie on the same VSWR circle.
- Fact 2: $Re(y_N) = 1$ and $Im(y_N)$ is due to the stub.
- The context of the “Load end” and “Generator end” is for the duration of Smith chart calculations and using the following design sequence.

Impedance Transformer Design

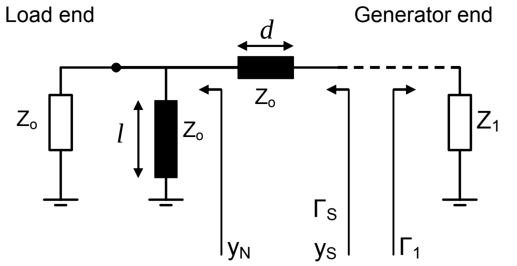


- If we want **conjugate matching at the input:**

  $\Gamma_S = \Gamma_1^*$

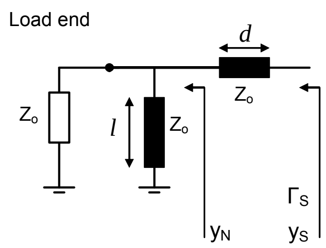
  and N1 is a matching network.
- Otherwise Γ_S could be arbitrary ($\Gamma_S \neq \Gamma_1^*$) to obtain a different outcome. In this case N1 would NOT be a matching network.

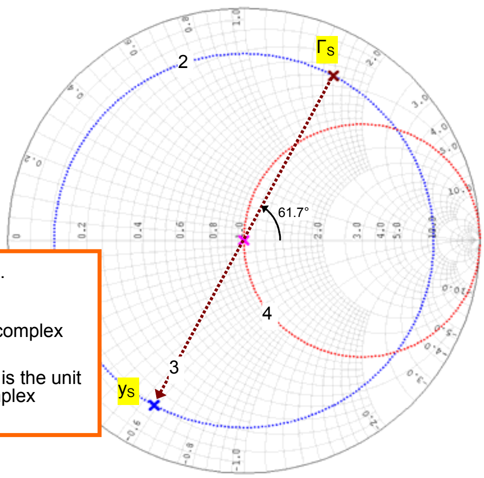
Impedance Transformer Design



- Suppose Γ_1 = 0.804 / -61.7° and we <u>want</u> a matched input.
- Then for conjugate match we want **Γ_S = 0.804 / 61.7°**
- What we are about to design is a circuit that transforms Γ = 0 to $\Gamma = \Gamma_S$ irrespective of whether it is matched to the transistor input. **Γ_S could otherwise have been arbitrary.**

Impedance Transformer Design





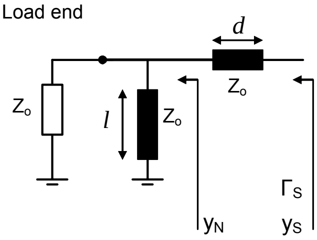
1. Plot Γ_S = 0.804 / 61.7° on Smith Chart.

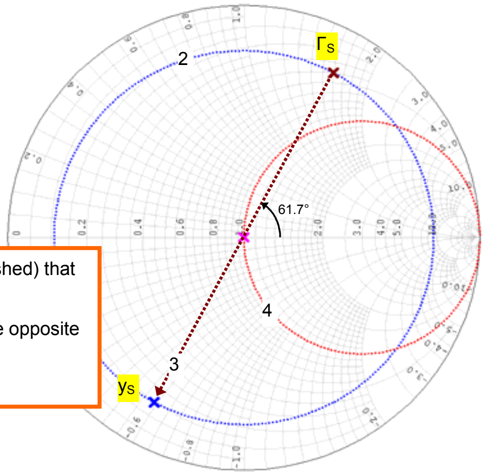
nb: Centre of Smith chart is origin of the complex reflection coefficient plane.

The circumference of the Smith chart is the unit circle centred on the origin of the complex reflection coefficient plane.

Impedance Transformer Design

Load end

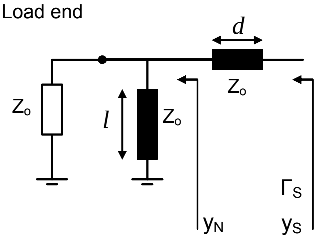


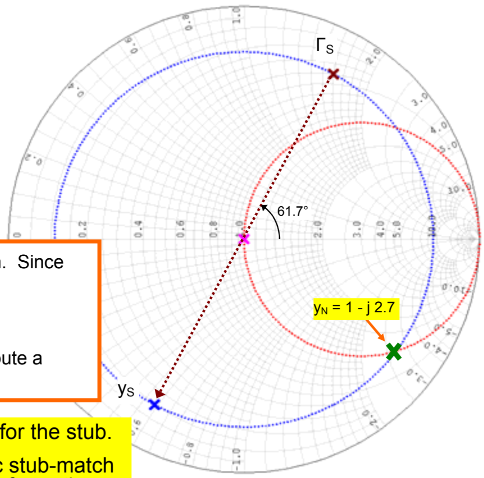


2. Draw constant VSWR circle (blue dashed) that passes through Γ_S
3. Locate point on constant VSWR circle opposite Γ_S. This point is y_S = 0.15 - j 0.59
4. Highlight the g = 1 circle (red).

Impedance Transformer Design

Load end





5. Choose the most suitable intersection. Since we would like a short-circuit stub.

   Choose: y_N = 1 - j 2.7.

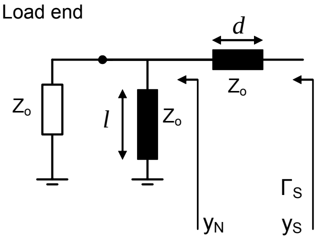
   This means that the stub must contribute a susceptance of -2.7.

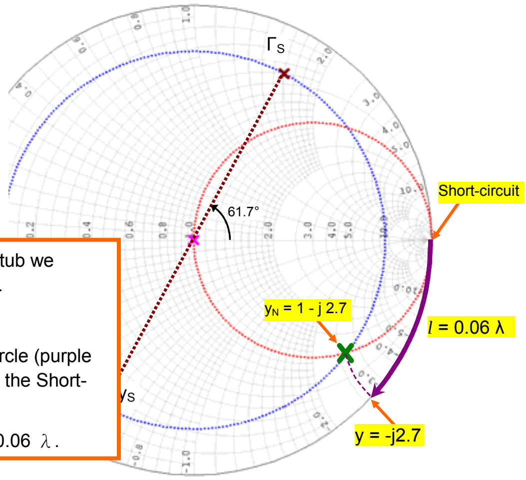
NB: Choose y = -j2.7 and NOT +j2.7 for the stub.

The approach here is NOT the classic stub-match method. It is general impedance transformation.

Impedance Transformer Design

Load end





6. Since we are using a short-circuit stub we should locate the short-circuit point.

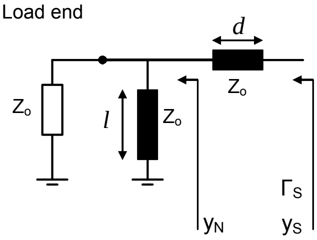
   Locate the point y = -j2.7.

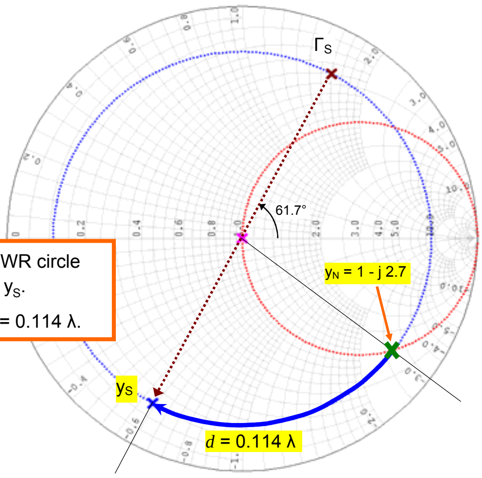
7. Rotate around the infinite VSWR circle (purple line) TOWARD GENERATOR from the Short-Circuit point to the point y = -j2.7.

   Note the angular displacement l = 0.06 λ.

Impedance Transformer Design

Load end





8. Rotate around the blue constant VSWR circle TOWARD GENERATOR from y_N to y_S.

   Note the angular displacement of d = 0.114 λ.

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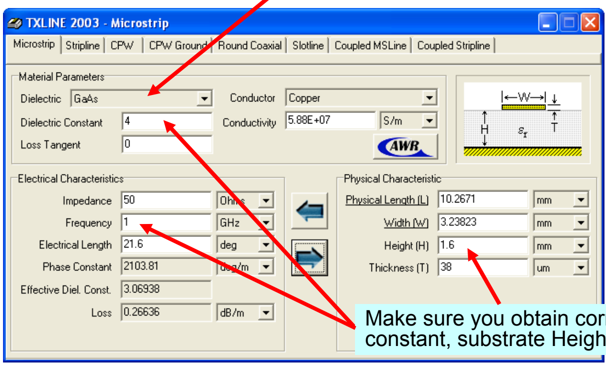
Impedance Transformer Design

- We can use the tool TXLine in MWO to design the microstrips
- Make sure that you use the substrate data applicable in YOUR case
- 1λ corresponds to 360°

Do not worry about name of material



Make sure you obtain correct dielectric constant, substrate Height and frequency.

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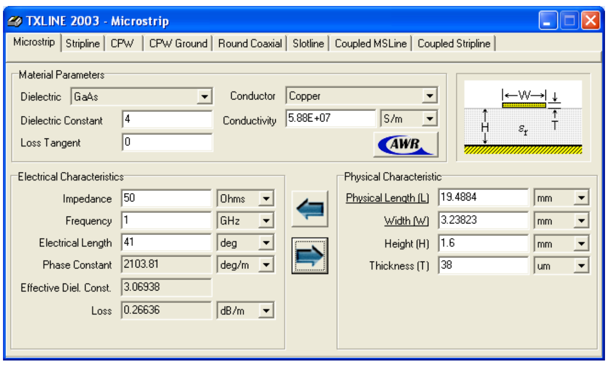
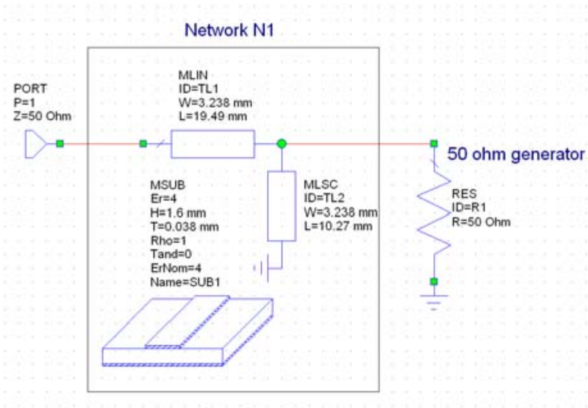
Impedance Transformer Design

- We can use the tool TXLine in MWO to design the microstrips
- Make sure that you use the substrate data applicable in YOUR case
- 1λ corresponds to 360°

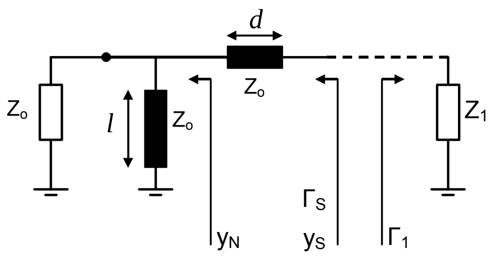


Impedance Transformer Design

- Resulting circuit. Try simulating this in MWO and see that the input reflection coefficient (S11) is the desired value at 1 GHz. Why isn't exactly what we want?

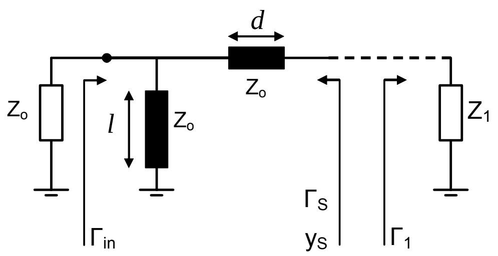


Impedance Transformer Design



- In this example, we have designed N1 to transform $\Gamma = 0$ to $\Gamma_S = \Gamma_1^*$. This is a special case of impedance transformation.
- Matching would only be achieved if $\Gamma_1 = \Gamma_S^*$.
- IF after N1 is implemented, the value of the transistor load (Γ_L) is changed, then the input will be mismatched as Γ_1 is dependent on Γ_L.

Impedance Transformer Design



- We could have designed N1 so that it transforms Γ_1 to $\Gamma_{in} = 0$.
- This approach would be the classic stub-matching method.
- Using this approach, N1 is constrained to be only a matching circuit and we would find that $\Gamma_S = \Gamma_1^*$.
- The solution for N1 would have been exactly the same as above.

Impedance Transformer Design

Remember:

- Only perform matching if you have decided that is what you want.
- Perform impedance transformation ($\Gamma = 0$ to desired value of $\Gamma = \Gamma_S$) for all other cases.
- **Never perform matching** when you have chosen Γ_S to be something other than Γ_1^*.
- Same rules apply at output.
- Γ_1 is function of Γ_L and Γ_2 is function of Γ_S.
- Transistor S-parameters are frequency and BIAS dependent.
- Simultaneous conjugate matching can only be obtained for an unconditionally stable active 2-port (transistor and emitter circuit).
- Simulate N1 and N2 separately to see if they do as you expect.

Remember

- Simulate final circuit layout
- In the CorelDraw layout file, copper tracks must be black (on white background)
- RF circuits cannot be bread-boarded
- RF circuits cannot be tested with conventional laboratory equipment
- RF circuit testing can only be done under supervision using specialised equipment
- It is not possible to modify RF circuitry using jumpers or cutting tracks. Errors can only be corrected by redesign and manufacture
- Adhere to file naming conventions stated in assignment guidelines

References

D. M. Pozar, Microwave Engineering, 3rd Ed., John Wiley, 2005.
[Basic coverage of microwave amplifiers.]

G. Gonzalez, Microwave Transistor Amplifiers: Analysis and Design, 2nd ed. Prentice-Hall, 1997.
[In depth coverage of microwave amplifiers and technology.]