

Assignment Problem:

Build CPU based on following requirements:

1. Word Size of CPU = 6
2. ALU Operations = XOR, ADD, SHR
3. Register Number = 4
4. Size of RAM = 8
5. Word size of ISA and RAM = 18
6. CPU Instructions = Register Mode, Immediate Mode, JMP, JE

Solution:

Simulator Design:

1. ALU Circuit (Top to Bottom all circuits):

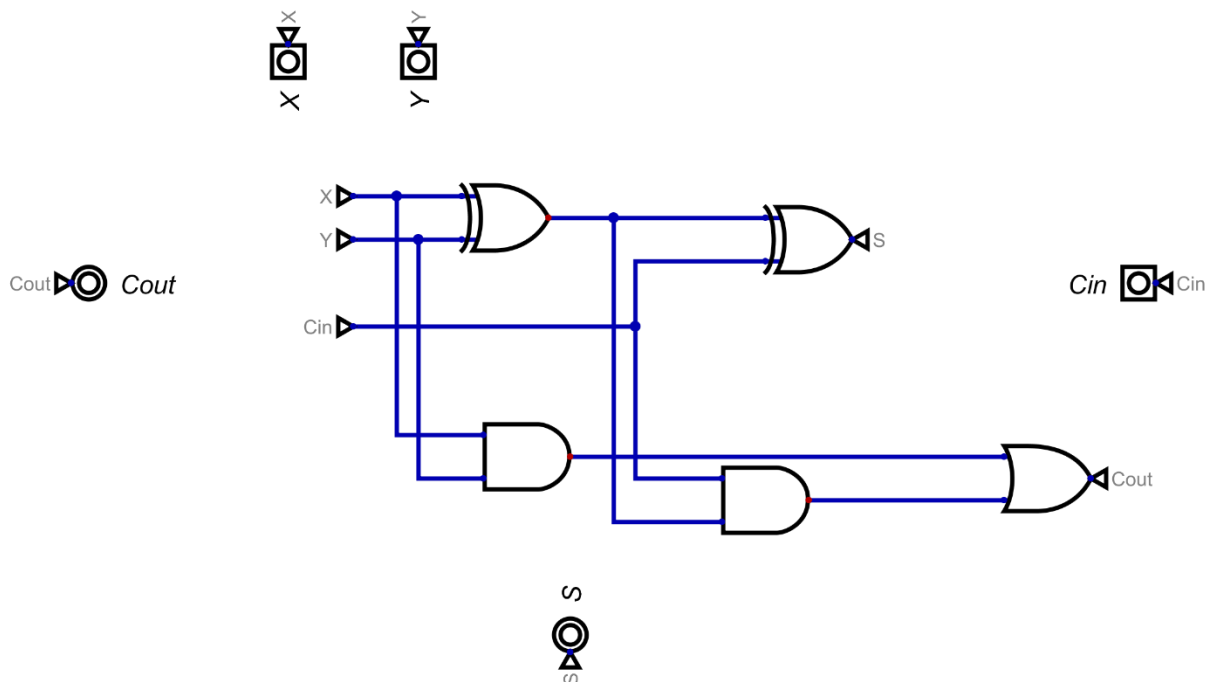


Figure 1: 1bit Full Adder Circuit

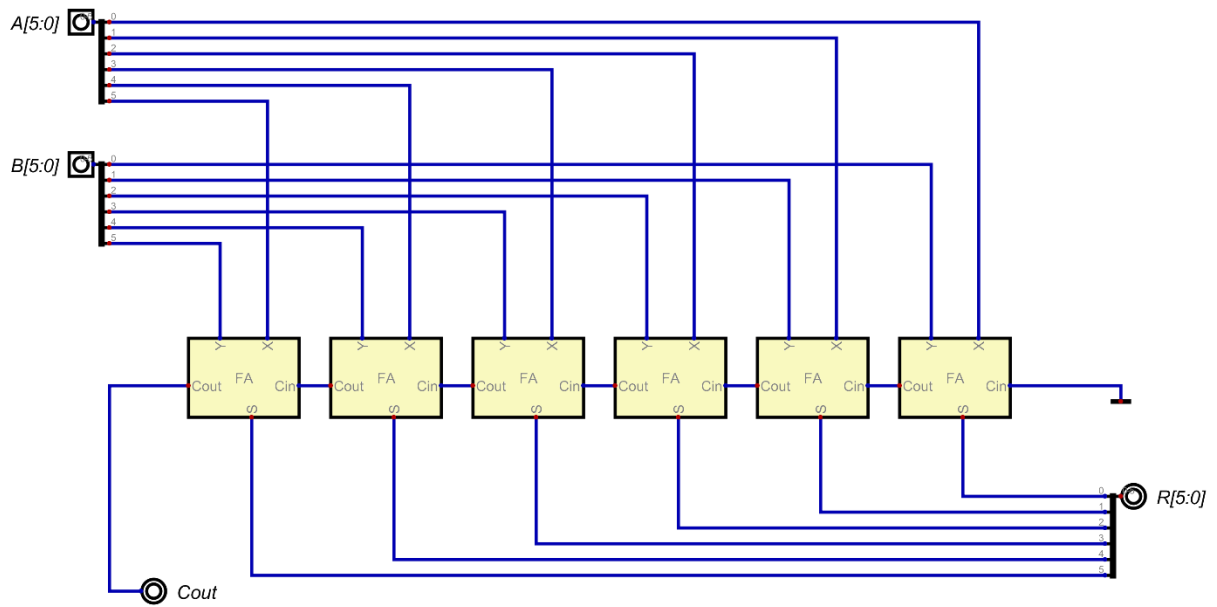


Figure 2: 6bit Adder Circuit

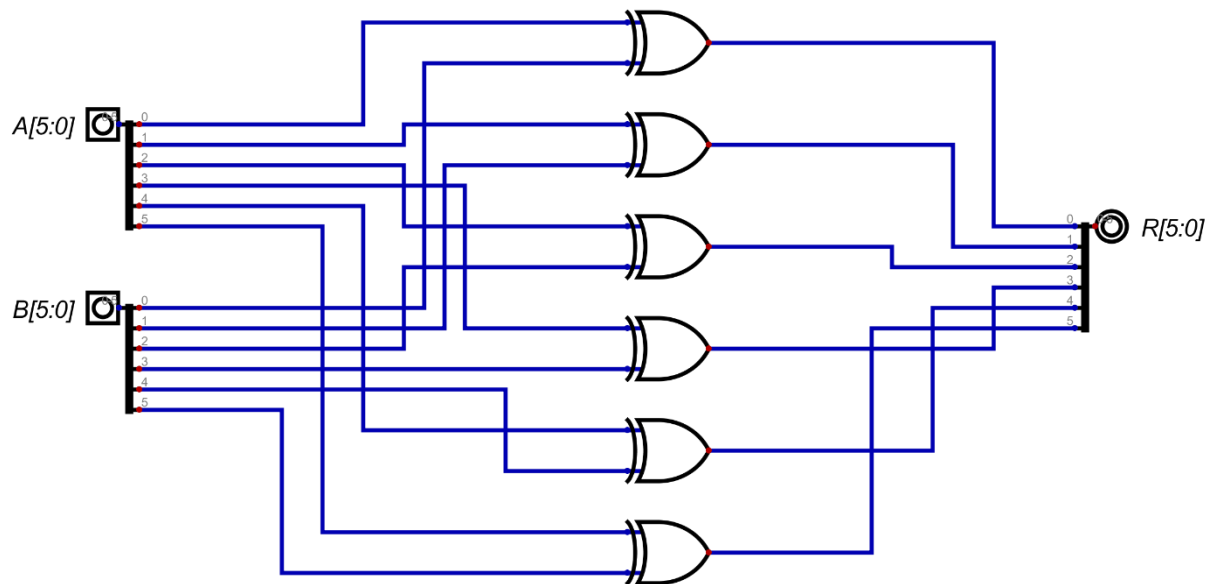


Figure 3: 6bit XOR Circuit

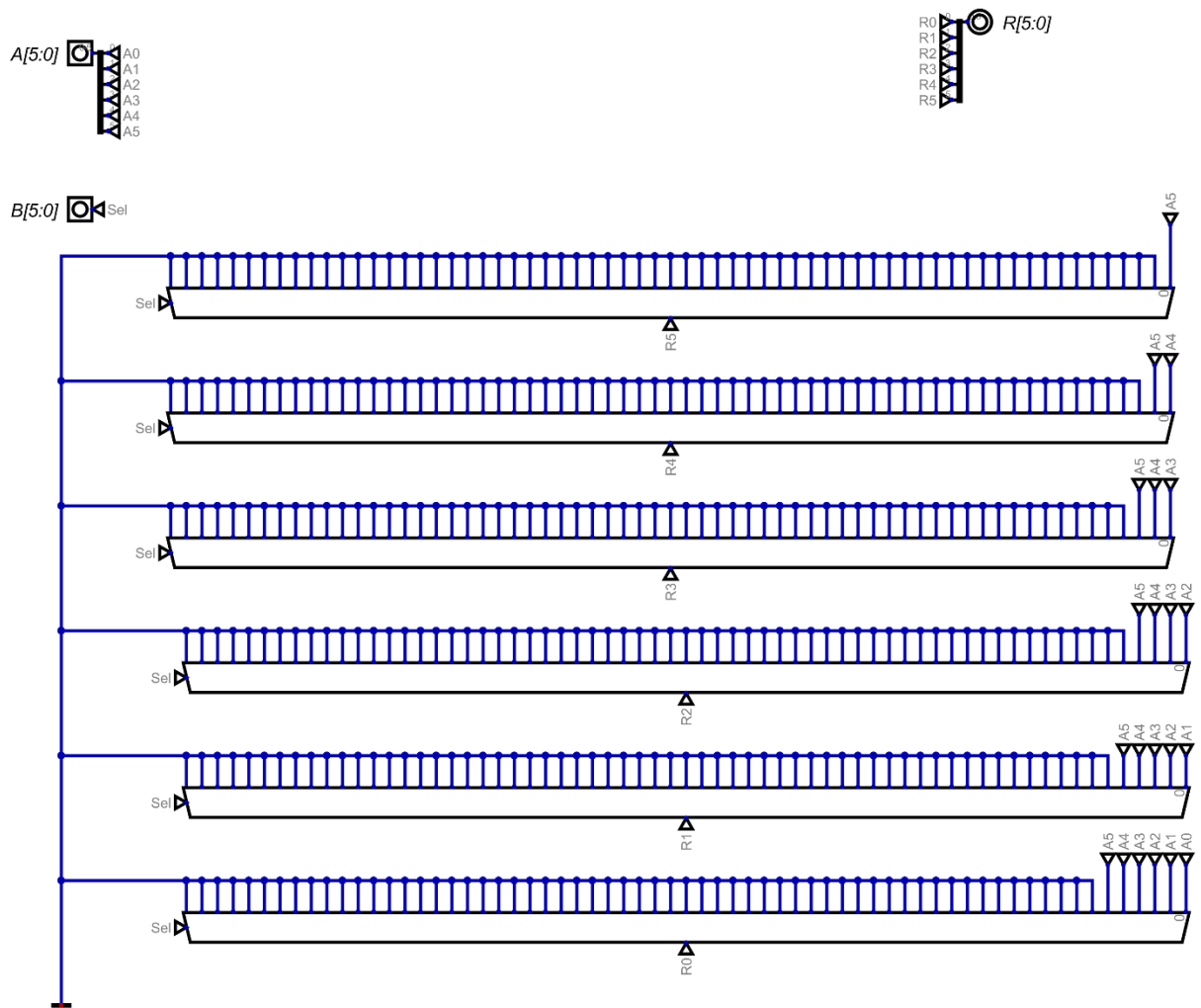


Figure 4: 6bit Right Shifter Circuit

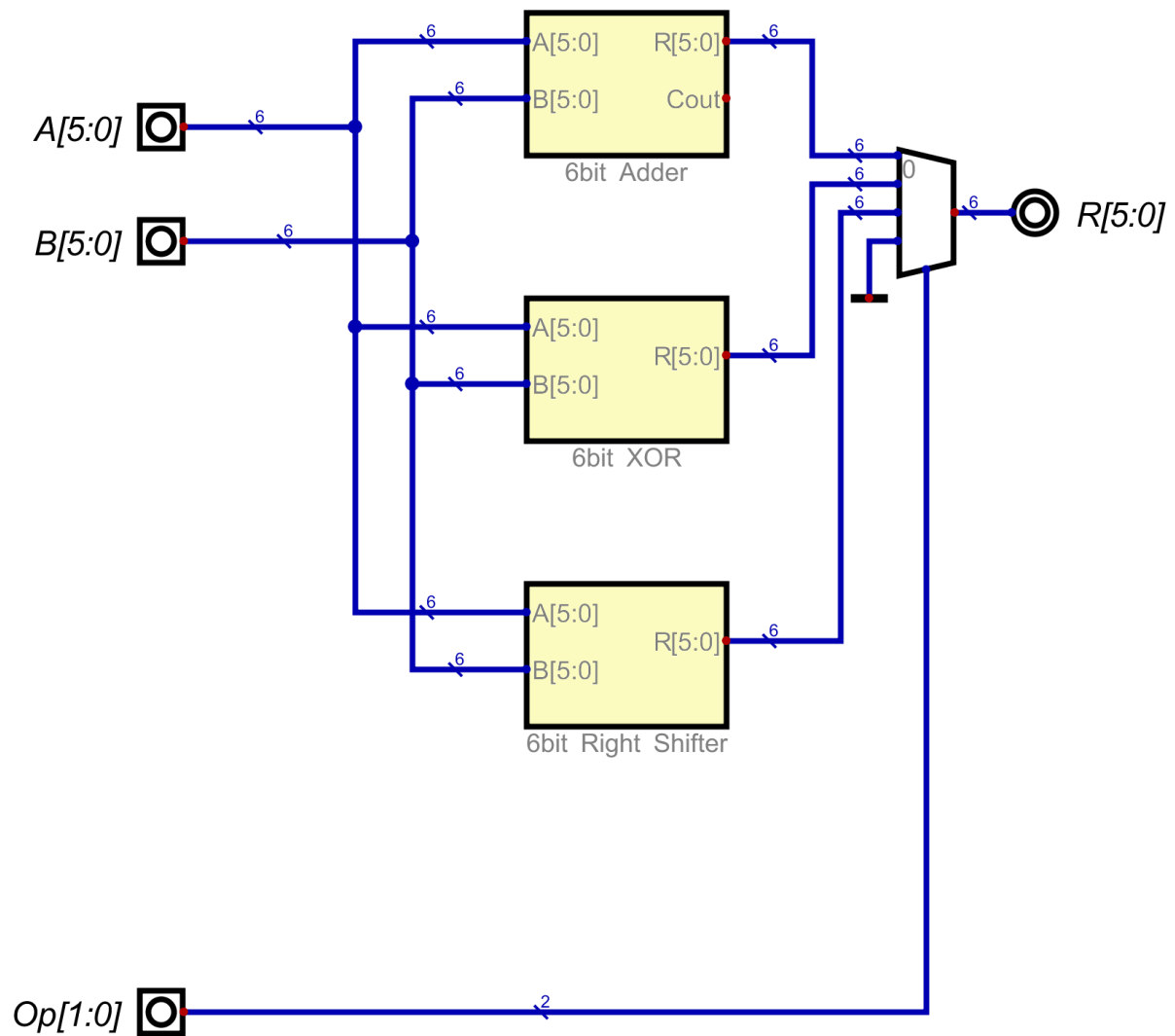


Figure 5: 6bit ALU Circuit

2. Register Set Circuit (Top to Bottom all circuits):

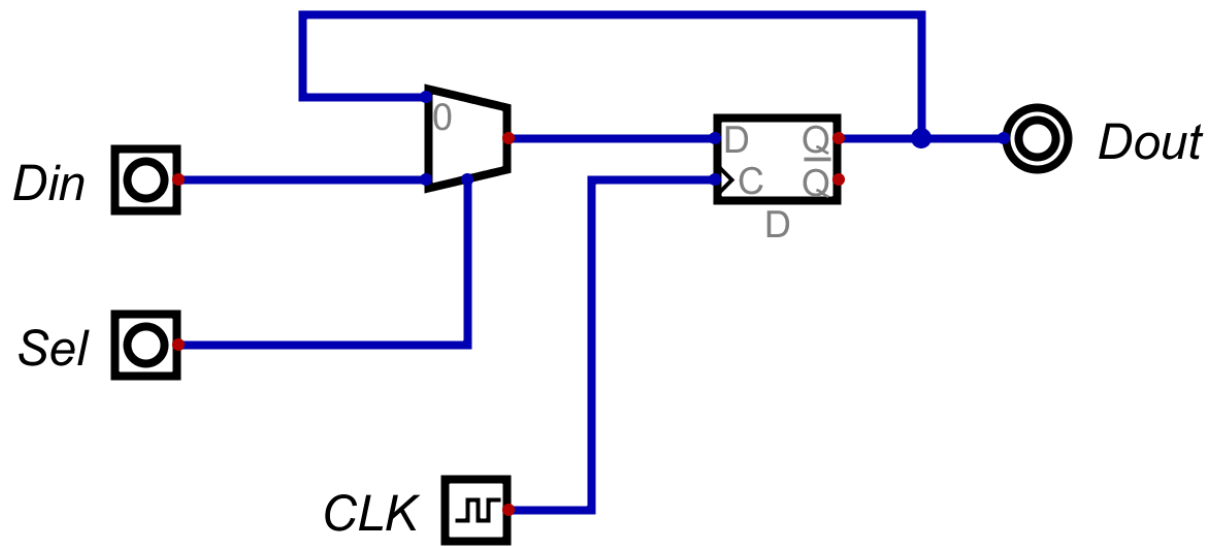


Figure 6: 1bit Register

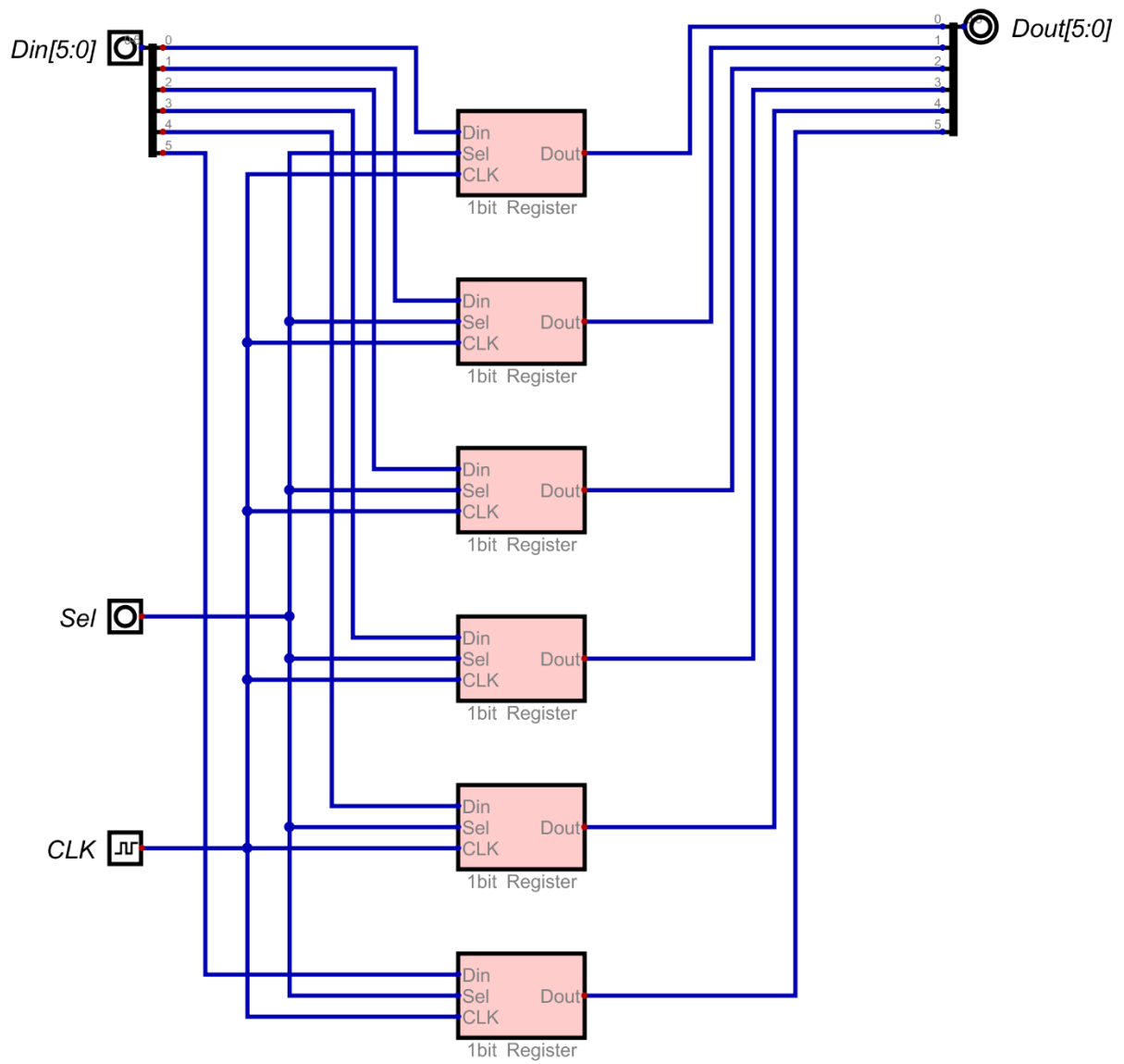


Figure 7: 1x6bit Register

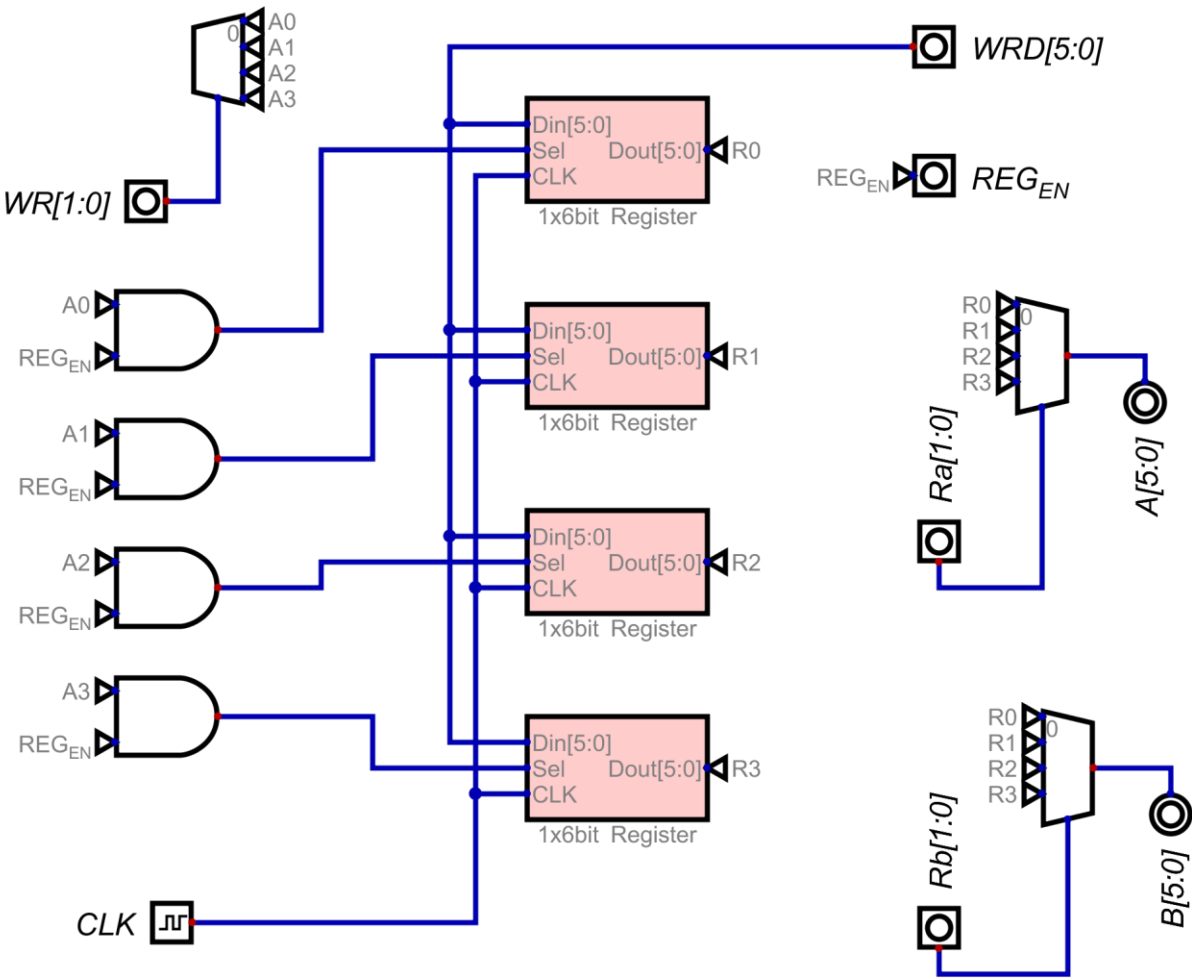


Figure 8: 4x6bit Register Set

3. RAM Circuit (Top to Bottom all circuits):

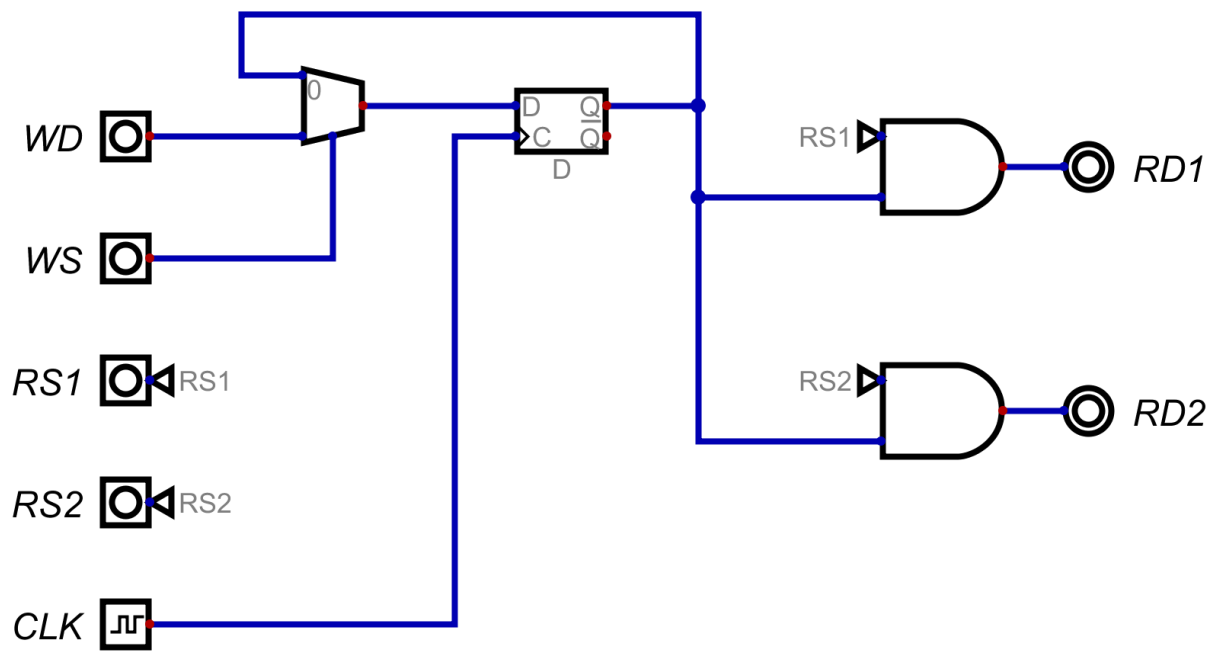


Figure 9: 1x1 SRAM

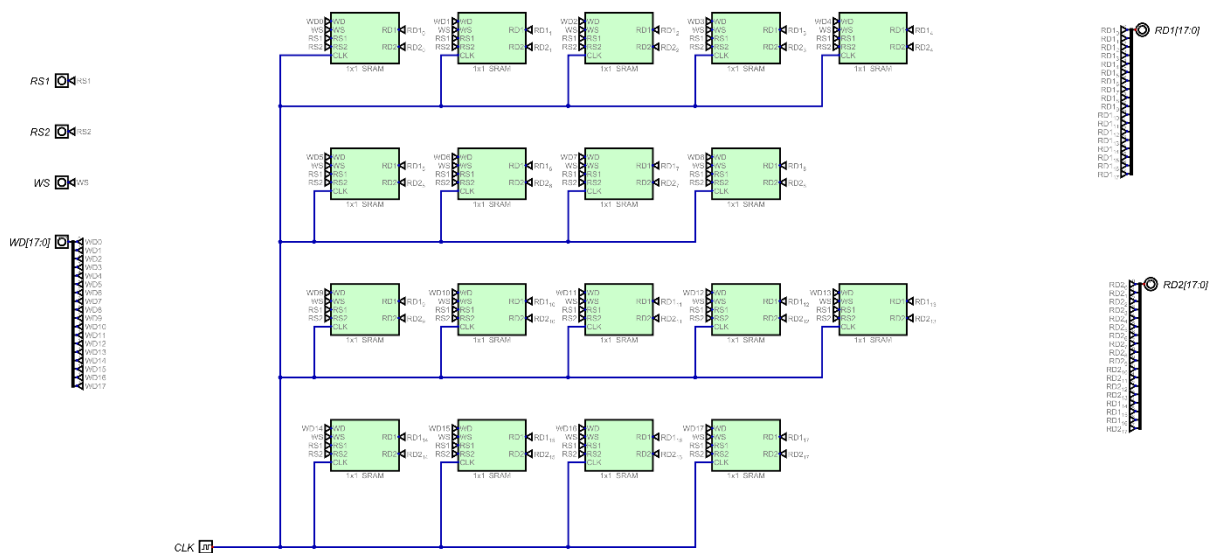


Figure 10: 1x18 SRAM

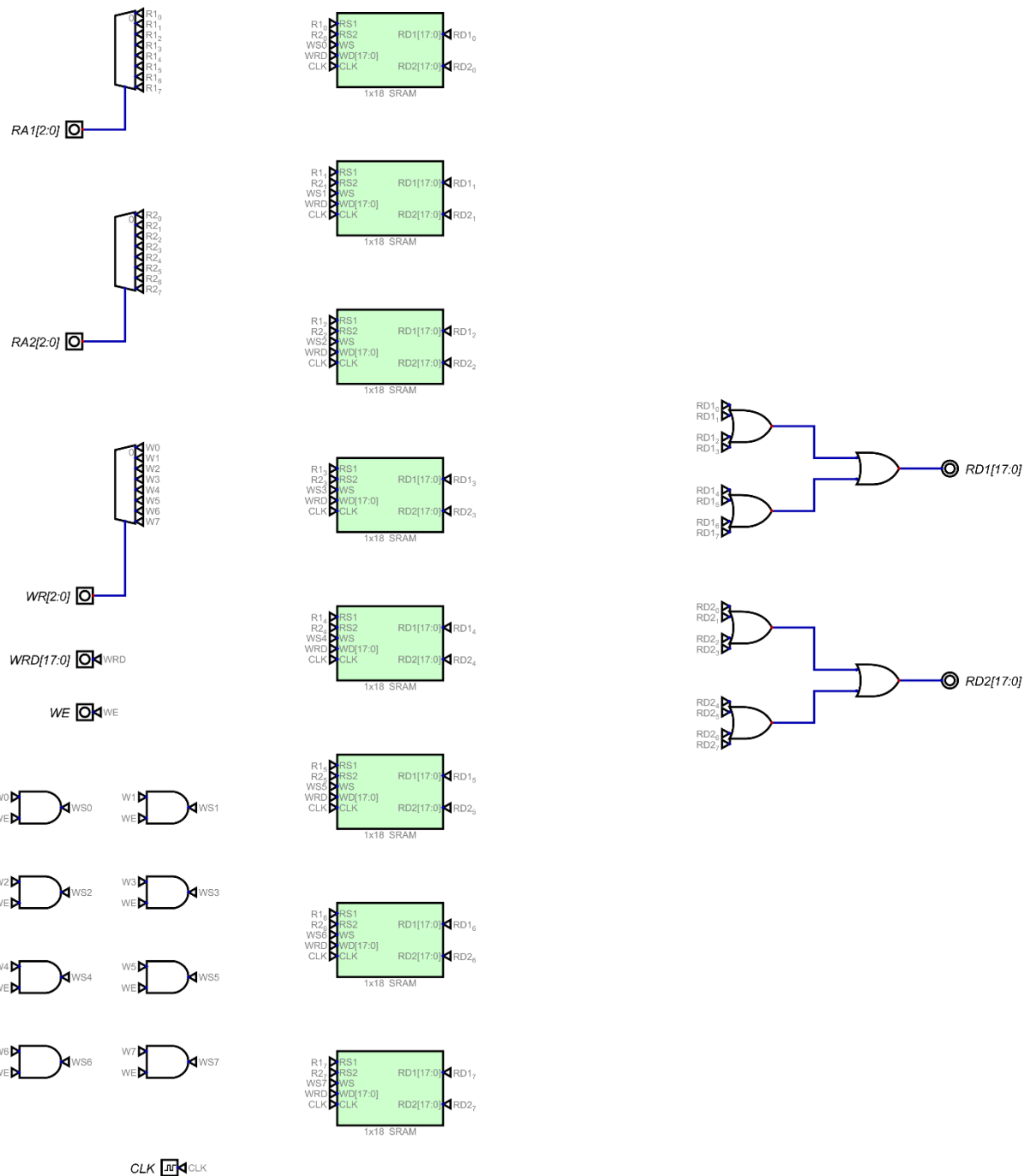


Figure 11: 8x18 SRAM

4. ISA

ISA for 6-bit CPU:

- i) Register Mode (Type of Op = 00) = 2 Bit (Type of OP) + 2 Bit (Operation) + 2 Bit (Reg 1) + 2 Bit (Reg 2) + 10 Bit unused
- ii) Immediate Mode (Type of Op = 01) = 2 Bit (Type of OP) + 2 Bit (Operation) + 2 Bit (Reg 1) + 6-bit data + 6 Bit unused
- iii) Branching Mode (Type of Op = 10) = 2 Bit (Type of OP) + 2 Bit (Operation) + 3 Bit JMP Label + 11 Bit Unused

OP Codes:

ADD = 00

XOR = 01

SHR = 10

JMP = 10 00

JE = 10 01

5. CPU (Top to Bottom all circuits):

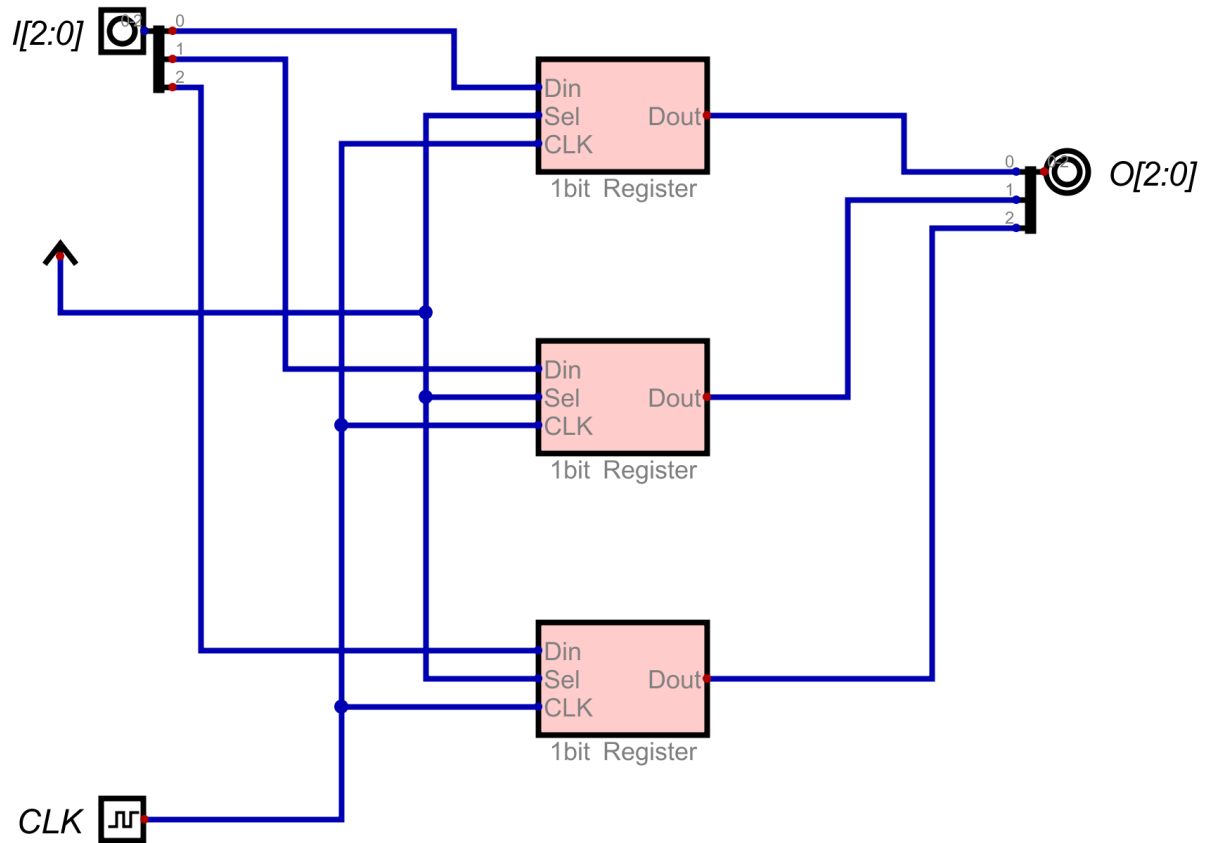


Figure 12: 3bit Program Counter Register

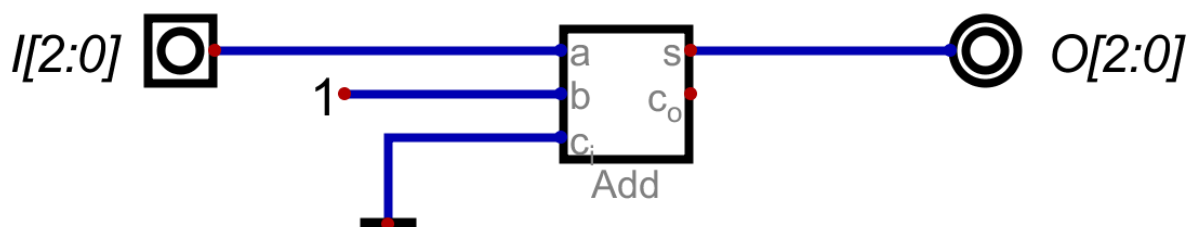


Figure 13: 3bit Program Counter Adder

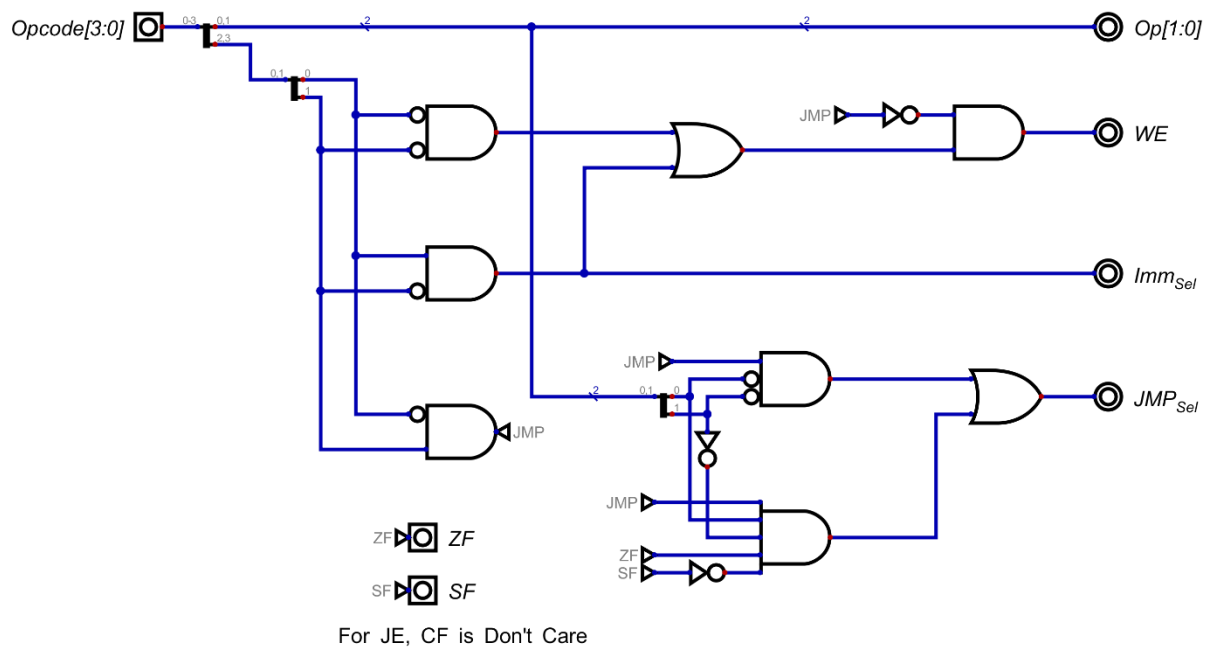


Figure 14: Control Unit

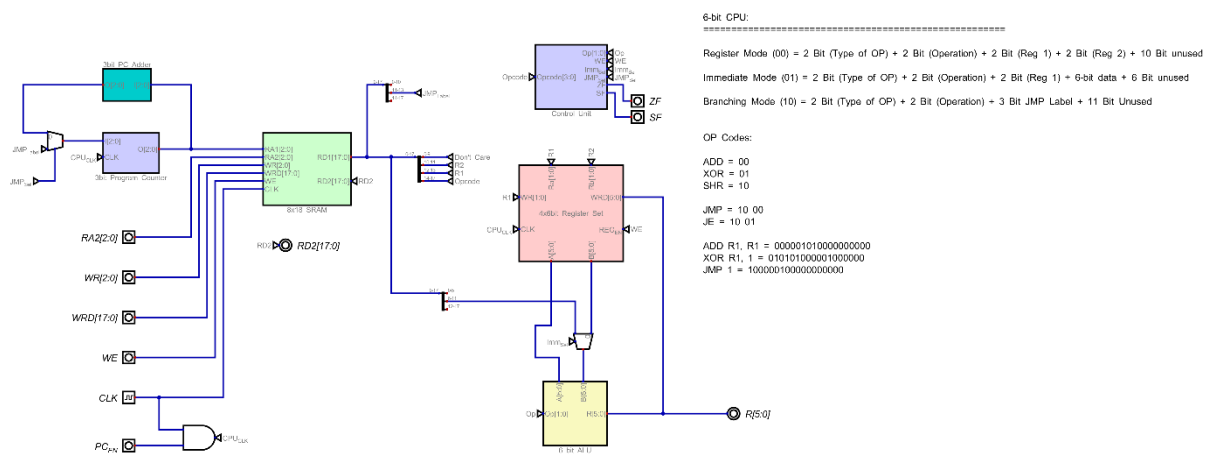


Figure 15: 6bit CPU

Verilog Code:

1. **ALU Circuit (Top to Bottom all circuits):**

2. **Register Set Circuit (Top to Bottom all circuits):**

3. **RAM Circuit (Top to Bottom all circuits):**

4. **CPU (Top to Bottom all circuits):**