CS 2110 Timed Lab 2: Finite State Machines

Your Amazing TAs

Fall 2020

Contents

Please take the time to read the entire document before starting the assignment. It is your responsibility to follow the instructions and rules.

1 Timed Lab Rules - Please Read

1.1 General Rules

1. You are allowed to submit this timed lab starting from the moment the assignment is released, until your individual lab period is over. This means you'll have the full 75 minutes that is reserved for lab - no more and no less (unless you have accommodations or special circumstances that have already been discussed with Professor Southern). Gradescope submissions will remain open but you are not allowed to submit after the lab period is over. **Submitting or resubmitting the assignment after this is a violation of the honor code - doing so will automatically incur a zero on the assignment and might be referred to the Office of Student Integrity.**
2. Although you may ask TAs for clarification in a private Piazza post, you are ultimately responsible for what you submit. **The information provided in this Timed Lab document takes precedence.** If in doubt, please make sure to indicate any conflicting information to your TAs.
3. Resources you are allowed to use during the timed lab:
   - Assignment files
   - Previous homework and lab submissions
   - Class Notes (Open Internet, Open Book)
   - Your mind :)
4. Resources you are **NOT** allowed to use:
   - Email/messaging
   - Contact in any form with any other person besides TAs

1.2 Submission Rules

1. Follow the guidelines under the Deliverables section.
2. You are also responsible for ensuring that what you turned in is what you meant to turn in. After submitting you should be sure to download your submission into a brand new folder and test if it works. No excuses if you submit the wrong files, what you turn in is what we grade. In addition, your assignment must be turned in via Gradescope. Under no circumstances whatsoever we will accept any email submission of an assignment. Note: if you were granted an extension you will still turn in the assignment over Gradescope.
3. Do not submit links to files. We will not grade assignments submitted this way as it is easy to change the files after the submission period ends.

1.3 Is collaboration allowed?

Absolutely NOT. No collaboration is allowed for timed labs.

2 Overview

In this timed lab, you will implement a **One-Hot State Machine** in CircuitSim. This Finite State Machine will take in one 1-bit input (G), and it will output four 1-bit outputs (A, B, C, D). The state machine is a Moore State Machine, where your output is based solely on the current state. Diagrams and detailed instructions are provided below.

3 Instructions

3.1 State Transition Diagram

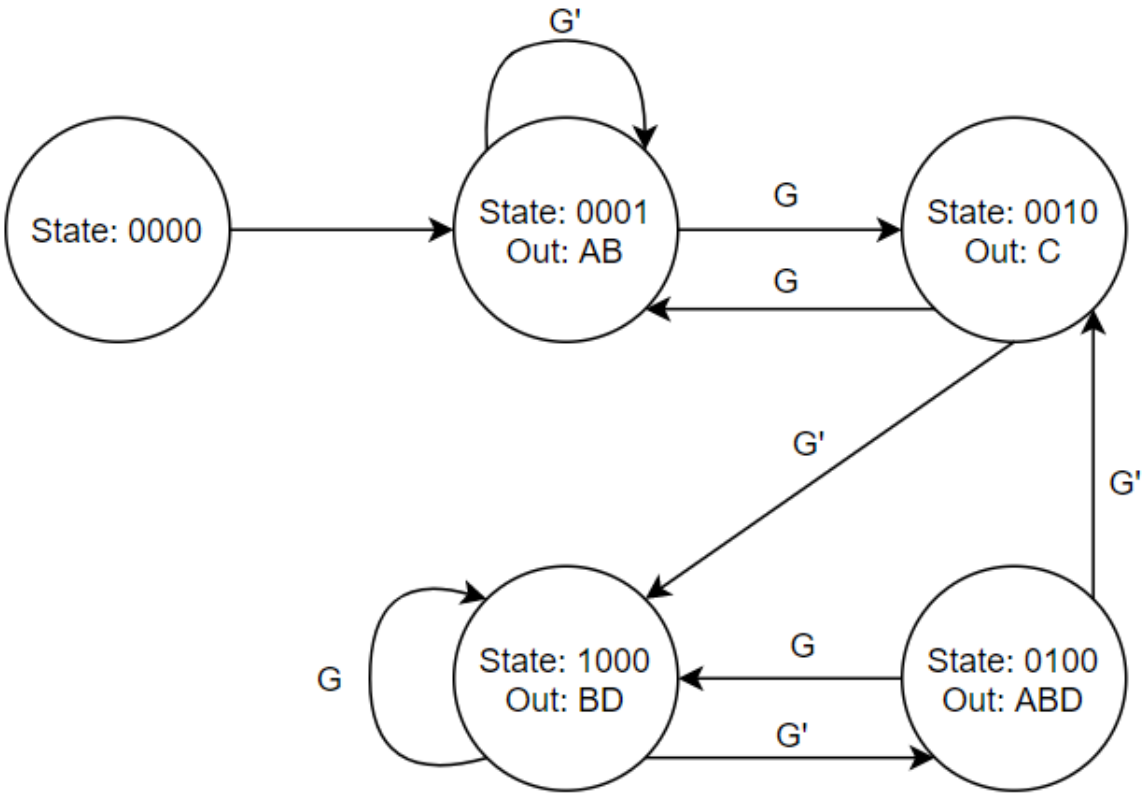

Figure 1: Transition diagram.

3.2 Building the Circuit

Build your circuit using the tl2.sim file provided on CircuitSim. Complete the circuit so that the logic matches the diagram above.

3.3 Restrictions

The input / output pins we have given you in the skeleton file must not be renamed. Do not add any additional input / output pins other than the ones we have given you. Do not rename the sub-circuit we

have given you. If you have issues, check out the "Common Errors" section below.
If you have any questions on what you may not use then assume you can't use it and ask a TA.

You are only allowed to use the following components in CircuitSim:

- Basic logic gates (NAND, NOR, AND, OR, NOT)
- Registers (for this assignment, **exactly ONE**).
- Wires, splitters/joiners, tunnels, constants, plexers

4 Common Errors

Use the autograder's output to determine where you have gone wrong. The names of the tests you fail should usually (but not always) point you in the right direction.
Some common errors and their remedies:

1. Make sure you haven't added extra any input / output pins to your circuit. It is common to confuse constants with input pins, and probes with output pins.
2. Make sure the input / output pins are named the way they were when we gave you the file. If you change the names of the pins (including from upper-case to lower-case, etc), the autograder will not be able to feed input in, and read your circuit's output.
3. Make sure you haven't changed the name of your sub-circuit. Keep it the same as what was given to you.
4. A common cause of short-circuits is two pins (on an AND gate, splitter, etc) being unintentionally connected. These are often hard to spot, since the pins are so close to each other, but if you zoom into your circuit you may find such an error and fix it.
5. Sometimes the bits on your splitter may be not be ordered correctly. For example, if the bits are ordered opposite to what you intended, you may fail all your tests (that depend on the splitter) since for each case, its complementary case is being tested.
6. Make sure the names on your tunnels match. The tunnel labels are case-sensitive, and they do not trim off whitespace. If two tunnels look the same but for some reason they aren't connecting, there may be a "space" hidden in the tunnel's label.

5 Rubric

To run the autograder locally, navigate to the directly containing your timed lab and the tester and run the following command:

```
java -jar tl2-tester.jar
```

The output of the autograder is an approximation of your score on this timed lab. It is a tool provided to students so that you can evaluate how much of the assignment expectations your submission fulfills. However, **we reserve the right to run additional tests, fewer tests, different tests, or change individual tests** - your final score will be determined by your instructors and no guarantee of tester output correlation is given.

6 Deliverables

Please upload the following files to Gradescope:

1. tl2.sim

Download and test your submission to make sure you submitted the right files