Efficient Parallel Implementation of Large-Scale Finite Difference Time Domain Electromagnetic Schemes Using Hash Table and Multicolor Ordering

[1]Toshio Murayama, [1]Kenzo Nishikawa and [2]Shinobu Yoshimura
[1]Production Group, Sony Corporation
5-1-12 Kitashinagawa, Shinagawa, Tokyo 141-0001, Japan
{Toshio.Murayama, Kenzoh.Nishikawa}@jp.sony.com
[2]Department of Systems Innovation, The University of Tokyo
7-3-1 Hongo, Bunkyo, Tokyo 113-8656, Japan
yoshi@sys.t.u-tokyo.ac.jp

Abstract— Fast and memory efficient parallel implementation of finite difference time domain electromagnetic schemes such as FDTD and FIT is introduced. Our implementation utilizes a coefficient hash table and optimal ordering of *E* and *H* field updates on a multi-core processor to decrease the number of load and save operations between a memory unit and CPU for effective use of limited memory bandwidth and cache. The same approach can be applied to the similar scheme like Latency Insertion Method (LIM). Experimental results show the efficiency of our implementation.

I. Introduction

While time domain electromagnetic algorithms such as FDTD are versatile algorithms [1], vast amount of computational resources are required to accurately model the electromagnetic behavior for volumetrically structures. We suggest a novel time-domain implementation which uses a hash table to save required memories, and optimizes cache reutilization by simultaneous *E* and *H* field updates resulting in a fast and memory effective algorithm.

II. Formulation

Conventional 3D FDTD Field updating formulation is described as follows:

$$E_x^n(i,j,k) = \frac{1-\frac{\sigma\Delta t}{2\varepsilon}}{1+\frac{\sigma\Delta t}{2\varepsilon}} E_x^{n-1}(i,j,k) + \frac{\frac{\Delta t}{\varepsilon}}{\Delta z\left(1+\frac{\sigma\Delta t}{2\varepsilon}\right)}\left[H_y^{n-\frac{1}{2}}(i,j,k-1) - H_y^{n-\frac{1}{2}}(i,j,k)\right] + \frac{\frac{\Delta t}{\varepsilon}}{\Delta y\left(1+\frac{\sigma\Delta t}{2\varepsilon}\right)}\left[H_z^{n-\frac{1}{2}}(i,j,k) - H_z^{n-\frac{1}{2}}(i,j-1,k)\right] \quad (1)$$

where $E_x^n(i,j,k)$ is an electric field in *X*-direction at time step *n* and location *(i,j,k)*. The other field elements are similarly formulated. Here, the data transfer between a memory unit and CPU is 8 loads ($E_x^{n-1}(i,j,k)$, the coefficients and *H fields*) and 1 store ($E_x^n(i,j,k)$) of floating point values. 7 floating point operations are performed. We re-formulate the above expression as (2).

Moreover, we make a hash table for $1-\frac{\sigma\Delta t}{2\varepsilon}$ and $1+\frac{\sigma\Delta t}{2\varepsilon}$. With this implementation, the number of data transfer decreases to 4 floating point values and 1 hash key load, and 1 store. The number of floating point operation is 6. Using the hash table, we can save required memory for the coefficients by 60 percent.

$$\Delta x E_x^n(i,j,k) = \frac{1-\frac{\sigma\Delta t}{2\varepsilon}}{1+\frac{\sigma\Delta t}{2\varepsilon}} \Delta x E_x^{n-1}(i,j,k) + \frac{\Delta x\frac{\Delta t}{\varepsilon}}{\Delta y\Delta z\left(1+\frac{\sigma\Delta t}{2\varepsilon}\right)}\left[\Delta y H_y^{n-\frac{1}{2}}(i,j,k-1) - \Delta y H_y^{n-\frac{1}{2}}(i,j,k) + \Delta z H_z^{n-\frac{1}{2}}(i,j,k) - \Delta z H_z^{n-\frac{1}{2}}(i,j-1,k)\right] \quad (2)$$

III. Multicolor Ordering

Our algorithm simultaneously updates *E* and *H* fields to utilize newly updated field data during residing in a cache as follows:

```
Do i, j, k loop
    Update E(i,j,k)
    Update H(i-1,j-1,k)
Enddo
```
(3)

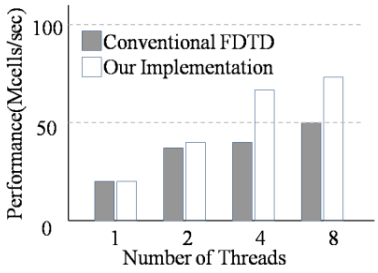

Fig.1. Performance comparisons between conventional FDTD and new implementation

IV. Numerical Results

Fig. 1 depicts the performance comparisons between the conventional FDTD and our implementation with multiple threads on Xeon 5482 at 3.2GHz. Our implementation shows excellent linearity and performance while the conventional FDTD saturates due to a memory bandwidth bottleneck.

V. References

[1] D. Orozco and G. Gao, "Mapping the FDTD Application to Many-Core Chip," *2009 International Conference on Parallel Processing*, pp. 309 – 316, September 2009.

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