NC State University

Department of Electrical and Computer Engineering

ECE 463/521: Fall 2015 (Rotenberg)

Project #3: Dynamic Instruction Scheduling

by

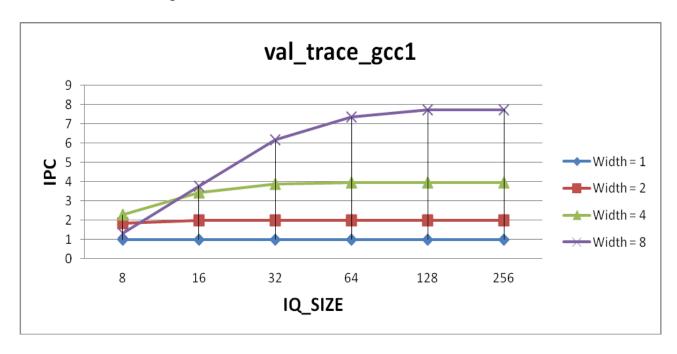
<< FALAK VIJAY RAVANI >>

NCSU Honor Pledge: "I have neither given nor received unauthorized aid cassignment."	on this test or
Student's electronic signature: Falak Vijay Ravani (sign by typing your name)	
Course number:521	

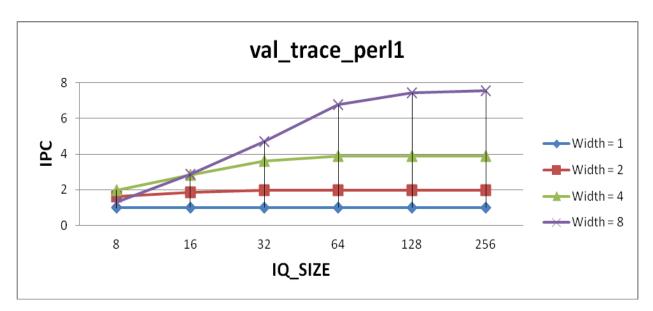
1) Large ROB, effect of IQ_SIZE

GRAPHS:-

a) val_trace_gcc1



b) val_trace_perl1



GRAPH ANALYSIS:-

	"Optimized IQ_SIZE per WIDTH" Minimum IQ_SIZE that still achieves within 5% of the IPC of the largest IQ_SIZE		
	val_trace_gcc1	val_trace_perl1	
$\mathbf{WIDTH} = 1$	8	8	
$\mathbf{WIDTH} = 2$	16	32	
$\mathbf{WIDTH} = 4$	32	64	
$\mathbf{WIDTH} = 8$	128	128	

DISCUSSION:-

The goal of a superscalar processor is to achieve an IPC that is close to its WIDTH. From the graphs, we can observe that for a particular WIDTH, as we go on increasing the IQ_SIZE, the IPC approaches WIDTH. For a particular WIDTH, there can be two bottlenecks. ROB_SIZE and IQ_SIZE. BY making ROB_SIZE sufficienty large, we have discarded the possibility of ROB_SIZE being the bottleneck.

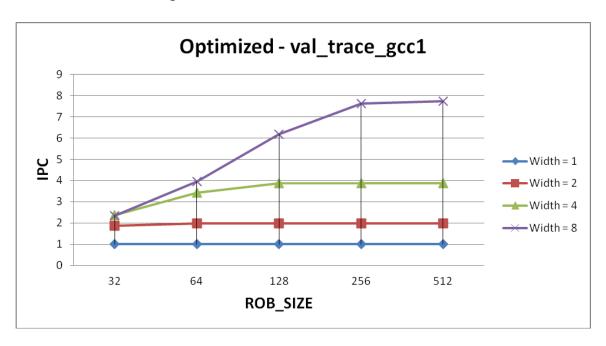
Now, when the WIDTH is big but IQ_SIZE is small, we oberve that IPC is very low as compared to the width. As we go on increasing the IQ_SIZE, the graph grows steeply and approaches WIDTH. This is because of the fact that even if the processor can fetch a significant number of instructions in a given cycle, the Issue queue is not large enough to accommodate them. Hence, they are stalled and IPC is less.

Yes, some benchmarks do show higher or lower IPC than other benchmarks for the same microarchitecture configuration. This is due to the fact that different benchmarks have different set of instructions with different latencies and dependencies. A benchmark whose instructions have less dependency as compared to other benchmarks will show a higher IPC. Also, if the latency is low, the instructions spends less time in Execute stage and hence, more number of instructions can be passed through the pipeline for unit time.

2) Effect of ROB_SIZE

GRAPHS:-

a) Val_trace_gcc1



b) val_trace_perl1

