**DMA INTRODUCTION**

Direct memory access (DMA) is a method that allows an input/output (I/O) device to send or receive data directly to or from the main memory, bypassing the CPU to speed up memory operations. The process is managed by a chip known as a DMA controller (DMAC).

A defined portion of memory is used to send data directly from a peripheral to the motherboard without involving the microprocessor, so that the process does not interfere with overall computer operation.

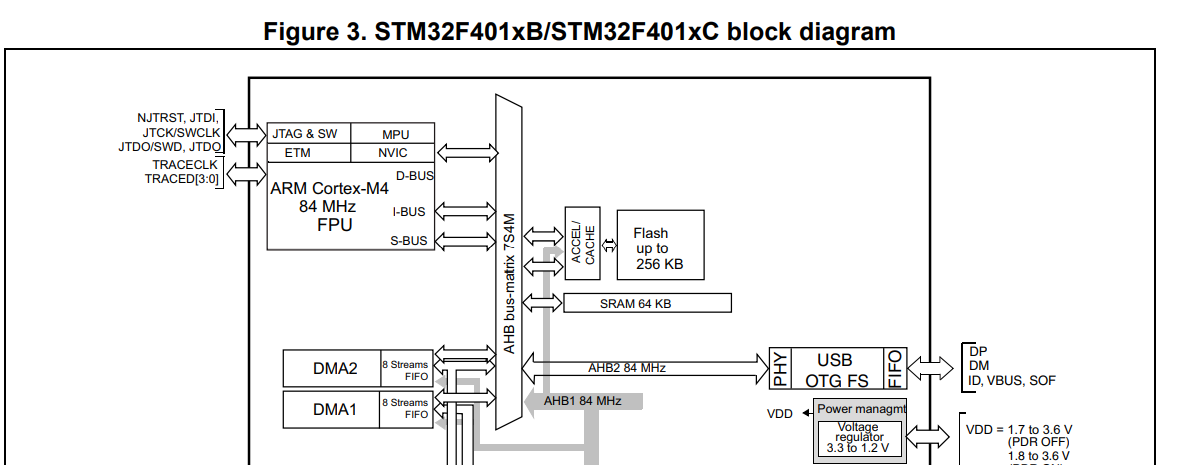
* During this operation, the main processor can execute other tasks and it is only interrupted when a whole data block is available for processing.
* Large amount of data can be transferred with no major impact on the system performance.

**DMA – Transfer properties**

* DMA STREAM / CHANNEL
* Stream priority
* Source and destination address
* Transfer mode
* Transfer size
* Source / destination data width
* Transfer type
* FIFO mode
* Source / destination burst size
* Double- buffer mode
* Flow control

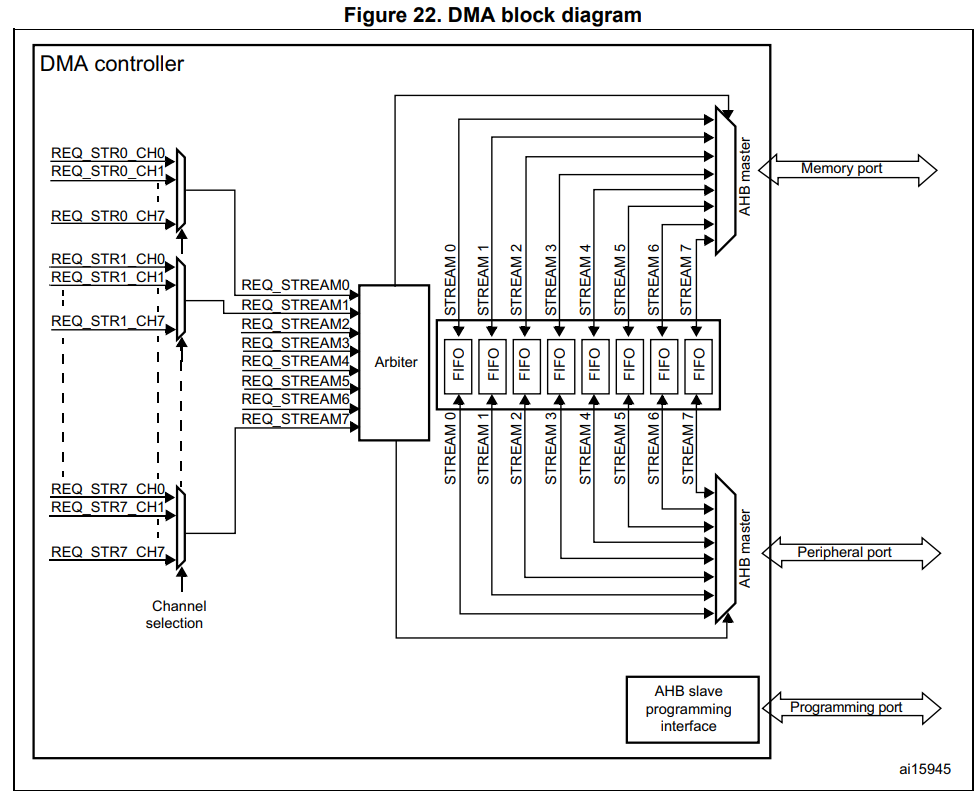
**Stm32f401 has two DMA ports:**

DMA\_1 and DMA\_2 are directly connected with AHB1.

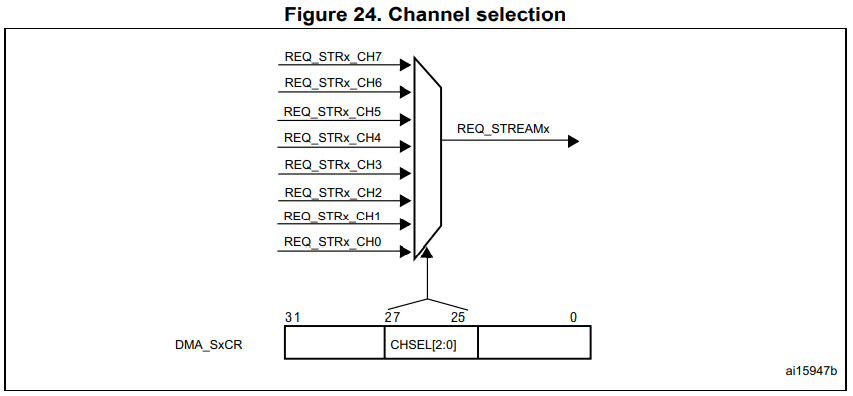


**DMA block diagram**:

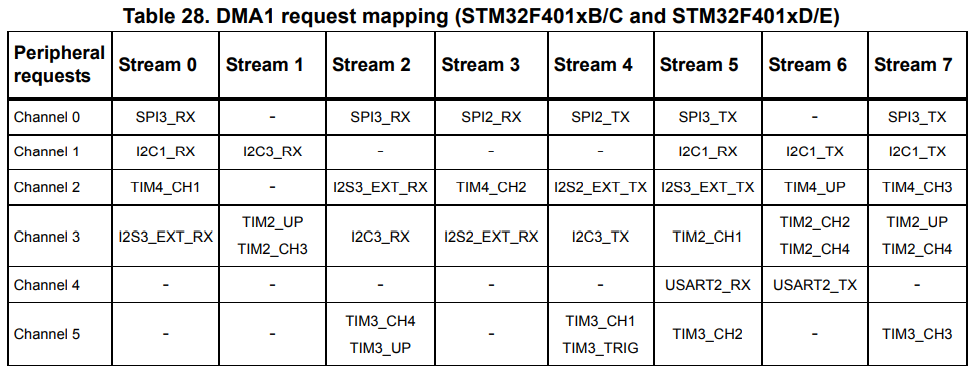
The DMA has two ports, one is peripheral port and other one is memory port.

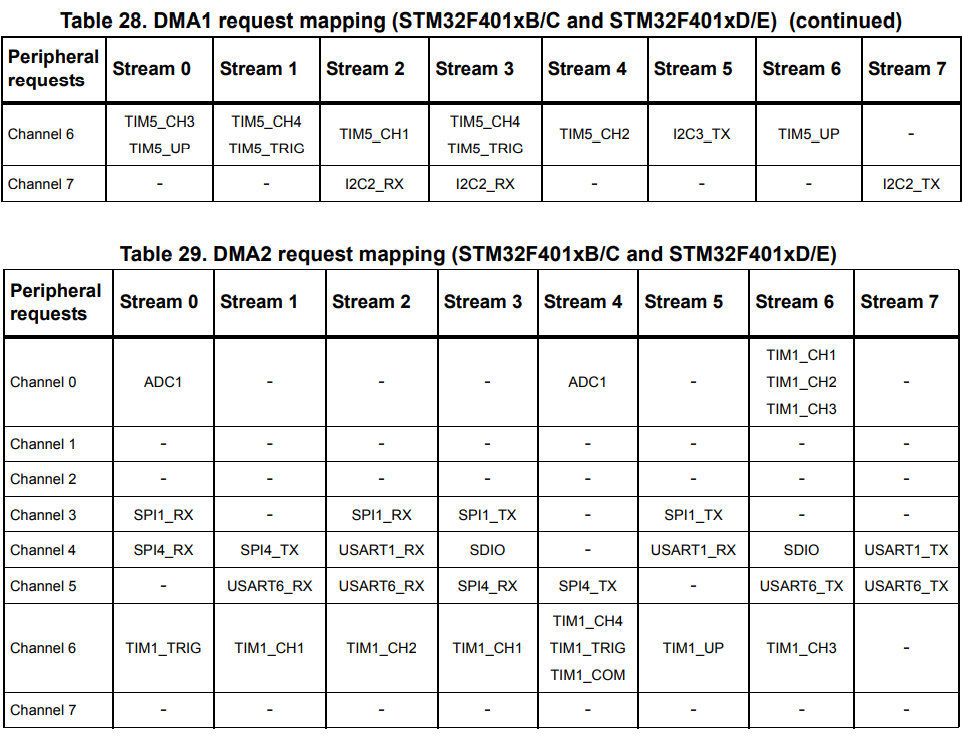


* Each module implements 8 different streams.
* Each stream is dedicated to managing memory access request from one or more peripherals.
* Each stream has up to 8 selectable channels (requests) in total. The selection is controlled by the CHSEL [2:0] bits in the DMA\_SxCR register.



* Only one channel/ request can be active at the same time in a stream.

**DMA REQUEST MAPPING FOR STM32F401xx:** 



**DMA Stream Priority:**

* The DMA has an arbiter for handling the priority between the DMA streams.
* Steam priority is software configurable
* There are four levels.
* If two or more DMA stream have the same software priority level, the hardware priority is used
* Hardware priority – Stream 0 has priority over Stream 1.

**DMA Source and Destination addresses:**

* A DMA transfer is defined by a source address and a destination address.
* Both the source and destination should be in the AHB or APB memory ranges

**DMA Number of data items to transfer:**

**DMA transfer modes:**

* Peripheral to memory
* Memory to peripheral
* Memory to memory **(Only the DMA2 controller is able to perform memory-to-memory transfers)**