BX3006 INTRODUCTION TO COMPUTER ORGANIZATION

MCA II Semester

ASSIGNMENT 2

1. Given the following MIPS instructions:

   lw $t0, 0($s0)
   sub $t3, $t0, $t2
   sw $t3, 4($s0)

   Assume a 5-stage pipeline (IF, ID, EX, MEM, WB).
   a) Draw the pipeline execution timing diagram for these instructions.
   b) Identify and explain any data hazards present.
   c) Suggest how forwarding or stalls could resolve the issue

2. Design a memory interfacing circuit to interface 2M words of 32 bits each with 256 K × 8 static memory chips