Assignment 2

1. MIPS Instructions Pipeline Instructions:

Instructions are:

```
lw  $t0, 0($s0)
sub $t3, $t0, $t2
sw  $t3, 4($s0)
```

5-stage pipeline:

- IF - Instruction Fetch
- ID - Instruction Decode
- EX - Execute
- MEM - Memory Access
- WB - Write Back

a) Pipeline Execution Timing Diagram (No Forwarding)

Cycle →	1	2	3	4	5	6	7
lw	IF	ID	EX	MEM	WB		
sub		IF	Stall	Stall	ID	EX	MEM
sw				IF	ID	EX	MEM

b) Identify and Explain Data Hazards Data Hazards

1. **RAW (Read After Write) Hazard:**

- Between **I1 and I2**:
  `I2` needs `$t0`, but it's produced by `I1`.
  `lw` writes to `$t0` at the **WB stage**, but `sub` reads it at **ID**, which is **too early**.
  ⇒ **Data hazard: RAW**

- Between **I2 and I3**:
  `I3` uses `$t3`, which is computed by `I2`.
  `sub` writes to `$t3` at **WB**, but `sw` uses it in **ID** stage for storing to memory.
  ⇒ **Data hazard: RAW**

c) Resolving Hazards Using Forwarding and/or Stalls with Forwarding Enabled

With Forwarding: The hazard between lw and (cycle 4), but sub cannot be resolved by forwarding alone because the data is available only in MEM sub needs it in EX (cycle 3). So one stall is still needed.

Cycle →	1	2	3	4	5	6	7
lw	IF	ID	EX	MEM	WB		
sub		Stall	IF	ID	EX	MEM	WB
sw				IF	ID	EX	MEM

- **Forwarding Paths:**
  - From MEM/WB to ID/EX for $t0 in sub
  - From EX/MEM of sub to ID/EX of sw for $t3

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2. Memory Interfacing Circuit Design

Step 1: Total Memory Required

- Required memory = 2M words = 2 × 1024K = **2048K words**
- Each word = **32 bits**
- Total memory required = 2048K × 32 = **65536 Kbits**

Step 2: Capacity of One SRAM Chip

- Each available chip = **256K × 8 bits**
- Therefore, each chip = **2048 Kbits**

Step 3: Number of Chips Required

- Total chips = 65536 Kbits ÷ 2048 Kbits/chip = **32 chips**

Step 4: Chip Organization

- Each word is 32 bits, so we need **4 chips in parallel** (8 bits each) to form one word.
- One such group of 4 chips can store **256K words**.
- Total words needed = 2048K
- Number of groups = 2048K ÷ 256K = **8 groups**
- Total chips = 8 groups × 4 chips/group = **32 chips**

Step 5: Address Lines and Decoder

- Each SRAM chip needs **18 address lines** to access 256K locations (2^{18} = 256K).
- Total required memory = 2M = 2^{21}, so we need **21 address lines (A0 to A20)**.
- Address line usage:
    - **A0–A17**: Connected to all chips for intra-group access.
    - **A18–A20**: Inputs to a **3-to-8 decoder** to select one of the 8 groups via chip enable.

Step 6: Data Bus Connection
Each group (4 chips) connects to the 32-bit data bus as follows:

- **Chip 1**: D0–D7
- **Chip 2**: D8–D15
- **Chip 3**: D16–D23
- **Chip 4**: D24–D31

Each of the 8 groups is thus connected in parallel to cover the full 32-bit data width.
