Computer Organization, Spring 2023

Lab 5: Pipeline CPU

Due : 2023/06/15 23:59:59

1. Goal

In this lab, please modify the single cycle processor designed in Lab4 to a pipelined processor. You don't have to consider the hazard issue.

2. Demands

A. Please use Vivado as your simulator.

B. Reg_file(negative-edge triggered), Program_Counter, and TestBench are supplied. Please add these modules to accomplish the design of your CPU.

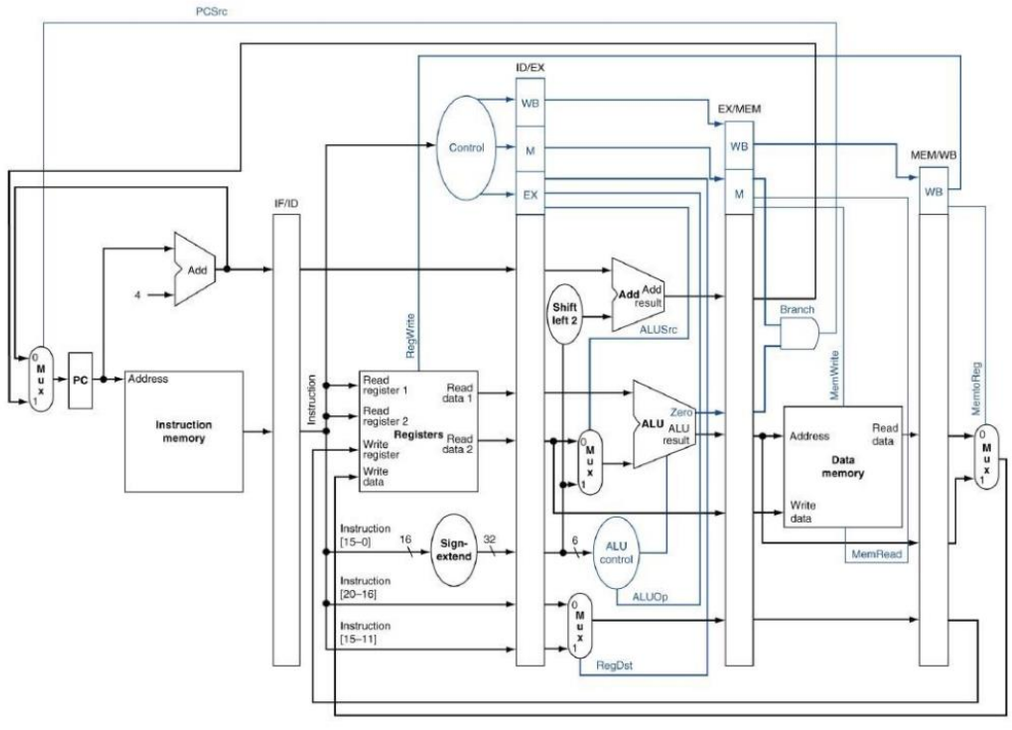
C. We have also provided template to assist you in completing Lab5.

D. You can create additional modules (.v files) for your design. However, it is essential to include an explanation in your report for the inclusion of these modules. Failure to mention any additional modules in your report may result in a deduction of 10 points from your grade.

E. Submit all *.v source files and report(pdf) on E3. Other form of file will get 10%.

3. Requirement description

A. Architecture Diagram



According to the above diagram, in this lab you should implement a five stage pipelined processor with IF, ID, EX, MEM, and WB stages. You should insert a pipeline register between each two stages. Each pipeline register should contain the fields for data and control signals. The pipeline registers are written when the positive clock edge occurs.

B. The description of pipeline stage

The function of each stage is described as follows:

IF stage: In this stage, the processor fetches an instruction from the instruction memory and performs PC + 4.

ID stage: In this stage, the processor decodes the instruction to generate the control signals, reads two source registers, and generates the signextended immediate value.

EX stage: In this stage, ALU_Ctrl generates control signals for function units according to ALUOp. At the same time, Register Write ID and branch target are also determined in this stage.

MEM stage: In this stage, the processor accesses data memory according to the control signals. The modification of PC from branch taken instruction is also performed in this stage.

WB stage: In this stage, the processor will write the value into register file according to the control signal when negative clock edge occurs.

C. Description of pipeline register

Please design five pipeline registers. Each pipeline register must be "positive-edge triggered", has default value 0. Then, insert these pipeline registers into your single-cycle CPU designed in Lab4 to accomplish the pipelined CPU required in this lab.

DO NOT set any delay time for the sequential circuits of the pipelined registers designed by you.

4. Test

CO_P4_test_data1.txt tests the basic instructions. There are 2 test patterns,

CO_P5_test_data1.txt and CO_P5_test_data2.txt.

Corresponding instructions and output answer are CO_P5_test1_ASM.txt and CO_P5_test2_ASM.

The default pattern is the first one.

5. Grade

a. Total score: 100pts. COPY WILL GET A 0 POINT!

b. Instruction score: Total 20 pts

c. Report: 20 pts – format is in CO_document. (up to 2 pages)

6. Hand in your assignment

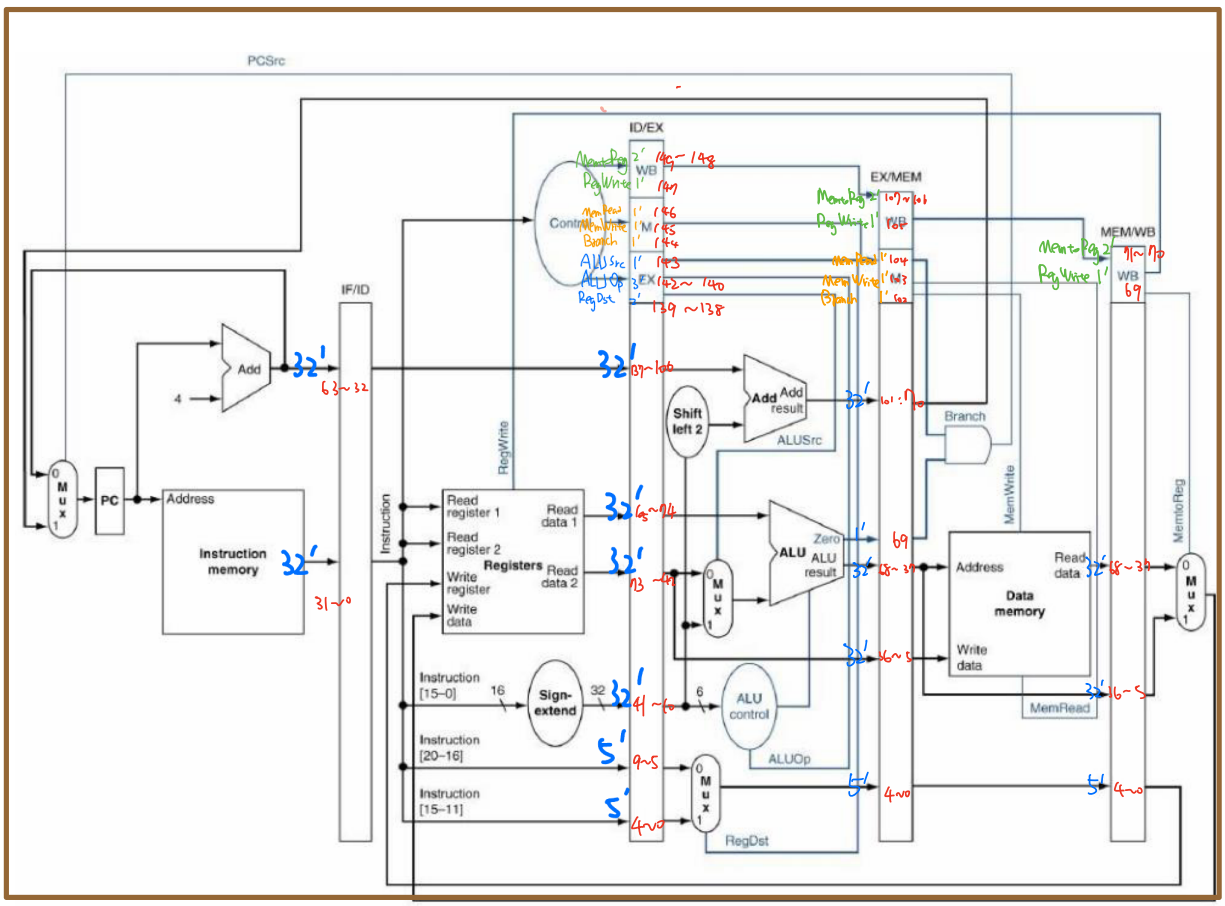
Please upload the assignment to the E3.

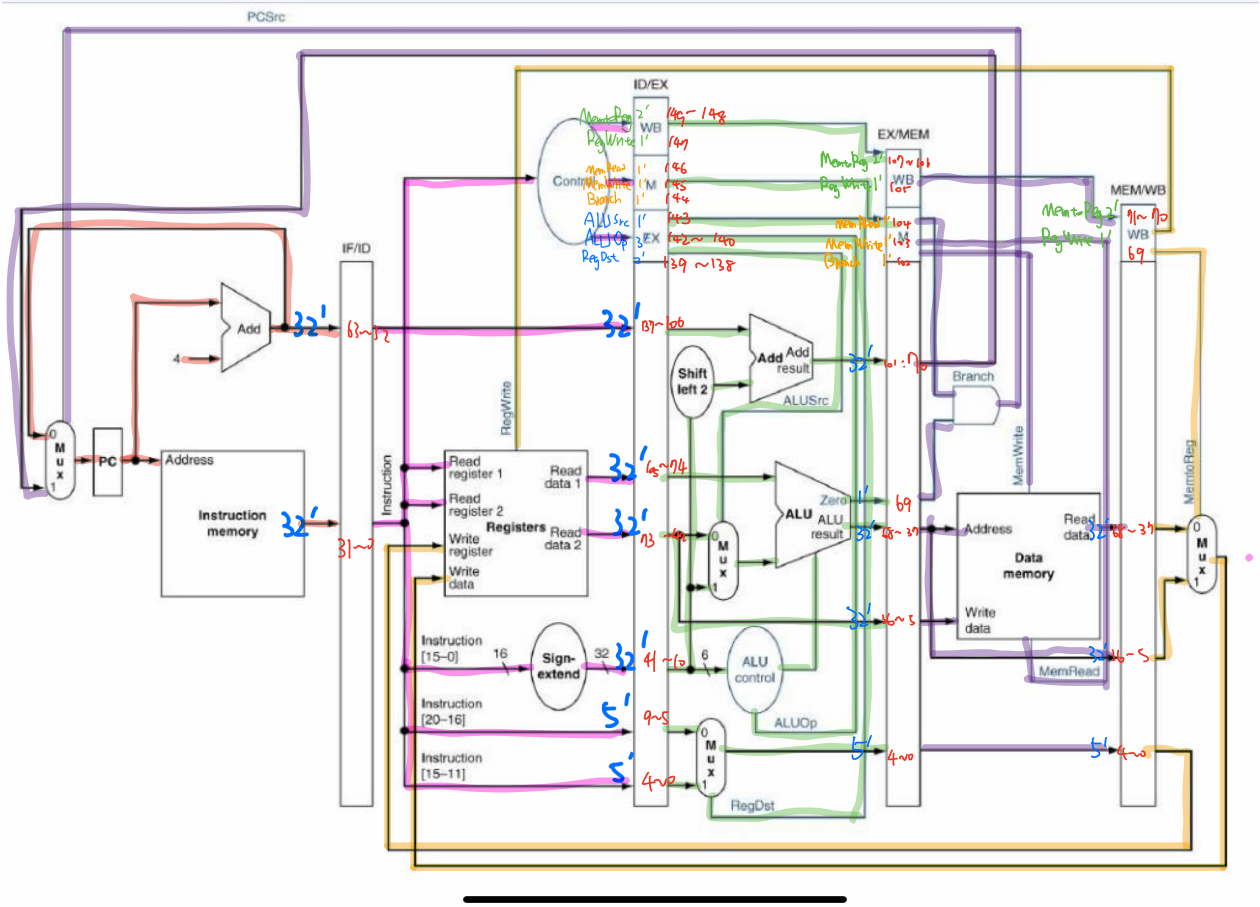
Put all of *.v source files and report into same compressed file.

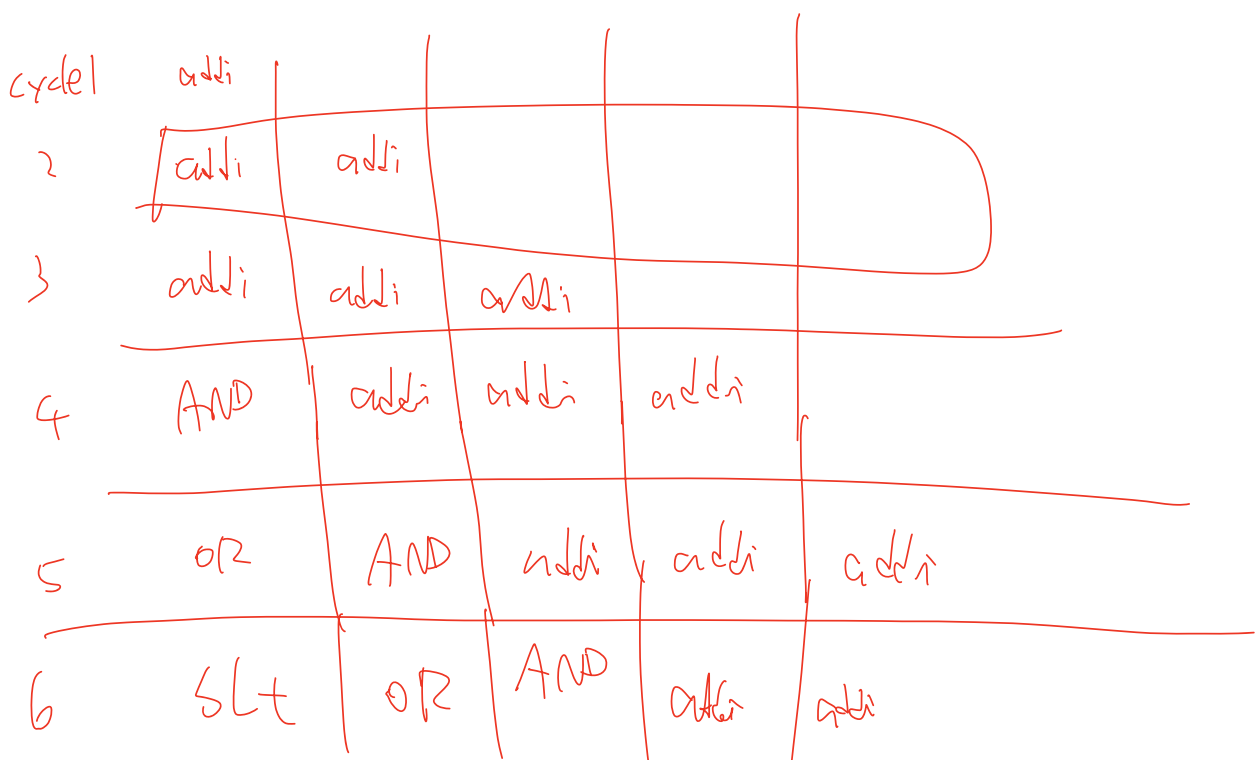
(Use Lab5_student ID to be the name of your compressed file, please make sure your files are correct)

7. Q&A

If you have any question, just send email to TAs.


PCSrc
ID/EX
EX/MEM
MEM/WB
IF/ID
WB
M
EX
Control
Add
4
M u x
PC
Address
Instruction memory
Instruction
RegWrite
Read register 1
Read register 2
Registers
Write register
Write data
Read data 1
Read data 2
Shift left 2
Add
Add result
ALUSrc
ALU
Zero
ALU result
Branch
MemWrite
MemtoReg
Address
Data memory
Read data
Write data
MemRead
Instruction [15–0]
16
Sign-extend
32
6
ALU control
ALUOp
Instruction [20–16]
Instruction [15–11]
RegDst


PCSrc
ID/EX
EX/MEM
MEM/WB
IF/ID
Add
4
M
u
x
PC
Address
Instruction memory
Instruction
RegWrite
Read register 1
Read register 2
Registers
Write register
Write data
Read data 1
Read data 2
Instruction [15–0]
Instruction [20–16]
Instruction [15–11]
16
Sign-extend
32
Shift left 2
Add
Add result
ALUSrc
ALU
Zero
ALU result
ALU control
ALUOp
RegDst
Branch
MemWrite
MemRead
MemtoReg
Data memory
Address
Read data
Write data
WB
M
EX


cycle1
addi
2
addi
addi
3
addi
addi
addi
4
AND
addi
addi
addi
5
OR
AND
addi
addi
addi
6
slt
OR
AND
addi
addi