DLD Assignment

1)

Sol

Truth table for JK flipflop

CLK	J	K	Q_{n+1}
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	$\overline{Q_n}$

for finding sequence at Q, Initially Q=0

& $J = \overline{Q} \Rightarrow J=1$ & $K=1$

Tabulating

Q_n	J	K	clock pulse	Q_{n+1}
0	1	1	1	1
1	0	1	2	0
0	1	1	3	1
1	0	1	4	0
0	1	1	5	1
1	0	1	6	0

∴ Sequence at output Q will be 010101

2)

i) convert SR flipflop to JK flipflop

Step1 available flip-flop : SR flipflop

Required : J-K flipflop

Step2 :-

characteristic table of required flipflop

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Step 3:

Excitation table of SR flip-flop

Q_{n+1}	Q_n	S	R
0	0	0	x
0	1	0	1
1	0	1	0
1	1	x	0

Step 4: combine both the table.

J	K	Q_n	Q_{n+1}	S	R
0	0	0	0	0	x
0	0	1	1	x	0
0	1	0	0	0	x
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	x	0
1	1	0	1	1	0
1	1	1	0	0	1

Expression for S

J \ KQn	$\bar{K}Q_n$	$\bar{K}\bar{Q}_n$	KQ_n	$K\bar{Q}_n$
$\bar{J}$	0	x	0	0
J	1	x	0	1

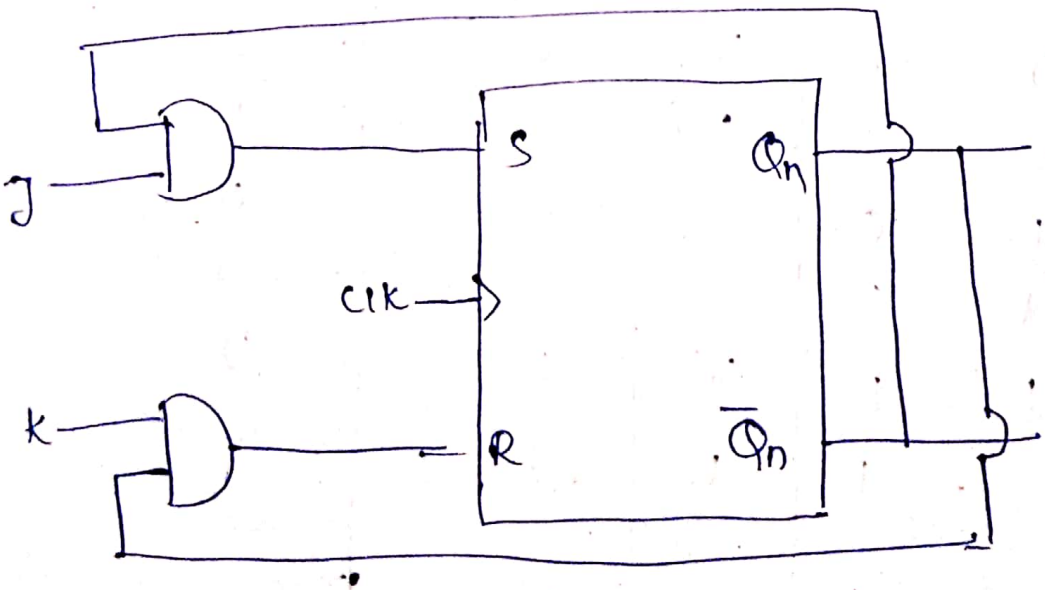
$S = J\bar{Q}_n$

Expression for R

J \ KQn	$\bar{K}Q_n$	$\bar{K}\bar{Q}_n$	KQ_n	$K\bar{Q}_n$
$\bar{J}$	x	0	1	x
J	0	0	1	0

$R = KQ_n$

Step 5:- circuit



Sig. of the Invigilator :

(ii) convert SR flipflop to T flipflop

Step 1: SR-flipflop (available)
T-flipflop (required)

Step 2: CT of T-flipflop

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Step 3: E.T of SR-flipflop

Q_{n+1}	Q_n	S & R
0	0	0 x
0	1	0 1
1	0	1 0
1	1	x 0

Step 4: combine both the tables

T	Q_n	Q_{n+1}	S & R
0	0	0	0 x
0	1	1	x 0
1	0	1	1 0
1	1	0	0 1

Expression for S:

T \ Q_n	$\bar{Q}_n$	Q_n
$\bar{T}$	0	x
T	(1)	0

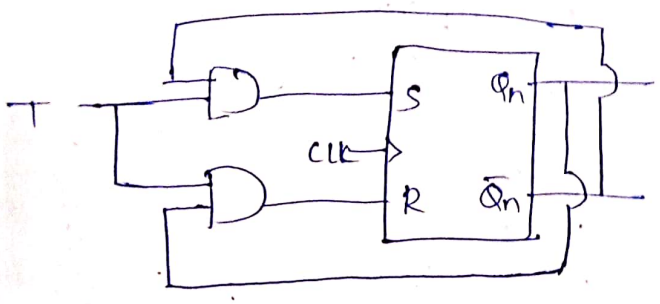
$S = \bar{Q}_n \cdot T$

Expression for R:

T \ Q_n	$\bar{Q}_n$	Q_n
$\bar{T}$	x	0
T	0	(1)

$R = Q_n T$

Step 5:- circuit



Sig. of the invigilator :

3) i) convert T-flipflop to JK flipflop

Step 1 :- : T-ff (available)
JK-ff (required)

Step 2 :- C.T of (JK-ff)

J	K	Qn	Qn+1
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

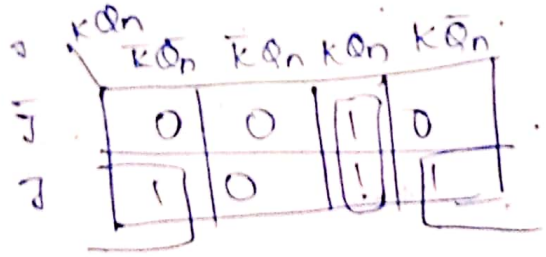
Step 3 :- E.T of T flipflop.

Qn	Qn+1	T
0	0	0
0	1	1
1	0	1
1	1	0

Step 4:- Combine and write both tables in a single table

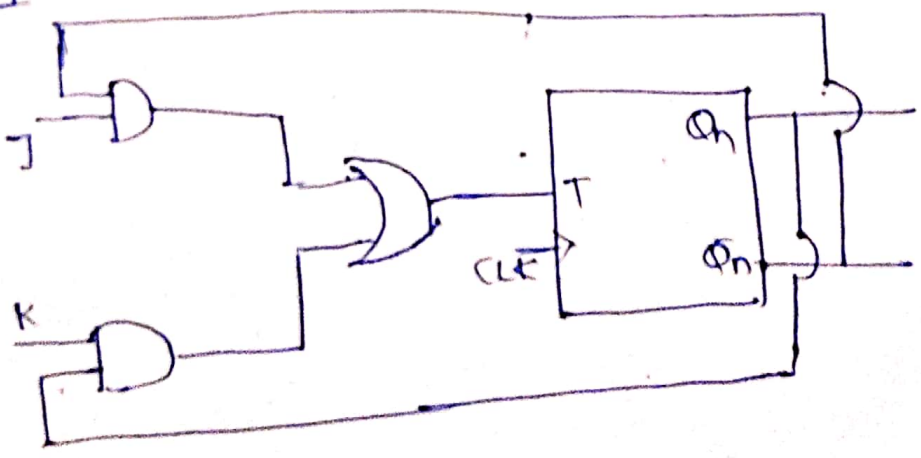
J	K	Q_n	Q_{n+1}	T
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	1
1	0	1	1	0
1	1	0	1	1
1	1	1	0	1

Expression for T



$T = K\bar{Q}_n + J\bar{Q}_n$

Step 5:- Circuit



3 ii) convert T-flipflop to D-flipflop.

step 1: T-flipflop (available) D-flipflop (Required)

step 2: C.T of D-flipflop

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

step 3: E.T of T-flipflop

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

step 4: combine

D	Q_n	Q_{n+1}	T
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

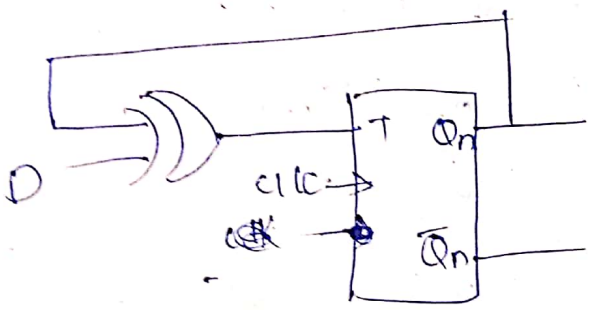
Expression for T

D \ Q_n	$\bar{Q}_n$	Q_n
D	0	1
P	1	0

$T = D\bar{Q}_n + DQ_n$

$= D \oplus Q_n$

Steps :-



4) Draw PLA circuit to implement the functions

$F1 = A'B + AC + A'BC'$

$F2 = (AC + AB + BC)'$

$F3 = AC' + ABC + A'B' + C$

$F1 = A'B + AC + A'BC'$

$= A'BC(1 + C') + AC$

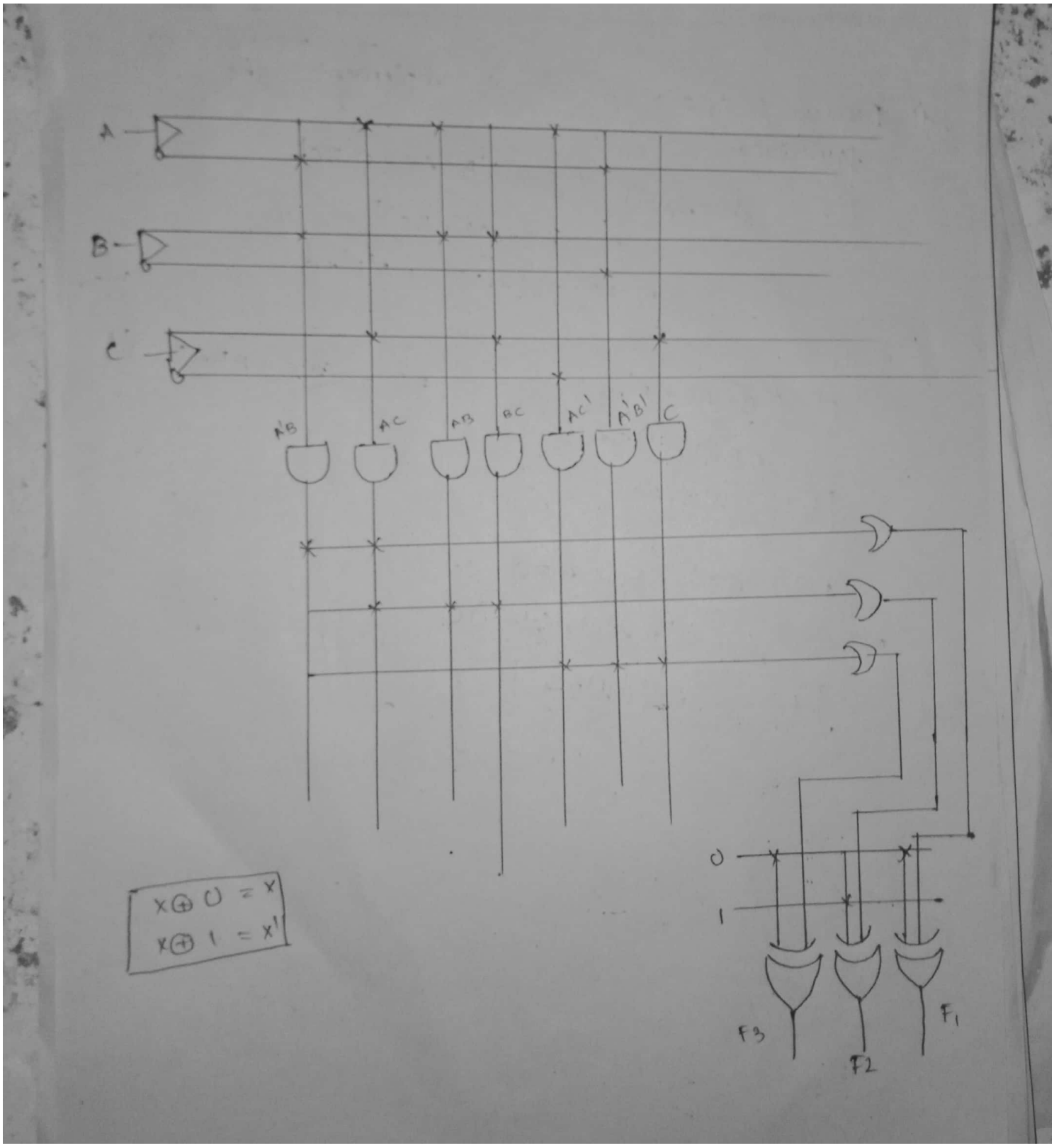
$\boxed{F1 = A'B + AC}$

$F2 = (AC + AB + BC)'$

$F3 = AC' + ABC + A'B' + C$

$= AC' + A'B' + (AB + 1)C$

$\boxed{F3 = AC' + A'B' + C}$



Sig. of the Invigilator: _____ Marks

5) Draw a PAL circuit to implement the functions

$A(x,y,z) = \Sigma(1,3,5,6)$

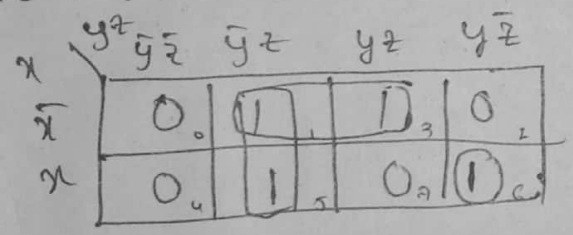
$B(x,y,z) = \Sigma(0,1,6,7)$

$C(x,y,z) = \Sigma(3,5)$

$D(x,y,z) = \Sigma(1,2,4,5,7)$

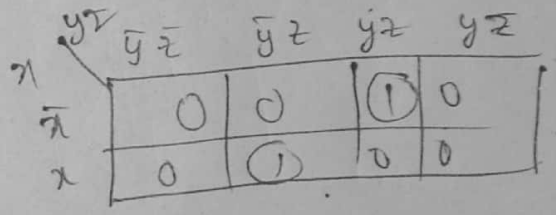
K-Map.

$A(x,y,z) = \Sigma(1,3,5,6)$



$A(x,y,z) = \bar{y}z + \bar{x}z + xy\bar{z}$

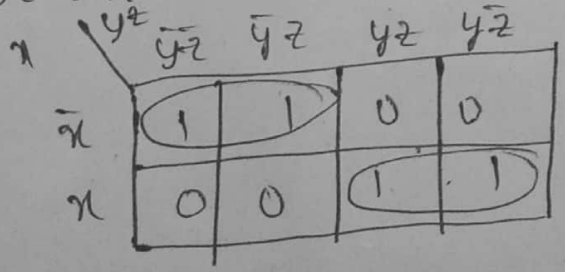
$C(x,y,z) = \Sigma(3,5)$



$C(x,y,z) = \bar{x}yz + x\bar{y}z$

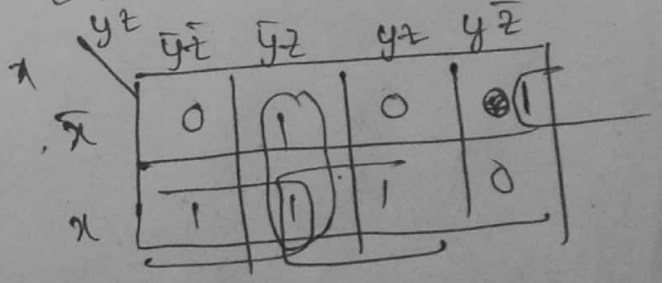
$= (\bar{x}y + x\bar{y})z$

$B(x,y,z) = \Sigma(0,1,6,7)$

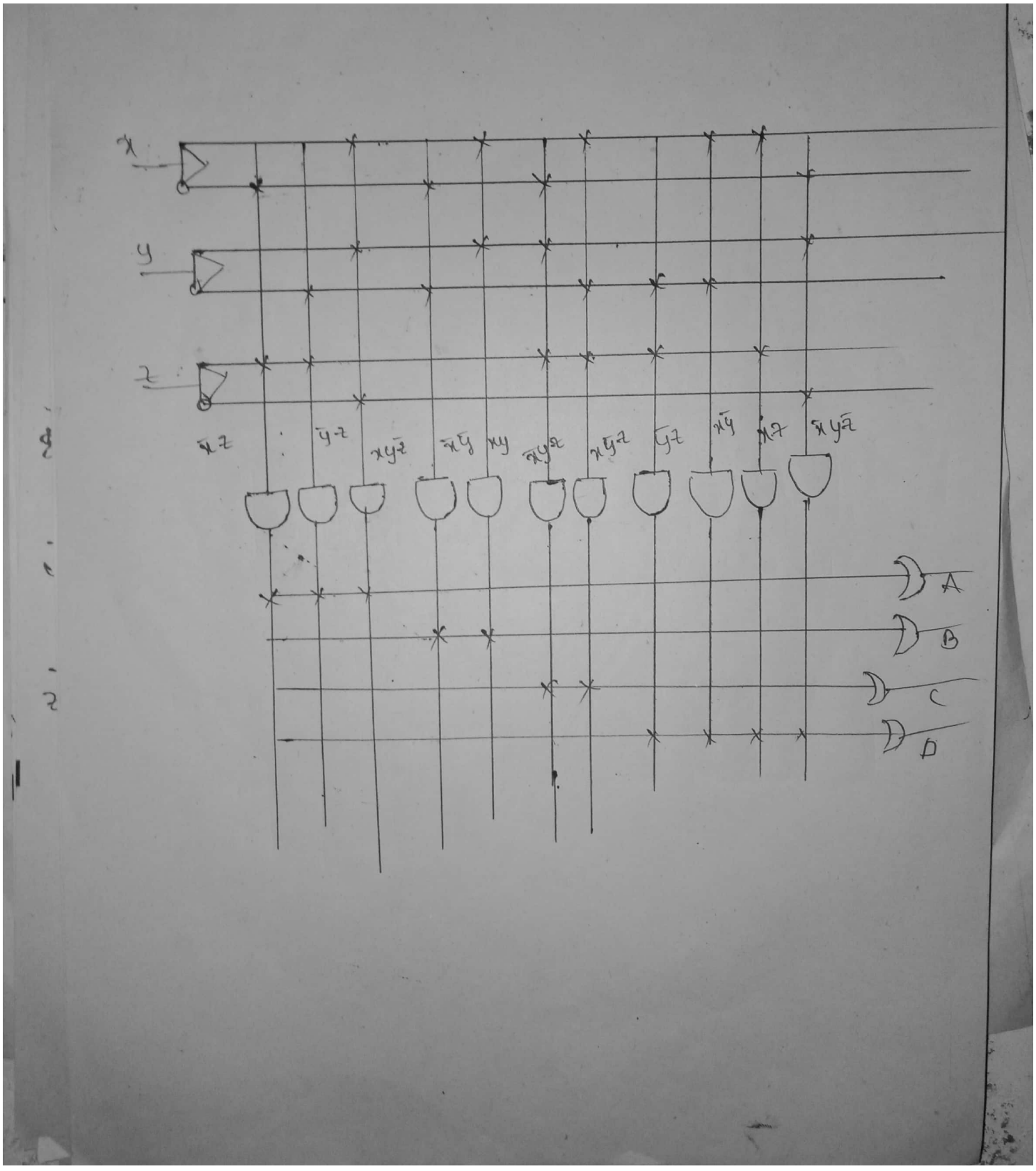


$B(x,y,z) = \bar{x}\bar{y} + xy.$

$D(x,y,z) = \Sigma(1,2,4,5,7)$



$D(x,y,z) = \bar{y}z + x\bar{y} + xz + \bar{x}y\bar{z}$



6) Draw a 8x4 PROM that implement boolean functions

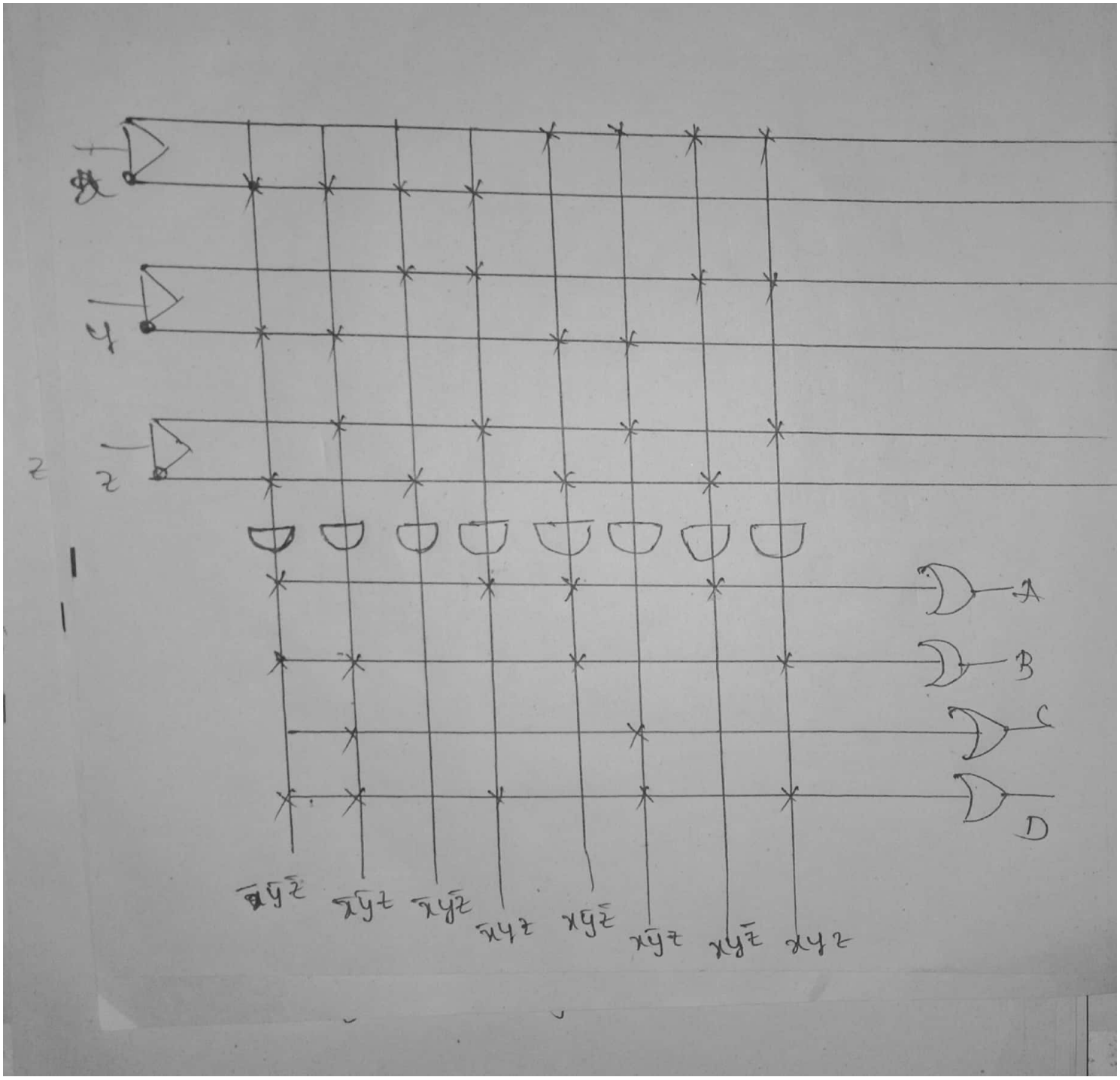
$A(x,y,z) = \Sigma(0,3,4,6)$

$B(x,y,z) = \Sigma(0,1,4,7)$

$C(x,y,z) = \Sigma(1,5)$

$D(x,y,z) = \Sigma(0,1,3,5,7)$

x	y	z	A	B	C	D
0	0	0	1	1	0	1
0	0	1	0	1	1	1
0	1	0	0	0	0	0
0	1	1	1	0	0	1
1	0	0	1	1	0	0
1	0	1	0	0	1	1
1	1	0	1	0	0	0
1	1	1	0	1	0	1



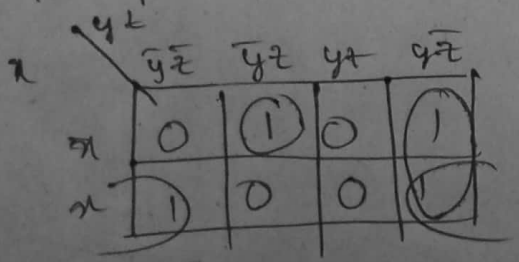
Sig. of the Invigilator : _____ Marks

=) The following is a truth table of 3-input, 4-output combinational circuit

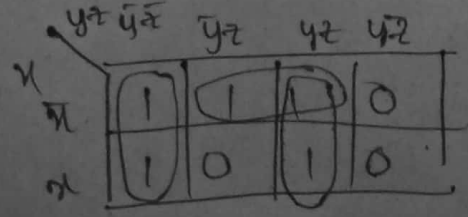
Input			output			
x	y	z	A	B	C	D
0	0	0	0	1	0	0
0	0	1	1	1	1	1
0	1	0	1	0	1	1
0	1	1	0	1	0	1
1	0	0	1	1	1	0
1	0	1	0	0	0	1
1	1	0	1	0	1	0
1	1	1	0	1	1	1

Draw a PAL fuse map for above outputs.

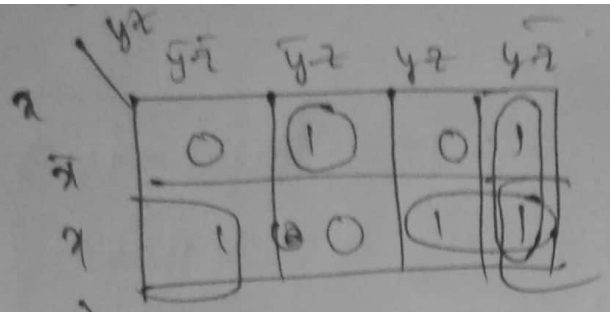
1) map of A



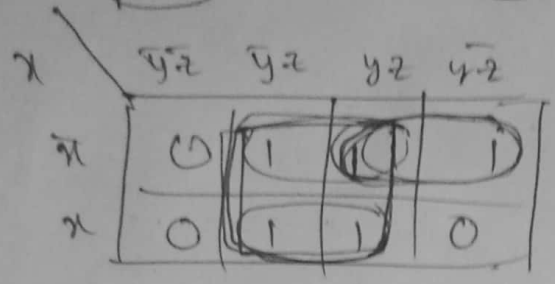
$$A = \bar{x}\bar{y}z + y\bar{z} + x\bar{z}$$



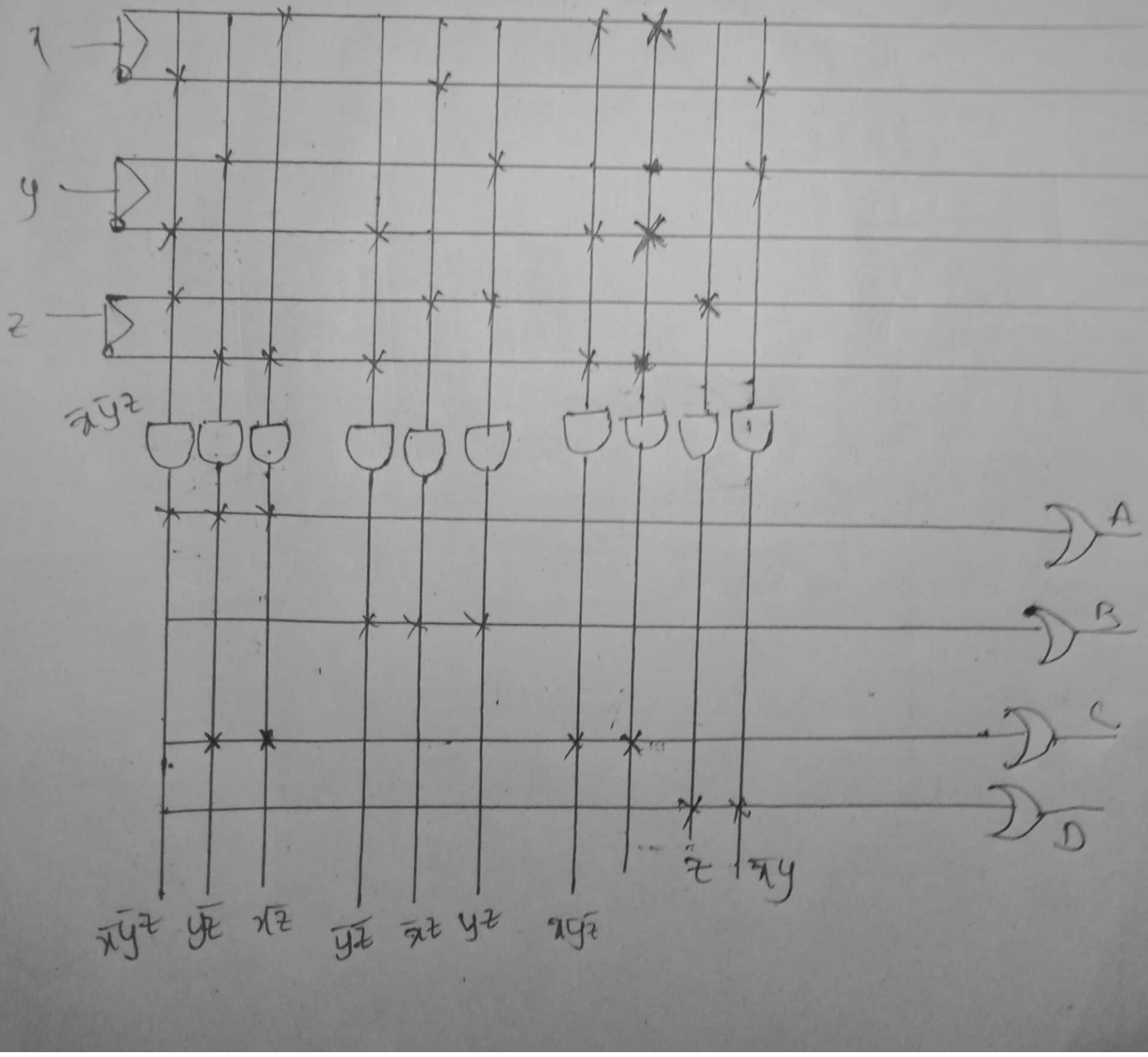
$$B = \bar{y}\bar{z} + \bar{x}z + yz$$



$$C = xz + x\bar{y}\bar{z} + \bar{y}z + \bar{x}y$$



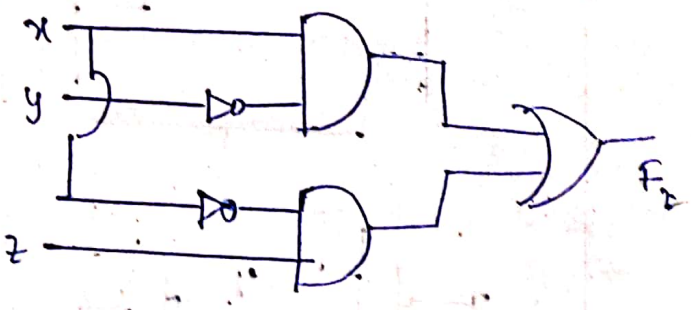
$$D = z + \bar{x}y$$



Marks

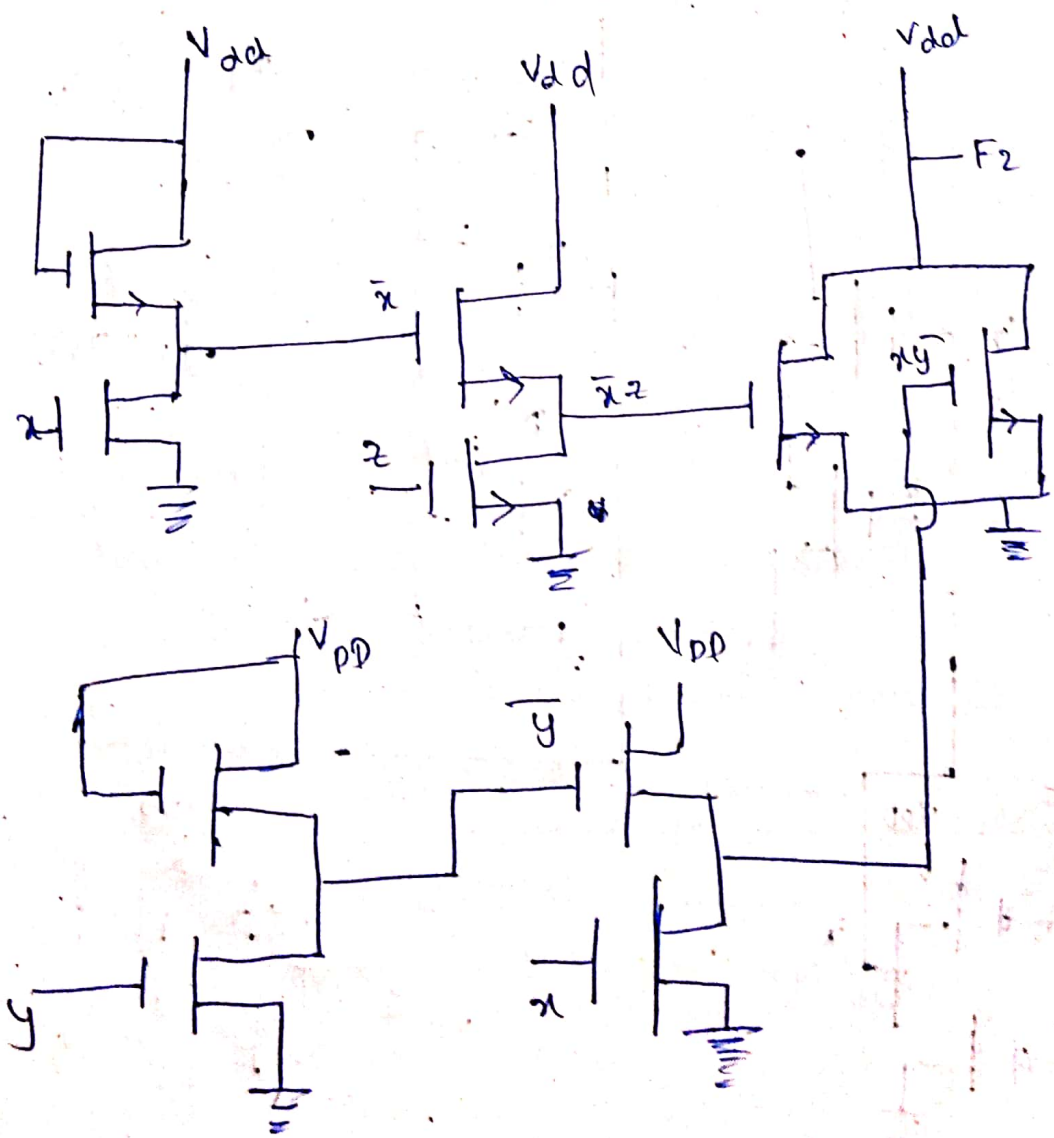
8) Implement the following circuit using

(i) (i) NMOS
(ii) CMOS

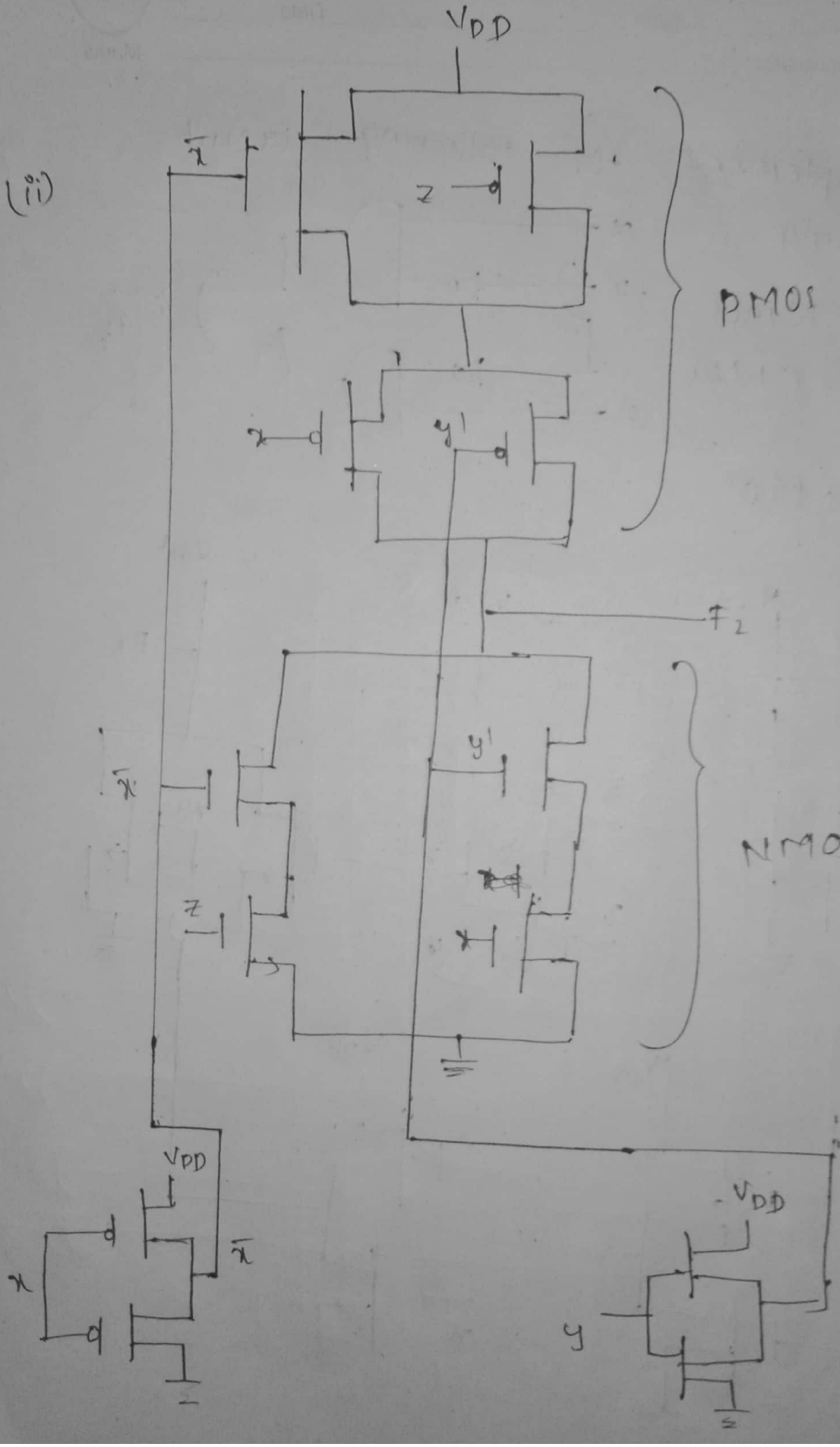


(i) NMOS

A —



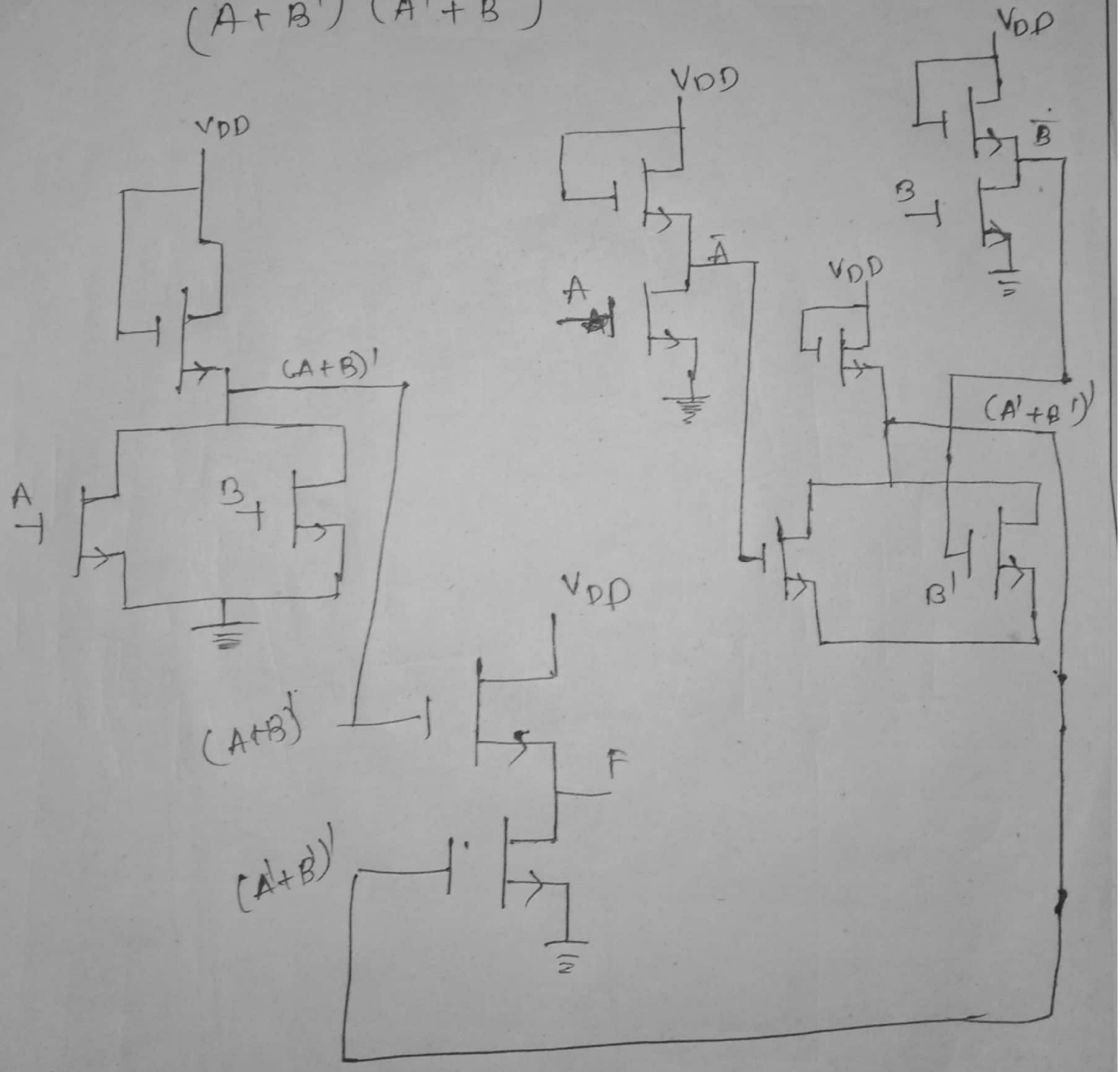
(ii)



9) Implement the following Boolean expression using (i) nMOS (only) (ii) CMOS

$(A+B')(A'+B')'$

(i)



(ii)