GEET GARG

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Academic Qualification

Degree	Institute	University	Performance
Dual Degree (B. Tech and M. Tech)	Indian Institute of Technology, Kharagpur	Indian Institute Of Technology	7.64 / 10 (after 8 semesters)
All India Senior Secondary Certificate Examination, 2005	St. Paul's School	ICSE	88.4%
All India Secondary School Examination, 2003	St. Paul's School	ISC	88.6%

Academic Awards \ Scholarships

- First position in Sai Maths Olympiad, 2002 at district level.
- Secured an All India Rank of 531 in IITJEE and was among the top 0.1% of the appearing 3,00,000 examinees.
- Secured an All India Rank of 239 in All India Engineering Entrance Examination (AIEEE) among 4,00,000 examinees.
- Secured a rank of 219 in Uttar Pradesh Technical University (UPTU) Entrance Test.

Extracurricular Activities

- Participated in Robotix-2007 in the event Step Climber and designed a mechanically controlled robot capable of climbing steps of varying heights.
- Volunteer KSHITIJ '07 team IIT Kharagpur, which manages KSHITIJ, the largest Techno-Management fest in India.
- Assistant coordinator KSHITIJ '08 team IIT Kharagpur, which manages KSHITIJ, the largest Techno-Management fest in India.

Computer Literacy Profile

Languages: C, C++, Java, Prolog, Verilog
Basic Knowledge of: OCAML, Python

Project Work

- **Protein-Protein Interaction Prediction**
  Worked in a team of 5 members, on a project to improve the accuracy of Protein-Protein Interaction Prediction for Homo Sapiens, using machine learning, particularly random forest approach, under the guidance of Dr. Madhavi Ganapathiraju, at Department of Biomedical Informatics, University of Pittsburgh, during the summers of 2009.

- **Graphics Editor**
  Built a Graphics Editor (implemented using JAVA) under the guidance of Prof. R. Mall, Department CSE, IIT Kharagpur. The software would allow the construction of a graphical drawing by drawing and editing of various geometric shapes such as ovals, polygons, lines etc. and importing other graphic drawings.
  Later, also incorporated a command user interface to the editor, allowing a more accurate drawing of the shapes, with exact measurements.

Term Projects

- **16-bit CPU**
  Designed and implemented a 16-bit CPU using Verilog and simulated it on FPGA board, capable of executing small programs stored on EPROM.

- **Compiler**
  Implemented a Compiler for a subset of C language.

- **Others**
  Designed and Implemented Booth's multiplier for two 16-bit numbers, 16-bit ALU similar to 74181, Wallace Tree Adders and Multipliers, using Verilog.

  Implemented using JAVA
  (i) Complete IIT Academic Course Management Software
  (ii) Automatic Multiple Choice Evaluator
  (iii) Super Market Management Software
  (iv) Snakes and Ladder Simulation Software
  and further documented using Life Cycle Models, SRS documentation, and drawing UML diagrams.