Future of Computing: Moore's Law & Its Implications
计算的未来：摩尔定律及其启示

100076202： 计算机系统导论

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摩尔定律的起源/Moore's Law Origins

April 19, 1965

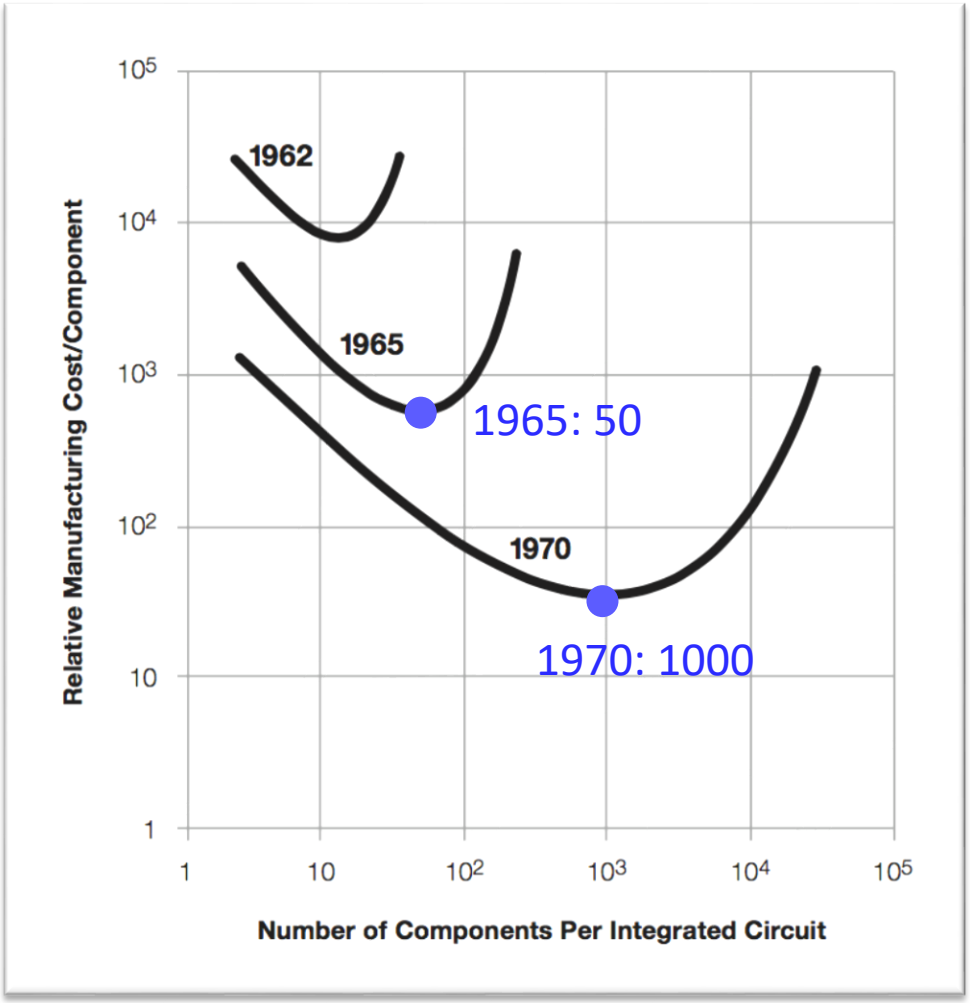
Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore

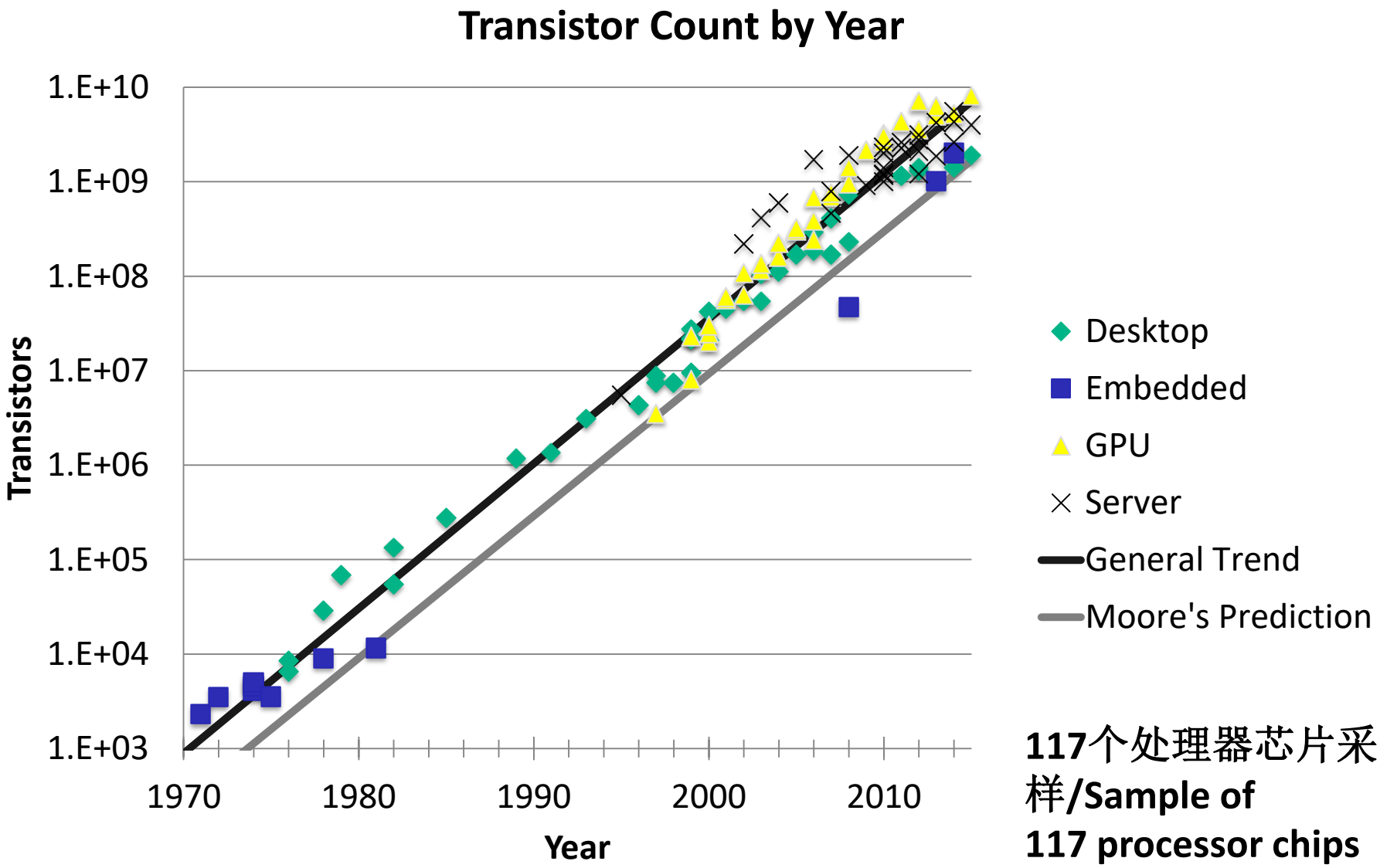
Director, Research and Development Laboratories, Fairchild Semiconductor division of Fairchild Camera and Instrument Corp.

摩尔定律的起源 / Moore's Law Origins



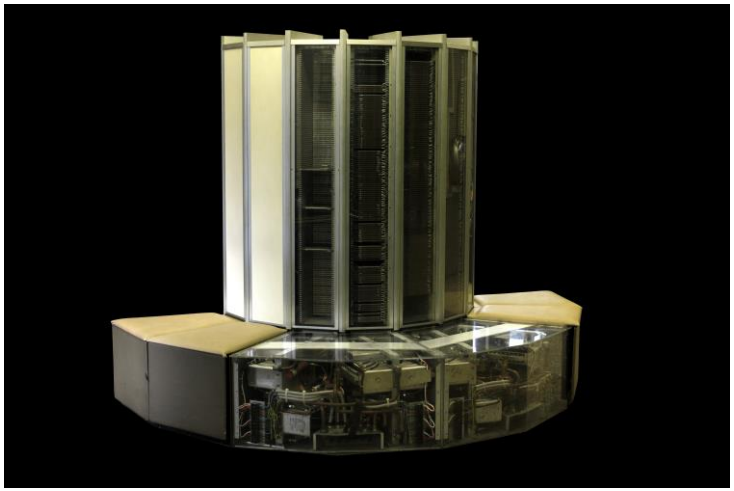
- 摩尔的论文/Moore's Thesis
  - 将每个设备的价格降至最低/Minimize price per device
  - 每年每个芯片上的晶体管数量变为2倍/Optimum number of devices / chip increasing 2x / year
- Later
  - 2x / 2 years
  - 摩尔预测/"Moore's Prediction"

摩尔定律50年/Moore’s Law: 50 Years



117个处理器芯片采样/Sample of 117 processor chips

摩尔定律的意义/What Moore's Law Has Meant



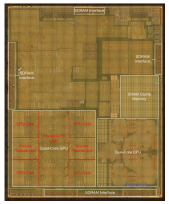
- **1976 Cray 1**
  - 250 M Ops/second
  - ~170,000 chips
  - 0.5B transistors
  - 5,000 kg, 115 KW
  - $9M
  - 80 manufactured

- **2014 iPhone 6**
  - > 4 B Ops/second
  - ~10 chips
  - > 3B transistors
  - 120 g, < 5 W
  - $649
  - 10 million sold in first 3 days

摩尔定律的意义/ What Moore's Law Has Meant

- **1965 Consumer Product**

- **2015 Consumer Product**



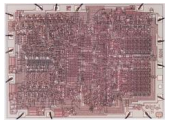
Apple A8 Processor
2 B transistors

迄今为止摩尔定律的可视化/Visualizing Moore's Law to Date

如果晶体管有一粒沙子那么大/

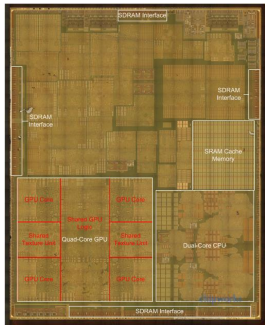
If transistors were the size of a grain of sand

Intel 4004
1970
2,300 transistors



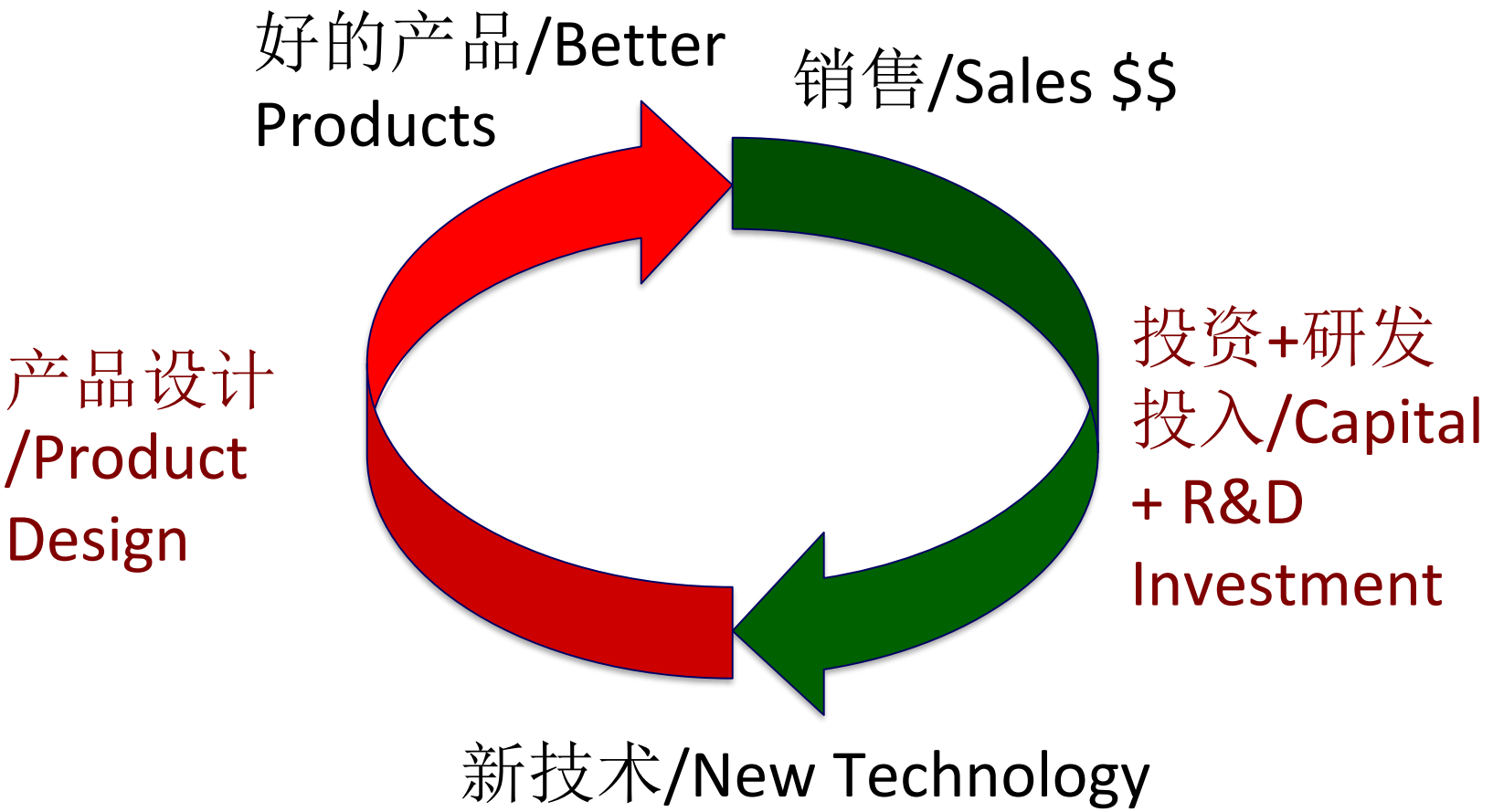
0.1 g

Apple A8
2014
2 B transistors



88 kg

摩尔定律经济学/Moore's Law Economics

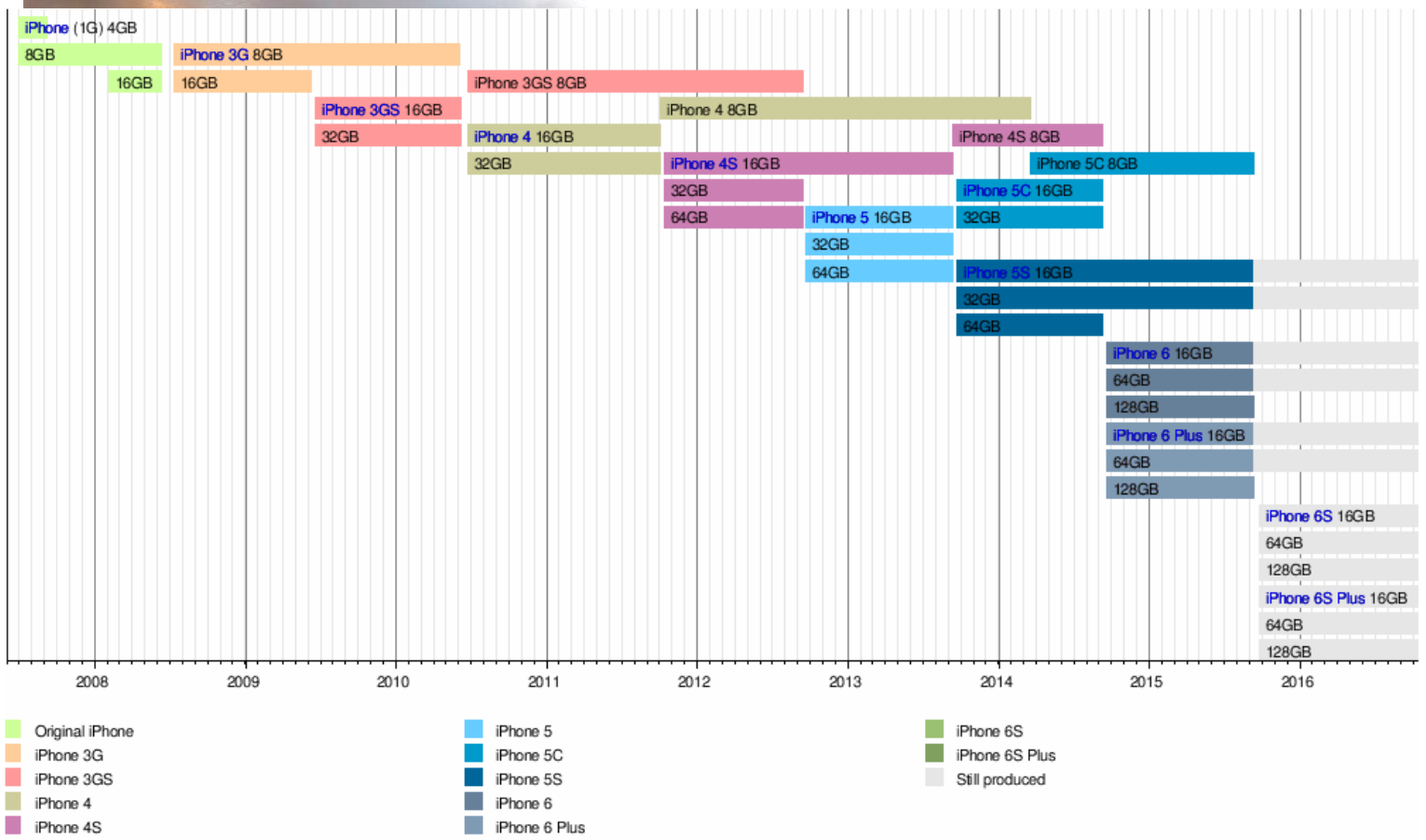


消费品支撑着价值3000亿美元的半导体产业/

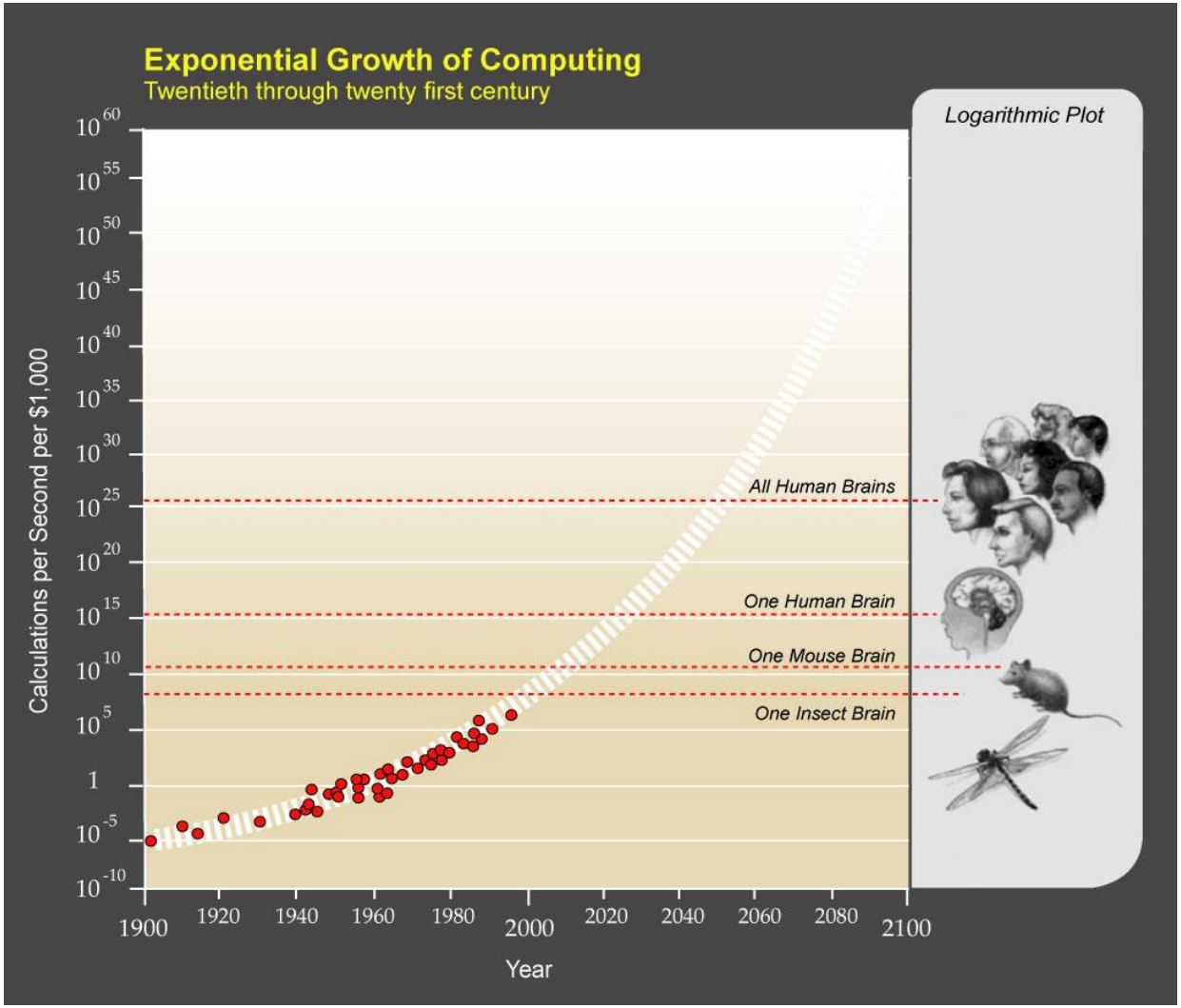
Consumer products sustain the $300B semiconductor industry

摩尔定律的意义/ What Moore's Law Has Meant

自2007年以来的9代iPhone/
9 generations of iPhone since 2007



摩尔定律的含义/What Moore's Law Could Mean



Kurzweil, *The Singularity is Near*, 2005

摩尔定律的含义/ What Moore's Law Could Mean

- **2015年消费品/2015 Consumer Product**

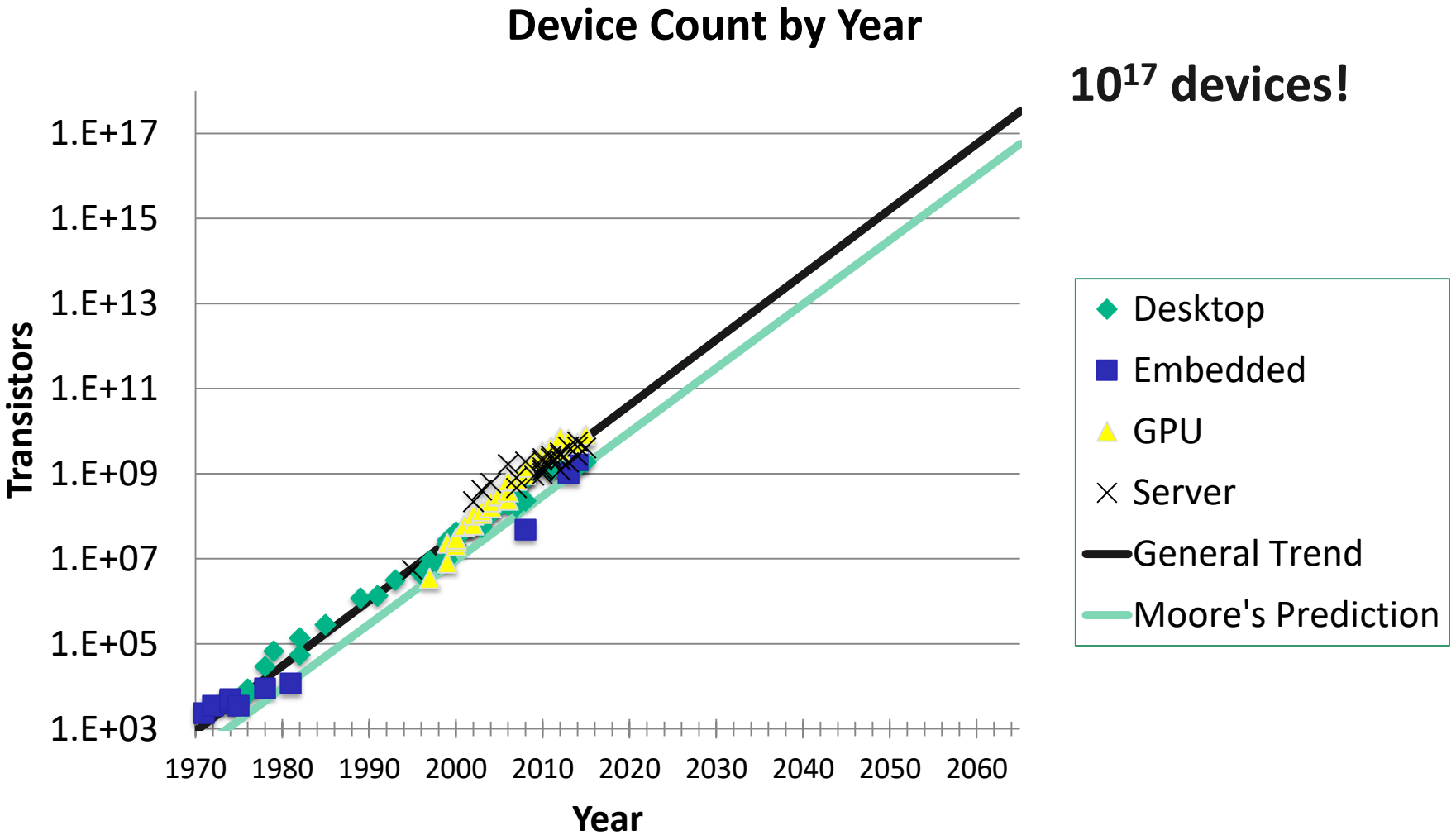
- **2065年消费品/2065 Consumer Product**

  - 便携式的/Portable
  - 低功耗/Low power
  - 将推动市场和创新/Will drive markets & innovation

未来技术要求/Requirements for Future Technology

- 必须适合便携式、低功耗操作/**Must be suitable for portable, low-power operation**
  - 消费品/Consumer products
  - 物联网组件/Internet of Things components
  - 不是低温，不是量子/Not cryogenic, not quantum
- 制造成本必须低廉/**Must be inexpensive to manufacture**
  - 与当前半导体技术相当/Comparable to current semiconductor technology
    - O(1) cost to make chip with O(*N*) devices
- 无需基于晶体管/**Need not be based on transistors**
  - 忆阻器、碳纳米管、DNA转录/Memristors, carbon nanotubes, DNA transcription, ...
  - 可能的新计算模型/Possibly new models of computation
  - 但是，仍然需要集成系统中的许多设备/But, still want lots of devices in an integrated system

摩尔定律100年/Moore's Law: 100 Years



10^{17} devices!

可视化10^{17}个设备/Visualizing 10^{17} Devices

如果装置有一粒沙子那么大/If devices were the size of a grain of sand

0.1 m^3
3.5 X 10^9 grains

1 million m^3
0.35 X 10^{17} grains

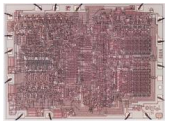
增加晶体管数量/Increasing Transistor Counts

1. **芯片变得更大/Chips have gotten bigger**
   - 每10年变大1倍/1 area doubling / 10 years
2. **晶体管变小了/Transistors have gotten smaller**
   - 4倍密度/10年/4 density doublings / 10 years

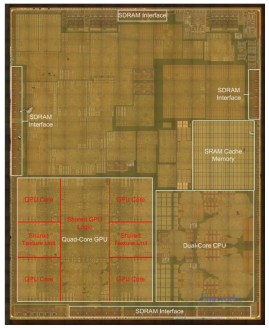
这些趋势还会继续吗？/Will these trends continue?

芯片变得更大了/Chips Have Gotten Bigger

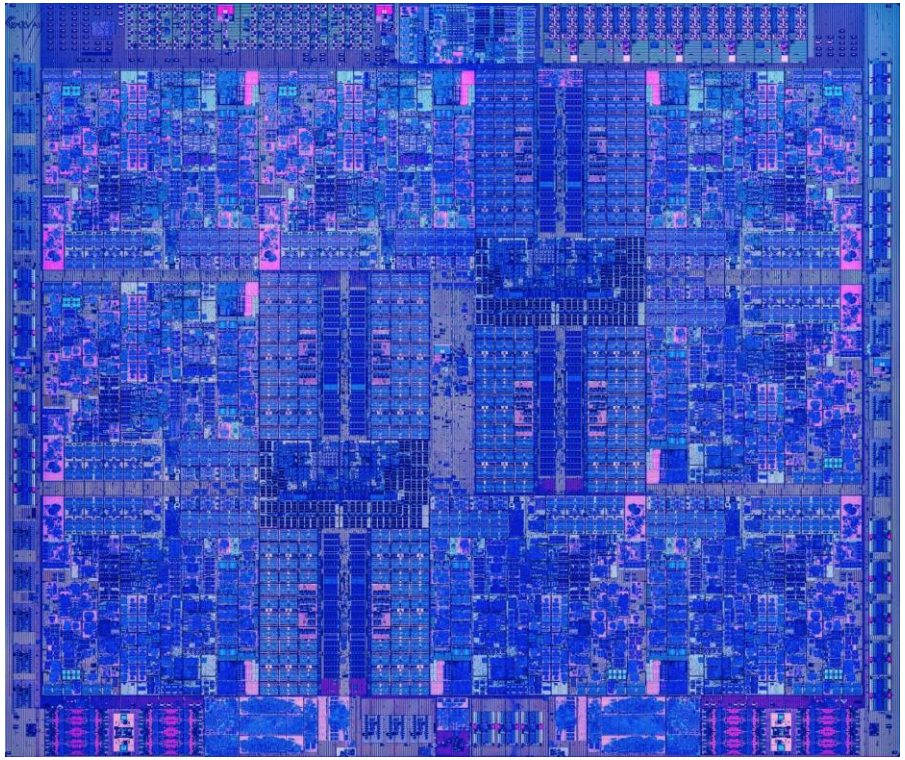
Intel 4004
1970
2,300 transistors
12 mm²



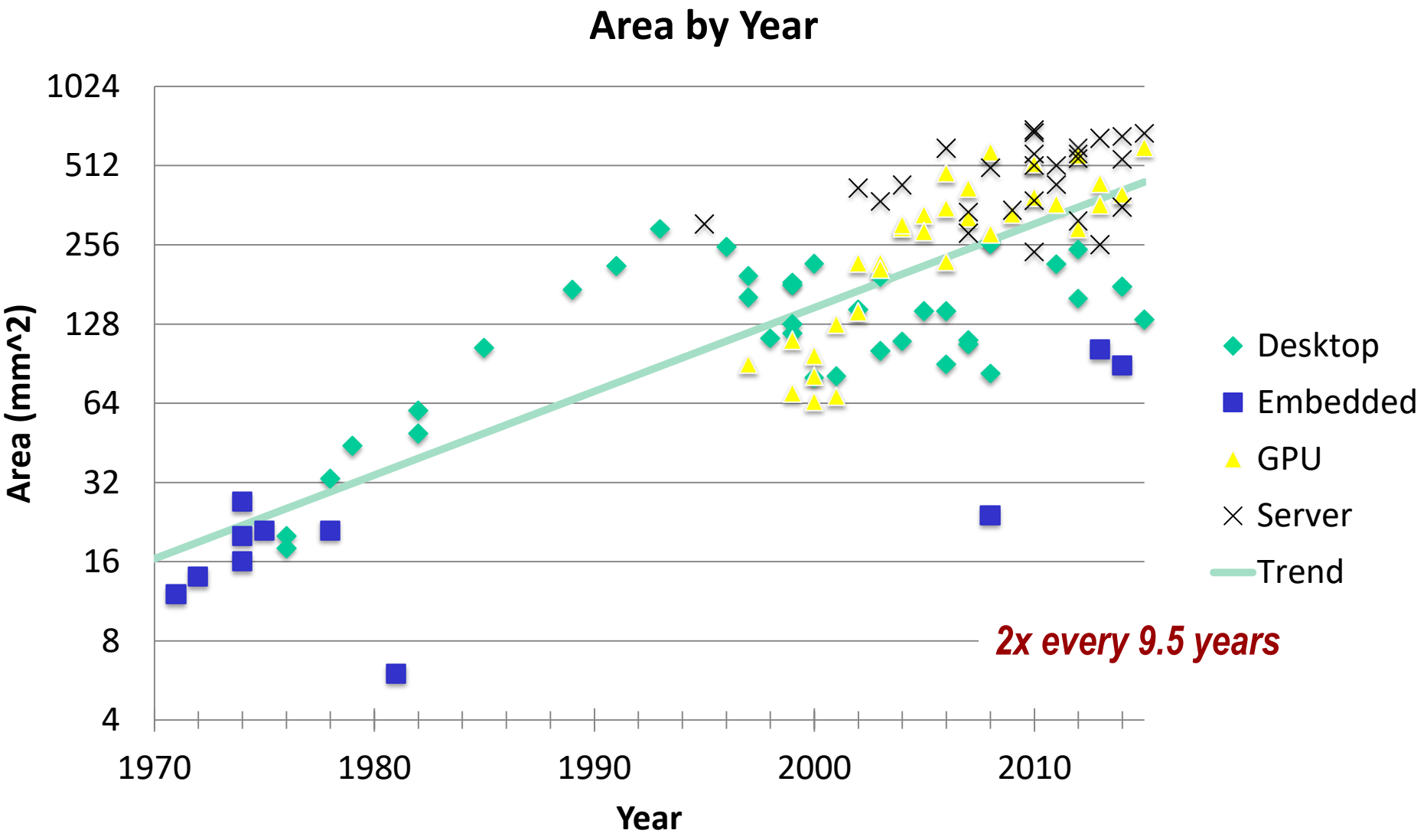
Apple A8
2014
2 B transistors
89 mm²



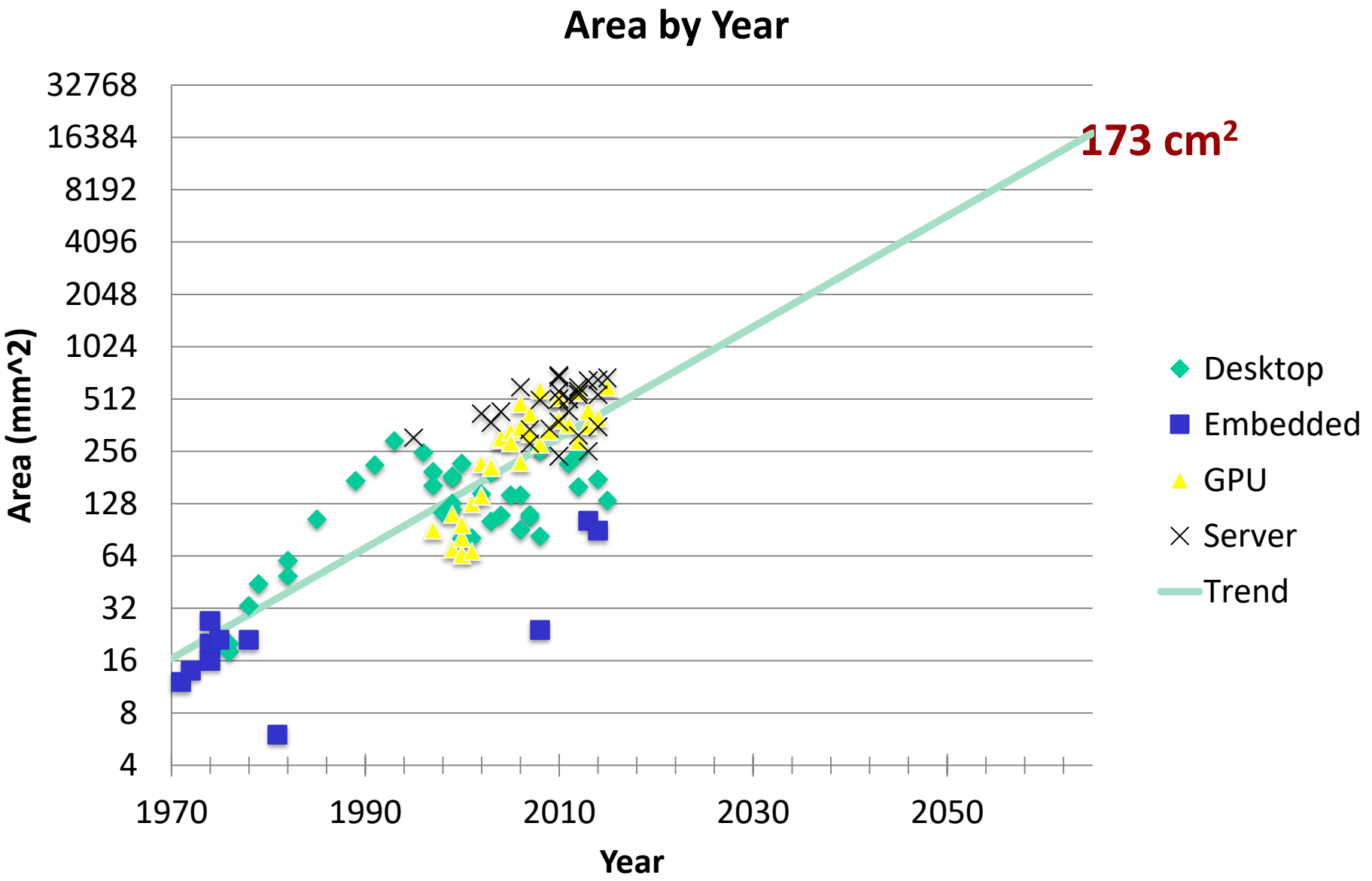
IBM z13
205
4 B transistors
678 mm²



芯片尺寸趋势/Chip Size Trend



芯片尺寸外推/Chip Size Extrapolation



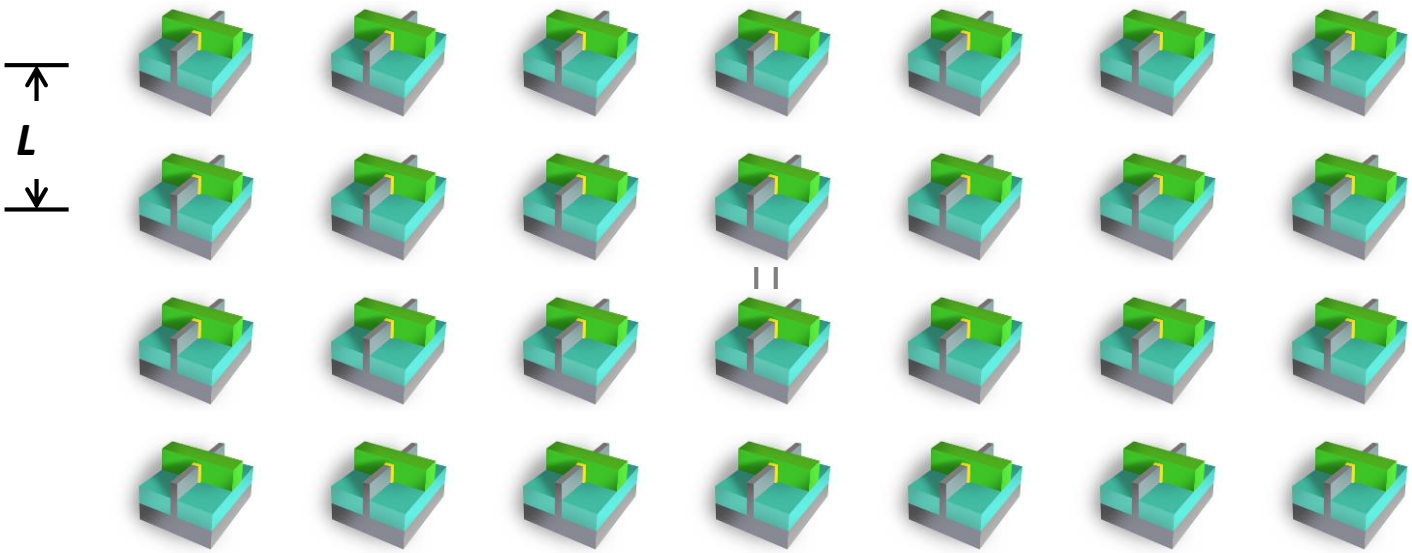
推断： iPhone 31/Extrapolation: The iPhone 31s

Apple A59
2065
10^{17} transistors
173 cm^2

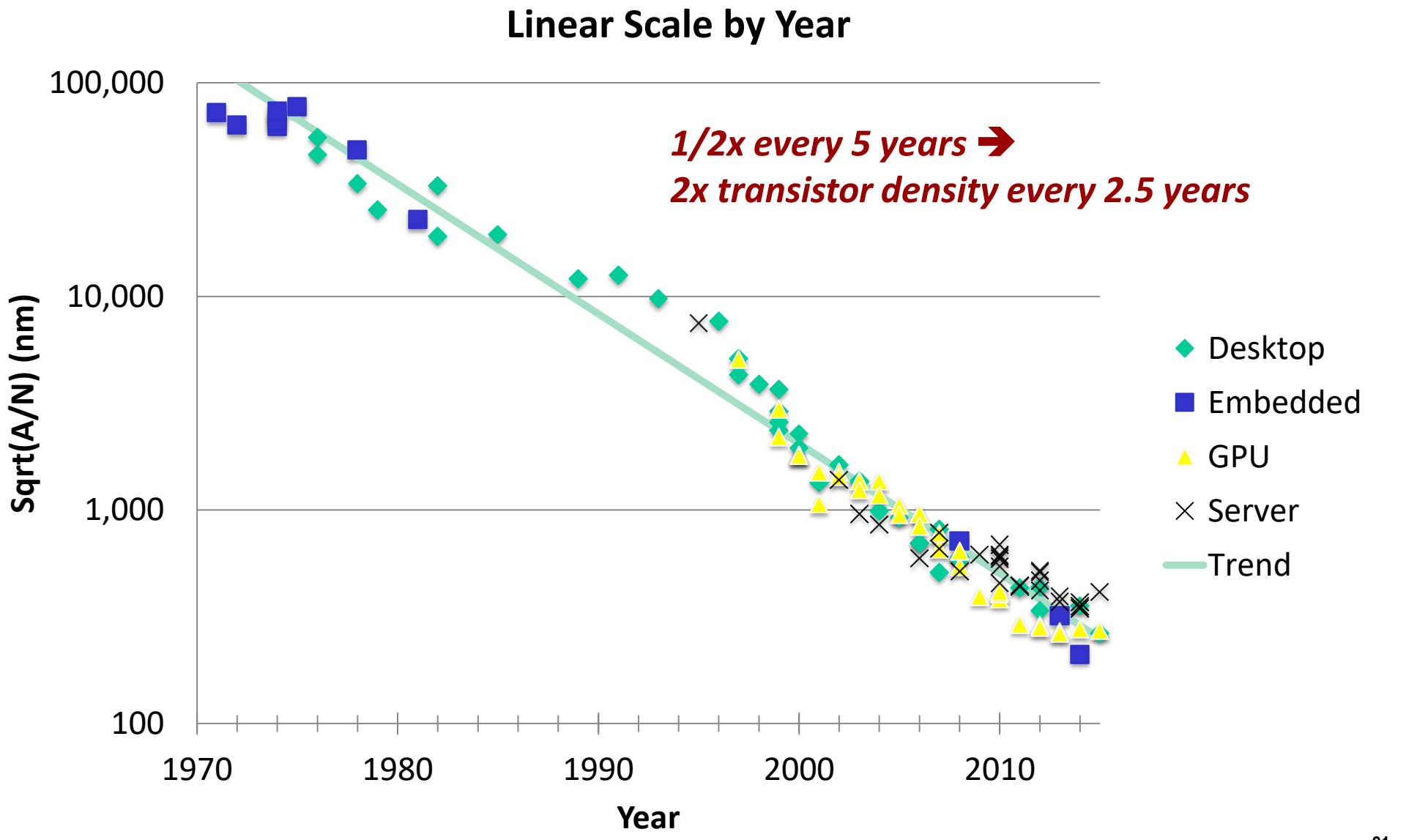
晶体管变小了/Transistors Have Gotten Smaller

- 面积/Area *A*
- *N* devices/设备
- 线性比例/Linear Scale *L*

$$L = \sqrt{A / N}$$

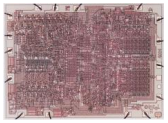


线性缩放趋势/Linear Scaling Trend

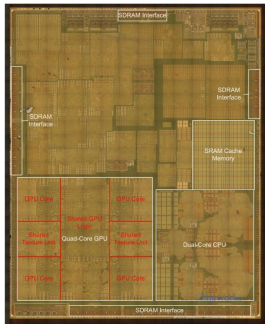


Decreasing Feature Sizes

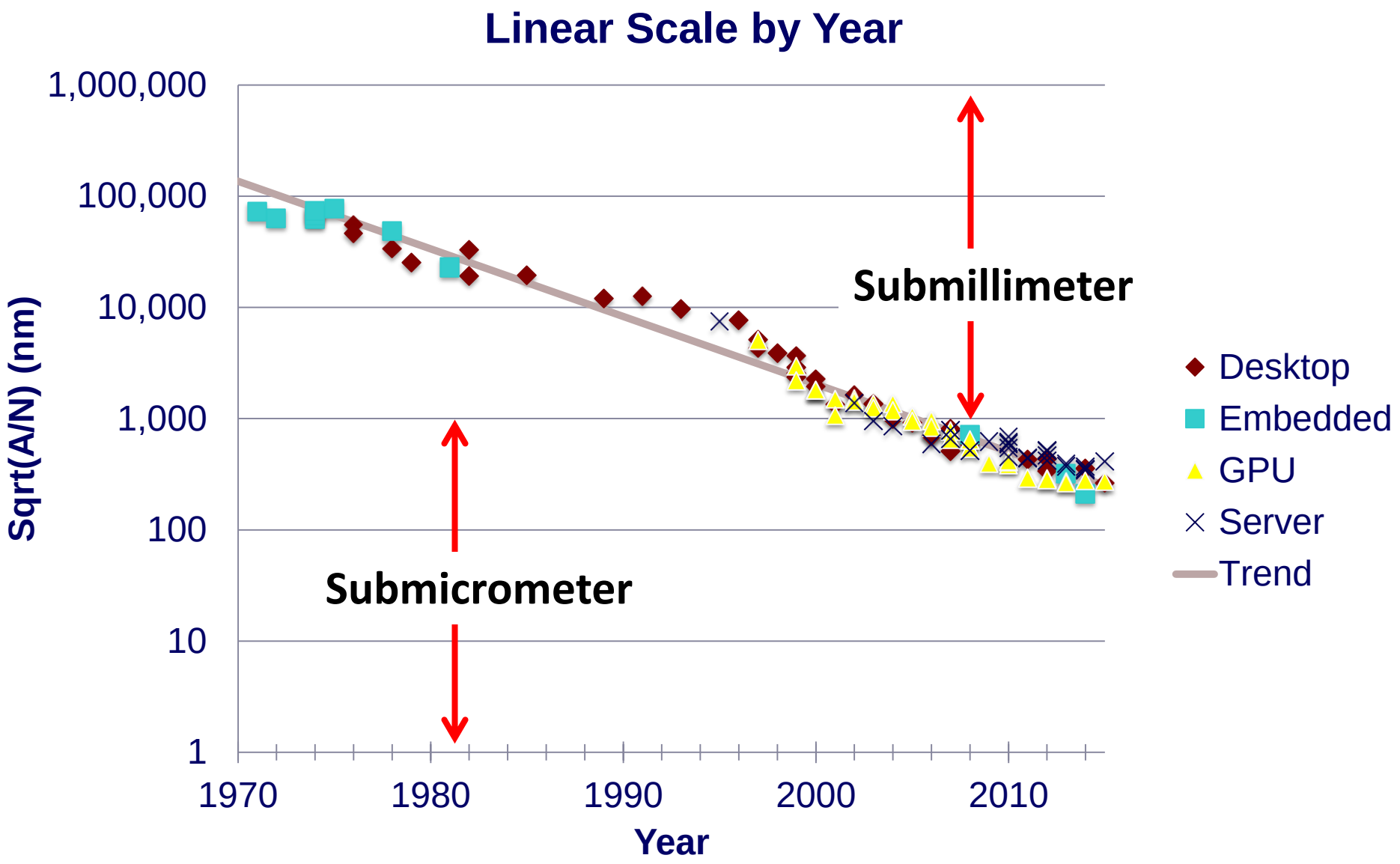
Intel 4004
1970
2,300 transistors
***L* = 72,000 nm**



Apple A8
2014
2 B transistors
***L* = 211 nm**



Linear Scaling Trend

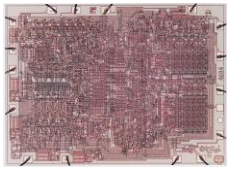


亚毫米尺寸/Submillimeter Dimensions

10^{-3} 1 millimeter (mm)

500µm: Length of amoeba

10^{-4}



72µm: Intel 4004 linear scale

50µm: Average size of cell in human body

10^{-5}

10µm: Thickness of sheet of plastic food wrap

5µm: Spider silk thickness

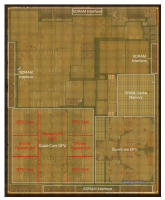
2µm: E coli bacterium length

10^{-6} 1 micrometer (µm)

亚毫米尺寸/ Submicrometer Dimensions

10^{-6} 1 micrometer

(



10^{-7}

400-700nm: Visible light wavelengths

211nm: Apple A8 linear scale

30nm: Minimum cooking oil smoke particle diameter

10^{-8}

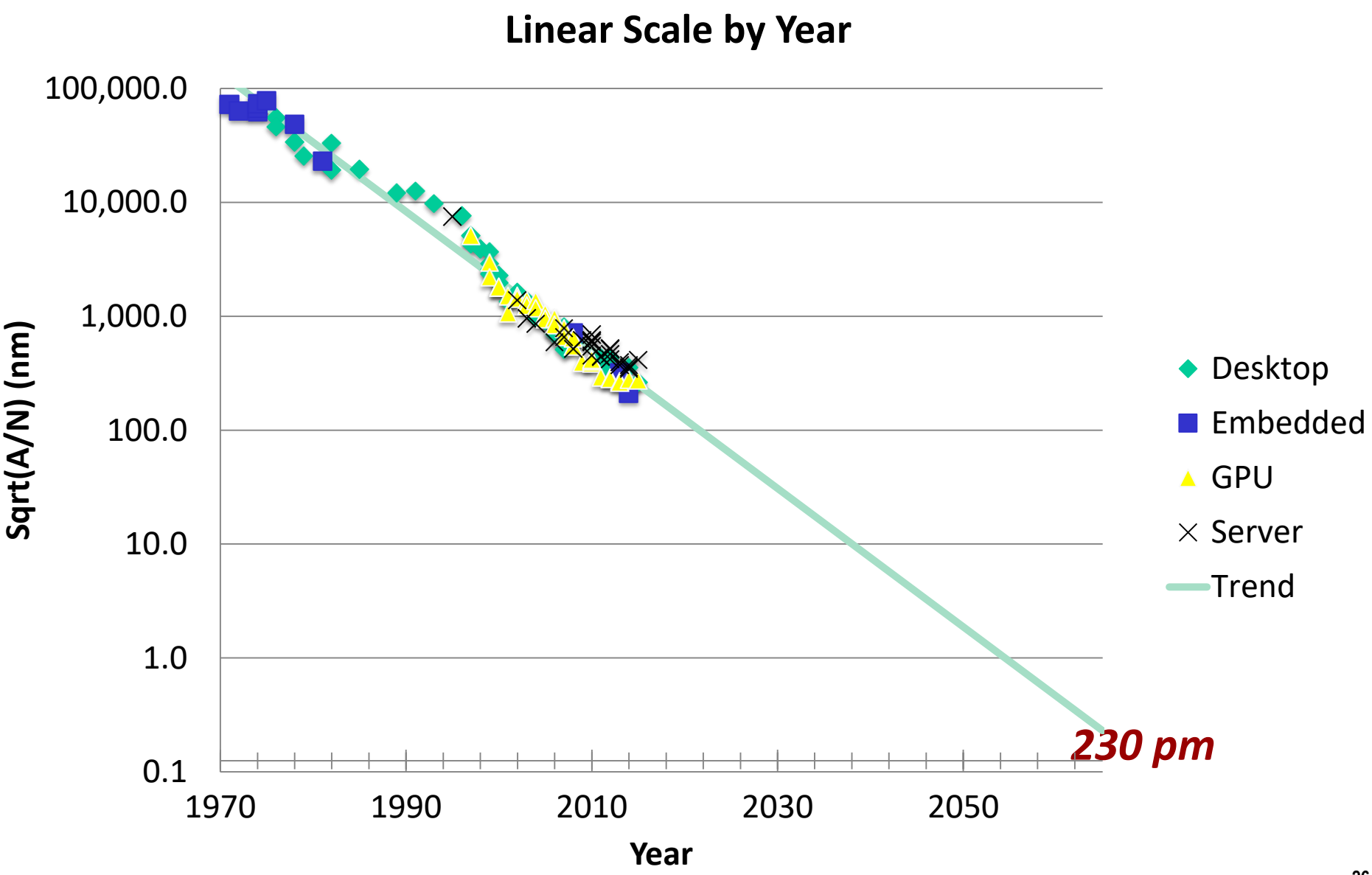
9nm: Cell membrane thickness

2nm: DNA helix diameter

10^{-9} 1 nanometer (nm)

1nm: Carbon nanotube diameter

线性缩放外推/Linear Scaling Extrapolation



亚毫米尺寸/ Subnanometer Dimensions

10^{-9} 1 nanometer (nm)

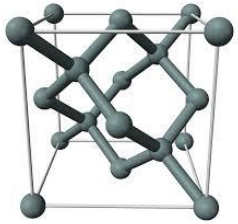
10^{-10}

10^{-11}

10^{-12} 1 picometer (pm)

1nm: 碳纳米管直径Carbon nanotube diameter

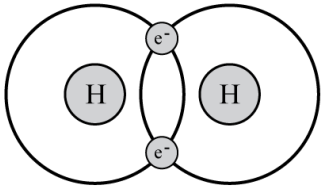
543pm: 硅晶格间距/Silicon crystal lattice spacing



230pm: 2065线性比例投影/2065 linear scale projection

74pm: 氢分子中原子间的间距Spacing between atoms in hydrogen molecule

53pm: 氢中的电子-质子间距（玻尔半径）/Electron-proton spacing in hydrogen (Bohr radiu



2.4pm: 电子波长（康普顿波长）/Electron wavelength (Compton wavelength)

实现2065年目标/Reaching 2065 Goal

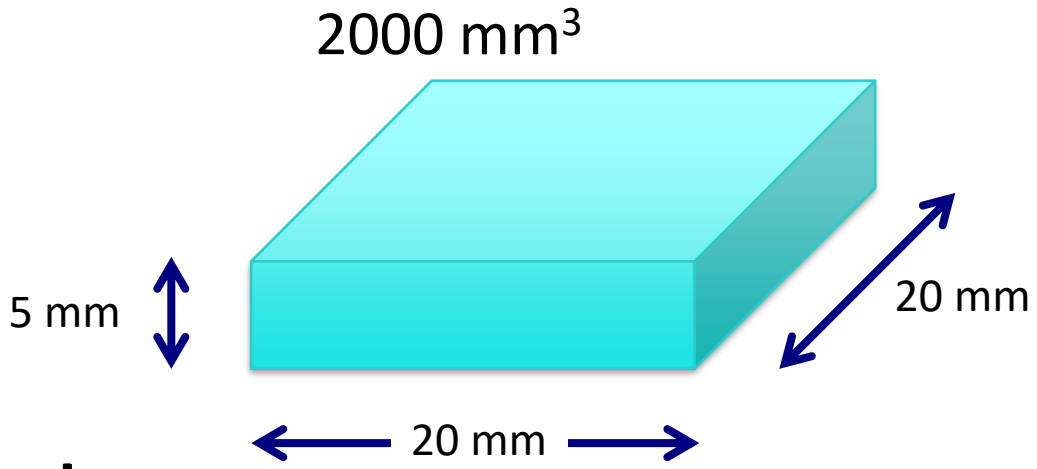
- **Target**
  - 10^{17} devices
  - 400 mm^2
  - L = 63 pm

- **这可能吗？ /Is this possible?**

No!

Not with 2-d fabrication

3D堆叠/Fabricating in 3 Dimensions



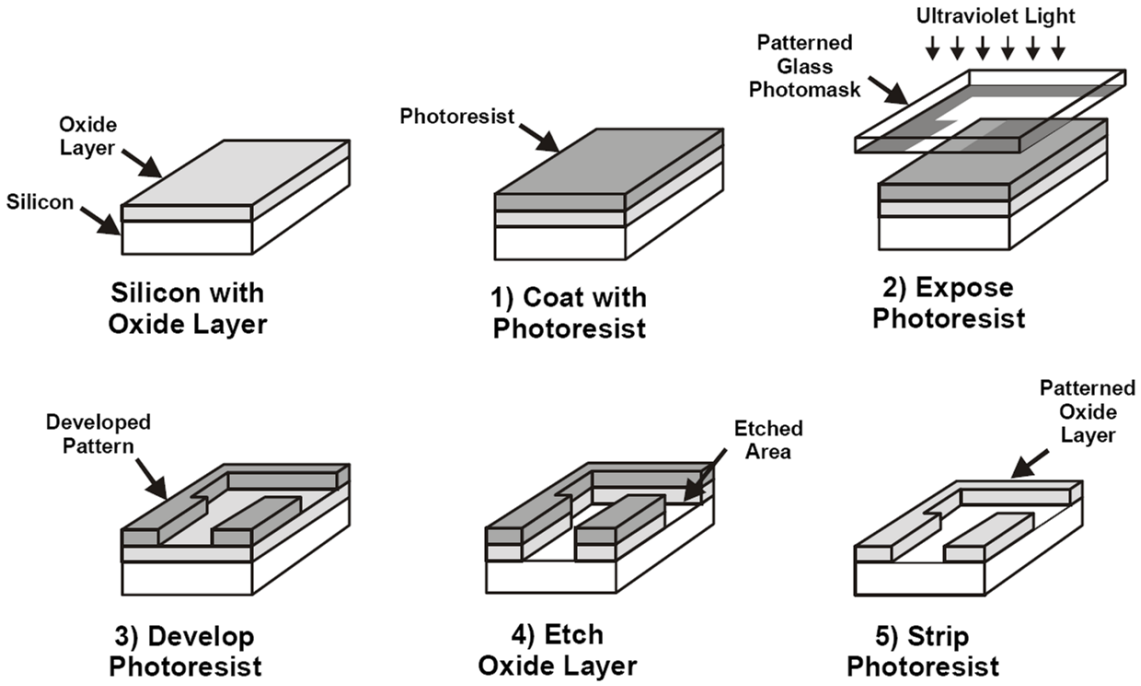
- 参数/Parameters
  - 10^{17} devices
  - 100,000 logical layers
    - Each 50 nm thick
    - ~1,000,000 physical layers
      - To provide wiring and isolation
  - *L* = 20 nm
    - 10x smaller than today

2065 mm³

3D堆叠挑战/3D Fabrication Challenges

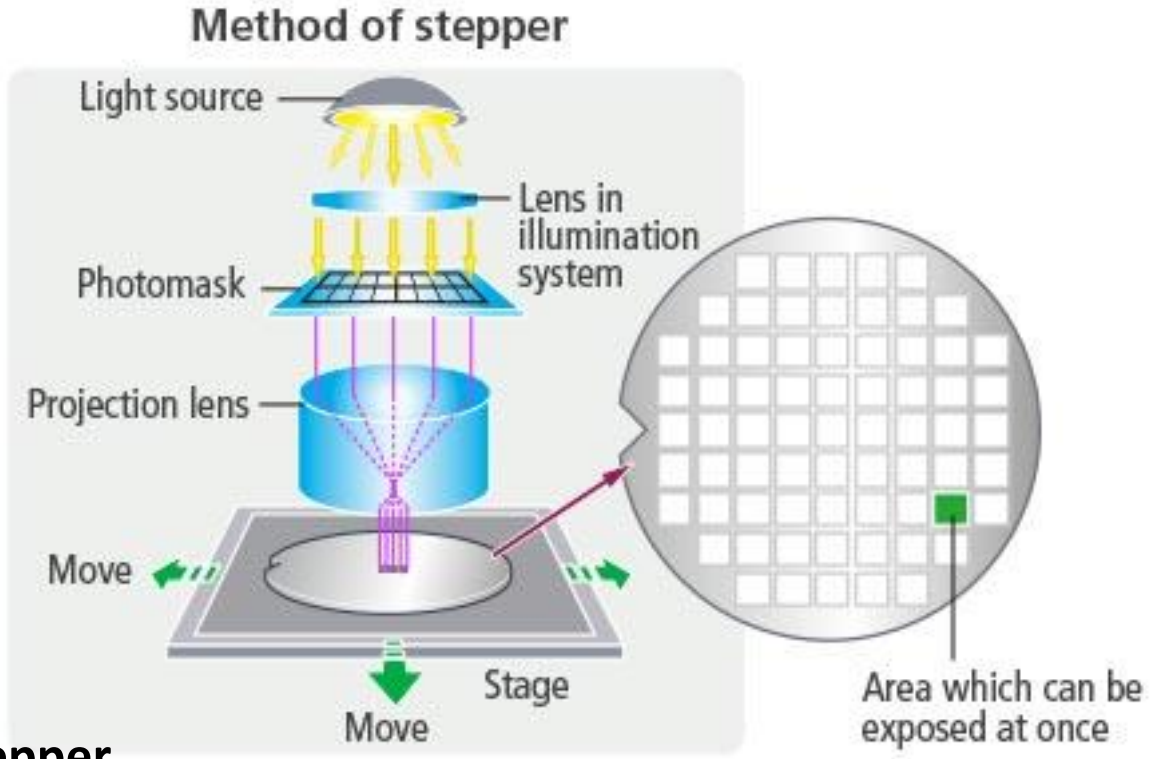
- **产量/Yield**
  - 如何避免或容忍缺陷/How to avoid or tolerate flaws
- **成本/Cost**
  - 光刻成本高/High cost of lithography
- **功耗/Power**
  - 将功耗保持在可接受的范围内/Keep power consumption within acceptable limits
  - 可用能源有限/Limited energy available
  - 散热能力有限/Limited ability to dissipate heat

光刻/Photolithography



- 一步成型整个芯片/Pattern entire chip in one step
- 现代芯片需要约60个光刻步骤/Modern chips require ~60 lithography steps
- 有限步制造N晶体管系统/Fabricate *N* transistor system with O(1) steps

制造成本/Fabrication Costs

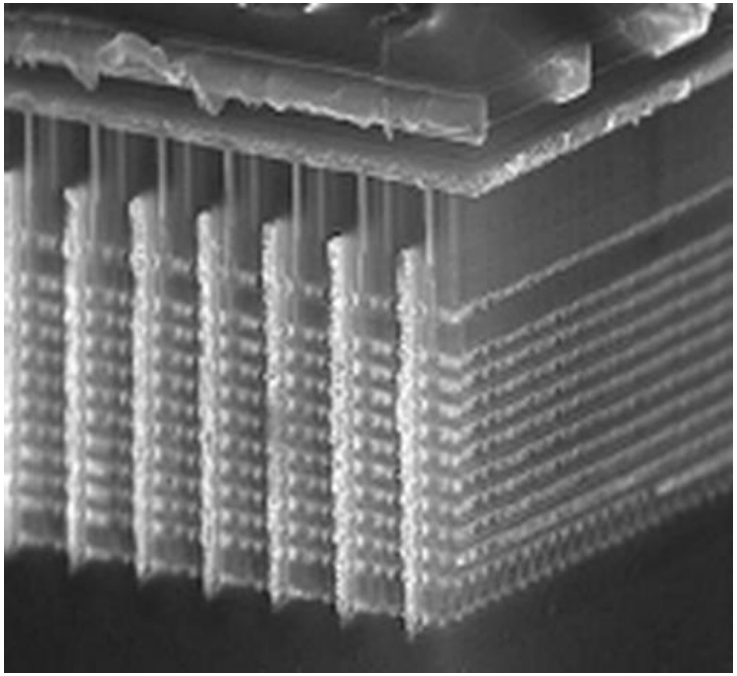


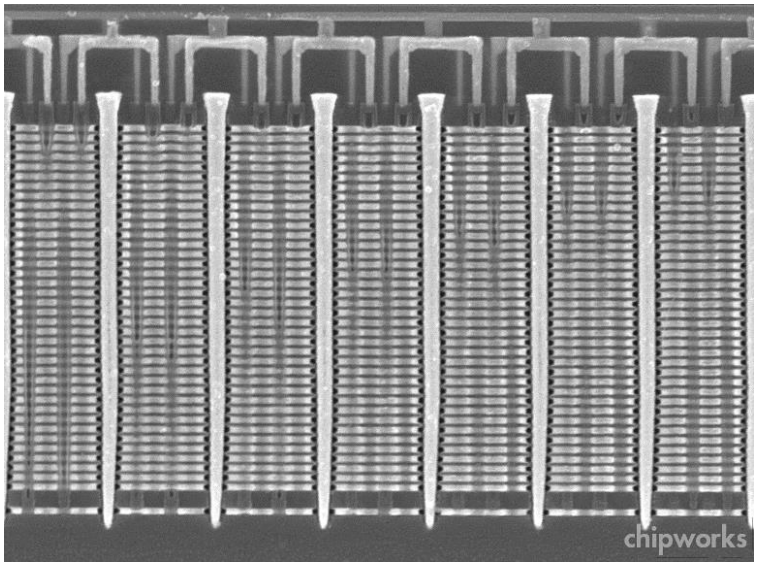
- **步进器/Stepper**
  - 制造设施中最昂贵的设备/Most expensive equipment in fabrication facility
  - 速率限制过程步骤/Rate limiting process step
    - 18s / wafer
  - 每步暴露858 mm2/Expose 858 mm^2 per step
    - 芯片面积的1.2%/1.2% of chip area

制造业经济学/Fabrication Economics

- 目前/Currently
  - 固定数量的光刻步骤/Fixed number of lithography steps
  - 制造成本10–20美元/芯片/Manufacturing cost $10–$20 / chip
    - 包括设施摊销/Including amortization of facility
- 制造1000000个物理层/Fabricating 1,000,000 physical layers
  - 无法在每个步骤上进行光刻/Cannot do lithography on every step
- 选项/Options
  - 化学自组装/Chemical self assembly
    - 设备通过化学过程自行生成/Devices generate themselves via chemical processes
  - 一次填充多个图层/Pattern multiple layers at once

三星V-Nand Flash示例/Samsung V-Nand Flash Example





- 建立未加图案的材料层/Build up layers of unpatterned material
- 然后使用光刻技术在所有层上切片、钻孔、蚀刻和沉积材料/Then use lithography to slice, drill, etch, and deposit material across all layers
- 约30个masking步骤/~30 total masking steps
- 多达48层存储单元/Up to 48 layers of memory cells
- 利用闪存电路的特殊结构/Exploits particular structure of flash memory circuits

迎接功耗限制/Meeting Power Constraints

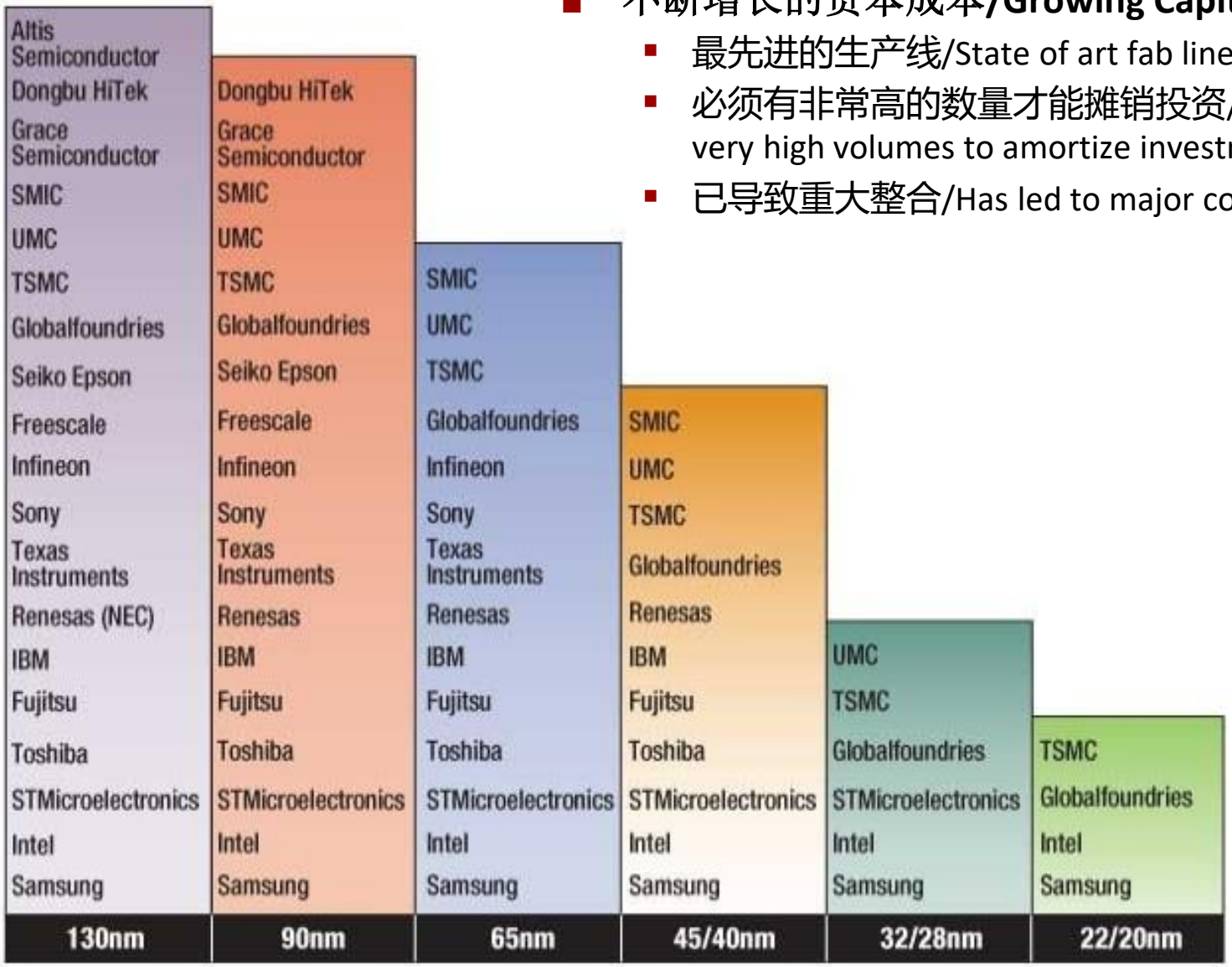
- 2 B transistors/晶体管
- 2 GHz operation/主频
- 1—5 W

- 64 B neurons/神经元
- 100 Hz operation/主频
- 15—25 W
  - 水冷/Liquid cooling
  - 高达身体总能耗的25%/Up to 25% body's total energy consumption

我们可以在不增加功率需求的情况下将设备数量增加50000x吗？ Can we increase number of devices by 500,000x without increasing power requirement?

摩尔定律的挑战：经济/Challenges to Moore's Law: Economic

- 不断增长的资本成本/**Growing Capital Costs**
  - 最先进的生产线/State of art fab line ~$20B
  - 必须有非常高的数量才能摊销投资/Must have very high volumes to amortize investment
  - 已导致重大整合/Has led to major consolidations

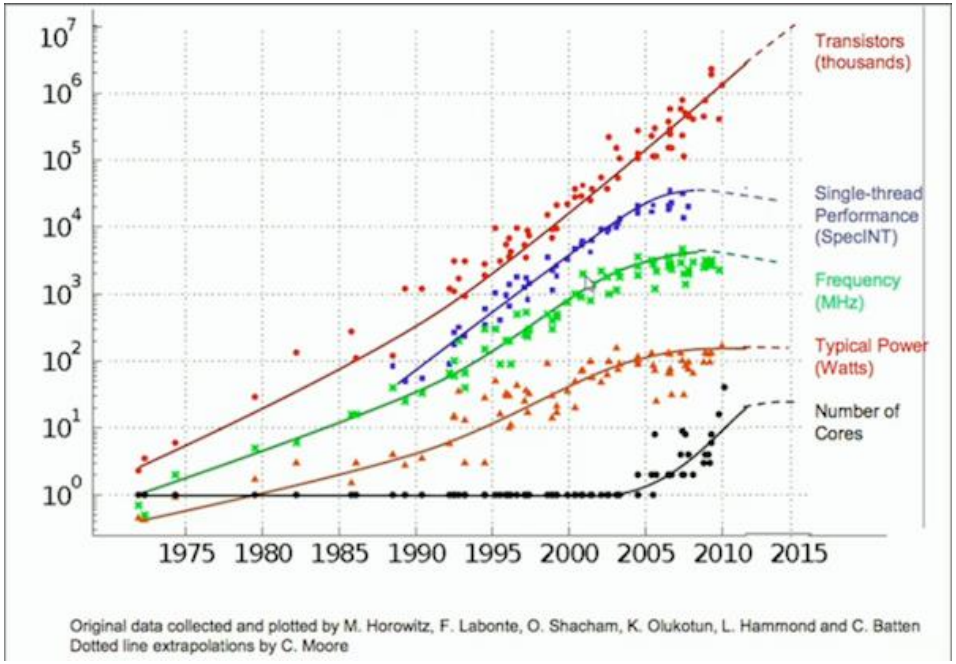


Dennard缩放定理/Dennard Scaling

- Robert Dennard 1974年在IBM工作期间提出/Due to Robert Dennard, IBM, 1974
- 量化摩尔定律的好处/Quantifies benefits of Moore's Law

- **如何缩小IC制造工艺/How to shrink an IC Process**
  - 在横向和纵向两个维度上缩小k倍/Reduce horizontal and vertical dimensions by *k*
  - 电压降低k倍/Reduce voltage by *k*
- **结果/Outcomes**
  - 晶体管密度增加k^2/Devices / chip increase by k^2
  - 核心频率增加k/Clock frequency increases by *k*
  - 单位面积功耗保持不变/Power / chip constant
- **关键点/Significance**
  - 增加了容量和性能/Increased capacity and performance
  - 功耗没有增加/No increase in power

Dennard缩放定理的终结/End of Dennard Scaling



- 发生了什么事情？/What Happened?
  - 电压不能低于~1V/Can't drop voltage below ~1V
  - 2004年已达到每个芯片的功率极限/Reached limit of power / chip in 2004
  - 片上有了更多的逻辑资源，但是却不能跑得更快/More logic on chip (Moore's Law), but can't make them run faster
    - 结果就是增加每个芯片上的核数/Response has been to increase cores / chip

Final Thoughts

- **与未来相比，过去50年似乎相当简单/Compared to future, past 50 years will seem fairly straightforward**
  - 使用光刻技术在二维表面上对晶体管进行构图的50年/50 years of using photolithography to pattern transistors on two-dimensional surface
- **关于未来集成系统的问题/Questions about future integrated systems**
  - 我们是否可以建造这样一个系统？/Can we build them?
  - 这是一个什么样的技术？/What will be the technology?
  - 它们在商业上可行吗？/Are they commercially viable?
  - 我们能保持低功耗吗？/Can we keep power consumption low?
  - 我们将如何处理它们？/What will we do with them?
  - 我们将如何编程/定制它们？/How will we program / customize them?