

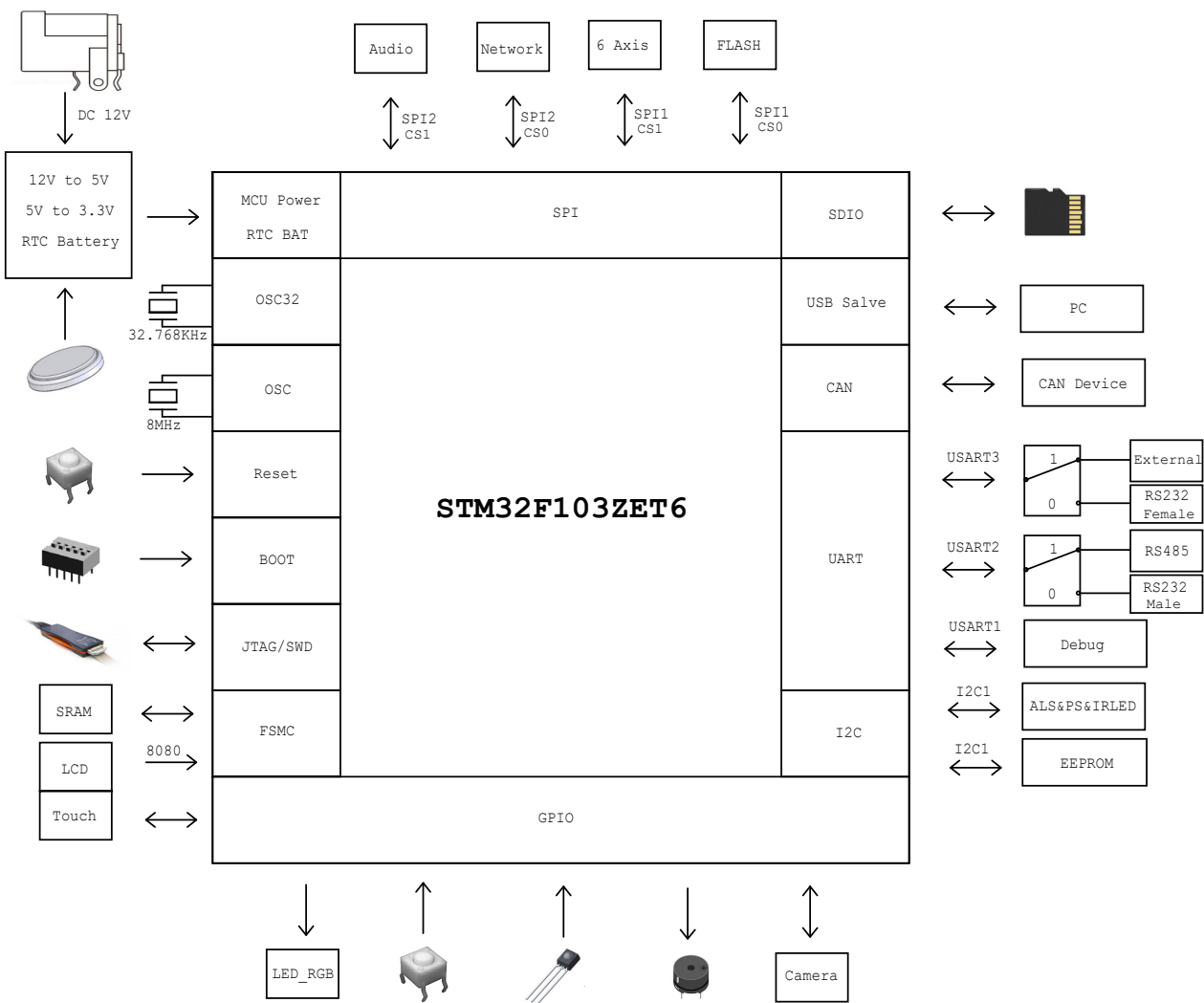
Block Diagram

D

C

B

A



Contents

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03	Boot & JTAG & Clock & Reset
04	Power
05	Modules
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09	Network
10	Audio
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Revision History

Date	Revision	Change Note
20200601	100ASK_STM32F103_V1.0	First editor
20201201	100ASK_STM32F103_V1.1	Second improvement
20210116	100ASK_STM32F103_V1.2	Third improvement

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Title:

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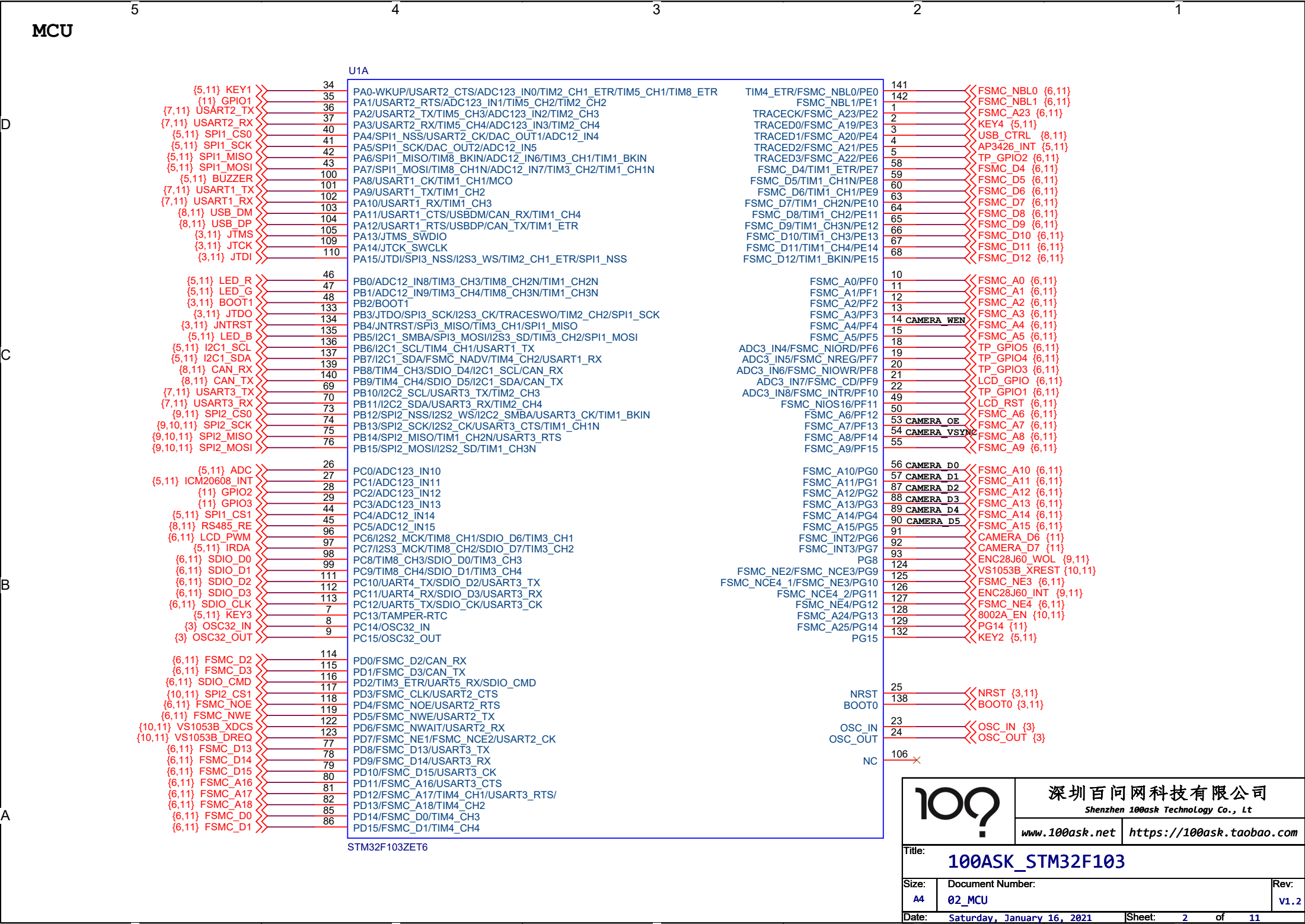
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Document Number: 01_Block Diagram

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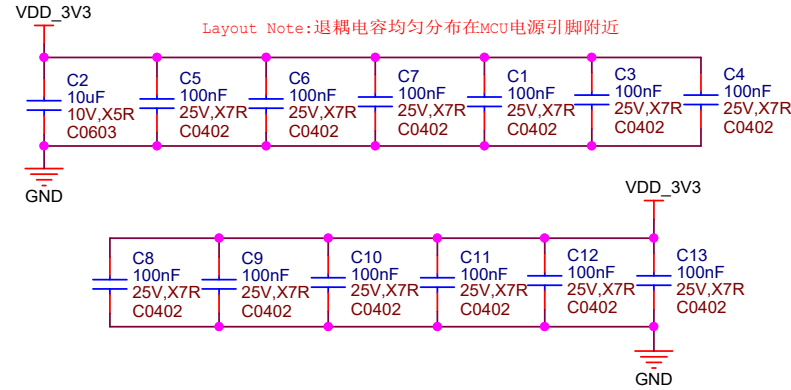
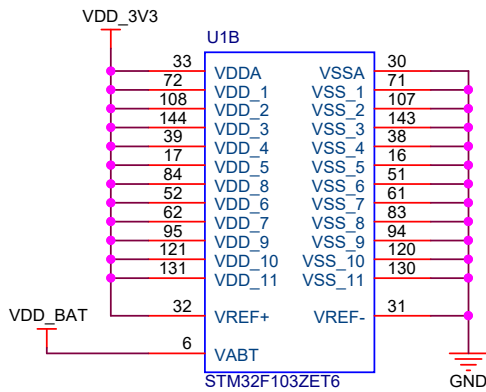
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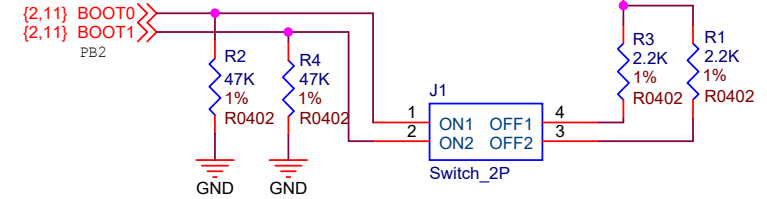
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Date: Saturday, January 16, 2021	Sheet: 2	of 11

MCU Power

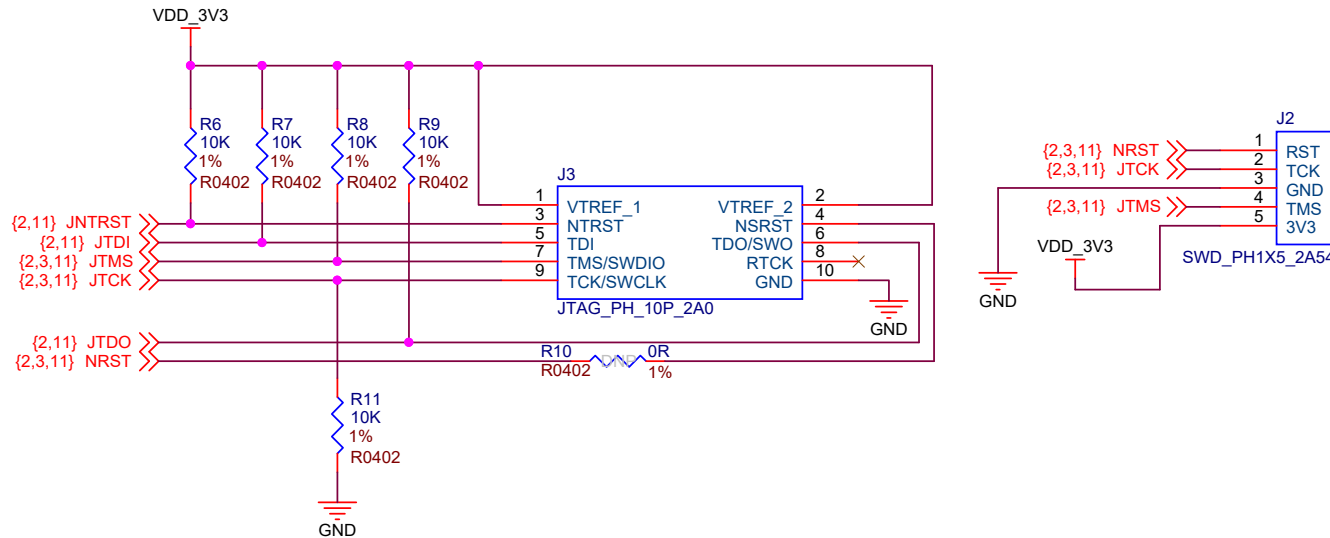


Boot Configure

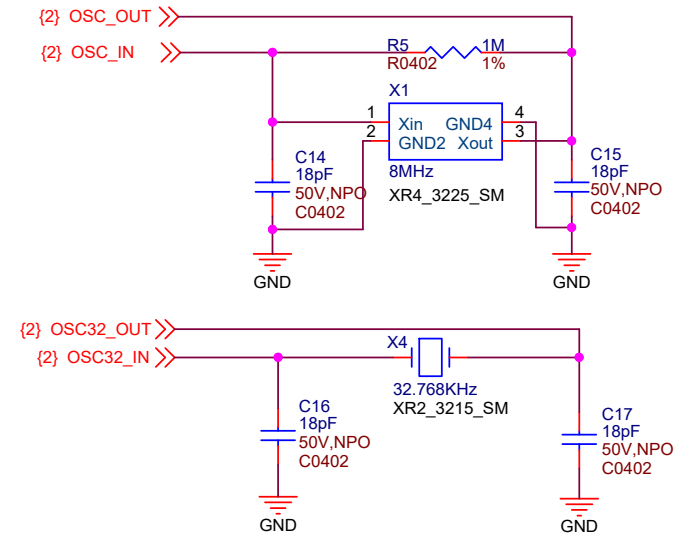


J1-1 (BOOT0)	J1-2 (BOOT1)	Description
OFF	*	Main Flash memory(Default)
ON	OFF	System memory
ON	ON	Embedded Memory(Debug)

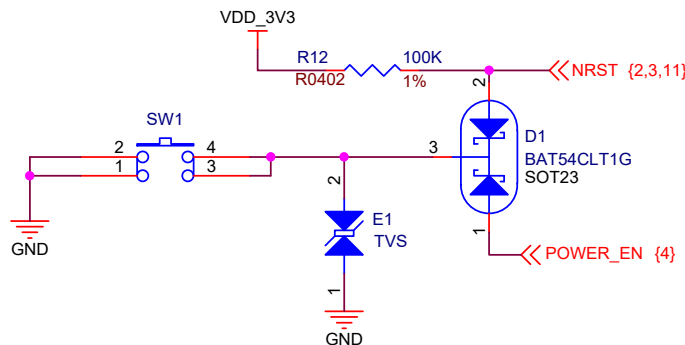
JTAG & SWD



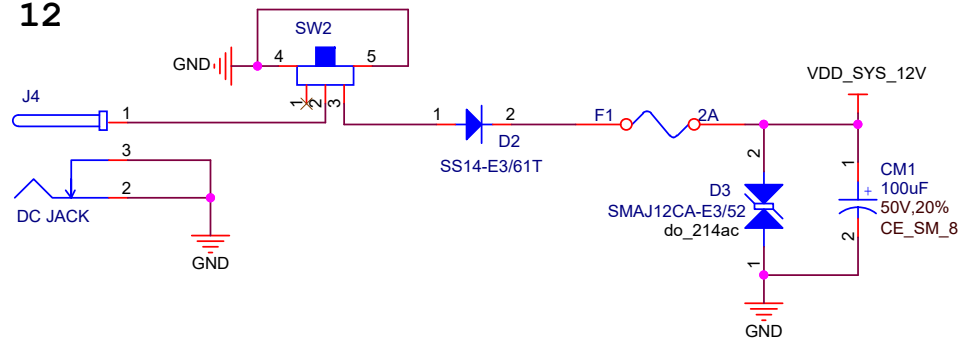
Clock



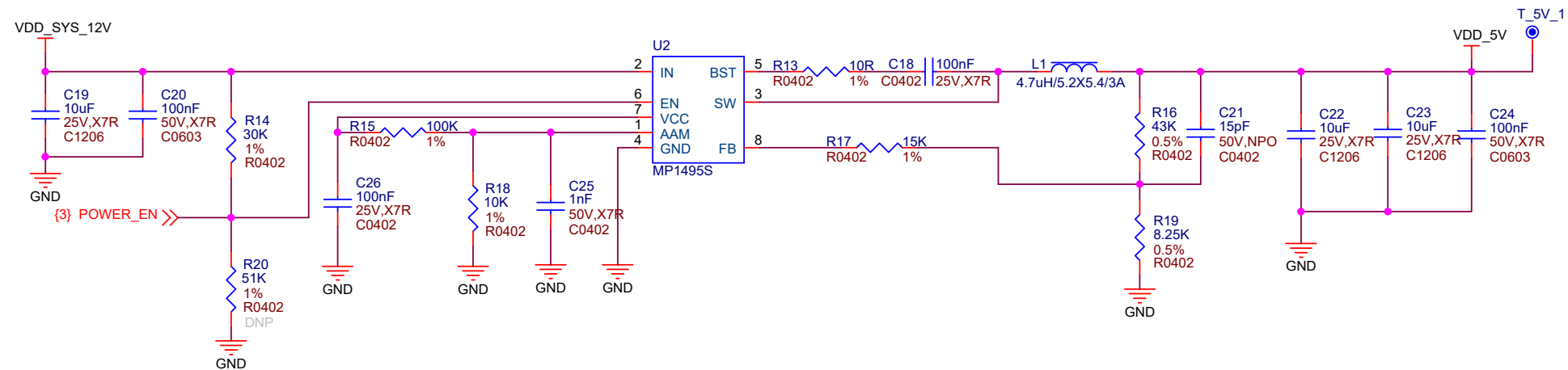
Reset



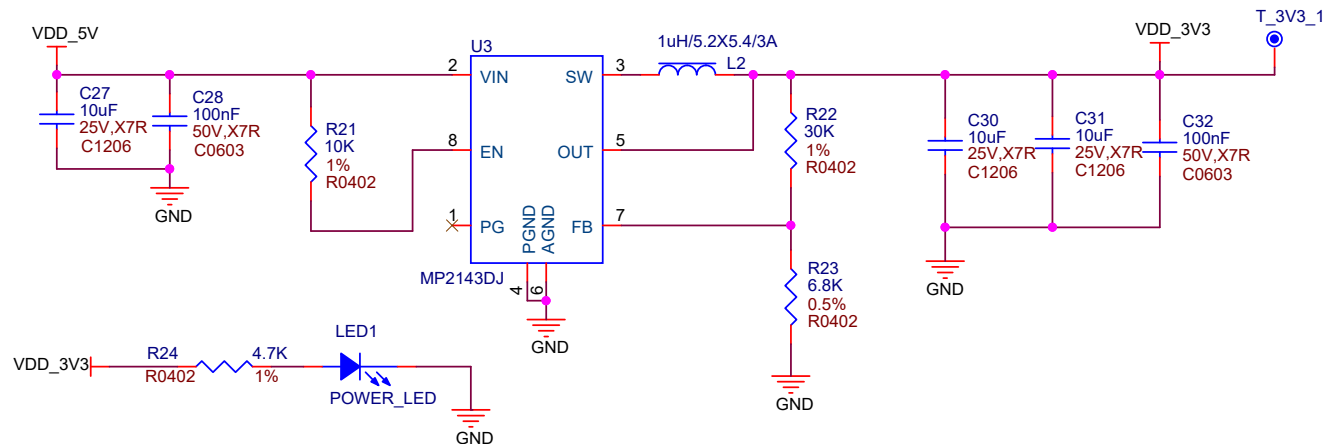
DC IN 12



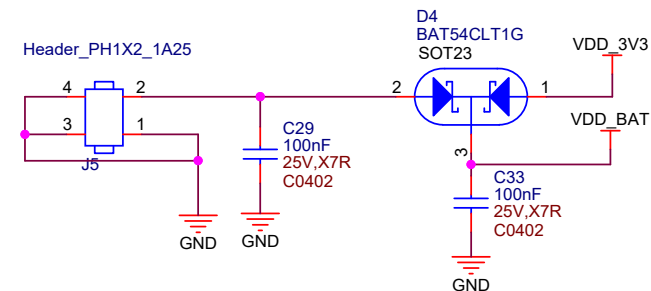
DC 12V to DC 5V



DC 5V to DC 3.3V



RTC BAT



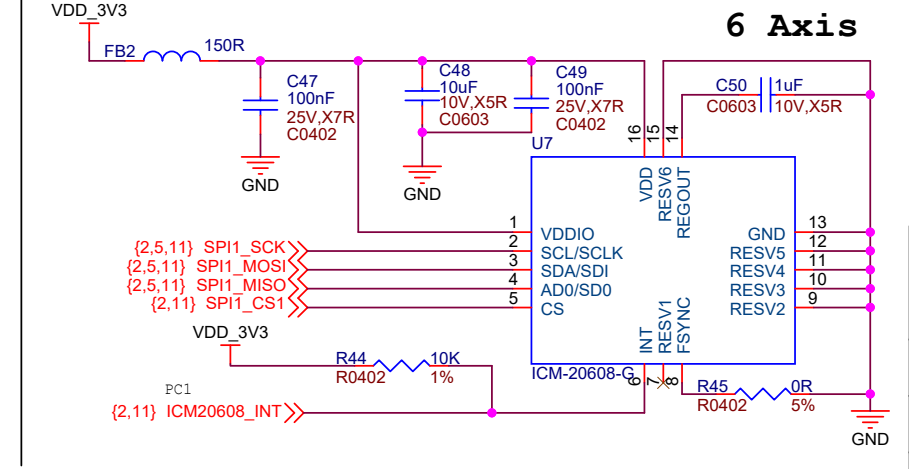
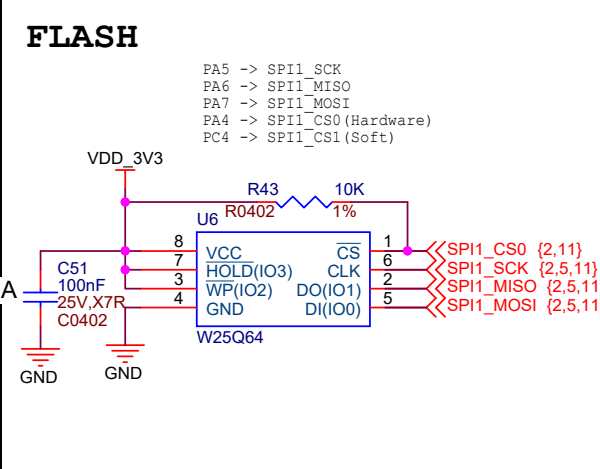
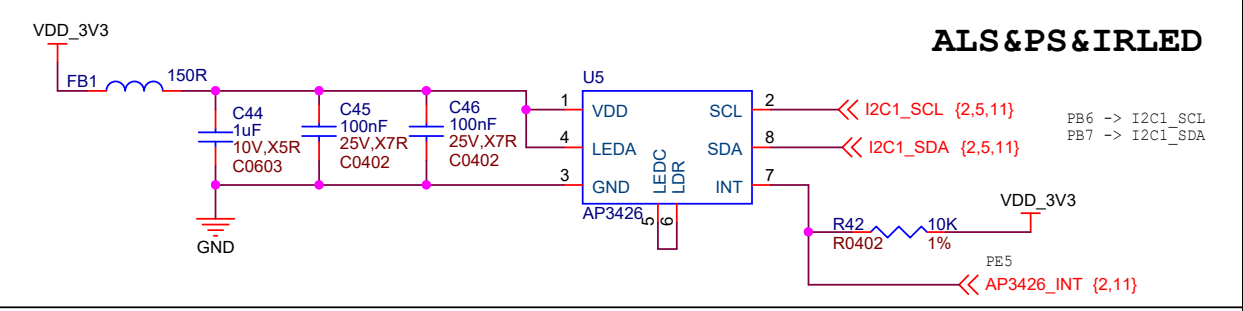
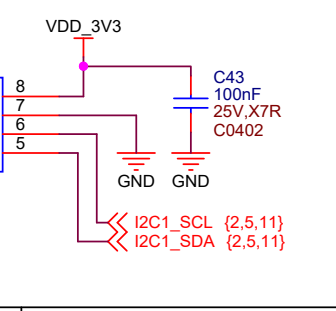
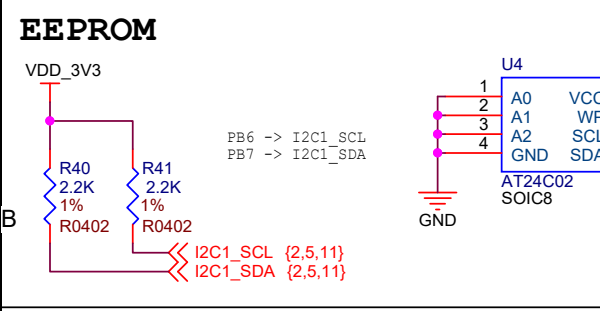
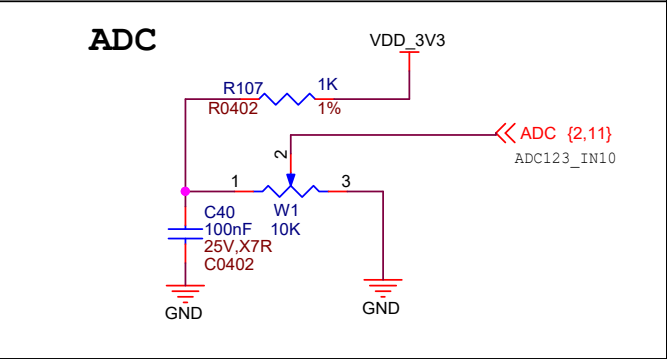
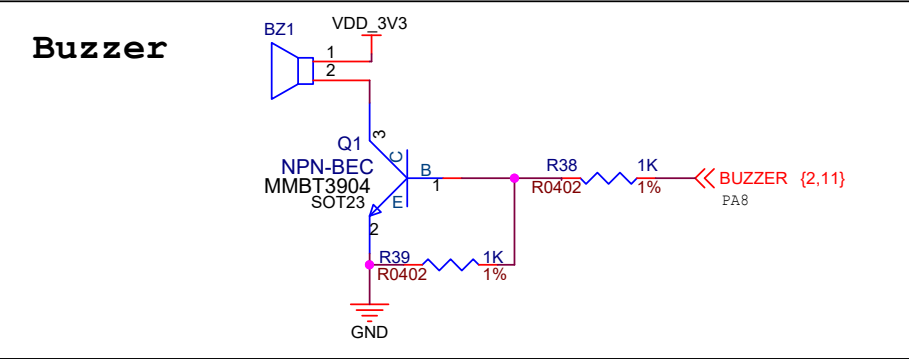
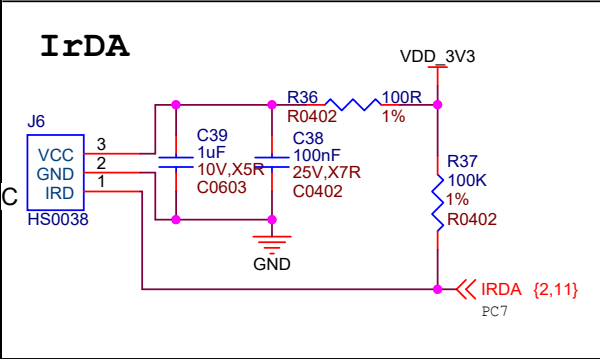
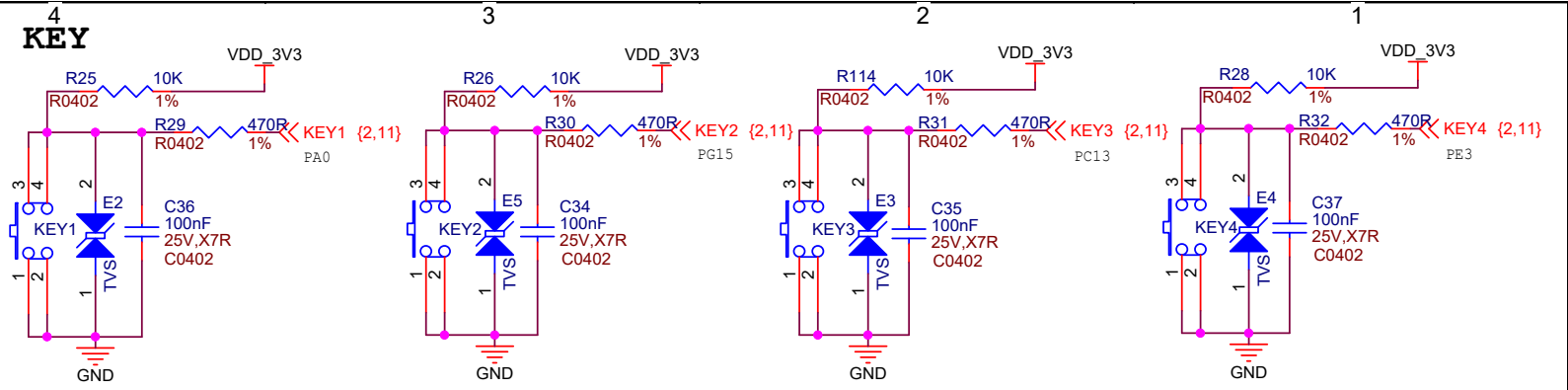
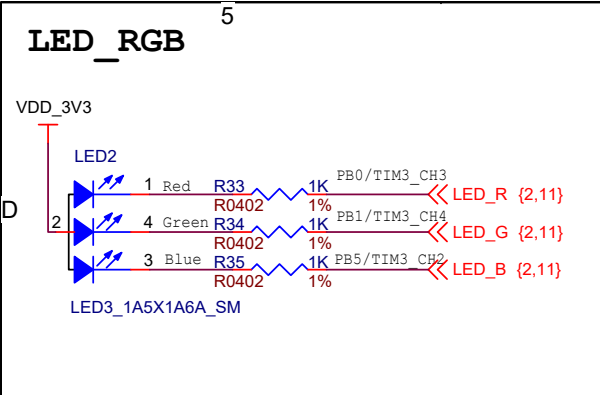
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Size: A4	Document Number: 04_Power	Rev: V1.2
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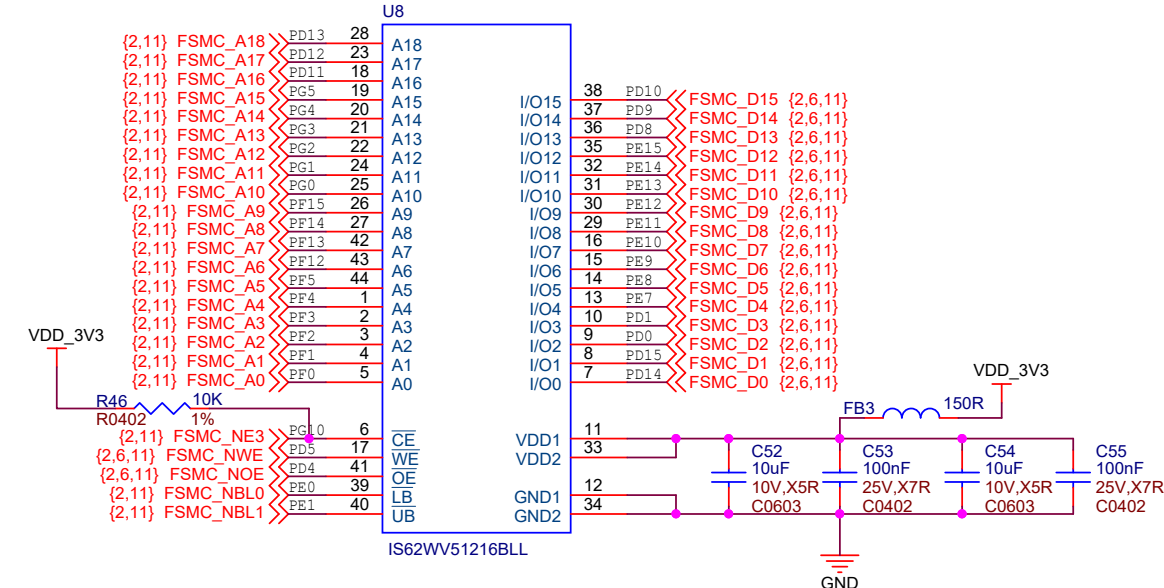
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Rev: V1.2

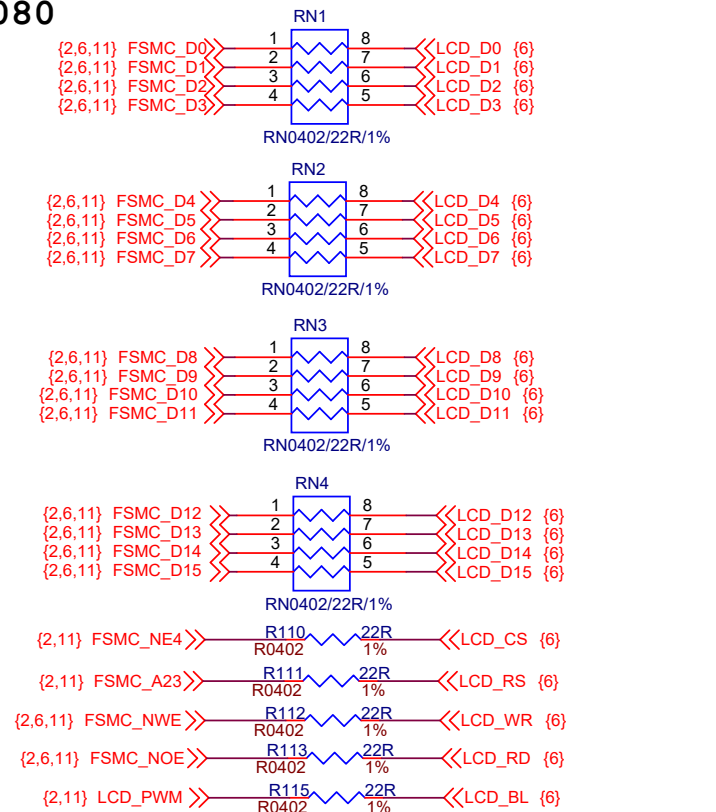
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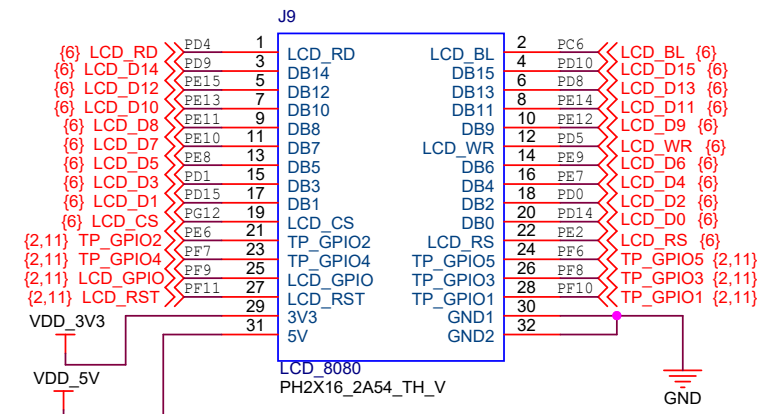
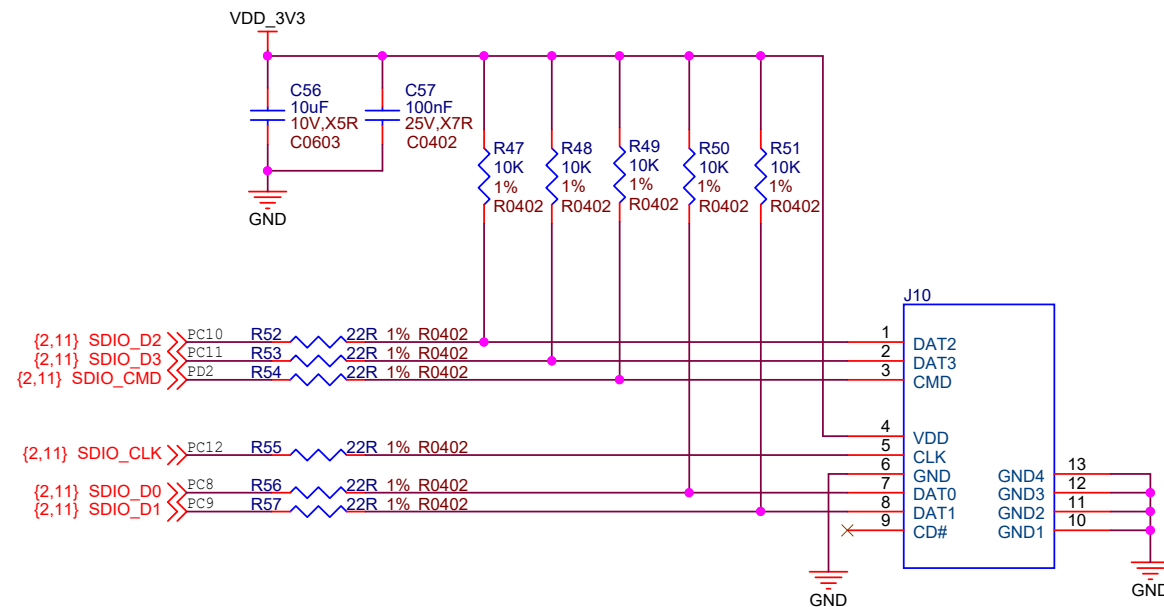
SRAM



LCD_8080



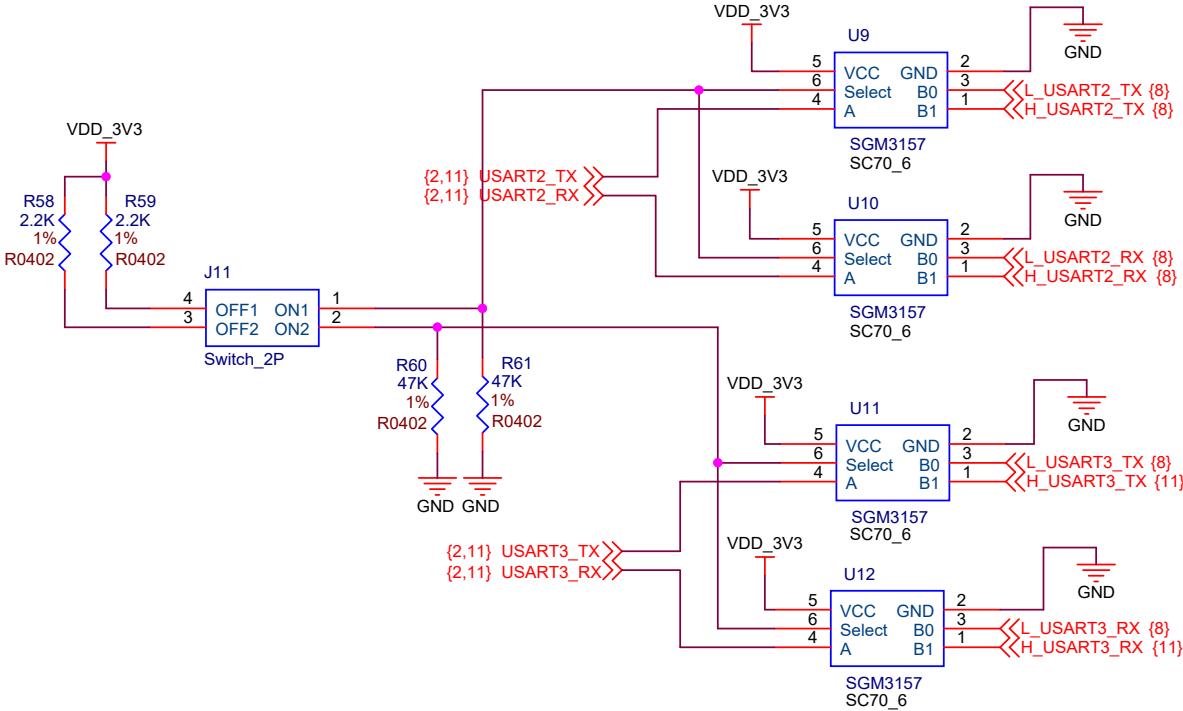
SD Card



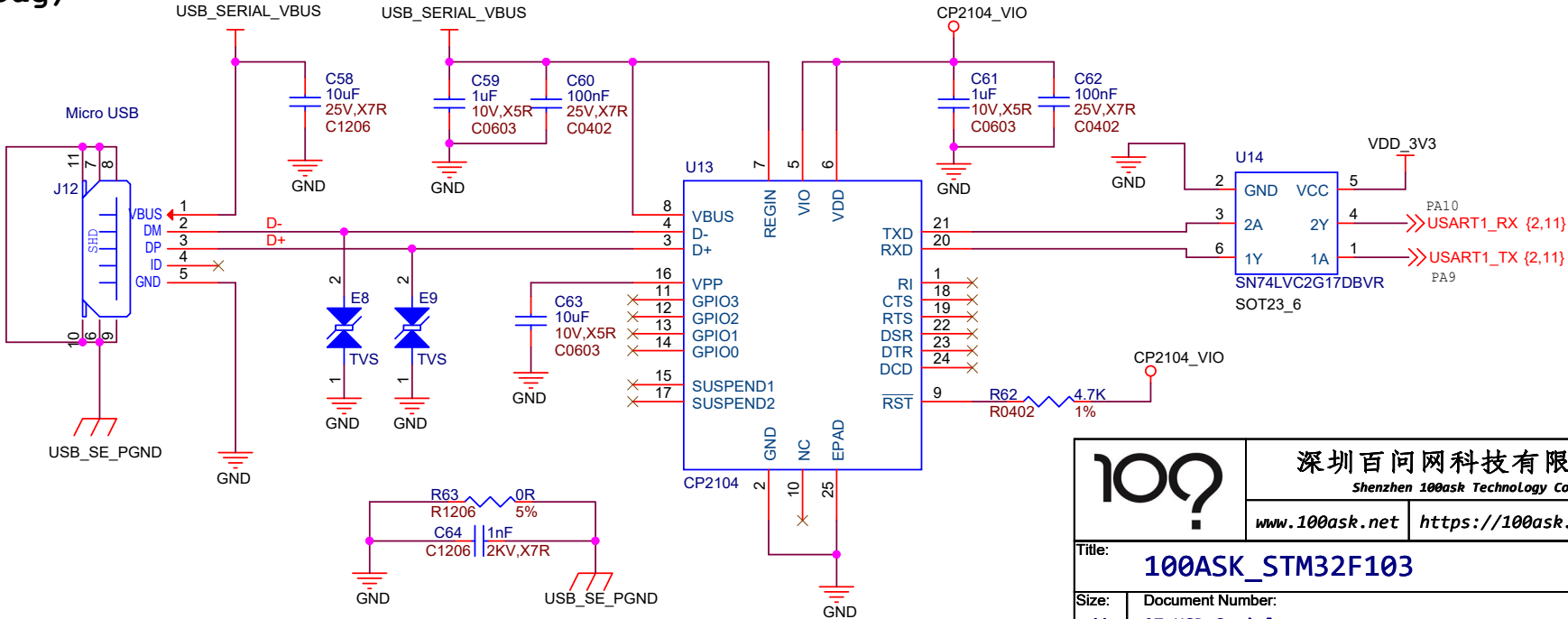
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Title: 100ASK_STM32F103		
Size: A4	Document Number: 06_SRAM & LCD & SD Card	Rev: V1.2
Date: Saturday, January 16, 2021	Sheet: 6 of 11	

USART Switch

J11-1	J11-2	Description
OFF	*	USART2 -> RS232 Male
ON	*	USART2 -> RS485
*	OFF	USART3 -> RS232 Female
*	ON	USART3 -> External



USB Serial (Debug)





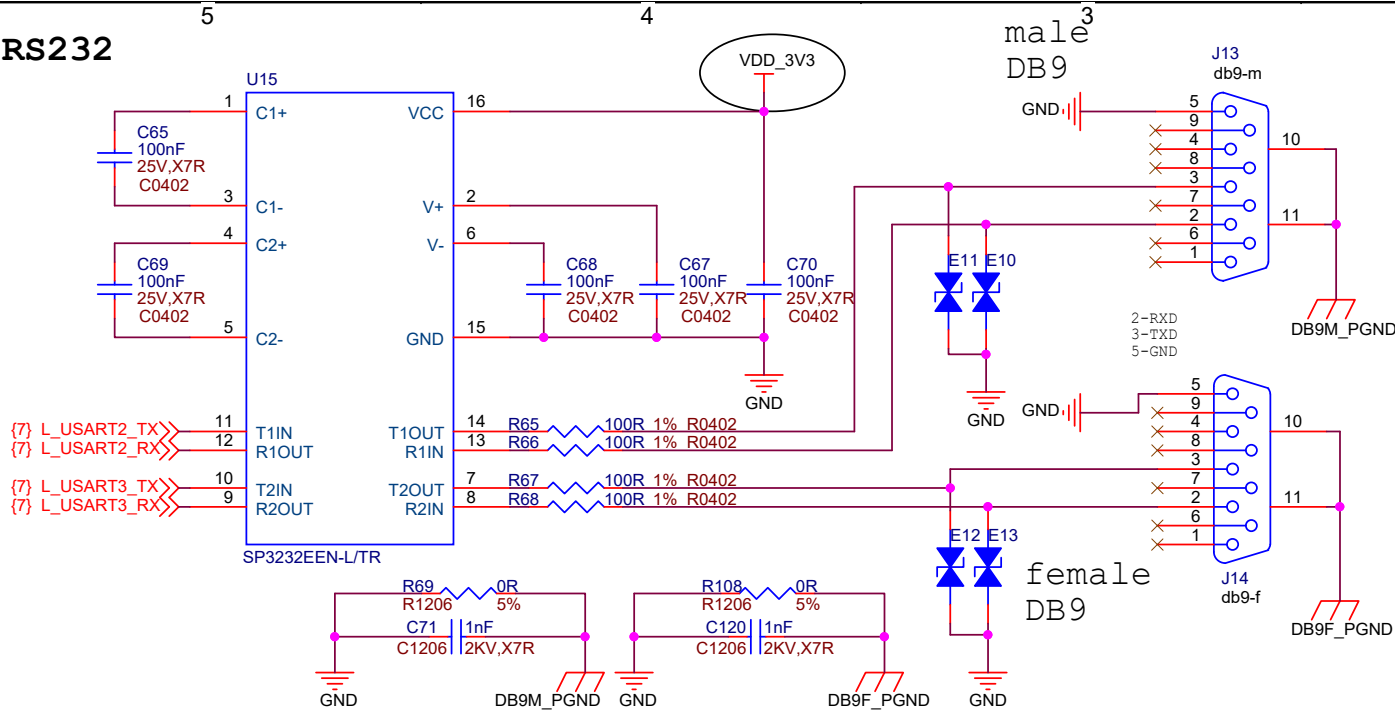
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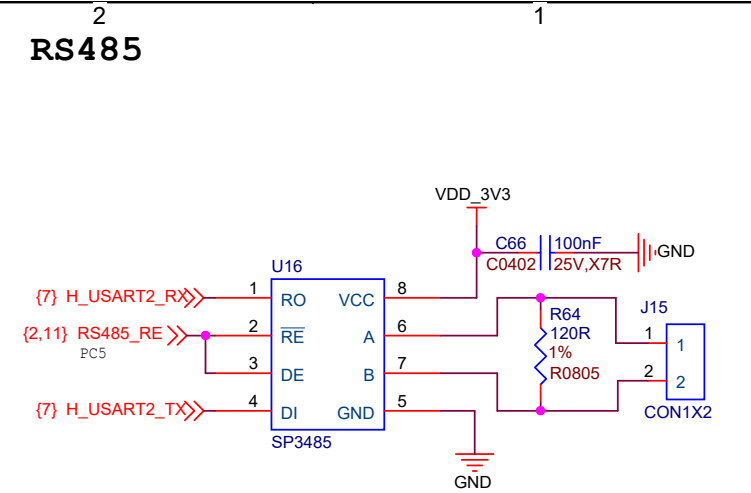
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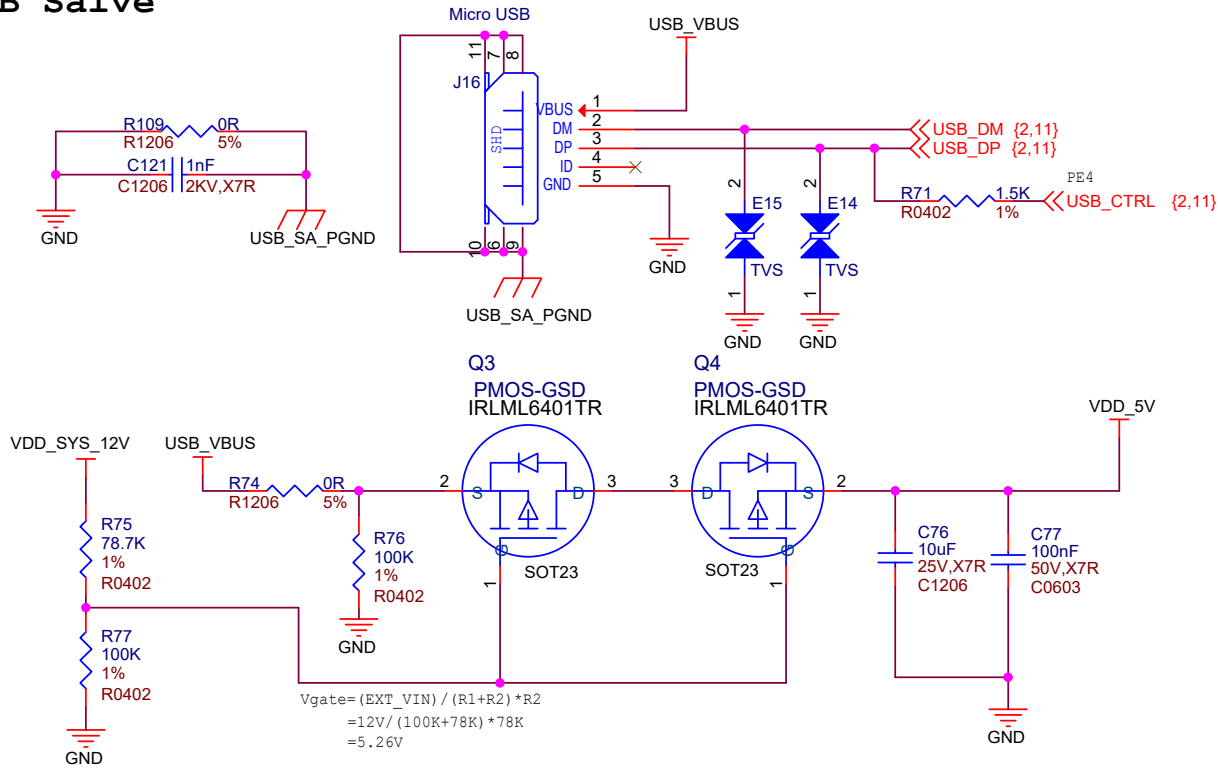
RS232



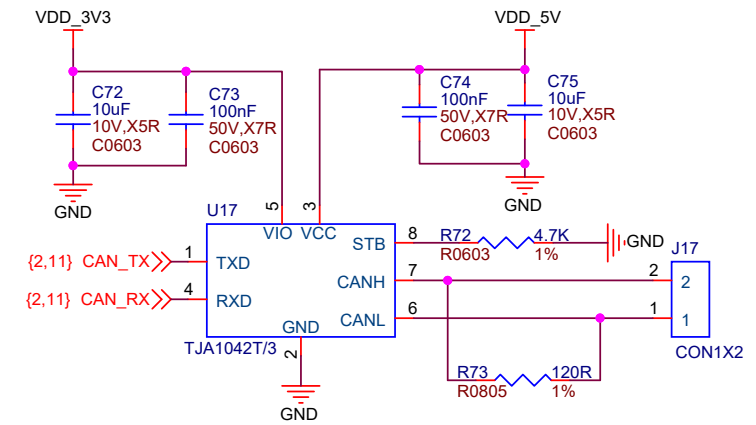
RS485



USB Salve



CAN



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Size: A4 Document Number: 08_RS232 & RS485 & CAN & USB

Rev: V1.2

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A



Audio Power

The diagram shows the internal circuit of an audio power amplifier. The central component is the RT9078-18GJ5 (U20), a SOT23_5 package. It is configured as a voltage follower. The non-inverting input (VIN) is connected to VDD_3V3 through a 10uF capacitor (C92). The output (OUT) is connected to CVDD through a 100nF capacitor (C95). The feedback network consists of a 150R resistor (FB8) and a 0R resistor (R94) connected to AGND. The IC is powered by VDD_5V and AVDD_5V, with decoupling capacitors C93 (22nF) and C94 (10uF) on the input and output lines respectively. The package is SOT23_5.

Earphone

huawei,iPhone: L+R+G+M

LINEIN R100 470R
R0603 1%

RIGHT

LEFT

R104 1K
R0603 1%

R105 1K
R0603 1%

C118 100nF
50V,X7R
C0603

C119 100nF
50V,X7R
C0603

AGND

AGND

J20
1 GND
2 MIC
3 R1
4 R2
5 L2
6 L1

PJ324B-P1

Amplifier

PG13

{2,11} 8002A_EN

R96 1K R0402 1%

R97 10K R0402 1%

U21

SHUTDOWN VO2 8

BYPASS GND 7

IN+ VCC 6

IN- VO1 5

8002A

R101 68K R0603 1%

C110 1uF C0603 10V,X5R

AGND

LEFT C113 220nF C0603 25V,X7R

R102 22K R0603 1%

RIGHT C115 220nF C0603 25V,X7R

AVDD_5V


C107 10uF C0603 10V,X5R

C108 100nF C0402 25V,X7R

AGND

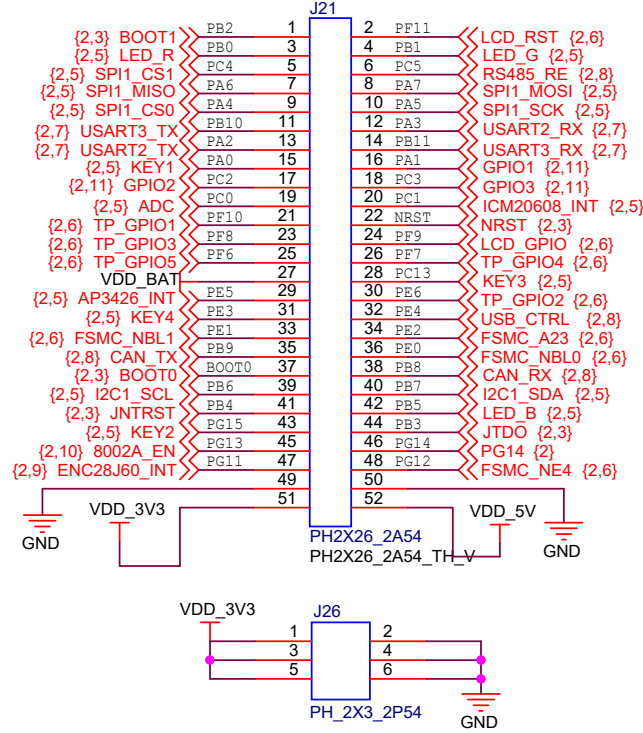
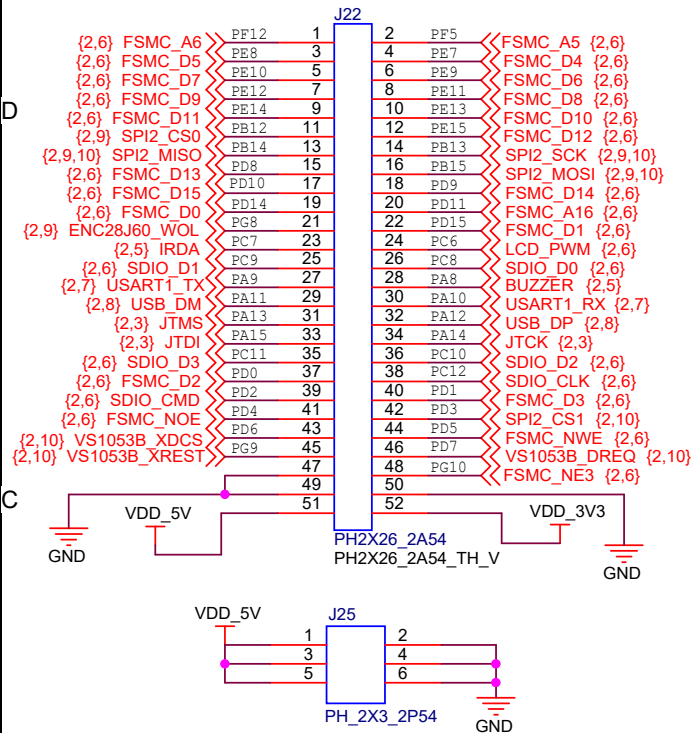
J19

SIP2_2_TH_V

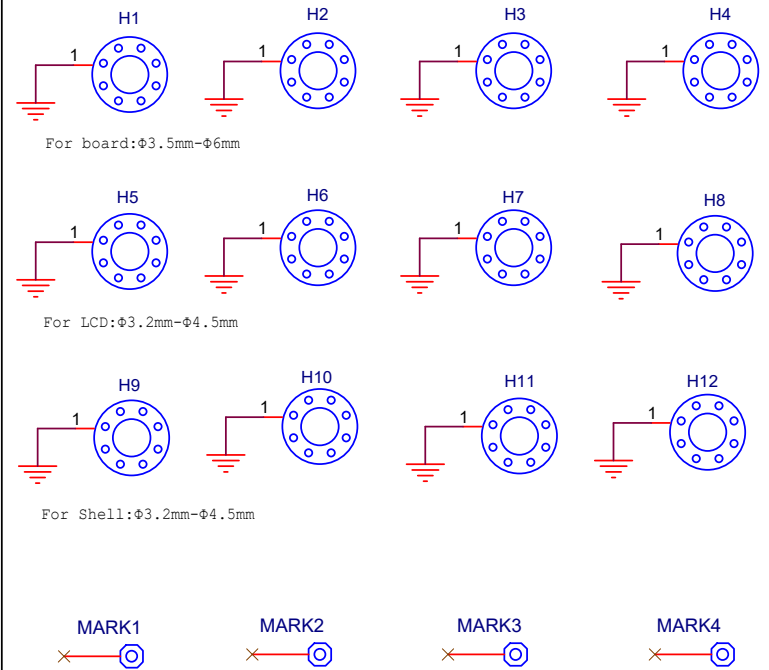
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Date: Saturday, January 16, 2021	Sheet: 10		of 11

GPIO Export

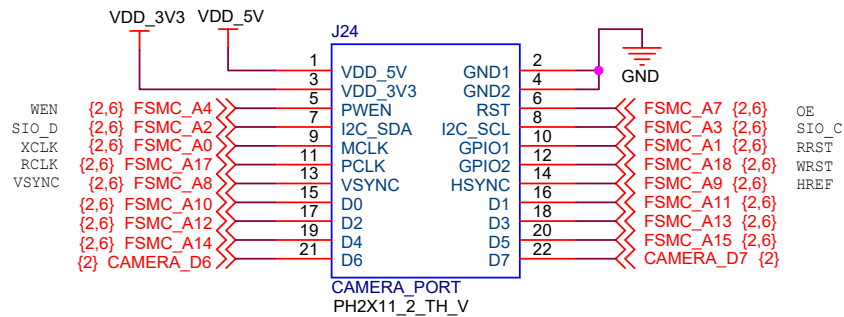
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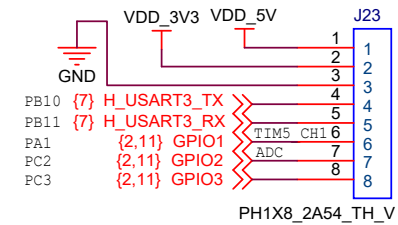
Hole



Camera



External Module



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Size: A4	Document Number: 11_GPIO Export & Camera	Rev: V1.2
Date: Saturday, January 16, 2021	Sheet: 11	of 11