

WENJI FANG

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RESEARCH INTERESTS

- Multimodal Circuit Foundation Model
- VLSI Design Quality Evaluation and Optimization
- Hardware Formal Verification

EDUCATION

Hong Kong University of Science and Technology	2024 – Present
<i>Ph.D.</i> in Electronic and Computer Engineering, advised by Prof. Zhiyao Xie	
Hong Kong University of Science and Technology (Guangzhou)	2022 – 2024
<i>M.Phil.</i> in Microelectronics, advised by Prof. Hongce Zhang and Prof. Zhiyao Xie	
Nanjing University of Aeronautics and Astronautics	2017 – 2021
<i>B.Eng.</i> in Electrical Engineering and Automation	

LEADING RESEARCH PROJECTS

Multimodal Circuit Foundation Model

Pre-training general multimodal circuit foundation model for various downstream tasks:

- *NetTAG*, a netlist foundation model fusing gate textual semantics using LLMs and circuit graph structure using graph transformer, published in **DAC’25**.
- *CircuitFusion*, an RTL foundation model fusing RTL code, operator graph, and functionality summary, published in **ICLR’25**.
- *CircuitEncoder*, exploring RTL-netlist cross-stage alignment, to appear in **ASPDAC’25**.
- *Large Circuit Model* (positional paper), published in **SCIS’24**.

RTL-Stage PPA Evaluation for Early Optimization

Predicting post-synthesis PPA metrics for RTL designs, enabling early optimization:

- *RTL-Timer*, the first RTL-stage fine-grained timing slack prediction tool, enabling RTL-stage timing optimizations, published in **DAC’24**.
- *MasterRTL*, an RTL-stage overall PPA estimation framework based on bit-level circuit representation, supporting transferred across technology library and corners, published in **ICCAD’23&TCAD’24**.

Hardware Formal Property Verification

Towards automatic and scalable hardware verification:

- *AssertLLM*, hardware verification assertions generation using LLM, to appear in **ASPDAC’25**.
- *WASIM*, a word-level abstract symbolic simulator on RTL, supporting formal property verification for processors, published in **TACAS’23&TCAD’23**.

FIRST-AUTHORED PUBLICATIONS

Conference:

1. **Wenji Fang**, Wenkai Li, Shang Liu, Yao Lu, Hongce Zhang and Zhiyao Xie, “NetTAG: A Multimodal RTL-and-Layout-Aligned Netlist Foundation Model via Text-Attributed Graph”, *IEEE/ACM Design Automation Conference (DAC)*, 2025.
2. **Wenji Fang**, Shang Liu, Jing Wang, and Zhiyao Xie, “CircuitFusion: Multimodal Circuit Representation Learning for Agile Chip Design”, *International Conference on Learning Representations (ICLR)*, 2025.

3. **Wenji Fang**, Shang Liu, Hongce Zhang, and Zhiyao Xie, “A Self-Supervised, Pre-Trained, and Cross-Stage-Aligned Circuit Encoder Provides a Foundation for Various Design Tasks”, *IEEE/ACM Asian and South Pacific Design Automation Conference (ASPDAC)*, 2025.
4. Zhiyuan Yan*, **Wenji Fang***, Mengming Li, Min Li, Shang Liu, Zhiyao Xie, and Hongce Zhang, “AssertLLM: Generating Hardware Verification Assertions from Design Specifications via Multi-LLMs”, *IEEE/ACM Asian and South Pacific Design Automation Conference (ASPDAC)*, 2025.
5. Shang Liu*, Yao Lu*, **Wenji Fang***, Mengming Li, and Zhiyao Xie, “OpenLLM-RTL: Open Dataset and Benchmark for LLM-Aided Design RTL Generation (Invited)”, *IEEE/ACM International Conference on Computer Aided Design (ICCAD)*, 2024.
6. **Wenji Fang**, Shang Liu, Hongce Zhang, and Zhiyao Xie, “Annotating Slack Directly on Your Verilog: Fine-Grained RTL Timing Evaluation for Early Optimization”, *IEEE/ACM Design Automation Conference (DAC)*, 2024.
7. **Wenji Fang**, Yao Lu, Shang Liu, Qijun Zhang, Ceyu Xu, Lisa Wu Wills, Hongce Zhang, and Zhiyao Xie, “MasterRTL: A Pre-Synthesis PPA Estimation Framework for Any RTL Design”. *IEEE/ACM International Conference on Computer Aided Design (ICCAD)*, 2023.
8. **Wenji Fang**, and Hongce Zhang, “WASIM: A Word-level Abstract Symbolic Simulation Framework for Hardware Formal Verification”, *International Conference on Tools and Algorithms for the Construction and Analysis of Systems (TACAS)*, 2023.

Journal:

1. **Wenji Fang**, Yao Lu, Shang Liu, Qijun Zhang, Ceyu Xu, Lisa Wu Wills, Hongce Zhang, and Zhiyao Xie, “Transferable Pre-Synthesis PPA Estimation for RTL Designs With Data Augmentation Techniques”, *IEEE Transactions on Computer Aided Design of Integrated Circuits and systems (TCAD)*, 2024.
2. **Wenji Fang**, Guangyu Hu, and Hongce Zhang, “r-map: Relating Implementation and Specification in Hardware Refinement Checking”, *IEEE Transactions on Computer Aided Design of Integrated Circuits and systems (TCAD)*, 2023.

EXPERIENCE

Hong Kong University of Science and Technology (Guangzhou)	Dec. 2021 – Jul. 2022
Research Assistant Advisor: Prof. Hongce Zhang	
Formal property verification of microprocessors	
Peng Cheng National Laboratory	Jul. 2021 – Dec. 2021
Digital IC Physical Design Intern Mentor: Dr. Biwei Xie & Prof. Yungang Bao	
Logic synthesis & physical design of an SoC and tape-out	

HONORS AND AWARDS

DAC Young Fellow	2024
LAD Best Paper Nomination	2024
Full Postgraduate Studentship, HKUST	2024-Present
ICCAD Student Scholar Program	2023
3rd Place Award of EDathon Contest	2023
Full Postgraduate Studentship, HKUST(GZ)	2022-2024
Infineon Technology Scholarship	2020
Academic Scholarship, NUAA	2017-2021