TrIM: <u>Tri</u>angular <u>I</u>nput <u>M</u>ovement Systolic Array for Convolutional Neural Networks—Part I: Dataflow and Analytical Modelling

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Abstract—In order to follow the ever-growing computational complexity and data intensity of state-of-the-art AI models, new computing paradigms are being proposed. These paradigms aim at achieving high energy efficiency, by mitigating the Von Neumann bottleneck that relates to the energy cost of moving data between the processing cores and the memory. Convolutional Neural Networks (CNNs) are particularly susceptible to this bottleneck, given the massive data they have to manage. Systolic Arrays (SAs) are promising architectures to mitigate the data transmission cost, thanks to high data utilization carried out by an array of Processing Elements (PEs). These PEs continuously exchange and process data locally based on specific dataflows (like weight stationary and row stationary), in turn reducing the number of memory accesses to the main memory. The hardware specialization of SAs can meet different workloads, ranging from matrix multiplications to multi-dimensional convolutions. In this paper, we propose TrIM: a novel dataflow for SAs based on a Triangular Input Movement and compatible with CNN computing. When compared to state-of-the-art SA dataflows, like weight stationary and row stationary, the high data utilization offered by TrIM guarantees $\sim 10\times$ less memory access. Furthermore, considering that PEs continuously overlap multiplications and accumulations, TrIM achieves high throughput (up to 81.8% higher than row stationary), other than requiring a limited number of registers (up to $15.6\times$ fewer registers than row stationary).

Index Terms—Artificial Intelligence, Convolutional Networks, Systolic Arrays, Weight Stationary, Data Utilization, Memory Accesses.

I. INTRODUCTION

NOWADAYS, Artificial Intelligence (AI) is a pervasive paradigm that has changed the way devices can assist everyday activities. However, in order to continuously meet high standards of accuracy, AI models are becoming ever more data-intensive, particularly when Deep Neural Networks (DNNs) are considered. Indeed, other than demanding a huge amount of computations, DNNs also require high memory capacity to manage learned weights, as well as inputs and outputs [1].

Convolutional Neural Network (CNN) [2] is an example of data-intensive DNN, since it executes convolutions on multi-dimensional arrays, named *feature maps*, to carry out

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tasks like image classification [3], image segmentation [4], [5], image generation [6], [7], object detection [8], [9] and speech recognition [10], [11]. Conventionally, Central Processing Units (CPUs) and Graphics Processing Units (GPUs) manage CNNs' workloads. However, these architectures suffer from the Von Neumann bottleneck [12], owing to the physical separation between the computing core and the memory. This significantly degrades the energy efficiency, given that data should be first fetched from an external Dynamic Random Access Memory (DRAM), then buffered on-chip, and finally processed by the computing core. For example, the normalized DRAM energy cost from a commercial 65nm process is $200\times$ higher than the cost associated to a Multiply-Accumulation (MAC) [13], which is the elementary operation performed by the computing core. High data utilization [14] is a way to mitigate such cost, by allowing inputs, weights, or partial sums (psums) to be held on-chip as long as they need to be consumed.

Systolic Arrays (SAs) are representative architectures that maximize data utilization by using an array of Processing Elements (PEs) interconnected with each other [15]. Data moves rhythmically, thus evoking the blood flow into the cardiovascular system, hence the term *systolic*. Conceived late 1970s [16], they have been mainly used for matrix multiplications. In recent years, the research community has put effort to allow SAs to meet the CNN's workflow [17]–[19]. For instance, the Convolution to General Matrix Multiplication conversion (Conv-to-GeMM) [20] introduces data redundancy to make inputs compliant with the SAs' dataflows. However, this reflects in higher memory requirements and, in turn, a higher number of memory accesses, thus negatively impacting area and energy. Weight Stationary (WS) based SAs are examples of architectures using Conv-to-GeMM. Inputs are moved and reused in one direction along the array, while weights are kept stationary. However, First-In-First-Out (FIFO) buffers must assist the data transfer from/to the memory, thus negatively affecting area, power and energy. The Google Tensor Processing Unit (TPU) is a WS-based SA consisting of 256×256 PEs, which outperforms CPUs and GPUs by $30\times$ in terms of energy efficiency [21]. In the Row Stationary (RS) dataflow [13], rows of inputs and weights are reused at the PE level through dedicated memory blocks, without requiring Conv-to-GeMM conversion. In this case, data redundancy is moved at the array level, where inputs are shared diagonally over multiple PEs, while weights are shared horizontally. In addition, inputs and weights circulate cycle-by-

cycle inside each PE, thus reducing the energy efficiency, other than making the micro-architecture of PEs more complex. Finally, the area covered by the SA depends on the inputs' sizes, thus making the deployment of large-scale architectures a challenge. Eyeriss [22] is the pioneer RS-based SA and consists of 168 PEs, outperforming existing SAs from $1.4\times$ to $2.5\times$ in terms of energy efficiency.

To address the drawbacks of previous art, we propose TrIM, a new dataflow that exploits a triangular input movement to maximize input utilization. Advantageously, this results in less memory accesses without the need to introduce data redundancy. A generic SA dealing with TrIM consists of $K \times K$ PEs, where weights are kept stationary and psums are propagated vertically and finally accumulated by an extra adder tree. The TrIM-based SA is compatible with the computation requirements of Convolutional Layers (CLs). When compared to WS, TrIM exhibits one order of magnitude less memory accesses. Moreover, TrIM ensures high performance efficiency since each PE works at the peak throughput of 2 OPs/cycle. Finally, the micro-architecture of PEs is fairly simple, translating into a limited number of registers, up to $15.6\times$ lower than RS with a kernel size of 7.

The contributions of this work are summarized as follows:

- We introduce the TrIM dataflow, which allows high data utilization through a triangular movement of inputs, thus significantly reducing the number of memory accesses from the main memory if compared to previous art.
- We present an analytical model for TrIM and state-of-the-art dataflows (i.e., WS and RS), including metrics like memory accesses, latency, throughput, number of registers.
- Given the analytical model, a thorough design space evaluation is performed, based on several kernel sizes and feature map sizes. WS and RS dataflows are considered for comparisons.
- According to the design space evaluation, we discuss the key benefits offered by TrIM.

The remainder of this paper is structured as follows: Section II, after introducing CNNs, provides a background about SAs and specific dataflows to manage convolutions; Section III introduces the proposed TrIM dataflow; Section IV presents an analytical model to characterize TrIM, RS and WS; using the referred model, Section V presents an in-depth design space evaluation to spotlight the advantages of TrIM over its counterparts; finally, section VI concludes the paper. In order to ease the readability of this manuscript, Table I collects all the abbreviations.

II. BACKGROUND

A. Convolutional Neural Networks

A CNN consists of a sequence of CLs that extract features of interest from input data [23], by emulating the behavior of human visual cortex to retrieve patterns, such as shapes and edges, from images. The feature maps (fmaps) generated from the last CL are eventually processed by Fully-Connected Layers (FCLs) [24] for classification. As shown in Fig. 1(a) Each CL performs N three-dimensional convolutions between

TABLE I
LIST OF ABBREVIATIONS

Abbreviation	Meaning
AI	Artifical Intelligence
CL	Convolutional Layer
CNN	Convolutional Neural Network
Conv-to-GeMM	Convolution to General Matrix Multiplication Conversion
CPU	Central Processing Unit
DNN	Deep Neural Network
DRAM	Dynamic Random Access Memory
FCL	Fully-Connected Layer
FIFO	First-In-First-Out Buffer
fmap	Feature Map
FPGA	Field Programmable Gate Array
GeMM	General Matrix Multiplication
GPU	Graphics Processing Unit
H_I, W_I	Height and Width of the input fmap (ifmap)
H_O, W_O	Height and Width of the output fmap (ofmap)
I	ifmap linear size if square
IS	Input Stationary Dataflow
K_H, K_W, K	Kernel's Height, Width, Linear size if square
L	Latency
M	Number of kernels per filters/number of fmaps
MA	Memory Access
MAC	Multiply-Accumulation
N	Number of 3-D filters/number of ofmaps
OP	Number of operations
OS	Output Stationary Dataflow
PE	Processing Element
Reg	Number of Registers
RS	Row Stationary Dataflow
S	Convolutional Stride
SA	Systolic Array
SRAM	Static Random Access Memory
SRB	Shift Register Buffer
T	Throughput
TPE	Throughput per PE
TPU	Tensor Processing Unit
TrIM	Triangular Input Movement dataflow
WS	Weight Stationary Dataflow

M input fmaps (ifmaps), each consisting of a $H_I \times W_I$ plane, and N filters, each consisting of M kernels of $K_H \times K_W$ weights. In other words, each filter scans the M ifmaps through sliding windows with stride S. In the rest of the paper, we consider $K_H = K_W = K$ and $S = 1$ as in common CNNs for classification. As a result, N output fmaps (ofmaps), each $H_O \times W_O$ wide, are generated, with $H_O = H_I - K + 1$ and $W_O = W_I - K + 1$. Each output element is named activation and follows equation (1):

$$O_{n,h_o,w_o} = \sum_{m=0}^{M-1} \sum_{k_h=0}^{K-1} \sum_{k_w=0}^{K-1} I_{m,h_o+k_h,w_o+k_w} \times W_{n,m,k_h,k_w}$$

(1)

O identifies the generic output activation, I is the generic input activation and W is the generic weight belonging to a kernel of one filter; n iterates over the N ofmaps, h_o iterates
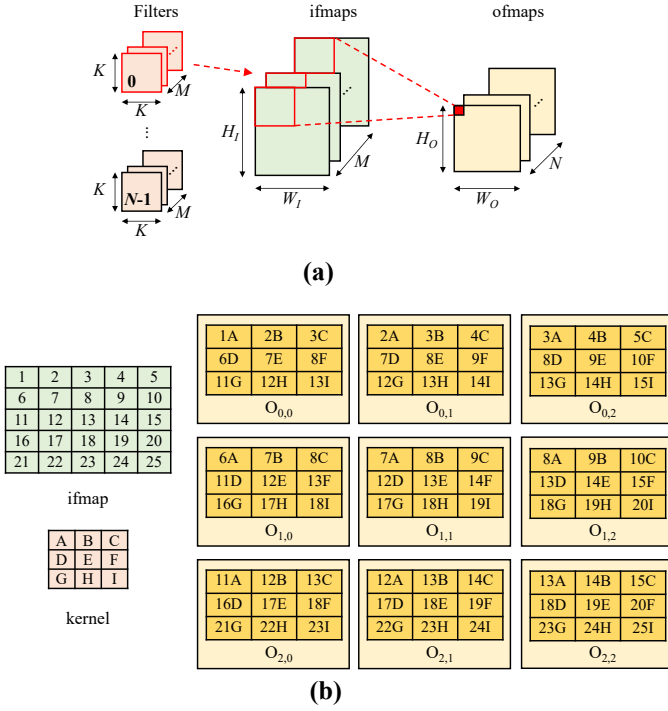
(a)

(b)

Fig. 1. Example of Convolutional Layer (CL): (a) a set of N three-dimensional filters are subjected to as many three-dimensional convolutions with M ifmaps. As a result, N ofmaps are generated. The portion of ifmaps highlighted in red is currently processed by the filters 0, in order to generate the red activation into the first ofmap; (b) example of two-dimensional convolution between a 5×5 ifmap and a 3×3 kernel. Each yellow box reports which multiplications are needed to generate the output $O_{i,j}$, with $0 \leq i, j < 3$.

over the H_O rows of each ofmaps, w_o iterates over the W_O elements belonging to each ofmap's row, m iterates over the M ifmaps, k_h and k_w iterate over the kernels' rows and columns, respectively. N biases can be eventually added to each output activation if required by the layer. Fig. 1(b) shows how a convolution between a 5×5 ifmap and a 3×3 kernel works.

Finally, CLs may be followed by non-linear functions [25] and pooling layers [26], which convert ofmaps in a different numerical domain and downsample their planar sizes, respectively.

B. Systolic Arrays

A SA is spatial architecture consisting of a 2-D array of PEs interconnected with each other in proper directions. Each PE usually performs a MAC operation using inputs supplied by either the main memory or neighbor PEs. With specific reference to DNNs, PEs are fed by input activations (inputs), weights and psums. High data utilization is met at two hierarchical levels: (a) at the PE level, one element among the input, weight and psum is retained in a register as long as it is required; (b) at the SA level, the other elements move rhythmically between adjacent PEs. The reused data at the PE level equips the SA with a specific stationary dataflow:
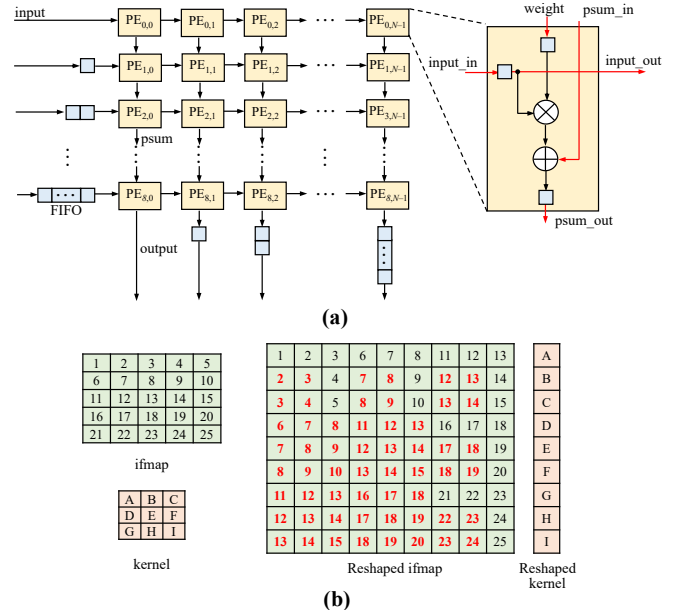

(a)

(b)

Fig. 2. WS-based SA: (a) a general architecture to manage filters with 3×3 kernels is reported. The different PEs' columns manage the kernels of N different filters, which in turn receive the same ifmap. Inputs move from left to right, while psums move from top to bottom. FIFOs are needed to correctly align inputs and psums over the time. The generic PE performs a MAC operation between the current input, weight and psum as well. Each data is registered to enable proper synchronization; (b) example of General Matrix-Multiplication (GeMM) between a 5×5 ifmap and a 3×3 kernel: the ifmap is reshaped as a 9×9 matrix, where redundant data are highlighted in red, while the kernel is reshaped as a vertical 9×1 array.

- Weight Stationary (WS): weights are retained inside the PEs and do not move. Inputs and psum moves between adjacent PEs throughout the process.
- Input Stationary (IS): a batch of inputs is retained inside the PEs, while weights and psums move between adjacent PEs throughout the process.
- Output Stationary (OS): psums are reused at the PE level until the final sum is generated. Inputs and weights move between adjacent PEs throughout the process.
- Row Stationary (RS): rows of inputs and weights are stored and reused at the PE level, using memory blocks that enable data circulation. Psums move between adjacent PEs throughout the process.

Since CNNs exploit *weight sharing* to process each fmap, WS and RS are commonly used. In the following sub-sections, the two dataflows are presented in detail.

1) Weight Stationary SAs: In a WS-based SAs, weights are preliminary fetched from the main memory and stored inside the PEs. Fig. 2(a) depicts an example of WS-based SA, where inputs are loaded from the left side and moved horizontally across the array. Differently, psums are accumulated following vertical interconnections. In order to correctly align data over time, First-In-First-Out buffers (FIFOs) for inputs and psums are placed at the left and bottom boundaries of the array, respectively. To make WS-based SAs compliant with CNNs, inputs and weights are subjected to Conv-to-GeMM [20]. The M ifmaps, consisting of $H_I \times W_I$ elements each, are reshaped as a matrix having $H_O \times W_O$ rows and $M \times K \times K$ columns.
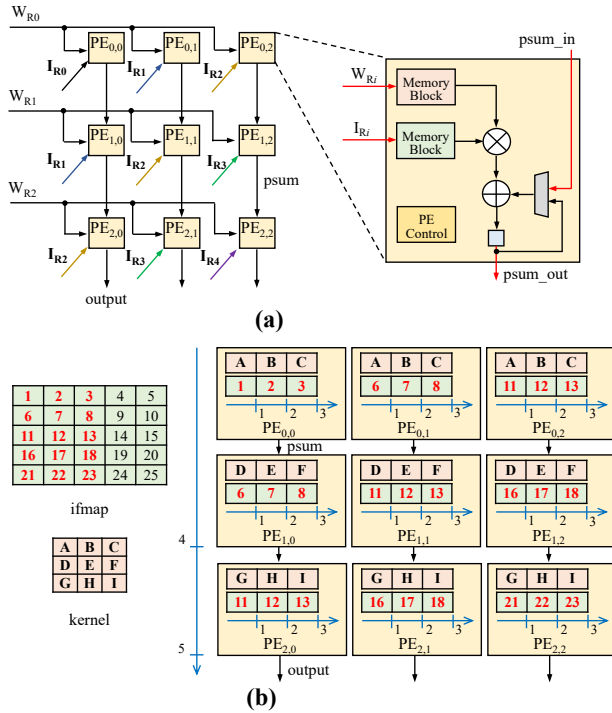
(a)

(b)

Fig. 3. Example of RS-based SA considering a 5×5 ifmap and a 3×3 kernel: (a) the architecture consists of 3×3 PEs, where weights' rows are broadcast horizontally, inputs' rows are broadcast diagonally (in the figure, different numbers and colors refer to different rows). Finally, psums are accumulated vertically. The generic PE, other than accommodating a MAC unit, hosts two memory blocks to circulate rows of inputs and weights, respectively, and a register to save the current psum. In addition, a multiplexer allows the adder to consider either the psum coming from a different PE or the internal psum; (b) an example, where the first three columns of each input row are processed. In each yellow box, which represent a specific PE, the products over time are reported. For instance, the $PE_{0,0}$ executes $1 \times A$ at cycle 1, $2 \times B$ at cycle 2, and $3 \times C$ at cycle 3. For each cycle, the previous product is also accumulated to the current one. At the SA level, psums are accumulated vertically at cycle 4 (first row and second row of the array) and at cycle 5 (second row and third row).

Each row contains one of the three-dimensional sliding windows covered by the filters that scan the ifmaps. Filters are reshaped as N column arrays, each consisting of $M \times K \times K$ entries (i.e., the number of weights of each filter). As a result, a GeMM-oriented SA consists of $M \times K \times K$ rows of N PEs each. In addition, $M \times K \times K - 1$ FIFOs must be adopted to ensure proper data-alignment over time. Fig 2(b) shows an example of Conv-to-GeMM between a 5×5 ifmap and a 3×3 kernel. Despite the above PEs' deployment allows WS-based SAs to meet CNNs' workloads, some drawbacks are evident: (i) Conv-to-GeMM introduces data redundancy since inputs are reshaped to guarantee the overlapping sliding windows of the original workflow. As a result, the main memory demands higher capacity, as well as higher number of memory accesses to feed the SA. These aspects negatively impact area and energy efficiency; (ii) furthermore, the larger the kernel size K and/or the number of kernels M and/or the number of filters N, the bigger the FIFOs. As a consequence, higher latency and switching activity impact the energy consumption, other than the area.

2) Row Stationary SAs: In a RS-based SA, the PEs are arranged as an array of K rows and H_O columns, where: (a) weights are fetched from the main memory and broadcast horizontally to all the PEs; (b) inputs are fetched and broadcast diagonally; (c) psum are accumulated vertically, by exploiting dedicated interconnections between PEs. High data utilization is handled at the PE level, despite requiring memory blocks to circulate inputs and weights. These data are typically loaded as rows of K elements, in order to allow the generic PE to perform 1-D convolutions. In other words, each PE is capable to perform K MACs, before forwarding the temporary psum vertically to another PE, which in the meantime has completed another 1-D convolution. The vertical connections finalize the 2-D convolution. Fig. 3(a) shows an example of RS-based SA using 3×3 PEs, where a 5×5 ifmap is subjected to a convolution with a 3×3 kernel. The generic PE consists of a MAC unit, two memory blocks for inputs and weights, as well as control logic. Fig. 3(b) illustrates the 2-D convolutions of a 5×5 ifmap, with details on the data shared among the PEs. Differently from Conv-to-GeMM, this dataflow moves data redundancy at the array level, where inputs are shared diagonally, while weights are shared horizontally. In addition, other drawbacks arise: (i) the hardware complexity of each PE is higher, considering that memory blocks (and proper control logic as well) are needed. Other than the area, this negatively impacts the energy dissipation due to the high switching activity of memory blocks to guarantee data circulation; (ii) despite inputs/weights broadcasting at the SA level enables parallel convolutions, thus the possibility to reduce the latency, this directly impacts the routability of the PEs, making the physical implementation phase challenging; (iii) finally, the area covered by the SA depends on ifmap's size, thus limiting scalability and PEs' utilization.

III. TRIANGULAR INPUT MOVEMENT SYSTOLIC ARRAY

The TrIM-based SA consists of $K \times K$ PEs, where weights are retained at the PE level, while inputs and psums are moved across the array to maximize data reuse. Before any computation, weights are read from the memory and provided to the PEs placed at the top side of the array; then, these are moved from top to down to allow the other weights to be accommodated. Inputs supply the PEs through a novel data movement that can be summarized in three steps: (i) first, inputs are fetched from the main memory and delivered to the PEs; (ii) then, such inputs move from right to left, until they reach the left edge of the array; (iii) finally, they move diagonally towards the upper PEs. According to the width of the ifmap under processing, the leftmost PEs may be connected to Shift Register Buffers (SRBs) with depth $W_I - K - 1$, which ensure the correct execution of the diagonal movement over time. Steps (i) to (iii) compose a right-triangular shape, hence the name *Triangular Input Movement* (TrIM). Fig. 4 schematizes a generic architecture coping with the proposed dataflow. Each PE is labelled as $PE_{i,j}$, with $0 \leq i, j < K$, and consists of a MAC unit, four registers, and two multiplexers to establish whether the current input is reused from a different PE or not. If reused, inputs can
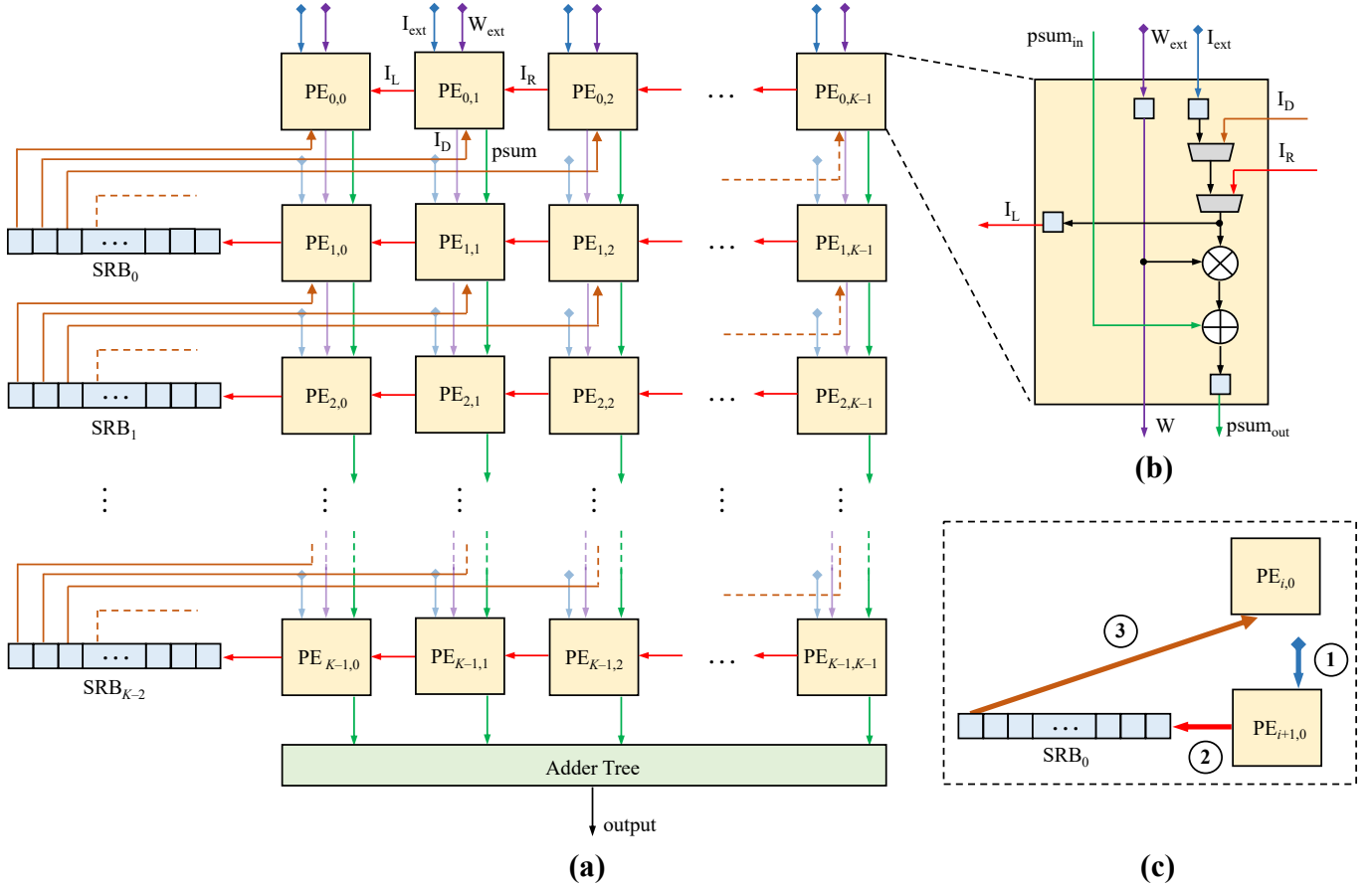
Fig. 4. The generic Triangular Input Movement SA. (a) This consists of $K \times K$ PEs, where weights are kept fixed. Inputs are reused internally through either right-to-left movements or bottom to diagonally up translations. Psums are accumulated vertically. Shift Register Buffers (SRBs) assist the diagonal movement. Finally, an adder tree is responsible to accumulate the psums coming from the bottom PEs. (b) The generic PE performs a multiplication between the weight W and the current input, and accumulates this to the psum coming from the top PE ($psum_{in}$), thus generating the current psum ($psum_{out}$). According to a multiplexing logic, the current input may be external (I_{ext}), reused from the right side (I_R) or reused diagonally from the bottom PE (I_D). The current input is forwarded to the PE/SRB placed at the left side (I_L). (c) Example of a triangular input movement between two PEs placed at the left-most side of the array: (1) The generic input is fetched externally and provided vertically to the PE; (2) such input is forwarded from right to left to the SRB; (3) after some cycles, it is supplied diagonally up to the top PE, thus closing the triangle.

move from right to left (thus from each $PE_{i,j+1}$ to $PE_{i,j}$), or they can be forwarded diagonally. In the latter case, they are first provided to the SRBs from each $PE_{i,0}$, then shifted along such buffers, and finally the inputs stored into the last K registers are supplied to the top $PE_{i-1,j}$ elements. Psums are accumulated vertically, thus from each $PE_{i,j}$ to each $PE_{i+1,j}$. Eventually, an adder tree accumulates the psums coming from the the bottom $PE_{K-1,j}$ elements. For very small ifmaps, with $W_I \leq 2K$, the number of registers may be lower than K, thus the diagonal connections may also interest some of the PEs.

To better understand how TrIM works, we consider the case reported in Fig. 5, where a 5×5 ifmaps, with $I = 1, 2, ..., 25$ being the inputs, and a 3×3 kernel, with $W = A, B, ..., I$ being the weights, are considered. The equivalent TrIM architecture is made of 3 rows (named Row_0, Row_1, and Row_2), each having 3 PEs. The leftmost PEs belonging to Row_1 and Row_2 are connected to SRBs with depth 1. A final adder tree, consisting of two adders, manages the psums coming from the PEs of Row_2. In what follows, the detailed functionality of the

dataflow is explained cycle-by-cycle. Preliminarily, K cycles are needed to load the $K \times K$ weights, arranged in rows of K weights per cycle. After this phase, the actual computations and input movements can start:

- **Cycle 1**: $I = 1, 2, 3$, supplied vertically to Row_0, are multiplied by the weights $W = A, B, C$.
- **Cycle 2**: Row_0 multiplies $I = 2, 3, 4$ with $W = A, B, C$, where $I = 2, 3$ are reused through right-to-left movements, while $I = 4$ is supplied externally. Row_1 multiplies the new inputs $I = 6, 7, 8$ with $W = D, E, F$, and accumulate these with the psums coming from Row_0.
- **Cycle 3**: Row_0 multiplies $I = 3, 4, 5$ with $W = A, B, C$, where $I = 3, 4$ are reused through right-to-left movements, while $I = 5$ is supplied externally. Row_1 multiplies the inputs $I = 7, 8, 9$ with $W = D, E, F$, and accumulate these with the psums coming from Row_0. While $I = 7, 8$ are reused through right-to-left movements, $I = 9$ is supplied externally. Row_2 multiplies the new inputs $I = 11, 12, 13$ with $W = G, H, I$, and accumulate these with the psums coming from Row_1. At
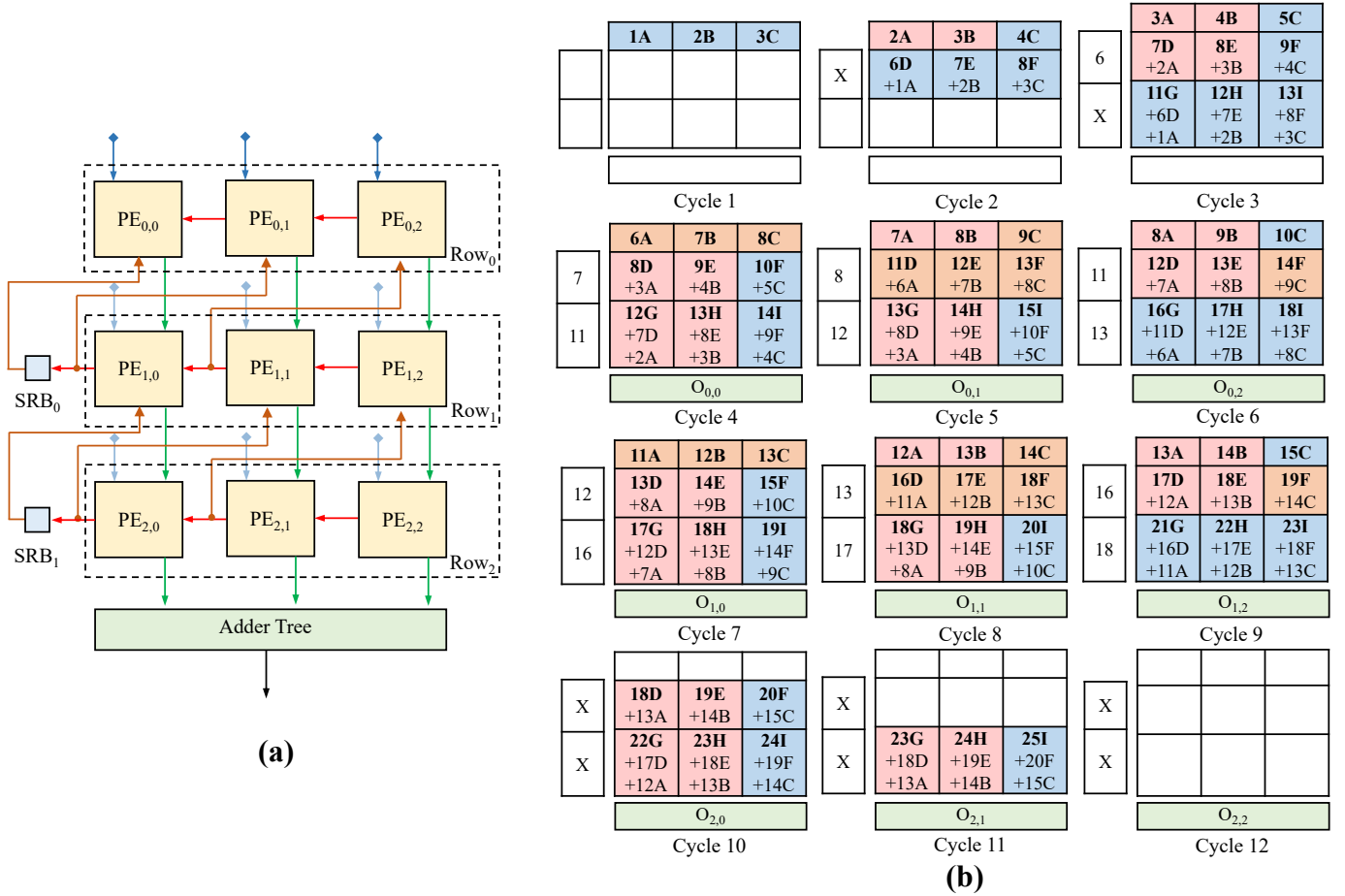
Fig. 5. The TrIM architecture and dataflow considering a 5×5 ifmap and a 3×3 kernel: (a) the SA consists of 3×3 PEs and 2 SRBs to enable the diagonal movement of inputs. An extra adder tree, consisting of two adders, accumulates the psums coming from the bottom PEs; (b) the evolution over the different cycles, reporting the computations performed by each PE, the data currently stored into the SRBs and the current output provided by the adder tree. Cells in blue refer to inputs fetched externally, while cells in red indicate inputs reused through a right-to-left movement. Conversely, cells in orange refer to diagonal reuse, either from a SRB or a different PE. Finally, the green boxes refer to the outputs provided by the adder tree. Bold numbers refer to active multiplications. Xs refer to don't care cases.

this cycle, SRB_0 receives $I = 6$ to be reused later.

- **Cycle 4**: Row_0 multiplies $I = 6, 7, 8$ with $W = A, B, C$, where $I = 6$ is reused diagonally from SRB_0, while $I = 7, 8$ are reused diagonally from $PE_{1,0}$ and $PE_{1,1}$, respectively. Row_1 multiplies the inputs $I = 8, 9, 10$ with $W = D, E, F$, and accumulate these with the psums coming from Row_0. While $I = 8, 9$ are reused through right-to-left movements, $I = 10$ is supplied externally. Row_2 multiplies the inputs $I = 12, 13, 14$ with $W = G, H, I$, and accumulate these with the psums coming from Row_1. While $I = 12, 13$ are reused through right-to-left movements, $I = 14$ is supplied externally. At this cycle, SRB_0 and SRB_1 receive $I = 7$ and $I = 11$, respectively. Finally, the psums coming from $PE_{2,0}$, $PE_{2,1}$, and $PE_{2,2}$ are accumulated through the adder tree to get the very first output activation $O_{0,0}$.

- **Cycle 5**: Row_0 multiplies $I = 7, 8, 9$ with $W = A, B, C$, where $I = 7, 8$ are reused through right-to-left movements, while $I = 9$ is reused diagonally from $PE_{1,1}$. Row_1 multiplies the inputs $I = 11, 12, 13$ with $W = D, E, F$, and accumulate these with the psums coming

from Row_0. $I = 11$ is reused diagonally from SRB_0, while $I = 12, 13$ are reused diagonally from $PE_{1,0}$ and $PE_{1,1}$, respectively. Row_2 multiplies the inputs $I = 13, 14, 15$ with $W = G, H, I$, and accumulate these with the psums coming from Row_1. While $I = 13, 14$ are reused through right-to-left movements, $I = 15$ is supplied externally. At this cycle, SRB_0 and SRB_1 receive $I = 8$ and $I = 12$, respectively. Finally, the psums coming from $PE_{2,0}$, $PE_{2,1}$, and $PE_{2,2}$ are accumulated through the adder tree to get the second output activation $O_{0,1}$.

- **Cycle 6**: Row_0 multiplies $I = 8, 9, 10$ with $W = A, B, C$, where $I = 8, 9$ are reused through right-to-left movements, while $I = 10$ is supplied externally. Row_1 multiplies the inputs $I = 12, 13, 14$ with $W = D, E, F$, and accumulate these with the psums coming from Row_0. While $I = 12, 13$ are reused through right-to-left movements, $I = 14$ is reused diagonally from $PE_{2,1}$. Row_2 multiplies the new inputs $I = 16, 17, 18$ with $W = G, H, I$, and accumulate these with the psums coming from Row_1. At this cycle, SRB_0 and SRB_1

receive $I = 11$ and $I = 13$, respectively. Finally, the psums coming from $PE_{2,0}$, $PE_{2,1}$, and $PE_{2,2}$ are accumulated through the adder tree to get the third output activation $O_{0,2}$.

- **Cycle 7**: Row_0 multiplies $I = 11, 12, 13$ with $W = A, B, C$, where $I = 11$ is reused diagonally from SRB_0, while $I = 12, 13$ are reused diagonally from $PE_{1,0}$ and $PE_{1,1}$, respectively. Row_1 multiplies the inputs $I = 13, 14, 15$ with $W = D, E, F$, and accumulate these with the psums coming from Row_0. While $I = 13, 14$ are reused through right-to-left movements, $I = 15$ is supplied externally. Row_2 multiplies the inputs $I = 17, 18, 19$ with $W = G, H, I$, and accumulate these with the psums coming from Row_1. While $I = 17, 18$ are reused through right-to-left movements, $I = 19$ is supplied externally. At this cycle, SRB_0 and SRB_1 receive $I = 12$ and $I = 16$, respectively. Finally, the psums coming from $PE_{2,0}$, $PE_{2,1}$, and $PE_{2,2}$ are accumulated through the adder tree to get the fourth output activation $O_{1,0}$.

- **Cycle 8**: Row_0 multiplies $I = 12, 13, 14$ with $W = A, B, C$, where $I = 12, 13$ are reused through right-to-left movements, while $I = 14$ is reused diagonally from $PE_{1,1}$. Row_1 multiplies the inputs $I = 16, 17, 18$ with $W = D, E, F$, and accumulate these with the psums coming from Row_0. $I = 16$ is reused diagonally from SRB_0, while $I = 17, 18$ are reused diagonally from $PE_{1,0}$ and $PE_{1,1}$, respectively. Row_2 multiplies the inputs $I = 18, 19, 20$ with $W = G, H, I$, and accumulate these with the psums coming from Row_1. While $I = 18, 19$ are reused through right-to-left movements, $I = 20$ is supplied externally. At this cycle, SRB_0 and SRB_1 receive $I = 13$ and $I = 17$, respectively. Finally, the psums coming from $PE_{2,0}$, $PE_{2,1}$, and $PE_{2,2}$ are accumulated through the adder tree to get the fifth output activation $O_{1,1}$.

- **Cycle 9**: Row_0 multiplies $I = 13, 14, 15$ with $W = A, B, C$, where $I = 13, 14$ are reused through right-to-left movements, while $I = 15$ is supplied externally. Row_1 multiplies the inputs $I = 17, 18, 19$ with $W = D, E, F$, and accumulate these with the psums coming from Row_0. While $I = 17, 18$ are reused through right-to-left movements, $I = 19$ is reused diagonally from $PE_{2,1}$. Row_2 multiplies the new inputs $I = 21, 22, 23$ with $W = G, H, I$, and accumulate these with the psums coming from Row_1. At this cycle, SRB_0 and SRB_1 receive $I = 16$ and $I = 18$, respectively. Finally, the psums coming from $PE_{2,0}$, $PE_{2,1}$, and $PE_{2,2}$ are accumulated through the adder tree to get the sixth output activation $O_{1,2}$.

- **Cycle 10**: Row_0 has completed the computations related to the current ifmap, so it starts to compute a sliding windows from a different ifmap. Row_1 multiplies the inputs $I = 18, 19, 20$ with $W = D, E, F$, and accumulate these with the psums coming from Row_0. While $I = 18, 19$ are reused through right-to-left movements, $I = 20$ is supplied externally. Row_2 multiplies the inputs $I = 22, 23, 24$ with $W = G, H, I$, and accumulate these

with the psums coming from Row_1. While $I = 22, 23$ are reused through right-to-left movements, $I = 24$ is supplied externally. From this cycle, SRB_0 and SRB_1 do not need to receive data anymore. Finally, the psums coming from $PE_{2,0}$, $PE_{2,1}$, and $PE_{2,2}$ are accumulated through the adder tree to get the seventh output activation $O_{2,0}$.

- **Cycle 11**: Row_0 and Row_2 have completed the computations related to the current ifmap, so they work on a different ifmap. Row_2 multiplies the inputs $I = 23, 24, 25$ with $W = G, H, I$, and accumulate these with the psums coming from Row_1. While $I = 23, 24$ are reused through right-to-left movements, $I = 25$ is supplied externally. Finally, the psums coming from $PE_{2,0}$, $PE_{2,1}$, and $PE_{2,2}$ are accumulated through the adder tree to get the eighth output activation $O_{2,1}$.

- **Cycle 12**: All the rows have completed the computations related to the current ifmap, so they work on a different ifmap. The adder tree provides the final output activation $O_{2,2}$.

The example just presented allows to appreciate how TrIM maximizes inputs utilization. In fact, the number of total memory accesses from the main memory is 29, of which only 4 accesses refer to inputs read more than once. To better spotlight this, let consider the case $I = 13$. This input is read once from the main memory (cycle 3) and reused 8 times (from cycle 4 to cycle 9) through right-to-left and diagonal movements.

IV. AN ANALYTICAL MODEL FOR SYSTOLIC ARRAYS

In order to highlight the advantages provided by TrIM, we built an analytical model to explore and evaluate the design space of TrIM, searching for optimum design points that lead the physical implementation phase. The aim of this model is twofold: (i) providing insights about memory accesses, throughput and local buffers/registers; (ii) comparing TrIM to WS and RS dataflows. Without loss of generality, all the metrics refer to a convolution between an $H_I \times W_I$ ifmap and a $K \times K$ kernel. However, these can be easily scaled to manage M ifmaps and N filters of M kernels.

A. Modelling WS and RS Dataflows

The number of memory accesses (MA) of the WS-based SA is dictated by Conv-to-GeMM and reported in equation (2):

$$MA_{WS} = K^2 \times (H_O \times W_O) \tag{2}$$

This conversion results in data redundancy and higher memory capacity, since ifmap's activations are arranged as $H_O \times W_O$ rows and K^2 columns. On the contrary, since no Conv-to-GeMM is required by the RS-based SA, the MA of the main memory are directly related to the ifmap's sizes ($H_I \times W_I$). However, the RS-based SA needs memory blocks at the PE level, usually implemented as SRAM-based scratch pads, which severely affect the energy footprint. Based on the Eyeriss implementation [22], the scratch pads energy is estimated to be from $\alpha = \sim 11\times$ to $\sim 16.3\times$ higher than the

memory energy. Therefore, the number of MA is summarized by equation (3):

$$MA_{RS} = (1 + \alpha) \times (H_I \times W_I) \tag{3}$$

The throughput (T) is expressed as the ratio between the number of operations carried out by the convolution and the total latency required for its completion, thus indicating how many operations are performed per cycle. First, to get the number of operations (OPs), we consider that K^2 multiplications and $K^2 - 1$ additions are performed to produce one output, which almost corresponds to $2 \times K^2$ operations. This is repeated $H_O \times W_O$ times to generate as many outputs. Thus, the total number of operations is given by equation (4):

$$OPs = 2 \times K^2 \times H_O \times W_O \tag{4}$$

When the WS-based SA is considered, the latency (L) is given by equation (5):

$$L_{WS} = K^2 + H_O \times W_O - 1 \tag{5}$$

Every PE requires one clock cycle to generate its own psum. Thus, K^2 cycles are required to generate one full output. After that, one valid output is provided per cycle. The RS-based SA behaves differently. Every PE requires K cycles to generate the temporary output of a 1-D convolution. After that, $K - 1$ extra cycles are needed to accumulate the psums vertically, in order to complete one 2-D convolution. Thus, L is given by equation (6):

$$L_{RS} = W_O \times (2 \times K - 1) \tag{6}$$

Considering the number of operations and the latency reported above, T is dictated by equations (7) and (8):

$$T_{WS} = \frac{2 \times K^2 \times H_O \times W_O}{K^2 + H_O \times W_O - 1} \tag{7}$$

$$T_{RS} = \frac{2 \times K^2 \times H_O}{2 \times K - 1} \tag{8}$$

For the sake of fair comparisons, T needs to be normalized by the number of PEs. Since the WS-based SA consists of $K \times K$ PEs, while the RS-based SA is made of $K \times H_O$ PEs, the T per PE (TPE) is given by equations (9) and (10):

$$TPE_{WS} = \frac{2 \times H_O \times W_O}{K^2 + H_O \times W_O - 1} \tag{9}$$

$$TPE_{RS} = \frac{2 \times K}{2 \times K - 1} \tag{10}$$

To consider local buffers and registers, FIFOs used in the WS-based SA and memory blocks inside the PEs of the RS-based SA are modelled as equivalent sets of registers. The WS-based SA requires 3 registers per PE, as well as $K^2 - 1$ FIFOs for inputs. The total number of equivalent registers (Reg) is dictated by equation (11):

$$Reg_{WS} = 3 \times K^2 + \frac{K^2 \times (K^2 - 1)}{2} \tag{11}$$

Conversely, the PEs inside the RS-based SA adopts two memory blocks, each equivalent to K registers, and a register for the psum. The total number of registers is given by equation (12):

$$Reg_{RS} = (2 \times K + 1) \times K \times H_O \tag{12}$$

B. Modelling TrIM Dataflow

The major advantage offered by TrIM is the substantial reduction of MA if compared to WS and RS dataflow. Indeed, the high data utilization enabled by the triangular input movement maximizes the number of operations per access. Two contributions concur in modelling the MA metric: (i) the initial read of the ifmap, which is given by $H_I \times W_I$ accesses; (ii) a very limited overhead (OV) to retrieve previous inputs, no more locally available. Therefore, MA is given by equation (13):

$$MA_{TrIM} = H_I \times W_I + OV \tag{13}$$

where OV is dictated by equation (14):

$$OV = \begin{cases} (W_I - K - 1) \times (K - 1) \times (H_I - K) & W_I < 2K \\ (K - 1)^2 \times (H_I - K) & W_I \geq 2K \end{cases} \tag{14}$$

The total latency is given by the number of outputs to be generated, other than an initial latency to fill the pipeline. This initial latency is dictated by the pipeline of the array (three cycles for the PEs, one cycle for the adder tree). Then, one new output is generated per cycle. Thus, the total L is given by equation (15):

$$L_{TrIM} = K + H_O \times W_O \tag{15}$$

As a result, T is given by equation (16):

$$T_{TrIM} = \frac{2 \times K^2 \times H_O \times W_O}{K + H_O \times W_O} \tag{16}$$

Since TrIM consists of $K \times K$ PEs, the TPE is given by equation (17):

$$TPE_{TrIM} = \frac{2 \times H_O \times W_O}{K + H_O \times W_O} \tag{17}$$

In order to retrieve the total number of registers, we consider that each PE uses four registers, while extra $K - 1$ SRBs, each containing $W_I - K - 1$ registers, are needed to ensure the diagonal reuse of inputs. In addition, the adder tree uses one register. Equation (18) summarizes the total number of registers:

$$Reg_{TrIM} = 3 \times K^2 + (K - 1) \times W_I + 2 \tag{18}$$

V. DESIGN SPACE EVALUATION

In this section, TrIM is compared to the WS-based SA and the RS-based SA through a design space evaluation. Memory accesses, throughput and number of registers are considered, following the equations introduced in Section IV. For each metric, different kernel sizes and ifmap's sizes are considered. K spans the range 3,5,7, extensively used in state-of-the-art CNNs [27], [28]. Square ifmaps ($H_I = W_I = I$) cover the range $I = [16, 32, 64, 128, 256]$.
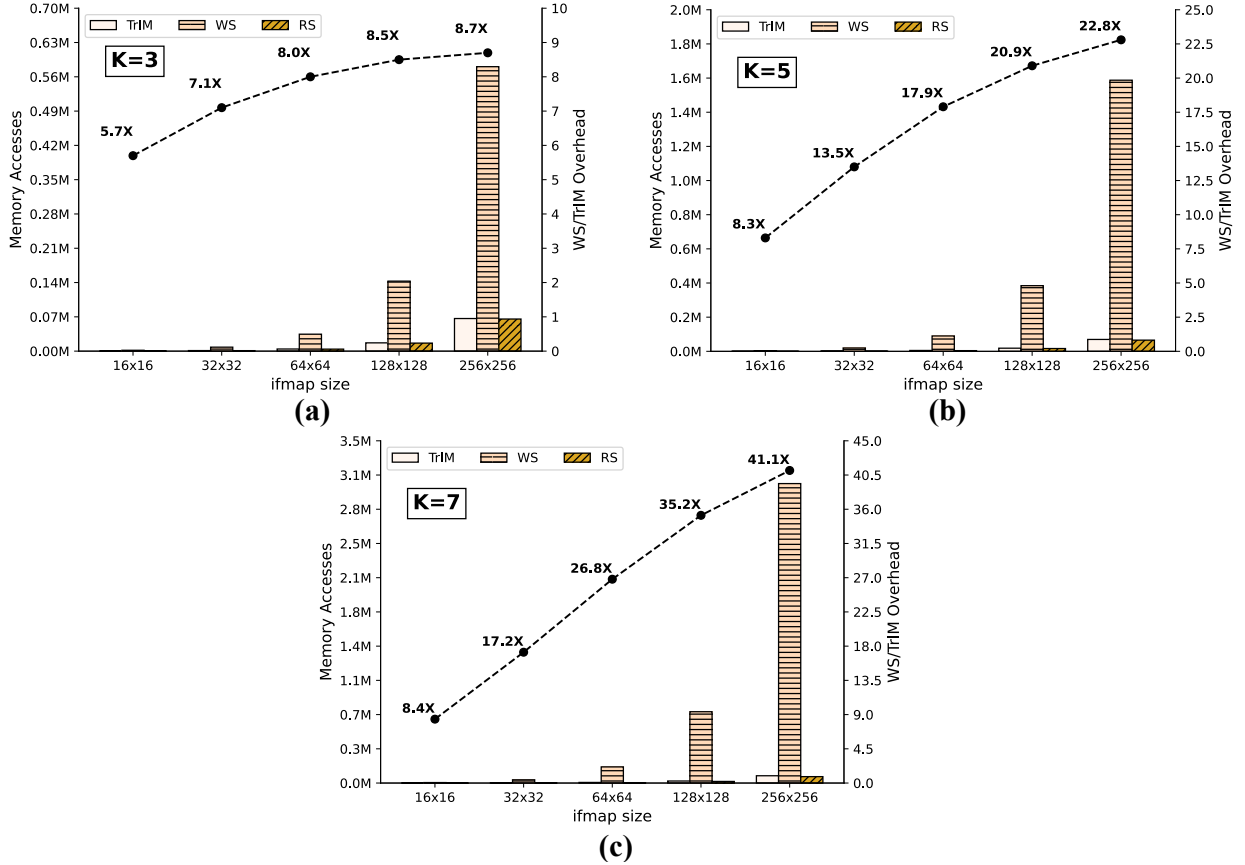
Fig. 6. Memory Accesses (MA) analysis. In each plot (a)-(c), the left vertical axis refers to MA, the right vertical axis refers to the ratio between WS and TrIM, whereas the horizontal axis refers to the ifmap size I. Bars are associated to the MA metric, dots and lines compare WS and TrIM. With more detail, bars in seashell highlight the MA in TrIM, bars in peachpuff with horizontal hashes are related to WS, while those in goldenrod with diagonal hashes refer to RS. The entire analysis covers $I = 16, 32, 64, 128, 256$. The bar plots reported in (a) are specific of $K = 3$, bar plots in (b) refer to $K = 5$, and (c) illustrates the case $K = 7$.

Fig. 7. Memory access comparison between TrIM and RS. Memory accesses are normnalized to the number of activations of the generic ifmap, and highlighted by the black line crossing 1.0. Black dots refer to the nromalized memory accesses for TrIM, and varying the ifmap size I from 16 to 256. The gray area between the red and blue dashed lines indicates the spectrum in which the Row Stationary dataflow moves.

A. Memory Accesses

Fig. 6 depicts the number of MA required by the different dataflows. Fig. 6(a) refers to $K = 3$, Fig. 6(b) refers to $K = 5$, while Fig. 6(c) refers to $K = 7$. TrIM significantly outperforms WS since no Conv-to-GeMM is performed, thus not introducing data redundancy and resulting in lower memory capacity. For example, when $K = 3$ and I spans from 16 to 256, TrIM requires from $5.7\times$ to almost one order of magnitude less MA. This improvement is more accentuated with higher K, reaching a reduction of up to $41.1\times$ when $K = 7$.

In the case of the RS dataflow, the total number of MA is given by two contributions: the main memory and the memory blocks for data circulation at the PE level. From the main memory, inputs are read once, therefore the MA corresponds to the number of activations of each ifmap. This contribution is reported in Fig. 6(a)-(c). TrIM's MA are practically close to the RS' main memory accesses. In fact, the overhead introduced by TrIM and previously reported in equation (14) is minimal. For example, when $K = 3$ and $I = 256$, TrIM uses only 1.5% more MA than RS. Fig. 7 illustrates the overhead required by RS and dictated by the use of memory blocks
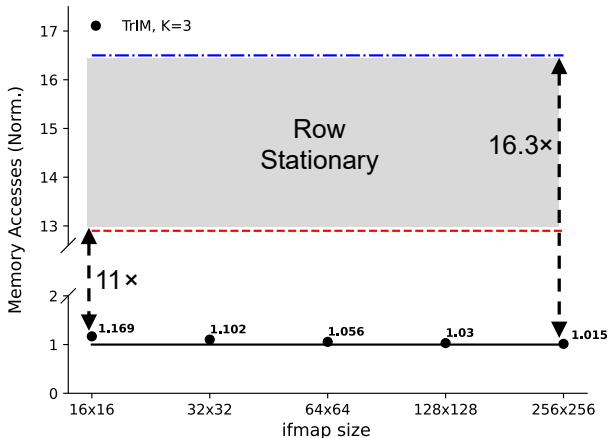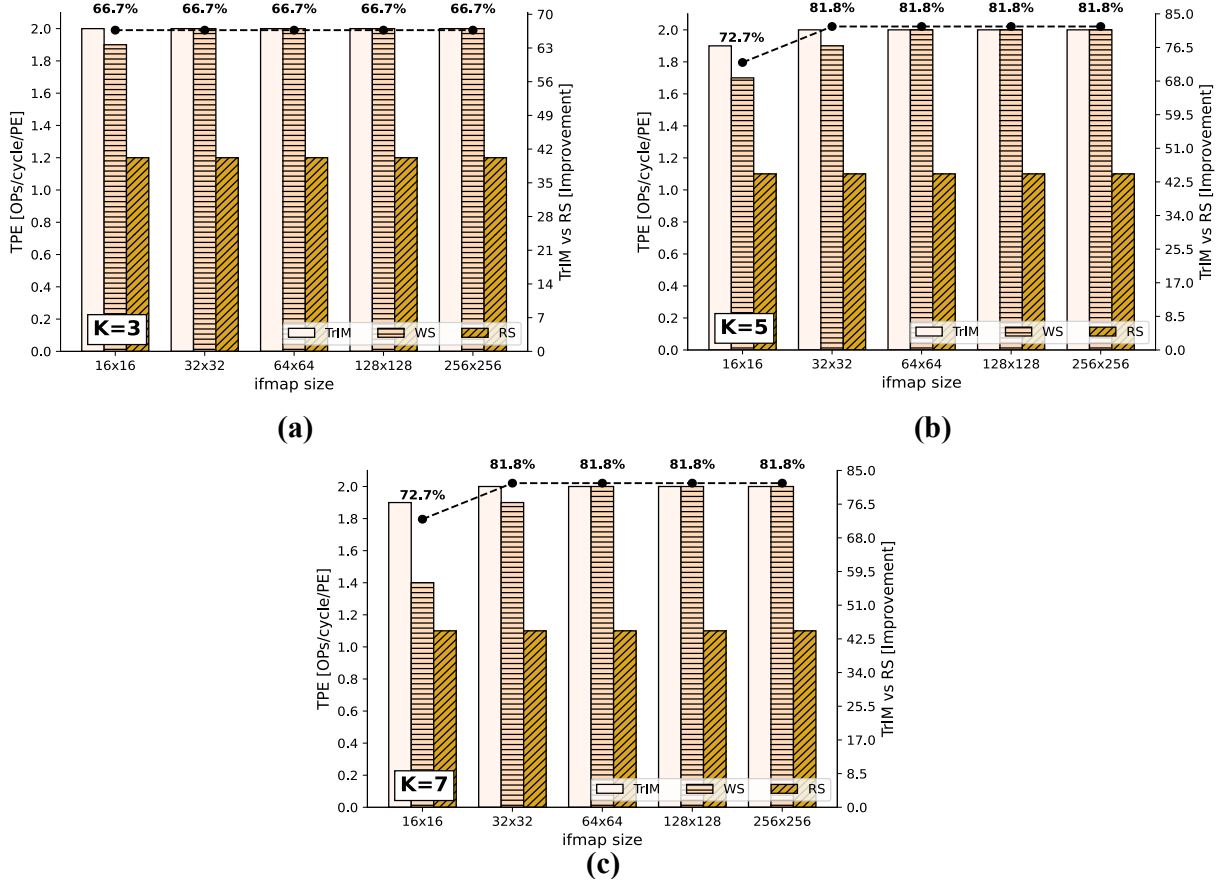
Fig. 8. Throughput Analysis: the Throughput per Processing Element (TPE) metric is considered. In each plot (a)-(c), the left vertical axis refers to the TPE, the right vertical axis refers to the percentage improvement between TrIM and RS, whereas the horizontal axis refers to the ifmap size I. Bars are associated to the TPE, dots and lines compare TrIM to RS. With more detail, bars in seashell highlight the TrIM performance, bars in peachpuff with horizontal hashes are related to WS, while those in goldenrod with diagonal hashes refer to RS. The entire analysis covers $I = 16, 32, 64, 128, 256$. The bar plots reported in (a) are specific of $K = 3$, bar plots in (b) refer to $K = 5$, and (c) illustrates the case $K = 7$.

at the PE level, usually in the form of scratch pads [22] . This contribution is from $\sim 11\times$ to $\sim 16.3\times$ higher than the memory accesses required to read data.

B. Throughput

Fig. 8 illustrates the TPE for each dataflow. Fig. 8(a) refers to $K = 3$, Fig. 8(b) refers to $K = 5$, while Fig. 8(c) refers to $K = 7$. Considering TrIM, the TPE is independent by K and I, and reaches the peak throughput of 2 OPs/cycle/PE. This result spotlights the performance efficiency of PEs coping with the TrIM dataflow. At the PE level, TrIM behaves similarly to the WS-based SA, since weights are not moved. As a result, the TPE of WS and TrIM is the same. However, when small ifmaps are considered, the performance of WS is degraded because of the synchronization requirements of WS. This drawback is even more accentuated with larger K. For example, fixed $I = 16$, TrIM outperforms WS by 5.3%, 11.8%, and 35.7% when $K = 3, 5, 7$, respectively.

TrIM also outperforms the TPE of RS. This because in RS each PE, after processing a row of K inputs and weights, has to wait for almost the same number of cycles to allow psums

to be vertically accumulated. Conversely, TrIM is an always-on dataflow, where the accumulations can be overlapped to the multiplications of new inputs and weights. The percentage improvement offered by TrIM is also reported in Fig. 8(a)-(c), reaching up to 81.8%.

C. Registers

Fig. 9 shows the total number of registers for each dataflow. Fig. 9(a) refers to $K = 3$, Fig. 9(b) refers to $K = 5$, while Fig. 9(c) refers to $K = 7$. The RS-based SA requires the highest number of registers, considering that memory blocks for inputs and weights must be accommodated into $K \times H_O$ PEs. For example, when $K = 3$ and $I = 256$, the registers of RS are $\sim 10\times$ more than those required by TrIM. Since the majority of RS' registers are memory blocks, the degradation in terms of energy is even worse.

When compared to WS, TrIM generally uses more registers if large ifmaps are considered. For example, when $I = 64$ and $K = 3$, TrIM requires $2.5\times$ more registers. However, the WS-based SA predominantly makes use of FIFOs for data synchronization ($\sim 57\%$ in the example case), which are more
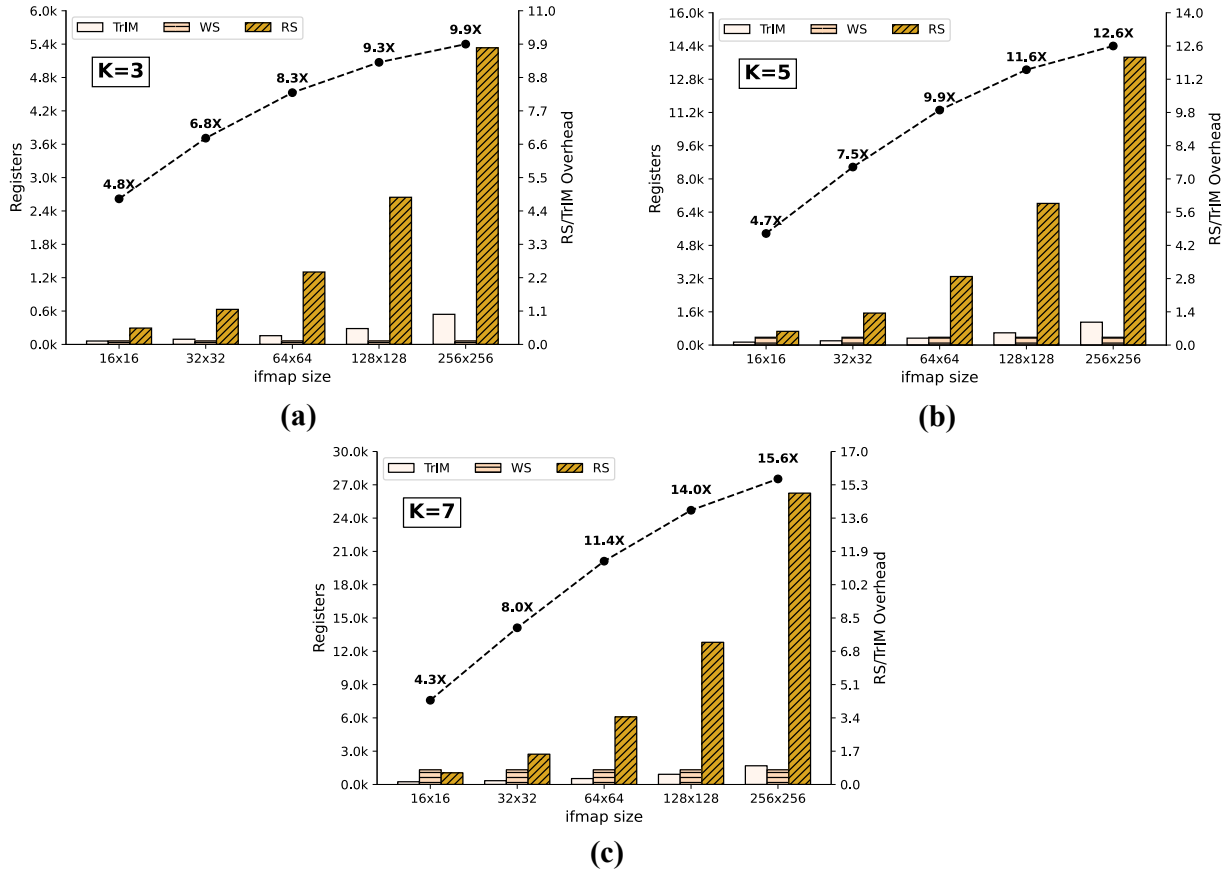
Fig. 9. Number of registers: in each plot (a)-(c), the left vertical axis refers to the number of registers, the right vertical axis refers to the overhead between RS and TrIM, whereas the horizontal axis refers to ifmap size I. Bars are associated to the number of registers, dots and lines compare RS and TrIM. With more detail, bars in seashell highlight the number of registers in TrIM, bars in peachpuff with horizontal hashes are related to WS, while those in goldenrod with diagonal hashes refer to RS. The entire analysis covers $I = 16, 32, 64, 128, 256$. The bar plots reported in (a) are specific of $K = 3$, bar plots in (b) refer to $K = 5$, and (c) illustrates the case $K = 7$.

energy demanding than SRBs in TrIM. On the contrary, when small ifmaps are considered, TrIM requires fewer registers than WS. This because SRBs are smaller than FIFOs. In fact, other than dealing with tiny ifmaps, part of the SRBs' workload may be shifted at the PE level (when $I \leq 2K$), where PEs of adjacent rows are diagonally connected. The inversion point (I_{IP}) between the two trends (i.e., WS better than TrIM and viceversa) follows equation (19), obtained imposing (11) = (18), with $W_I = I_{IP}$:

$$I_{IP} = \left\lceil \frac{K^4 - K^2 - 4}{2 \times (K-1)} \right\rceil \tag{19}$$

$I_{IP} = 17, 75, 196$ when $K = 3, 5, 7$, respectively.

D. Discussion

The design space analysis presented in this Section allow us to highlight several insights:

- TrIM exhibits the lowest number of memory accesses among the competitors. This because of the high data utilization offered by TrIM. In addition, thanks to the tri-angular movement of inputs, TrIM does not require Conv-to-GeMM, resulting in no data redundancy and, therefore,

lower memory capacity than WS. When $K = 3$, TrIM outperforms WS by almost $10\times$, and up to $41\times$ with larger K. Furthermore, the simple micro-architecture of PEs in TrIM allows significant improvement compared to RS. In fact, RS requires memory blocks at the PE level, in the form of SRAM-based scratch pads, that contribute up to $16.3\times$ more than the memory accesses associated to the main memory.

- The real throughput achieved by PEs in TrIM matches the peak throughput of 2 OPs/cycle and it is independent by K and I. On the contrary, WS exhibits a lower throughput when small ifmaps are considered, due to the FIFO synchronization that negatively impacts the latency. Finally, the computation scheduling in RS significantly degrades the throughput, considering that multipliers must be stalled at regular intervals to allow the vertical accumulations of psums.

- TrIM requires from $9.9\times$ to $15.6\times$ fewer registers when compared to RS at different K. This is due to the simpler micro-architecture of TrIM's PEs, which do not use memory blocks. Moreover, TrIM is advantageous when also compared to WS and for small ifmaps, considering

that SRBs are smaller than synchronization FIFOs in WS. Furthermore, the larger K, the larger the ifmaps that can be managed by TrIM by using a lower number of registers than WS. This is advantageous with CNNs that make use of different K where, usually, larger K are exploited by larger ifmaps.

VI. CONCLUSION

This paper introduces TrIM, an innovative dataflow for SAs that is compatible with CNN computing. The dataflow has two levels of granularity: at the PE level, weights are kept stationary; high inputs utilization is guaranteed at the SA level, based on a triangular movement. To achieve this, $K \times K$ PEs are interconnected with each other in different directions, and local shift registers are put at the left edge of the array to assist the triangular movement of inputs. We built an analytical model to characterize the array before the physical implementation phase. Memory accesses, throughput and number of registers are subjected to in-depth design space exploration. When compared to WS dataflow, TrIM requires one order of magnitude less memory accesses considering that no data redundancy is exploited. Furthermore, TrIM requires less memory access than RS since no micro-architectural memory blocks assist data circulation. The simpler PEs in TrIM also result in $15.6\times$ fewer registers than RS. Finally, thanks to the overlap between multiplications and accumulations, TrIM's real throughput achieves the peak throughput of 2 OPs/cycle/PE, overcoming RS by 81.8%. In the second part, we present a complete architecture dealing with TrIM and compatible with multi-dimensional convolutions for CNNs. As a case study, the architecture is characterized considering the VGG-16 CNN [29], and compared with state-of-the-art competitors.

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