

# ECE 6775 Final Project: FPGA Acceleration of Post-Quantum Cryptography

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## Introduction

With the increasing reliance on digital systems in the modern age, maintaining the security and privacy of important data is more critical than ever. As such, cryptographic algorithms for securely storing and communicating data have widespread usage. To maintain security, these algorithms are centered around computational problems that are infeasible for classical processors to solve; these are known as *NP-hard* problems, which have no known polynomial time solution. Users with a secret key are able to decrypt the encoded messages, but users without would have to solve this NP-hard problem to access the encrypted data, which are designed to take an astronomical number of years to solve with brute-force.

The advent of quantum computers have called the strengths of many of these algorithms into question. For example, both RSA (a popular asymmetric-key algorithm with widespread use) and Diffie-Hellman (an algorithm for securely establishing a common shared key, for use in symmetric-key encryption) rely on the difficulty of factoring large numbers for their security. Algorithms for quantum computers to solve such problems in polynomial time have existed for a while [1], but have never had a computer advanced enough to run them. However, modern advances in quantum computing have demonstrated that computers may be available soon that can crack these algorithms. Even just earlier this week, Google unveiled a new quantum computer, "Willow", that can achieve speedups over the fastest classical processors on select problems by a factor of  $10^{30}$  [2].

While such computers aren't currently able to break modern cryptographic algorithms, many experts suspect it's only a matter of time before current cryptographic algorithms become insecure [3]. To this end, NIST (the National Institute of Standards and Technology) has standardized the use of RSA-2048 only until 2030, and noted that updated strengths are heavily affected by any progress on quantum computing [4]. Additionally, to prepare for the advance of quantum computing, NIST has standardized additional, *quantum-resistant* algorithms [5]. These algorithms are centered around different computational problems for which there is no known algorithm to efficiently solve for both classical and quantum computers. This *post-quantum cryptography* (PQC) will have increasing significance as advances in quantum computers are made. Additionally, since malicious adversaries could already be recording data to later decrypt once sufficient quantum computers are available, PQC algorithms are already being recommended and used for extremely sensitive data, such as government operations [6].

For public-key encryption (where the encrypting and decrypting keys are different), as well as key establishment (for securely establishing a shared secret key over an insecure network), NIST recommends CRYSTALS-Kyber, or simply **Kyber**. Since such an algorithm would be widely used in communication, speeding up its operation would have large impacts for a variety of applications. For our project, we explored implementing Kyber using custom hardware on an FPGA.

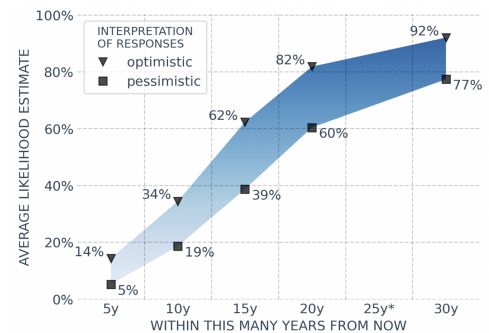


Figure 1: A timeline of when experts believe that RSA-2048 will be able to be broken by a quantum computer in 24 hours [3]

# Problem Description - Kyber

## Components of the Kyber Algorithm

## Optimization of NTT

## Implementations

## FPGA Adaptation

## Code Changes

## Simulation

## Host Implementation

## Evaulation

## Synthesis

## Experimental

## Project Management

## Milestones

The project was initially divided into four main milestones for each week, but as the project progressed it split into two main goals. First, we focused on optimizing a single kernel, the NTT kernel, which was the most computationally intensive part of the Kyber algorithm. Second, we also focused on optimizing the entire Kyber algorithm as a whole. As such, the main milestones of the project were

1. Synthesis of the NTT kernel on the FPGA.
2. Synthesis of the entire Kyber algorithm on the FPGA.
3. Optimization of the NTT kernel.
4. Optimization of the entire Kyber algorithm.

## Timeline

### Week of 11/17: Research and Planning

- |   |               |
|---|---------------|
| 1. Research on the Kyber cryptographic algorithm.                 | Everyone      |
| 2. Find a suitable C/C++ implementation of Kyber in software.     | Everyone      |
| 3. Implement test cases for the HLS implementations.              | Barry         |
| 4. Creating a build system for the HLS implementations.           | Aidan, Edmund |
| 5. Begin converting software implementation for synthesizability. |               |
| (a) Converting types to HLS compatible types.                     | Aidan         |
| (b) Removing standard library calls.                              | Barry         |
| (c) Converting arguments to template parameters.                  | Edmund        |
| 6. Preliminary work synthesizing NTT kernel.                      | Nita          |

### Week of 11/24: Preliminary HLS Implementation and Results

- |   |             |
|---|-------------|
| 1. Finish initial HLS implementation of NTT.  | Aidan, Nita |
| 2. Initial optimizations of NTT Kernel  | Barry       |
| 3. Synthesize and verify correctnesses of HLS implementation on CSIM, and COSIM RTL simulation. | Aidan       |
| 4. Refactor project to create fully synthesizable Kyber algorithm.                              | Edmund      |

### Week of 12/01: Optimization and Final Results

- |   |        |
|---|--------|
| 1. Optimize HLS implementation of NTT to minimize latency and area. | Nita   |
| 2. Create zeboard host software for NTT kernel.                     | Aidan  |
| 3. Create zedboard host software for full Kyber algorithm.          | Edmund |
| 4. Further optimizations on full Kyber algorithm.                   | Barry  |
| 5. Finish DUT and verify full Kyber algorithm with CSIM and COSIM.  | Barry  |

### Week of 12/08: Finalized Results, Report, and Presentation

- |   |               |
|---|---------------|
| 1. Refactor zedboard host software to use batched testing for averaged results. | Aidan, Edmund |
| 2. Finalize results and create presentation.                                    | Everyone      |
| 3. Record final presentation and upload.  | Everyone      |
| 4. Create final report.   | Everyone      |

## Challenges and Setbacks

The main challenge faced by the team was in the compatibility of the reference software implementation with HLS and FPGA. Although the implementation was already written in C, many of the kernels used arrays of unknown lengths in arguments, and a number of functions used pointer arithmetic and other non-synthesizable constructs. This required longer than expected to convert the software implementation into a synthesizable form, which was why we decided to focus on the NTT kernel first. We eventually resolved these issues by using many template arguments as many of the array lengths were known at compile time, and we also had to rewrite some of the functions to eliminate standard library calls and pointer arithmetic. This also required us to move all implementations into header files for linking purposes, which required refactoring the build system as well.

## Conclusion

## Acknowledgements

## References

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