FAN, Hanwei 樊瀚伟

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Research interests: Machine Learning for EDA, Efficient AI, Computer Architecture

Educational Background

The Hong Kong University of Science and Technology (Guangzhou) **09/2021-Now**

✧ **MPhil,** major in **Microelectronics**
✧ **GPA: 3.7 / 4.3**
✧ **Supervisor：** Prof. Dr. Wei ZHANG 张薇
✧ **Core Courses：** Advanced Computer Architecture，Advanced Algorithms, Cross-disciplinary Research Methods

The Hong Kong University of Science and Technology **09/2019-06/2020**

✧ **MSc,** major in **Electronic Engineering**
✧ **GPA: 3.963 / 4.3**
✧ **Core Courses:** Computer Architecture, Embedded Systems, Signal Analysis & Pattern, CMOS VLSI Design, Robotics, Modern Control Systems Design, Engineering Research and Career Development

Beijing Institute of Technology (BIT) **09/2015-06/2019**

✧ **BEng**, major in **Automation**
✧ **GPA: 84.2/100**
✧ **Core Courses:** Automatic Control Theory, Computer Control System, Fundamentals of Intelligent Control, Electrical/Fluid Transmission & Control, Analog/Digital Electronic Technology, Principle of Microcomputer & Interface Technology, Signals and Systems, Power Electronics

Project Experiences

✧ **Homomorphic Encryption (HE) Cost-aware Neural Architecture Search** **09/2022-Now**

- Design a regularization function for differentiable NAS to minimize the computational cost of HE
- Design a computational graph to produce the differentiable computational cost and record the noise level of HE
- Cooperating with Computing Technology Lab, Alibaba DAMO Academy

✧ **Explainable ML for Micro-Architecture Design Space Exploration** **06/2022-Now**

- Design an explainable neural architecture for micro-architecture DSE
- Design a reinforcement learning framework to train the proposed neural network
- Modify the Chipyard to obtain the desired performance information from HPM and print-out traces
- Cooperating with Computing Technology Lab, Alibaba DAMO Academy

✧ **Large-scale system verification framework based on Chipyard** **07/2021-01/2022**

- Design the Python-Chipyard interface
- Design and implement a specialized Ring-bus for Chipyard
- Testing of basic functions based on RISC-V toolchain

✧ **A Bayesian Optimization Framework for CNN Auto Compression** **01/2021-02/2022**

- Propose algorithms that improve the performance of BO for CNN pruning
- Implement the framework using Pytorch and GPy
- Open-source code: https://github.com/fanhanwei/BOCR

✧ **A Design of T-NPC 3-Level 3-Phase Electrical Load Simulator** **10/2018-05/2019**

- Utilize the SVPWM and Redundant Small Vector Action Time Allocation scheme to control the system
- Set up the mathematical model and build the system simulation by MATLAB/SIMULINK.
- Draw the PCB board to drive the IGBTs in the main circuit
- Design Verilog and C programs for FPGA and DSP respectively

Work Experiences

✧ Research Intern – Computing Technology Lab, Alibaba DAMO Academy **06/2022-Now**

✧ Research Assistant –Reconfigurable Computing Systems Lab, HKUST **09/2020-08/2021**

✧ Publications

✧ Hanwei FAN, Jiandong MU, Wei ZHANG, Bayesian Optimization with Clustering and Rollback for CNN Auto Pruning. 17th European Conference on Computer Vision, ECCV 2022

✧ Additional Information

Programing Languages:

Python, Chisel, Verilog, C, C++, C#

Extracurricular Activities:

✧ Served as the as Vice Head of the Literature and Art Department of BIT Student Union (2016-2017)

✧ Staff member of BIT Student Congress (2017)

Awards:

✧ BIT people’s scholarship Second Prize (2018, 2019)

✧ Won the Second Prize in the Beijing College-Student Electronics Design Contest (2018)