CURRICULUM VITAE

Chao Wang

July 20, 2019

PERSONAL INFORMATION

Position: Associate Professor of Computer Science

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EDUCATION HISTORY

2004 Ph.D. in Electrical and Computer Engineering, University of Colorado at Boulder, USA

1999 M.S. in Electrical Engineering, Peking University, China

1996 B.S. in Electrical Engineering, Peking University, China

EMPLOYMENT HISTORY

2017 to present: Associate Professor, Department of Computer Science, University of Southern California (USC), Los Angeles, CA, USA

2016 to 2017: Assistant Professor, Department of Computer Science, University of Southern California (USC), Los Angeles, CA, USA

2016 to 2018: Adjunct Associate Professor, Department of Electrical and Computer Engineering, Virginia Tech, Blacksburg, VA, USA

2011 to 2016: Assistant Professor, Department of Electrical and Computer Engineering, Virginia Tech, Blacksburg, VA, USA

2004 to 2011: Research Staff Member, NEC Laboratories America, Inc., Princeton, NJ, USA

HONORS AND AWARDS

2018 ACM SIGSOFT Distinguished Paper Award (ESEC/FSE), for a paper on timing side channel analysis

2014 Early Adopter Award, NSF/IEEE-TCPP Curriculum Initiative

2013 FMCAD Best Paper Award, for a paper on formal program synthesis

2013 ONR Young Investigator (YIP) Award, U.S. Office of Naval Research

2013 Outstanding New Assistant Professor, College of Engineering, Virginia Tech, Blacksburg, VA, USA

2012 NSF CAREER Award, U.S. National Science Foundation

2010 ACM SIGSOFT Distinguished Paper (FSE), for a paper on concurrent program analysis

2008 Best Paper of the Year Award, ACM Transactions on Design Automation of Electronic Systems, for a paper on software model checking

2006 Technology Commercialization Award, NEC Laboratories America, Inc., for developing a software verification tool named F-Soft

2004 ACM Outstanding Ph.D. Dissertation Award in Electronic Design Automation, for developing abstraction refinement techniques for large-scale model checking

RESEARCH GRANTS

Ongoing Projects

1. **[PI]** NSF, "CSR: Small: Collaborative Research: Safety Guard: A Formal Approach to Safety Enforcement in Embedded Control Systems," $250,000 (2018-2021); Personal share (USC) is 100%
2. **[PI]** NSF, "SaTC: CORE: Medium: Collaborative: Energy-Harvested Security for the Internet of Things," $349,997 (2017-2021); Personal share (USC) is 100%
3. **[PI]** ONR, "Ensuring Security of Android Software via Tailorable Multi-Layer Customization," $1,135,027 (2017-2020), with co-PIs William Halfond and Nenad Medvidovic; Personal share (USC) is 31%
4. **[PI]** NSF, "SHF: Small: Program Analysis-based Makeover for HPC Application Resilience," $420,000 (2016-2019); Personal share (USC) is 100%
5. **[PI]** NSF, "TWC: Small: Security by Compilation: An Automated Approach to Side Channel Resistance," $500,000 (2016-2019), with co-PI Patrick Schaumont; Personal share (USC) is 50%
6. **[co-PI]** NSF, "CSR Medium: Pythia: An Application Analysis and Online Modeling Based Prediction Framework for Scalable Resource Management," $750,000 (2014-2019), with PI Ali Butt; Personal credit (at Virginia Tech) is 50%

Completed Projects

7. **[co-PI]** NSF, "SaTC-EDU: Development and Analysis of a Spiral Theory-based Cybersecurity Curriculum," $299,947 (2016-2018), with PI Vinod Lohani and others: Personal credit (at VT) is 16%
8. **[co-PI]** DARPA, "CRAFT Verification Task (Phase I)," $411,585 (2016-2017), with PI Michael Hsiao; Personal credit (at Virginia Tech) is 50%
9. **[PI]** ONR YIP Award, "Automated Software Model Generation for Identifying and Mitigating Concurrency Vulnerabilities," $510,000 (2013-2017); Personal credit (VT) is 100%
10. **[PI]** NSF CAREER Award, "Automated Concurrency Debugging: An Essential Ingredient for Safety-Critical System Design and Security," $478,000 (2012-2017) with additional $48,000 for REU supplement; Personal credit (at VT) is 100%
11. **[PI]** NSF, "EAGER: Systematic and Scalable Testing of Concurrent Software in the Cloud," $54,202 (2015-2016); Personal credit (VT) is 100%
12. **[co-PI]** NSF, "STTR Phase II, Enhanced Security Monitoring and Intrusion Detection Using Power Fingerprinting for SDR and CR Wireless Systems" (Subcontract from PFP, Inc.), $229,359 (2014-2016), with PI A.A. Beex; Personal credit (VT) is 50% (developing a symbolic execution tool)
13. **[co-PI]** NSF CNS-1128903, "TWC: Medium: SDR Shield: A Hardware-based Security Solution for Software Defined Radio," $700,000 (2012-2016), with PI Yaling Yang and co-PI Jeffery Reed; Personal credit (VT) is 33% (developing a controller synthesis tool)
14. **[PI]** NSF/IEEE TCPP Curriculum Committee, "Integrating NSF/TCPP Curriculum Guidelines into an Undergraduate Core Course at Virginia Tech," $1,500 (2014-2015)
15. **[PI]** Virginia Tech ICTAS Junior Faculty Collaboration Grant, "Automated Synthesis of Software Countermeasures to Defend Against Side-Channel Attacks," $120,000 (2014-2016), with co-PI Patrick Schaumont; Personal credit (VT) is 75%
16. **[PI]** Virginia Tech ICTAS Junior Faculty Collaboration Grant, "Co-Verification of Critical Cyber-Physical Systems: A Formal Approach," $120,000 (2012-2014), with co-PI Michael Hsiao; Personal credit (VT) is 75%

PUBLICATIONS

Notation: asterisk (*) – the author is my student; underscore – the author is the PI of the project

Books

1. Shuvendu K. Lahiri and **Chao Wang** (Eds.). *Automated Technology for Verification and Analysis*. Springer, 2018, 560 pages. ISBN 978-3-030-01089-8. Lecture Notes in Computer Science, 11138.
2. **Chao Wang**, Gary Hachtel, and Fabio Somenzi. *Abstraction Refinement for Large Scale Model Checking*. Springer, 2006, XIV, 179 pages. ISBN-10:0-387-34155-2. The book was based on the first-author's doctoral research, which won 2003-2004 ACM Outstanding PhD Dissertation Award in Electronic Design Automation

Book Chapters

1. Aarti Gupta, Malay Ganai, and **Chao Wang**. "SAT-based verification methods and applications in hardware verification." *Formal Methods for Hardware Verification*, pp. 108-143. Lecture Notes in Computer Science 3965. Springer, 2006. **(Lecture notes for the 6th International School on Formal Methods)**

Refereed Journal Articles

1. Pengfei Gao, Jun Zhang, Fu Song, and and **Chao Wang**. "Verifying and quantifying side-channel resistance of masked software implementation." ACM Transactions on Software Engineering and Methodology. 2019.
2. Tingting Yu, Zunchen Huang*, and **Chao Wang**. "ConTesa: Directed Test Suite Augmentation for Concurrent Software." IEEE Transactions on Software Engineering. 2018.
3. Qiuping Yi, Zijiang Yang, Shengjian Guo, **Chao Wang**, Jian Liu, and Chen Zhao. "Eliminating path redundancy via postconditioned symbolic execution." *IEEE Transactions on Software Engineering*. February 2018.
4. Bettina Konighofer, Mohammed Alshiekh, Roderick Bloem, Laura Humphrey, Robert Konighofer, Ufuk Topcu, and **Chao Wang**. "Shield synthesis." *International Journal on Formal Methods in Systems Design*. September 2017.
5. Mitra Befrouei, **Chao Wang**, and Georg Weissenbacher. "Abstraction and mining of traces to explain concurrency bugs." *International Journal on Formal Methods in System Design*, 49(1-2), pp.1-32. 2016.
6. Kiran Adhikari*, James Street*, **Chao Wang**, Yang Liu, and Shaojie Zhang. "Verifying a quantitative relaxation of linearizability via refinement." *International Journal on Software Tools for Technology Transfer*, 18(4), pp. 393-407. Springer, 2016.
7. Lu Zhang*, Arijit Chattopadhyay*, and **Chao Wang**. "Round-Up: Runtime verification of quasi linearizability for concurrent data structures." *IEEE Transactions on Software Engineering*. 41(12), pp. 1202-1216. 2015.
8. Qiuping Yi, Zijiang Yang, Jian Liu, Chen Zhao, and **Chao Wang**. "Explaining software failures by cascade fault localization." *ACM Transactions on Design Automation of Electronic Systems*. 20(3), pp. 41:1-28. 2015.
9. Hassan Eldib*, **Chao Wang**, Mostafa Taha, and Patrick Schaumont. "Quantitative masking strength: Quantifying the power side-channel resistance of software code." *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems*, 34(10), pp. 1558-1568. 2015.
10. Hassan Eldib*, **Chao Wang**, and Patrick Schaumont. "Formal verification of software countermeasures against side-channel attacks." *ACM Transactions on Software Engineering and Methodology*, 24(2), pp. 11:1-24. 2014.
11. Hassan Eldib* and **Chao Wang**. "An SMT based method for optimizing arithmetic computations in embedded software code." *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems*, 33(11), pp. 1611-1622. 2014.
12. **Chao Wang**, Sudipta Kundu*, Malay Ganai, and Aarti Gupta. "Symbolic predictive analysis of concurrent programs." *J. Formal Aspects of Computing*, 23(6), pp. 781-805. Springer, 2011.

13. Zijiang Yang, **Chao Wang**, Aarti Gupta, and Franjo Ivancic. "Model checking sequential software programs via mixed symbolic analysis." *ACM Transactions on Design Automation of Electronic Systems*, 14(1), pp. 1-26. 2009.
14. **Chao Wang**, Zijiang Yang, Franjo Ivancic, and Aarti Gupta. "Disjunctive image computation for software model checking." *ACM Transactions on Design Automation of Electronic Systems*, 12(2), pp. 1-26. ACM, 2007. (**Best Paper of the Year Award**)
15. **Chao Wang**, Bing Liu, Hoonsang Jin, Gary Hachtel, and Fabio Somenzi. "Improving Ariadne's bundle by following multiple counterexamples in abstraction refinement." *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems*, 25(11), pp. 2297-2316. 2006.
16. **Chao Wang**, Roderick Bloem, Kavita Ravi, Gary Hachtel, and Fabio Somenzi. "Compositional SCC analysis for language emptiness checking." *International Journal on Formal Methods in Systems Design*, 28(1), pp. 5-36. Springer, 2006.
17. Bing Li, **Chao Wang**, and Fabio Somenzi. "Abstraction refinement in symbolic model checking using satisfiability as the only decision procedure." *International Journal on Software Tools for Technology Transfer*, 7(2), pp. 143-155. Springer, 2005.

Refereed Conference Papers

1. **[FMCAD'19]** Meng Wu*, Jingbo Wang*, Jyotirmoy Deshmukh and **Chao Wang**. "Shield synthesis for real: Enforcing safety in cyber physical systems." *Proc. Intl. Conf. Formal Methods in Computer-Aided Design*, 2019.
2. **[FSE'19]** Jingbo Wang*, Chungha Sung* and **Chao Wang**. "Mitigating power side channels during compilation." *Proc. ACM Joint European Software Engineering Conference and Symposium on the Foundations of Software Engineering*. 2019
3. **[PLDI'19]** Meng Wu* and **Chao Wang**. "Abstract interpretation under speculative execution." *Proc. ACM SIGPLAN Symp. Programming Language Design and Implementation*. 2019.
4. **[FSE'18]** Shengjian Guo*, Meng Wu* and **Chao Wang**. "Adversarial symbolic execution for detecting concurrency-related cache timing leaks." *Proc. ACM Joint European Software Engineering Conference and Symposium on the Foundations of Software Engineering*. 2018. (**ACM SIGSOFT Distinguished Paper Award**)
5. **[ASE'18]** Chungha Sung*, Shuvendu Lahiri, Constantin Enea and **Chao Wang**. "Datalog-based scalable semantic diffing of concurrent programs." *Proc. IEEE/ACM Intl. Conf. Automated Software Engineering*. 2018.
6. **[ASE'18]** Chungha Sung*, Brandon Paulsen * and **Chao Wang**. "CANAL: A cache timing analysis framework via LLVM transformation." *Proc. IEEE/ACM Intl. Conf. Automated Software Engineering*, Tool Demonstration Track. 2018.
7. **[ISSTA'18]** Meng Wu*, Shengjian Guo*, Patrick Schaumont and **Chao Wang**. "Eliminating timing side-channel leaks using program repair." *Proc. ACM SIGSOFT Intl. Symp. Software Testing and Analysis*. 2018.
8. **[CAV'18]** Jun Zhang, Pengfei Gao, Fu Song and **Chao Wang**. "SCInfer: Refinement-based verification of software countermeasures against side-channel attacks." *Proc. Intl. Conf. Computer Aided Verification*. 2018.
9. **[ASE'17]** Chungha Sung*, Markus Kusano* and **Chao Wang**. "Modular verification of interrupt-driven software." *Proc. IEEE/ACM Intl. Conf. Automated Software Engineering*. 2017.
10. **[ASE'17]** Lin Cheng, Zijiang Yang, and **Chao Wang**. "Systematic reduction of GUI test sequences." *Proc. IEEE/ACM Intl. Conf. Automated Software Engineering*. 2017.
11. **[FSE'17]** Markus Kusano* and **Chao Wang**. "Thread-modular static analysis for relaxed memory models." *Proc. ACM SIGSOFT Symp. Foundations of Software Engineering*, 2017.
12. **[FSE'17]** Shengjian Guo*, Meng Wu* and **Chao Wang**. "Symbolic execution of programmable logic controller code." *Proc. ACM SIGSOFT Symp. Foundations of Software Engineering*, 2017.
13. **[FSE'17]** Tingting Yu, Tarannum Zaman, and **Chao Wang**. "DESCRY: Reproducing system-level concurrency failures." *Proc. ACM SIGSOFT Symp. Foundations of Software Engineering*, 2017.

14. **[ICSE'17]** Lu Zhang* and **Chao Wang**. "RClassify: Classifying race conditions in web applications via deterministic replay." *Proc. IEEE/ACM Intl. Conf. Software Engineering*, pp. 278-288, 2017.

15. **[FSE'16]** Markus Kusano* and **Chao Wang**. "Flow-sensitive composition of thread-modular abstract interpretation." *Proc. ACM SIGSOFT Symp. Foundations of Software Engineering*, pp. 799-809, 2016.

16. **[FSE'16]** Chungha Sung*, Markus Kusano*, Nishant Sinha and **Chao Wang**. "Static DOM event dependency analysis for testing web applications." *Proc. ACM SIGSOFT Symp. Foundations of Software Engineering*, pp. 447-459, 2016.

17. **[ASE'16]** Shengjian Guo*, Markus Kusano* and **Chao Wang**. "Conc-iSE: Incremental symbolic execution of concurrent software." *Proc. IEEE/ACM Intl. Conf. Automated Software Engineering*, pp. 531-542. 2016.

18. **[ASE'16]** Li Cheng, Jialiang Chang, Zijiang Yang and **Chao Wang**. "GUICat: GUI testing as a service." *Proc. IEEE/ACM Intl. Conf. Automated Software Engineering*, pp. 858-863. 2016.

19. **[CAV'16]** Hassan Eldib*, Meng Wu *, and **Chao Wang**. "Synthesizing fault-attack countermeasures for cryptographic circuits." *Proc. Intl. Conf. Computer Aided Verification*. July 2016.

20. **[NFM'16]** Meng Wu*, Haibo Zeng, and **Chao Wang**. "Synthesizing runtime enforcer of safety properties under burst error." *Proc. NASA Formal Methods Symposium*, June 2016.

21. **[FSE'15]** Shengjian Guo*, Markus Kusano*, **Chao Wang**, Zijiang Yang, and Aarti Gupta. "Assertion guided symbolic execution of multithreaded programs." *Proc. ACM SIGSOFT Symp. Foundations of Software Engineering*, pp. 854-865. August 2015.

22. **[ISSTA'15]** Sepideh Khoshnood*, Markus Kusano*, and **Chao Wang**. "ConcBugAssist: Constraint solving for diagnosis and repair of concurrency bugs." *Proc. ACM Intl. Symp. Software Testing and Analysis*, pp. 165-176. July 2015.

23. **[PLDI'15]** Naling Zhang*, Markus Kusano*, and **Chao Wang**. "Dynamic partial order reduction for relaxed memory models." *Proc. ACM SIGPLAN Conf. Programming Language Design and Implementation*, pp. 250-259. June 2015.

24. **[ICSE'15]** Markus Kusano*, Arijit Chattopadhyay*, and **Chao Wang**. "Dynamic generation of likely invariants for multithreaded programs." *Proc. IEEE/ACM Intl. Conf. Software Engineering*, pp. 835-846. May 2015.

25. **[ICSE'15]** Qiuping Yi, Zijiang Yang, Jian Liu, Chen Zhao, and **Chao Wang**. "A synergistic analysis method for explaining failed regression tests." *Proc. IEEE/ACM Intl. Conf. Software Engineering*. pp. 257-267. May 2015.

26. **[ICST'15]** Qiuping Yi, Zijiang Yang, Shengjian Guo, **Chao Wang**, Jian Liu, and Chen Zhao. "Post-conditioned symbolic execution," *Proc. IEEE Intl. Conf. Software Testing, Verification, and Validation*, pp. 1-10. April 2015.

27. **[TACAS'15]** Roderick Bloem, Bettena Konighofer, Robert Konighofer, and **Chao Wang**. "Shield synthesis: Runtime enforcement for reactive systems." *Proc. Intl. Conf. Tools and Algorithms for Construction and Analysis of Systems*, pp. 533-548. Lecture Notes in Computer Science Volume 9035. Springer, April 2015.

28. **[ASE'14]** Markus Kusano* and **Chao Wang**. "Assertion guided abstraction: a cooperative optimization for dynamic partial order reduction." *Proc. IEEE/ACM Intl. Conf. Automated Software Engineering*, pp. 175-186. September 2014.

29. **[ISSTA'14]** Lu Zhang* and **Chao Wang**. "Runtime prevention of concurrency related type-state violations in multithreaded applications." *Proc. ACM Intl. Symp. Software Testing and Analysis*, pp. 1-12. July 2014.

30. **[CAV'14]** Hassan Eldib* and **Chao Wang**. "Synthesis of masking countermeasures against side channel attacks." *Proc. Intl. Conf. Computer Aided Verification*, pp. 114-130. Lecture Notes in Computer Science Volume 8559. Springer, July 2014.

31. **[DAC'14]** Hassan Eldib*, **Chao Wang**, Mostafa Taha, and Patrick Schaumont. "QMS: Evaluating the side-channel resistance of masked software from source code." *Proc. ACM/IEEE Design Automation Conference*, pp. 1-6. June 2014.

32. **[TACAS'14]** Hassan Eldib*, **Chao Wang**, and Patrick Schaumont. "SMT-based verification of software countermeasures against side-channel attacks." *Proc. Intl. Conf. Tools and Algorithms for Construction and Analysis of Systems*, pp. 62-77. Lecture Notes in Computer Science Volume 8413. Springer, 2014.

33. **[VMCAI'14]** **Chao Wang** and Kevin Hoang*. "Precisely deciding control state reachability in concurrent traces with limited observability." *Proc. Intl. Conf. Verification, Model Checking, and Abstract Interpretation*, pp. 376-394. Lecture Notes in Computer Science Volume 8318. Springer, 2014.

34. **[RV'14]** Mitra Befrouei, **Chao Wang**, and Georg Weissenbacher. "Abstraction and mining of traces to explain concurrency bugs." *Proc. Intl. Conf. Runtime Verification*, pp. 162-177. Lecture Notes in Computer Science Volume 8734. Springer, 2014.

35. **[ASE'13]** Lu Zhang*, Arijit Chattopadhyay*, and **Chao Wang**. "Round-Up: Runtime checking quasi linearizability of concurrent data structures." *Proc. IEEE/ACM Intl. Conf. Automated Software Engineering*, pp. 4-14. 2013.

36. **[ASE'13]** Markus Kusano* and **Chao Wang**. "CCmutator: A mutation generator for concurrency constructs in multithreaded C/C++ applications." *Proc. IEEE/ACM Intl. Conf. Automated Software Engineering*, pp. 722-725. 2013.

37. **[FMCAD'13]** Hassan Eldib* and **Chao Wang**. "An SMT based method for optimizing arithmetic computations in embedded software code." *Proc. Intl. Conf. Formal Methods in Computer-Aided Design*, pp. 129-136. 2013. **(Best Paper Award)**

38. **[SPIN'13]** Kiran Adhikari*, James Street*, **Chao Wang**, Yang Liu, and Shaojie Zhang. "Verifying a quantitative relaxation of linearizability via refinement." *Proc. Intl. SPIN Symposium on Model Checking of Software*, pp. 24-42. Lecture Notes in Computer Science Volume 7976. Springer, 2013.

39. **[GLS-VLSI'13]** Rashmi Moudgil, Dinesh Ganta, Leyla Nazhandali, Michael Hsiao, **Chao Wang**, and Simin Hall. "A novel statistical and circuit-based technique for counterfeit detection in existing ICs." *Proc. the 23rd ACM Intl. Conf. Great Lakes Symposium on VLSI*, pp. 1-6. ACM, 2013.

40. **[HST'13]** Avinash Desai, Dinesh Ganta, Michael Hsiao, Leyla Nazhandali, **Chao Wang**, and Simin Hall. "Anti-counterfeit integrated circuits using fuse and tamper-resistant time-stamp circuitry." *Proc. IEEE Intl. Conf. Technologies for Homeland Security)*, pp. 480-485. IEEE, 2013.

41. **[CAV'12]** Vineet Kahlon and **Chao Wang**. "Lock removal for concurrent trace programs." *Proc. Intl. Conf. Computer Aided Verification*, pp. 227-243. Lecture Notes in Computer Science Volume 7358. Springer, 2012.

42. **[ICSE'11]** **Chao Wang**, Mahmoud Said*, and Aarti Gupta. "Coverage guided systematic concurrency testing." *Proc. IEEE/ACM Intl. Conf. Software Engineering*, pp. 221-230. 2011.

43. **[POPL'11]** Nishant Sinha and **Chao Wang**. "On interference abstraction." *Proc. ACM Symp. Principles of Programming Languages*, pp. 423-434. 2011.

44. **[ASE'11]** Malay Ganai, Nipun Arora, **Chao Wang**, Aarti Gupta, and Gogul Balakrishnan. "BEST: A symbolic testing tool for predicting multi-threaded program failures." *Proc. IEEE/ACM Intl. Conf. Automated Software Engineering*, pp. 596-599. 2011.

45. **[MEMOCODE'11]** Arnab Sinha*, Sharad Malik, **Chao Wang**, and Aarti Gupta. "Predictive analysis for detecting serializability errors through trace segmentation," *Proc. IEEE/ACM Intl. Conf. Formal Methods and Models for Codesign*, pp. 99-108. 2011.

46. **[NFM'11]** Mahmoud Said*, **Chao Wang**, Zijiang Yang, and Karem Sakallah. "Generating data race witnesses by an SMT-based analysis," *Proc. NASA Formal Methods*, pp. 313-327. Lecture Notes in Computer Science Volume 6617. Springer, 2011.

47. **[HVC'11]** Arnab Sinha*, Sharad Malik, **Chao Wang**, and Aarti Gupta. "Predicting serializability violations: SMT-based search vs. DPOR-based search," *Proc. Intl. Haifa Verification Conference*, pp. 95-114. Lecture Notes in Computer Science Volume 7261. Springer, 2011.

48. **[FSE'10]** Nishant Sinha and **Chao Wang**. "Staged concurrent program analysis," N. Sinha and Chao Wang. *Proc. ACM Symp. Foundations of Software Engineering*, pp. 47-56. 2010. **(ACM SIGSOFT Distinguished Paper Award)**

49. **[CAV'10]** Vineet Kahlon and **Chao Wang**. "Universal causality graphs: a precise happens-before model for detecting bugs in concurrent programs." *Proc. Intl. Conf. Computer Aided Verification,* pp. 434-449. Lecture Notes in Computer Science Volume 6174. Springer, 2010.

50. **[CAV'10]** Sudipta Kundu*, Malay Ganai, and **Chao Wang**. "CONTESSA: Concurrency Testing Augmented with Symbolic Analysis." *Proc. Intl. Conf. Computer Aided Verification,* pp. 127-131. Lecture Notes in Computer Science Volume 6174. Springer, 2010.

51. **[ICCAD'10]** Malay Ganai, **Chao Wang**, and Weihong Li. "Efficient state space exploration: Interleaving stateless and state-based model checking." *Proc. IEEE/ACM Intl. Conf. Computer-Aided Design*, pp. 786-793. 2010.

52. **[TACAS'10]** **Chao Wang**, Rhishikesh Limaye*, Malay Ganai, and Aarti Gupta. "Trace-based symbolic analysis for atomicity violations" *Proc. Intl. Conf. Tools and Algorithms for the Construction and Analysis of Systems*, pp. 328-342. Lecture Notes in Computer Science Volume 6015. Springer, 2010.

53. **[RV'10]** Malay Ganai and **Chao Wang**. "Interval analysis for concurrent trace programs using transaction sequence graphs," *Proc. Intl. Conf. Runtime Verification,* pp. 253-269. Lecture Notes in Computer Science Volume 6418. Springer, 2010.

54. **[FM'09]** **Chao Wang**, Sudipta Kundu*, Malay Ganai, and Aarti Gupta. "Symbolic predictive analysis of concurrent programs." *Proc. Intl. Symp. Formal Methods,* pp. 256-272. Lecture Notes in Computer Science Volume 5850. Springer, 2009.

55. **[FSE'09]** **Chao Wang**, Swarat Chaudhuri, Aarti Gupta, and Yu Yang*. "Symbolic pruning of concurrent program executions." *Proc. ACM Symp. Foundations of Software Engineering*, pp. 23-32. 2009.

56. **[CAV'09]** Vineet Kahlon, **Chao Wang**, and Aarti Gupta. "Monotonic partial order reduction: an optimal symbolic POR technique." *Proc. Intl. Conf. Computer Aided Verification*, pp. 298-413. Lecture Notes in Computer Science Volume 5643. Springer, 2009.

57. **[TACAS'08]** **Chao Wang**, Zijiang Yang, Vineet Kahlon, and Aarti Gupta. "Peephole partial order reduction." *Proc. Intl. Conf. Tools and Algorithms for the Construction and Analysis of Systems*, pp. 382-396. Lecture Notes in Computer Science Volume 4963. Springer, 2008.

58. **[FSE'08]** Fang Yu*, **Chao Wang**, Aarti Gupta, and Tevfik Bultan. "Modular verification of web services using efficient symbolic encoding and summarization." *Proc. ACM Intl. Symp. Foundations of Software Engineering*, pp. 192-202. 2008.

59. **[ATVA'08]** **Chao Wang**, Yu Yang*, Aarti Gupta, and Ganesh Gopalakrishnan. "Dynamic model checking with property driven pruning to detect race conditions," *Proc. Intl. Symp. Automated Technology for Verification and Analysis*, pp. 126-140. Lecture Notes in Computer Science Volume 5311. 2008.

60. **[FMCAD'07]** **Chao Wang**, Aarti Gupta, and Franjo Ivancic. "Induction in CEGAR for detecting counterexamples." *Proc. Intl. Conf. Formal Methods in Computer Aided Design*, pp. 77-84. 2007.

61. **[ICCAD'07]** **Chao Wang**, Hyondeuk Kim*, and Aarti Gupta. "Hybrid CEGAR: combining variable hiding and predicate abstraction." *Proc. IEEE/ACM Intl. Conf. Computer-Aided Design*, pp. 310-317. 2007.

62. **[CAV'07]** **Chao Wang**, Zijiang Yang, Aarti Gupta, and Franjo Ivancic. "Using counterexamples for improving the precision of reachability computation with polyhedra." *Proc. Intl. Conf. Computer Aided Verification,* pp. 352-365. Lecture Notes in Computer Science Volume 4590. Springer, 2007.

63. **[CAV'06]** Himanshu Jian*, Franjo Ivancic, Aarti Gupta, Ilya Shlyakhter, and **Chao Wang**. "Using statically computed invariants inside the predicate abstraction and refinement loop." *Proc. Intl. Conf. Computer Aided Verification,* pp. 137-151. Lecture Notes in Computer Science Volume 4144. Springer, 2006.

64. **[DAC'06]** **Chao Wang**, Aarti Gupta, and Malay Ganai. "Predicate learning and selective theory deduction for a difference logic solver." *Proc. ACM/IEEE Design Automation Conference*, pp. 235-240. 2006.

65. **[DATE'06]** **Chao Wang**, Zijiang Yang, Franjo Ivancic, and Aarti Gupta. "Disjunctive image computation for embedded software verification." *Proc. Design, Automation and Test in Europe,* pp. 1205-1210. 2006.

66. **[ATVA'06]** **Chao Wang**, Zijiang Yang, Franjo Ivancic, and Aarti Gupta. "Whodunit? Causal analysis for counterexamples," *Proc. Intl. Symp. Automated Technology for Verification and Analysis,* pp. 82-95. Lecture Notes in Computer Science Volume 4218. Springer, 2006.

67. **[MEMOCODE'06]** Zijiang Yang, **Chao Wang**, Aarti Gupta, and Franjo Ivancic. "Mixed symbolic representations for model checking software programs," *Proc. ACM/IEEE Intl. Conf. Formal Methods and Models for Codesign,* pp. 17-26. 2006.

68. **[LPAR'05]** **Chao Wang**, Franjo Ivancic, Malay Ganai and Aarti Gupta. "Deciding separation logic formulae by SAT and incremental negative cycle elimination," *Proc. Intl. Conf. Logic for Programming Artificial Intelligence and Reasoning,* pp. 322-336. Lecture Notes in Computer Science Volume 3835. Springer, 2005.

69. **[ICCD'04]** **Chao Wang**, Gary Hachtel, and Fabio Somenzi. "Fine-grain abstraction and sequential don't cares for large scale model checking." *Proc. IEEE Intl. Conf. Computer Design,* pp. 112-118. 2004.

70. **[DAC'04]** **Chao Wang**, Hoonsang Jin, Gary Hachtel, and Fabio Somenzi. "Refining the SAT decision ordering for bounded model checking." *Proc. ACM/IEEE Design Automation Conference (**DAC**),* pp. 535-538. 2004.

71. **[ICCAD'03]** **Chao Wang**, Bing Li, Hoonsang Jin, Gary Hachtel, and Fabio Somenzi. "Improving Ariadne's bundle by following multiple threads in abstraction refinement." *Proc. IEEE/ACM Intl. Conf. Computer-Aided Design,* pp. 408-415. 2003.

72. **[ICCAD'03]** **Chao Wang**, Gary Hachtel, and Fabio Somenzi. "The compositional far side of image computation." *Proc. IEEE/ACM Intl. Conf. Computer-Aided Design,* pp. 334-340. 2003.

73. **[CAV'03]** Aarti Gupta, Malay Ganai, **Chao Wang**, Zijiang Yang, and Pranav Ashar. "Abstraction and BDDs complement SAT-based BMC in DiVer." *Proc. Intl. Conf. Computer Aided Verification,* pp. 206-209. Lecture Notes in Computer Science Volume 2725. Springer, 2003.

74. **[DAC'03]** Aarti Gupta, Malay Ganai, **Chao Wang**, Zijiang Yang, and Pranav Ashar. "Learning from BDDs in SAT-based bounded model checking." *Proc. ACM/IEEE Design Automation Conference,* pp. 824-829. 2003.

75. **[FMCAD'02]** **Chao Wang** and Gary Hachtel. "Sharp disjunctive decomposition for language emptiness checking." *Proc. Intl. Conf. Formal Methods in Computer Aided Design,* pp. 106-122. Lecture Notes in Computer Science Volume 2517. Springer, 2002.

76. **[CONCUR'01]** **Chao Wang**, Roderick Bloem, Gary Hachtel, Kavita Ravi, and Fabio Somenzi. "Divide and compose: SCC refinement for language emptiness." *Proc. Intl. Conf. Concurrency Theory,* pp. 456-474. Lecture Notes in Computer Science Volume 2154. Springer, 2001.

Other Scholarly Publications (invited, tutorial, or workshop papers)

77. Meng Wu*, Haibo Zeng, **Chao Wang**, and Huafeng Yu. "Safety Guard: Runtime enforcement for safety-critical cyber-physical systems," *Proc. ACM/IEEE Design Automation Conference (**DAC**),* June 2017. **(Invited paper)**

78. **Chao Wang** and Patrick Schaumont. "Security by Compilation: An automated approach to comprehensive side-channel resistance," ACM SIGLOG News, 4(2), April 2017. **(Newsletter article)**

79. Lixin Li and **Chao Wang**. "Dynamic analysis and debugging of binary code for security applications." *Proc. Intl. Conf. Runtime Verification (**RV**),* pp. 403-423. Lecture Notes in Computer Science Volume 8174. Springer, 2013. **(Tutorial paper)**

80. Avinash Desai, Michael Hsiao, **Chao Wang**, Leyla Nazhandali, and Simin Hall. "Interlocking obfuscation for anti-tamper hardware," *Proc.8th Annual Cyber Security and Information Intelligence Research Workshop (**CSIIRW**),* pp. 1-8. ACM, 2013.

81. **Chao Wang** and Malay Ganai. "Predicting concurrency failures in the generalized execution traces of x86 executables," *Proc. Intl. Conf. Runtime Verification (**RV**),* pp. 4-18. Lecture Notes in Computer Science Volume 7186. Springer, 2011. **(Tutorial paper)**

82. Gogul Balakrishnan, Malay Ganai, Aarti Gupta, Franjo Ivancic, Vineet Kahlon, Weihong Li, Naoto Maeda, Nadia Papakonstantinou, Sriram Sankaranarayanan, Nishant Sinha, and **Chao Wang**. "Scalable and precise program analysis at NEC," *Proc. Intl. Conf. Formal Methods for Computer Aided Design (**FMCAD**),* pp. 273-274. 2010. **(Invited paper)**

83. Yu Yang*, Xiaofang Chen, Ganesh Gopalakrishnan, and **Chao Wang**. "Automatic discovery of transition symmetry in multithreaded programs using dynamic analysis," *Proc. Intl. SPIN Workshop on Model Checking Software (**SPIN**)*, pp. 279-295. Lecture Notes in Computer Science Volume 5578. Springer, 2009.
84. Malay Ganai, Aarti Gupta, Franjo Ivancic, Vineet Kahlon, Weihong Li, N. Papakonstantinou, Sriram Sankaranarayanan, and **Chao Wang**. "Towards precise and scalable verification of embedded software," *Design and Verification Conference (**DVCon**)*, pp. 1-9. 2008. **(Invited paper)**
85. Franjo Ivancic, I. Shlyakhter, Aarti Gupta, Malay Ganai, Vineet Kahlon, **Chao Wang** and Zijiang Yang. "Model checking C programs using F-Soft," *Proc. IEEE Intl. Conf. Computer Design (**ICCD**)*, pp. 297-308. 2005. **(Invited paper)**
86. Franjo Ivancic, Sriram Sankaranarayanan, and **Chao Wang**. "Foreword: Special issue on numerical software verification," *J. Formal Methods in System Design*, 35(3): 227-228. Springer, 2009. **(Guest editor)**
87. Bing Li, **Chao Wang** and Fabio Somenzi. "A satisfiability-based approach to abstraction refinement in model checking," *Proc. Intl. Workshop Bounded Model Checking (**BMC**)*. Electronic Notes in Theoretical Computer Science 89(4):608-622 (2003).

Patents Awarded

1. Vineet Kahlon and **Chao Wang**, "Universal causality graphs for bug detection in concurrent programs." *US Patent 8,769,499 (2014)*.
2. Vineet Kahlon and **Chao Wang**, "Lock removal for concurrent programs." *US Patent 8,612,940* (2013).
3. Nishant Sinha and **Chao Wang**, "Systems and methods for concurrency analysis." *US Patent 8,595,708* (2013).
4. Malay Ganai, **Chao Wang**, and Weihong Li, "System and method for model checking by interleaving stateless and state-based methods." *US Patent 8,589,126* (2013).
5. Nishant Sinha and **Chao Wang**, "Precise thread-modular summarization of concurrent programs." *US Patent 8,561,029 (2013).*
6. Vineet Kahlon, **Chao Wang**, and Aarti Gupta, "System and method for monotonic partial order reduction." *US Patent 8,381,226 (2013)*.
7. **Chao Wang**, Aarti Gupta, Swarat Chaudhuri, and Yu Yang, "Symbolic reduction of dynamic executions of concurrent programs." *US Patent 8,359,578 (2013)*.
8. **Chao Wang** and Aarti Gupta, "Dynamic model checking with property driven pruning to detect race conditions." *US Patent 8,200,474 (2012)*.
9. **Chao Wang**, Zijiang Yang, Vineet Kahlon, and Aarti Gupta, "Partial order reduction using guarded independence relations." *US Patent 8,176,496 (2012)*.
10. **Chao Wang**, Zijiang Yang, and Aarti Gupta, "Reachability analysis for program verification." *US Patent 7,926,039 (2011)*.
11. **Chao Wang**, Aarti Gupta, Zijiang Yang, and Franjo Ivancic, "Disjunctive image computation for sequential systems." *US Patent 7,693,690 (2010)*.

Talks

1. "Security by Compilation: Formal verification and synthesis tools for side-channel resistance,"
    a. *Short plenary talk, NSF Workshop on Side and Covert Channels in Computing Systems, Washington, DC,* March 2018.
2. "Security by Compilation: An automated approach to side-channel resistance,"
    a. *Keynote talk, SolCal Programming Languages and Systems Workshop, Riverside, CA,* September 2017.
    b. *HRL Laboratories, LLC, Malibu, CA,* August 2017.
    c. *Invited talk, ISSTA 2017 Workshop on Testing Embedded and Cyber-Physical System,* July 2017.

   d. *CS Colloquium at UT Dallas*, April 2017.
   e. *Annual Research Review at USC Center for Systems and Software Engineering*, April 2017

3. "RClassify: Classifying race conditions in web applications via deterministic replay,"
   a. *International Conference on Software Engineering (ICSE), Buenos Aires, Argentina*, May 2017.
4. "Synthesizing fault-attack countermeasures for cryptographic circuits,"
   a. *International Conference on Computer Aided Verification (CAV), Toronto, Canada,* July 2016.
5. "Synthesizing runtime enforcer of safety properties under burst error,"
   a. *Theoretical CPS Mini-Workshop at USC,* April 2017.
   b. *SoCal Programming Languages and Systems Workshop, Irvine, CA,* November 2016.
   c. *NASA Formal Methods Symposium, Minneapolis, MN*, June 2016.
6. "Constraint-based analysis for verifying and debugging concurrent software,"
   a. *Keynote talk, Workshop on Causal Reasoning for Embedded and Safety-critical System Technologies (CREST*), Eindhoven, the Netherlands, April 2016.
7. "Detecting and mitigating failures in concurrent data structures,"
   a. *Invited talk at the CS Department, Texas A&M University*, September 2015.
8. "Shield synthesis: Runtime enforcement for reactive systems,"
   a. *Talk at the DIFT 2015 workshop, Austin, TX,* September 2015.
9. "SMT for cryptographic and concurrent software verification,"
   a. *Invited lecture at the 2014 SAT/SMT Summer School, Semmering, Austria*, July 2014.
10. "Symbolic predictive analysis for improving the reliability and security of concurrent software,"
   a. *Invited talk at Vienna University of Technology (TU Wien), Vienna, Austria,* September 2013.
   b. *Invited talk at Fujitsu Laboratories of America, Inc., Sunnyvale, CA,* August 2013.
   c. *Invited talk at NASA Ames Research Center, CA,* August 2013.
   d. *Invited talk at DOE Sandia Laboratory, Livermore, CA,* August 2013.
11. "Runtime verification methods for concurrent data structures,"
   a. *Talk at the EC2 workshop: Exploiting Concurrency Efficiently and Correctly, St. Petersburg, Russia*, July 2013.
12. "Dynamic analysis and debugging of binary code for security applications,"
   a. *Tutorial presentation at Intl. Conf. Runtime Verification (RV), Rennes, France*, September 2013.
13. "Predicting concurrency failures in the generalized execution traces of x86 executables,"
   a. *Tutorial presentation at Intl. Conf. Runtime Verification (RV), San Francisco, CA*, September 2011.
14. "Generating data race witnesses by an SMT-based analysis,"
   a. *Talk at the SMT workshop: 9th International Workshop on Satisfiability Modulo Theories, Snowbird, Utah*. July, 2011.
15. "Symbolic predictive analysis for concurrent programs,"
   a. *Lecture in the Research Symposium on Embedded Security, Arlington, VA,* March 2013.
   b. *Talk in the CS Colloquium, Virginia Tech,* September 2011.
   c. *Talk in the CS Colloquium, University of California, Santa Barbara,* April 2011.
   d. *Talk in the CS Colloquium, University of Colorado at Boulder,* August 2010.

e. *Talk at the EC2 workshop: Exploiting Concurrency Efficiently and Correctly*, Edinburgh, UK, July 2010.

f. *Talk in the Northeastern Verification Seminar, New York University*, April 2010.

16. "Embedded software verification: challenges and solutions," co-presented with D. Kroening and S. Lahiri.

a. *Full-day tutorial presentation at Intl. Conf. Computer Aided Design (ICCAD)*, November 2008.

17. "Predicate learning and selective theory propagation for a difference logic solver,"

a. *Talk at the PDPAR workshop: Pragmatics of Decision Procedures in Automated Reasoning*, Seattle, WA, July 2006.

18. "Abstraction refinement for large scale model checking,"

a. *Talk at Jasper Design Systems, Inc.*, May 2004.

b. *Talk at NEC Laboratories America, Inc.*, April 2004

c. *Talk at Cadence Design Systems, Inc.*, April 2004

d. *Talk at Mentor Graphics, Inc.*, April 2004.

e. *Talk at the CS Colloquium, Columbia University*, March 2004.

f. *Talk at the CS Colloquium, University of Colorado at Boulder*, March 2004

Software Artifacts Released

SC-Eliminator (2018 – present)

- LLVM compiler based tool for mitigating instruction- and cache-timing side channels in cryptographic software code (C/C++ programs). LINK: https://doi.org/10.5281/zenodo.1299357

EcDiff (2018 – present)

- A semantic diffing tool for concurrent programs using Datalog-based declarative program analysis techniques. LINK: https://github.com/ChunghaSung/EC-Diff

CANAL (2018 – present)

- Modeling cache timing behaviors of C programs via LLVM compiler transformation for verification tools. LINK: https://github.com/canalcache/canal

Watts and FruitTree (2016 – present)

- Thread-modular static analyzer based on abstraction interpretation, for both sequential consistency and relaxed memory models (TSO, PSO, and RMO). https://github.com/markus-kusano/watts

JSDep (2016 – present)

- Static DOM event dependency analyzer for JavaScript-based web applications, to speed up the testing tool named Artemis. LINK: https://github.com/sch8906/JSdep

Shield Synthesizer (2016 – present)

- Synthesizing a shield from temporal logic formulas, to protect reactive systems from safety violations with certainty. LINK: https://bitbucket.org/mengwu/shield-synthesis/

Glitch Remover (2016 – present)

- Re-synthesizing the Boolean circuits that implement cryptographic algorithms to remove timing side channels due to clock glitching. LINK: https://bitbucket.org/mengwu/fac_syn/

Conc-BugAssist (2015 – present)

- A tool for automatically diagnosing concurrency bugs and suggesting potential repairs. Based on bounded model checking (CBMC) and MAX-SAT. Link: http://www-bcf.usc.edu/~wang626/project_concbugassist.htm

SC Sniffer (2014 – present)

- An SMT solver-based static analysis tool for detecting power side-channel leaks in cryptographic software and for synthesizing masking countermeasures. Link: http://www-bcf.usc.edu/~wang626/project_sniffer.htm

Round-Up (2013 – present)

- A runtime verification tool for detecting linearizability violations and other bugs in concurrent data structures. Link: http://www-bcf.usc.edu/~wang626/project_roundup.htm

CCmutator (2013 – present)

- A Clang/LLVM based mutation generation tool for POSIX Threads and C++11 concurrency constructs. Link: https://github.com/markus-kusano/CCMutator

Fusion (2008–2011)

- A collection of testing and verification tools for multithreaded C/C++ programs. Based on model checking, trace-based static analysis, and symbolic reasoning. I was the architect of the Fusion platform.

F-Soft (2004–2008)

- An in-house verification tool for C/C++ programs in commercial settings. Based on a synergy of static analysis and model checking. I received a NEC *technology commercialization award* for my contributions in 2006.

DiVer (2004–2008)

- A formal verification tool for hardware designs in commercial settings. Based on symbolic model checking, BDDs, SAT, and abstraction refinement.

VIS (2000–2004)

- An academic model checking tool for VLSI circuits co-developed at U. of Colorado, Berkeley, and UT-Austin. I contributed to the VIS-2.0 and VIS-2.1 releases. Link: http://vlsi.colorado.edu/~vis/

MENTORING

Doctoral Students (Graduated)

1. Meng Wu, Ph.D., Virginia Tech, 2019. Dissertation: "Analysis and Enforcement of Properties in Software Systems." **ACM SIGSOFT Distinguished Paper Award (2018)**. First employment: Software Engineer at Ant Financial, Inc.
2. Shengjian (Daniel) Guo, Ph.D., Virginia Tech, 2018. Dissertation: "Efficient Symbolic Execution of Concurrent Software." **ACM SIGSOFT Distinguished Paper Award (2018)**. First employment: Software Engineer at Baidu X-Lab, Inc.
3. Markus Kusano, Ph.D., Virginia Tech, 2018. Dissertation: "Constraint-Based Thread-Modular Abstract Interpretation." **NSF Graduate Research Fellowship (2016), Bradley Fellowship (2014).** First employment: Software Engineer at Google, Inc.
4. Lu Zhang, Ph.D., Virginia Tech, 2016. Dissertation: "Runtime Verification and Debugging of Concurrent Software." First employment: Software Engineer at Oracle, Inc.
5. Hassan Eldib, Ph.D., Virginia Tech, 2015. Dissertation: "Constraint based Program Synthesis for Embedded Software." **FMCAD Best Paper Award (2013).** First employment: Postdoc at Rice University and then Assistant Professor at AAST, Egypt

Doctoral Students (Current – USC)

1. Zunchen Huang, since August 2018.
2. Chenggang (Oscar) Li, since July 2019.
3. Yannan Li, since August 2018.
4. Brandon Paulsen, since August 2017.

5. Chungha Sung, since August 2017.
6. Jingbo Wang, since August 2017.

Masters Students (Graduated)

1. Sepideh Khoshnood, M.S., Virginia Tech, 2015. Thesis title: "Constraint Solving for Diagnosing Concurrency Bugs." First employment: Software Engineer at Microsoft, USA
2. Arijit Chattopadhyay, M.S., Virginia Tech, 2014. Thesis title: "Dynamic Invariant Generation for Concurrent Programs." First employment: Software Engineer at Bloomberg, USA
3. Kiran Adhikari, M.S., Virginia Tech, 2013. Thesis title: "Verifying a Quantitative Relaxation of Linearizability via Refinement." First employment: Engineer at Intel Corporation, USA

Doctoral Dissertation Committees

1. Pooyan Behnamghader, Ph.D. in Computer Science (USC), 2019. Advisor: Barry Boehm
2. Celia Chen, Ph.D. in Computer Science (USC), 2019. Advisor: Barry Boehm
3. Abdulmajeed Alameer, Ph.D. in Computer Science (USC), 2019. Advisor: William G.J. Halfond
4. Jiaping Gui, Ph.D. in Computer Science (USC), 2019. Advisor: William G.J. Halfond
5. Duc Le, Ph.D. in Computer Science (USC), 2018. Advisor: Nenad Medvidovic
6. Arman Shahbazian, Ph.D. in Computer Science (USC), 2018. Advisor: Nenad Medvidovic
7. Yazeed Alabdulkarim, Ph.D. in Computer Science (USC), 2018. Advisor: Shahram Ghandeharizadeh
8. Sonal Mahajan, Ph.D. in Computer Science (USC), 2018. Advisor: William G.J. Halfond
9. Vireshwar Kumar, Ph.D. in Computer Engineering (Virginia Tech), 2016. Advisor: Jung-Min Park
10. Nahid Farhady Ghalaty, Ph.D. in Computer Engineering (Virginia Tech), 2016. Advisor: Patrick Schaumont
11. Kelson Gent, Ph.D. in Computer Engineering (Virginia Tech), 2016. Advisor: Michael Hsiao
12. Kevin Zeng, Ph.D. in Computer Engineering (Virginia Tech), 2016. Advisor: Peter Athanas
13. Shin Hong, Ph.D. in Computer Science (KAIST, Korea), 2015. Advisor: Moonzoo Kim
14. Mahesh Nanjundappa, Ph.D. in Computer Engineering (Virginia Tech), 2015. Advisor: Sandeep Shukla
15. Matthew Eric Anderson, Ph.D. in Computer Engineering (Virginia Tech), 2015. Advisor: Sandeep Shukla
16. Alexandru Turcu, Ph.D. in Computer Engineering (Virginia Tech), 2014. Advisor: Binoy Ravindran
17. Mahmoud Atef Elbayoumi, Ph.D. in Computer Engineering (Virginia Tech), 2014. Advisor: Michael Hsiao
18. Sarvesh Prabhu, Ph.D. in Computer Engineering (Virginia Tech), 2014. Advisor: Michael Hsiao
19. Chu Duc Hiep, Ph.D. in Computer Science (NUS, Singapore), 2013. Advisor: Joxan Jaffar
20. Mahmoud Said, Ph.D. in Computer Science (Western Michigan University), 2012. Advisor: Zijiang Yang
21. Arnab Sinha, Ph.D. in Electrical Engineering (Princeton University), 2012 (served as a thesis "reader"). Advisor: Sharad Malik
22. Zhaohui Fu, Ph.D. in Electrical Engineering (Princeton University), 2007 (served as a thesis "reader"). Advisor: Sharad Malik

Master's Thesis Committees

1. Tatsuhiko Tomita, M.S. in Computer Science (USC), 2017
2. Tonmoy Roy, M.S. in Computer Engineering (Virginia Tech), 2017

3. Prateek Puri, M.S. in Computer Engineering (Virginia Tech), 2015
4. Zeying Yuan, M.S. in Computer Engineering (Virginia Tech), 2015
5. Vineeth Acharya, M.S. in Computer Engineering (Virginia Tech), 2015
6. Michael Dylan Dsouza, M.S. in Computer Engineering (Virginia Tech), 2015
7. Sharad Bagri, M.S. in Computer Engineering (Virginia Tech), 2015
8. Ajithchandra Saya, M.Eng. in Computer Engineering (Virginia Tech), 2015
9. Suraj Das, M.Eng. in Computer Engineering (Virginia Tech), 2015
10. Kaushik Rangarajan, M.Eng. in Computer Engineering (Virginia Tech), 2015
11. Nikhil Parlapalli, M.Eng. in Computer Engineering (Virginia Tech), 2015
12. Gautam Chopra, M.Eng. in Computer Engineering (Virginia Tech), 2015
13. Moein Pahlavan Yali, M.S. in Computer Engineering (Virginia Tech), 2014
14. David Gabriel Katz, M.S. in Computer Engineering (Virginia Tech), 2014
15. Shuchi Pandit, M.S. in Computer Engineering (Virginia Tech), 2014
16. Frank Cuitis Alvert, M.S. in Computer Engineering (Virginia Tech), 2014
17. Zhenhe Pan, M.S. in Computer Engineering (Virginia Tech), 2014
18. Matthew Wallace Kracht, M.S. in Computer Engineering (Virginia Tech), 2014
19. Sree Ram Mohanan, M.Eng. in Computer Engineering (Virginia Tech), 2014
20. Vijeyendra Vallam, M.Eng. in Computer Engineering (Virginia Tech), 2014
21. Avinash Desai, M.S. in Computer Engineering (Virginia Tech), 2013
22. Thomas Jacob Plummer, M.Eng. in Computer Engineering (Virginia Tech), 2013
23. Robin James, M.Eng. in Computer Engineering (Virginia Tech), 2013
24. James Joshua Street, M.Eng. in Computer Engineering (Virginia Tech), 2013
25. Gyanendra Shrestha, M.S. in Computer Engineering (Virginia Tech), 2012

Intern Students Supervised (* means the internship led to a co-authored scholarly publication)

1. Jie Yu (University of Michigan), interned at NEC Labs of America in Summer 2011
2. Arnab Sinha (Princeton University), interned at NEC Labs of America in Summer 2010**
3. Mahmoud Said (Western Michigan University), interned at NEC Labs of America in Spring and Fall 2010**
4. Rhishikesh Limaye (UC Berkeley), interned at NEC Labs of America in Summer 2009*
5. Yu Yang (University of Utah), interned at NEC Labs of America in Summer 2008***
6. Sudipta Kundu (UC San Diego), interned at NEC Labs of America in Summer 2008**
7. Fang Yu (UC Santa Barbara), interned at NEC Labs of America in Summer 2007 and Summer 2008*
8. Pritam Roy (UC Santa Cruz), interned at NEC Labs of America in Summer 2007
9. Hyondeuk Kim (University of Colorado at Boulder), interned at NEC Labs of America in Summer 2006*
10. Himanshu Jain (Carnegie Mellon University), interned at NEC Labs of America in Summer 2005*

TEACHING

Courses Developed

Automated Reasoning and Verification, CSCI 599 (USC): Graduate course on formal verification, Credit hours: 4.0

- Fall 2017 Class size: 6

Introduction to Software Synthesis, CSCI 699 (USC): Graduate course on program synthesis, Credit hours: 4.0

- Fall 2017 Class size: 7

Courses Taught

Introduction to Artificial Intelligence, CSCI 360 (USC): Undergraduate course, Credit hours: 4.0

- Spring 2019 Class size: 80

Introduction to Software Engineering, CSCI 310 (USC): Undergraduate course, Credit hours: 4.0

- Fall 2019 Class size: 145
- Fall 2018 Class size: 138

Advanced Verification Techniques for Software Systems, ECE 5984 (Virginia Tech): Graduate course on software verification, Credit hours: 3.0

- Fall 2015 Class size: 8

Testing and Verification of Digital Systems, ECE 5506 (Virginia Tech): Graduate-level course on formal hardware verification, Credit hours: 3.0

- Spring 2016 Class size: 23
- Spring 2015 Class size: 20
- Spring 2014 Class size: 17
- Spring 2013 Class size:17
- Spring 2012 Class size: 10

Multiprocessor Programming, CS/ECE 5510 (Virginia Tech): Graduate-level course on foundations of concurrency and parallel programming, Credit hours: 3.0

- Fall 2012 Class size: 28

Introduction to Data Structures and Algorithms, ECE 2574 (Virginia Tech): Undergraduate core course in computer engineering, Credit hours: 3.0

- Fall 2014 Class size: 52
- Spring 2014 Class size: 55
- Fall 2011 Class size: 28

Guest Lectures

CS 109: Introduction to Computing, University of Southern California, Fall 2016

- Guest lecture on "software safety, reliability, and security."

CS 697: Ph.D. Student Seminar, University of Southern California, Fall 2016

- Guest lecture on "symbolic predictive analysis for concurrent software."

International SAT/SMT Summer School, Semmering, Austria, July 2014

- Invited lecture on "SMT solvers for cryptographic/concurrent software verification."

NSF Sponsored STEP Program, College of Engineering, Virginia Tech, Summer 2013

- Guest lecture on "reliable software systems."

Engineering Research Seminar, College of Engineering, Virginia Tech, Fall 2012

- Guest lecture on "reliable software and systems."

Research Symposium on Embedded Security, Arlington, VA, March 2013

- Tutorial on techniques for "software testing."

CS 598D: Formal Methods in Networking, Princeton University, Spring 2010

- Guest lecture on "SAT/SMT solvers."

Formal Verification of VLSI Systems, ECE 5939 (University of Colorado at Boulder), Fall 2003

- Guest lecture on "bounded model checking."

Analysis and Design of Algorithms, CS 5454 (University of Colorado at Boulder), Spring 2002

- Teaching assistant.

SERVICE

Department Service

2018 – 2019 Member of the PhD Admission Committee, CS Department, USC
2017 – 2018 Member of the PhD Admission Committee, CS Department, USC
2016 – 2017 Member of the Faculty Search Committee (Programming Languages), CS Department, USC
2016 – 2017 Member of the PhD Admission Committee, CS Department, USC
2015 – 2016 Member of the Curriculum Committee, ECE Department, Virginia Tech
2015 – 2016 Member of the Graduate Committee, ECE Department, Virginia Tech
2015 – 2016 Graduate Admission Officer (Computer Engineering), ECE Department, Virginia Tech
2015 – 2016 Member of the Faculty Search Committee (Mobile Systems), ECE Department, Virginia Tech
2014 – 2015 Co-organizer of the annual CESCA Day Symposium, ECE Department, Virginia Tech
2013 – 2015 Graduate Admission: Area Recruitment Representative, ECE Department, Virginia Tech
2013 – 2015 Member of the Faculty Advisory Committee, ECE Department, Virginia Tech
2013 – 2014 Organizer of the weekly CESCA Seminar series, ECE Department, Virginia Tech
2012 – 2015 Member of the Social Committee, ECE Department, Virginia Tech
2011 – 2012 Organizer of the weekly CESCA Seminar series, ECE Department, Virginia Tech

School/University Service

2018 – present Member of the Viterbi School of Engineering Research Committee, USC
2017 – 2018 Member of the Viterbi School of Engineering Academic Integrity Committee, USC
2017 – 2018 Member of the Viterbi School of Engineering IT Advisory Council (ViTAC), USC
2013 – 2014 Member of the Faculty Search Committee (Software Engineering), CS Department, Virginia Tech
2012 – 2013 Member of the Faculty Search Committee (Computer Systems), CS Department, Virginia Tech

External Service – Journal Editor

2018 – present IEEE Transactions on Software Engineering, Editorial Board (Associate Editor)

External Service – Conference Chair or Organizer

2020 International Conference on Computer Aided Verification (CAV) PC co-chair

2018 International Symposium on Automated Technology for Verification and Analysis (ATVA) PC co-chair

2017 International Symposium on Software Testing and Analysis (ISSTA) workshop co-chair

2016 International Workshop on Exploiting Concurrency Efficiently and Correctly (EC2) PC co-chair

2015 International Workshop on Design and Implementation of Formal Tools and Systems, co-chair

2015 International Conference on Formal Methods in Computer Aided Design (FMCAD) tutorial chair

2011 The Thirteenth International Workshop on Verification of Infinite-State Systems, co-chair

2009 The Fifth Northeastern Verification Seminar (organizer)

2008 The First International Workshop on Numerical Abstraction for Software Verification (co-chair)

2008 ICCAD Full Day Tutorial on Embedded Software Verification (co-organizer)

External Service – Conference Program Committee

2020 ACM International Conference on Software Engineering (ICSE)

2019 ACM Joint European Software Engineering Conference and Symposium of the Foundations of Software Engineering (ESEC/FSE)

2019 International Conference on Computer Aided Verification (CAV)

2019 ACM International Conference on Software Engineering (ICSE) - Program Board

2018 ACM Joint European Software Engineering Conference and Symposium of the Foundations of Software Engineering (ESEC/FSE) – Industry Track

2018 International Symposium on Software Testing and Analysis (ISSTA) - Industry Track

2018 International Workshop on Software Debloating and Delayering (SALAD)

2018 Workshop on Testing, Analysis, and Verification of Cyber-Physical Systems and Internet of Things

2018 International Symp. Dependable Software Engineering: Theories, Tools, and Applications (SETTA)

2018 International Conference on Runtime Verification (RV)

2017 ACM International Conference on Software Engineering (ICSE)

2017 International Symposium on Software Testing and Analysis (ISSTA)

2017 International Symp. Dependable Software Engineering: Theories, Tools, and Applications (SETTA)

2017 International Conference on Runtime Verification (RV)

2017 International Conference on Formal Methods in Computer Aided Design (FMCAD)

2017 International Symposium on Automated Technology for Verification and Analysis (ATVA)

2017 ACM SIGDA Ph.D. Forum at the ACM/IEEE Design Automation Conference (DAC)

2017 International Workshop on Security Proofs for Embedded Systems (PROOFS)

2016 International Symposium on Theoretical Aspects of Software Engineering (TASE)

2016 International Symposium on Automated Technology for Verification and Analysis (ATVA)

2016 ACM SIGDA Ph.D. Forum at the ACM/IEEE Design Automation Conference (DAC)

2016 International Symp. Dependable Software Engineering: Theories, Tools, and Applications (SETTA)

2016 International Workshop on Causal Reasoning for Embedded and Safety-critical Systems (CREST)

2016 International Workshop on Specification, Comprehension, Testing and Debugging of Concurrent Programs
2016 ACM International Conference on Software Engineering (ICSE)
2016 India Software Engineering Conference (ISEC)
2015 ACM SIGDA Ph.D. Forum at the ACM/IEEE Design Automation Conference (DAC)
2015 International Workshop on Security Proofs for Embedded Systems (PROOFS)
2015 International Conference on Engineering of Complex Computer Systems (ICECCS)
2014 ACM SIGSOFT International Symposium on the Foundations of Software Engineering (FSE)
2014 International Symposium on Automated Technology for Verification and Analysis (ATVA)
2014 The 19th International Symposium on Formal Methods (FM)
2014 International Symposium on Software Testing and Analysis (ISSTA) Tool Demo
2014 ACM/SIGDA Ph.D. Forum at the ACM/IEEE Design Automation Conference (DAC)
2014 International Workshop on Design and Implementation of Formal Tools and Systems (DIFTS)
2014 International Workshop on Exploiting Concurrency Efficiently and Correctly (EC2)
2013 IEEE International Conference on Computer Design (ICCD)
2013 ACM SIGDA Ph.D. Forum at the ACM/IEEE Design Automation Conference (DAC)
2013 International Workshop on Design and Implementation of Formal Tools and Systems (DIFTS)
2013 International Conference on Engineering of Complex Computer Systems (ICECCS)
2012 ACM SIGSOFT International Symposium on the Foundations of Software Engineering (FSE)
2012 ACM SIGPLAN Object-Oriented Programming, Systems, Languages, and Applications (OOPSLA)
2012 ACM SIGDA Ph.D. Forum at the ACM/IEEE Design Automation Conference (DAC)
2012 IEEE International Conference on Computer Design (ICCD)
2011 International Symposium on Automated Technology for Verification and Analysis (ATVA)
2011 International Workshop on Design and Implementation of Formal Tools and Systems (DIFTS)
2011 ACM SIGDA Ph.D. Forum at the ACM/IEEE Design Automation Conference (DAC)
2011 ACM/IEEE International Conference on Computer Aided Design (ICCAD)
2011 IEEE International Conference on Computer Design (ICCD)
2010 ACM SIGDA Ph.D. Forum at the ACM/IEEE Design Automation Conference (DAC)
2010 IEEE International Conference on Computer Design (ICCD)
2009 ACM SIGDA Ph.D. Forum at the ACM/IEEE Design Automation Conference (DAC)
2009 International Workshop on System Software Verification
2009 IEEE International Conference on Computer Design (ICCD)
2008 ACM SIGDA Ph.D. Forum at the ACM/IEEE Design Automation Conference (DAC)
2007 ACM Symposium on Applied Computing, the Software Verification Track
2007 ACM SIGDA Ph.D. Forum at the ACM/IEEE Design Automation Conference (DAC)
2007 Workshop on Constraints in Formal Verification
2006 Workshop on Constraints in Formal Verification
2005 International Workshop on Software Verification and Validation

External Service – Grant Review

NSF (National Science Foundation) Panelist	2019, 2018, 2017, 2016, 2015, 2013, 2012, 2009, 2008, 2007
DOE (Department of Energy) ASCR Panelist	2015
NSERC Discovery Grant (Canada) Reviewer	2015

External Service – Reviewer for Journal/Conference

Journals (recent):

ACM Trans. Software Engineering and Methodology, 2017

Proceedings of IEEE, 2017

IEEE Trans. Embedded Computing Systems, 2017

J. Formal Methods in Systems Design, 2017

IEEE Trans. Embedded Computing Systems, 2016

IEEE Trans. Software Engineering, 2015

IEEE Trans. Software Engineering, 2014

IEEE Trans. VLSI Systems, 2014

IEEE Trans. Computer Aided Design of Integrated Circuits and Systems (T-CAD), 2013

IEEE Trans. Computer (TC), 2013

IEEE Trans. Computer (TC), 2012

J. Formal Methods in Systems Design, 2012

Embedded Systems Letters, 2012

Journals (before 2011):

IEEE Trans. Computer, IEEE Trans. Computer Aided Design of Integrated Circuits and Systems (T-CAD), ACM Trans. Design Automation of Electronic Systems (TODAES), J. Formal Methods in Systems Design (FMSD), J. Satisfiability, Boolean Modeling and Computation (JSAT), J. Computer Science and Technology (JCST), The Computer Journal (CJ), J. Universal Computer Science (JUCS), IEE Proceedings on Computers and Digital Techniques, J. Computer and Operational Research (JCOR)

Conferences (recent):

IEEE International Symposium on Hardware Oriented Security and Trust (HOST), 2017

IEEE Real-Time Systems Symposium, 2015

Intl. Workshop on RFID Security, 2015

USENIX Security Symposium, 2014

Intl. Conf. Formal Methods in Computer Aided Design, 2013

ACM/IEEE Design Automation Conference, 2012

ACM SIGSOFT Symp. Foundations of Software Engineering, 2011

Intl. Test Conference, 2011

Conferences (before 2011):

Intl. Conf. Computer Aided Verification (CAV), Intl. Conf. Runtime Verification (RV), ACM/IEEE Design Automation Conference (DAC), Intl. Conf. Formal Methods in Computer Aided Design (FMCAD), High Level Design Validation and Test (HLDVT), Intl. Conf. System-on-a-Chip Design (ISOCC), Intl. Sym. Quality Electronic

Design (ISQED), IEEE Sym. Circuits and Systems (ISCAS), Design, Automation and Test in Europe (DATE), Asia-Pacific Design Automation Conference (ASP-DAC), International Test Conference (ITC)

(The End)