






# BTOR2 , BtorMC and Boolector 3.0

Aina Niemetz<sup>1,2</sup> , Mathias Preiner<sup>1,2</sup> ,  
Clifford Wolf<sup>3</sup>, and Armin Biere<sup>1</sup> 

<sup>1</sup> Johannes Kepler University Linz, Linz, Austria

<sup>2</sup> Stanford University, Stanford, USA

[niemetz@cs.stanford.edu](mailto:niemetz@cs.stanford.edu)

<sup>3</sup> Symbiotic EDA, Vienna, Austria



**Abstract.** We describe BTOR2, a word-level model checking format for capturing models of hardware and potentially software in a bit-precise manner. This simple, line-based and easy to parse format can be seen as a sorted extension of the word-level format BTOR. It uses design principles from the bit-level format AIGER and follows semantics of the SMT-LIB logics of bit-vectors with arrays. This intermediate format can be used in various verification flows and is perfectly suited to establish a word-level model checking competition. It is supported by our new open source model checker BtorMC, which is built on top of version 3.0 of our SMT solver Boolector. We further provide new word-level benchmarks on which these open source tools are evaluated.

Our format BTOR2 generalizes and extends the BTOR [5] format, which can be seen as a word-level generalization of the initial version of the bit-level format AIGER [2]. BTOR is a format for quantifier-free formulas over bit-vectors and arrays with SMT-LIB [1] semantics but also provides sequential extensions for specifying word-level model checking problems with registers and memories. In contrast to BTOR, which is tailored towards bit-vectors and one-dimensional bit-vector arrays, BTOR2 has explicit sort declarations. It further allows to explicitly initialize registers and memories (instead of implicit initialization in BTOR) and extends the set of sequential features with witnesses, invariant and fairness constraints, and liveness properties. All of these are word-level variants lifted from corresponding features in the latest AIGER format [4], the input format of the hardware model checking competition (HWMCC) [3, 6] since 2011. We provide an open source BTOR2 tool suite, which includes a generic parser, random simulator and witness checker. We further implemented a reference bounded model checker BtorMC on top of our SMT solver Boolector. We consider BTOR2 as an ideal candidate to establish a word-level hardware model checking competition.

## 1 Format Description

The syntax of BTOR2 is shown in Fig. 1. The `sort` keyword is used to define arbitrary bit-vector and array sorts. This not only allows to specify multi-dimensional

---

Supported by Austrian Science Fund (FWF) under NFN Grant S11408-N23 (RiSE).

© The Author(s) 2018

H. Chockler and G. Weissenbacher (Eds.): CAV 2018, LNCS 10981, pp. 587–595, 2018.

[https://doi.org/10.1007/978-3-319-96145-3\\_32](https://doi.org/10.1007/978-3-319-96145-3_32)

$\langle \text{num} \rangle$	::=	positive unsigned integer (greater than zero)
$\langle \text{uint} \rangle$	::=	unsigned integer (including zero)
$\langle \text{string} \rangle$	::=	sequence of whitespace and printable characters without '\n'
$\langle \text{symbol} \rangle$	::=	sequence of printable characters without '\n'
$\langle \text{comment} \rangle$	::=	';' $\langle \text{string} \rangle$
$\langle \text{nid} \rangle$	::=	$\langle \text{num} \rangle$
$\langle \text{sid} \rangle$	::=	$\langle \text{num} \rangle$
$\langle \text{const} \rangle$	::=	'const' $\langle \text{sid} \rangle$ [0-1]+
$\langle \text{constd} \rangle$	::=	'constd' $\langle \text{sid} \rangle$ ['-'](uint)
$\langle \text{consth} \rangle$	::=	'consth' $\langle \text{sid} \rangle$ [0-9a-fA-F]+
$\langle \text{input} \rangle$	::=	('input'   'one'   'ones'   'zero') $\langle \text{sid} \rangle$   $\langle \text{const} \rangle$   $\langle \text{constd} \rangle$   $\langle \text{consth} \rangle$
$\langle \text{state} \rangle$	::=	'state' $\langle \text{sid} \rangle$
$\langle \text{bitvec} \rangle$	::=	'bitvec' $\langle \text{num} \rangle$
$\langle \text{array} \rangle$	::=	'array' $\langle \text{sid} \rangle$ $\langle \text{sid} \rangle$
$\langle \text{node} \rangle$	::=	$\langle \text{sid} \rangle$ 'sort' ( $\langle \text{array} \rangle$   $\langle \text{bitvec} \rangle$ )   $\langle \text{nid} \rangle$ ( $\langle \text{input} \rangle$   $\langle \text{state} \rangle$ )   $\langle \text{nid} \rangle$ $\langle \text{opidx} \rangle$ $\langle \text{sid} \rangle$ $\langle \text{nid} \rangle$ $\langle \text{uint} \rangle$ [ $\langle \text{uint} \rangle$ ]   $\langle \text{nid} \rangle$ $\langle \text{op} \rangle$ $\langle \text{sid} \rangle$ $\langle \text{nid} \rangle$ [ $\langle \text{nid} \rangle$ [ $\langle \text{nid} \rangle$ ]]   $\langle \text{nid} \rangle$ ('init'   'next') $\langle \text{sid} \rangle$ $\langle \text{nid} \rangle$ $\langle \text{nid} \rangle$   $\langle \text{nid} \rangle$ ('bad'   'constraint'   'fair'   'output') $\langle \text{nid} \rangle$   $\langle \text{nid} \rangle$ 'justice' $\langle \text{num} \rangle$ ( $\langle \text{nid} \rangle$ )+
$\langle \text{line} \rangle$	::=	$\langle \text{comment} \rangle$   $\langle \text{node} \rangle$ [ $\langle \text{symbol} \rangle$ ] [ $\langle \text{comment} \rangle$ ]
$\langle \text{btor} \rangle$	::=	( $\langle \text{line} \rangle$ '\n' )+

**Fig. 1.** Syntax of BTOR2. Non-terminals  $\langle \text{opidx} \rangle$  and  $\langle \text{op} \rangle$  are indexed and non-indexed operators as defined in Table 1 (sequential part in red). (Color figure online)

arrays but can be extended to support (uninterpreted) functions, floating points and other sorts. As a consequence, BTOR2 is not backwards compatible with BTOR. For clarity, in Fig. 1 we distinguish between node (line) identifiers  $\langle \text{nid} \rangle$  and sort identifiers  $\langle \text{sid} \rangle$ , and do not allow an identifier to occur in both sets. Introducing sorts renders type specific keywords such as `var`, `array` and `acond` from BTOR obsolete. Instead, BTOR2 uses the keyword `input` to declare bit-vector and array variables of a given sort. Bit-vector constants are created as in BTOR with the keywords `const[dh]`, `one`, `ones` and `zero`.

Bit-vector and array operators as supported by BTOR2 and their respective sorts are shown in Table 1. We use  $\mathcal{B}^n$  for a bit-vector sort of width  $n$ , and  $\mathcal{I}$  and  $\mathcal{E}$  for the index and element sorts of an array sort  $\mathcal{A}^{\mathcal{I} \rightarrow \mathcal{E}}$ . Note that some bit-vector operators can be interpreted as *signed* or *unsigned*. In signed context, as in SMT-LIB, bit-vectors are represented in two's complement.

## 2 Sequential Extension

As shown in Fig. 1, the sequential extension of BTOR2 introduces a `state` keyword, which allows to specify registers and memories. In contrast to BTOR, where registers are implicitly zero-initialized and memories are uninitialized, BTOR2 provides a keyword `init` to explicitly define initialization functions for states. This enables us to also model partial initialization. For example, initializing a memory with a bit-vector constant zero, zero-initializes the whole memory, whereas

**Table 1.** Operators supported by BTOR2, where  $\mathcal{B}^n$  represents a bit-vector sort of size  $n$  and  $\mathcal{A}^{\mathcal{I} \rightarrow \mathcal{E}}$  represents an array sort with index sort  $\mathcal{I}$  and element sort  $\mathcal{E}$ .

<b>indexed</b>		
[su]ext $w$	(un)signed extension	$\mathcal{B}^n \rightarrow \mathcal{B}^{n+w}$
slice $u \ l$	extraction, $n > u \geq l$	$\mathcal{B}^n \rightarrow \mathcal{B}^{u-l+1}$
<b>unary</b>		
not	bit-wise	$\mathcal{B}^n \rightarrow \mathcal{B}^n$
inc, dec, neg	arithmetic	$\mathcal{B}^n \rightarrow \mathcal{B}^n$
redand, redor, redxor	reduction	$\mathcal{B}^n \rightarrow \mathcal{B}^1$
<b>binary</b>		
iff, implies	Boolean	$\mathcal{B}^1 \times \mathcal{B}^1 \rightarrow \mathcal{B}^1$
eq, neq	(dis)equality	$\mathcal{S} \times \mathcal{S} \rightarrow \mathcal{B}^1$
[su]gt, [su]gte, [su]lt, [su]lte	(un)signed inequality	$\mathcal{B}^n \times \mathcal{B}^n \rightarrow \mathcal{B}^1$
and, nand, nor, or, xnor, xor	bit-wise	$\mathcal{B}^n \times \mathcal{B}^n \rightarrow \mathcal{B}^n$
rol, ror, sll, sra, srl	rotate, shift	$\mathcal{B}^n \times \mathcal{B}^n \rightarrow \mathcal{B}^n$
add, mul, [su]div, smod, [su]rem, sub	arithmetic	$\mathcal{B}^n \times \mathcal{B}^n \rightarrow \mathcal{B}^n$
[su]addo, [su]divo, [su]mulo, [su]subo	overflow	$\mathcal{B}^n \times \mathcal{B}^n \rightarrow \mathcal{B}^1$
concat	concatenation	$\mathcal{B}^n \times \mathcal{B}^m \rightarrow \mathcal{B}^{n+m}$
read	array read	$\mathcal{A}^{\mathcal{I} \rightarrow \mathcal{E}} \times \mathcal{I} \rightarrow \mathcal{E}$
<b>ternary</b>		
ite	conditional	$\mathcal{B}^1 \times \mathcal{B}^n \times \mathcal{B}^n \rightarrow \mathcal{B}^n$
write	array write	$\mathcal{A}^{\mathcal{I} \rightarrow \mathcal{E}} \times \mathcal{I} \times \mathcal{E} \rightarrow \mathcal{A}^{\mathcal{I} \rightarrow \mathcal{E}}$

partially initializing a register can be achieved by applying a bit-mask to an uninitialized register.

Transition functions for both registers and memories are defined with the `next` keyword. It takes the current and next states as arguments. A state variable without associated next function is treated as a *primary* input, i.e., it has the same behaviour as inputs defined via keyword `input`. Note that BTOR provides a `next` keyword for registers and an `anext` keyword for memories. Using sorts in BTOR2 avoids such sort specific keyword variants.

As in the latest version of AIGER [4], BTOR2 supports *bad* state properties, which are essentially negations of safety properties. Multiple properties can be specified by simply adding multiple *bad* state properties. Invariant constraints can be introduced via the `constraint` keyword and are assumed to hold globally. A witness for a bad state property is an initialized finite path, which reaches (actually, contains) a bad state and satisfies all invariant constraints.

Again as in AIGER [4], keywords `fair` and `justice` allow to specify (global) fairness constraints and (negations of) liveness properties. Each *justice* property consists of a set of Büchi conditions. A witness for a justice property is an infinite initialized path on which all Büchi conditions and all global fairness constraints

are satisfied infinitely often. In addition, all global invariant constraints have to hold. The **justice** keyword takes a number (the number of Büchi conditions) and an arbitrary number of nodes (the Büchi conditions) as arguments.

### 3 Witness Format

The syntax of the BTOR2 witness format is shown in Fig. 2. A BTOR2 witness consists of a sequence of valid input assignments grouped by (time) frames. It starts with 'sat' followed by a list of properties that are satisfied by the witness. A property is identified by a prefix 'b' (for bad) and 'j' (for justice) followed by a number  $i$ , which ranges over the number of defined *bad* and *justice* properties starting from 0. For example, 'b0 j0' refers to the first bad and first justice property in the order as they occur in the BTOR2 input. The list of properties is followed by a sequence of  $k + 1$  frames at time  $t \in \{0, \dots, k\}$ . A *frame* is divided into a state and input part. The *state* part starts with '#t' and is mandatory for the first frame ( $t = 0$ ) and optional for later frames ( $t > 0$ ). It contains state assignments at time  $t$ . The *input* part starts with '@t' and consists of input assignments of the transition from time  $t$  to  $t + 1$ . If states are uninitialized (no init), their initial assignment is required to be specified in frame '#0'. The state part is usually omitted for  $t > 0$  since state assignments can be computed from states and inputs at time  $t - 1$ . While don't care inputs can be omitted, our witness checker assumes that they are zero. Input and state assignments use the same numbering scheme as properties, i.e., states and inputs are numbered separately in the order they are defined, starting from 0. For example, 0 in frame '#t' (or '@t') refers to the first state (or input) as defined in the BTOR2 input. For justice properties we assume the witness to be lasso shaped, i.e., the next state, which can be computed from the last state and inputs at time  $k$ , is identical to one of the previous states at time  $t = 0 \dots k$ . As in AIGER, a BTOR2 witness is terminated with '.' on a separate line.

<u>&lt;binary-string&gt;</u>	::=	[0-1]+
<u>&lt;bv-assignment&gt;</u>	::=	<binary-string>
<u>&lt;array-assignment&gt;</u>	::=	'[' <binary-string> ']' <binary-string>
<u>&lt;assignment&gt;</u>	::=	<uint> ( <bv-assignment>   <array-assignment> ) [ <symbol> ]
<u>&lt;model&gt;</u>	::=	( <comment> '\n'   <assignment> '\n' ) +
<u>&lt;state part&gt;</u>	::=	'#' <uint> '\n' <model>
<u>&lt;input part&gt;</u>	::=	'@' <uint> '\n' <model>
<u>&lt;frame&gt;</u>	::=	[ <state part> ] <input part>
<u>&lt;prop&gt;</u>	::=	( 'b'   'j' ) <uint>
<u>&lt;header&gt;</u>	::=	'sat' \n' ( <prop> ) + '\n'
<u>&lt;witness&gt;</u>	::=	( <comment> '\n' ) +   ( <header> ) ( <frame> ) + '.'

**Fig. 2.** BTOR2 model and witness format syntax (sequential part in red). (Color figure online)

Figure 3 illustrates a simple C program (left), the corresponding BTOR2 model with the negation of the assertion as a **bad** property (center), and a

```

#include <assert.h>
#include <stdio.h>
#include <stdlib.h>
#include <stdbool.h>
static bool read_bool () {
    int ch = getc (stdin);
    if (ch == '0') return false;
    if (ch == '1') return true;
    exit (0);
}
int main () {
    bool turn;           // input
    unsigned a = 0, b = 0; // states
    for (;;) {
        turn = read_bool ();
        assert (!(a == 3 && b == 3));
        if (turn) a = a + 1;
        else      b = b + 1;
    }
}

```

1	sort bitvec 1	sat
2	sort bitvec 32	b0
3	input 1 turn	#0
4	state 2 a	@0
5	state 2 b	0 1 turn@0
6	zero 2	@1
7	init 2 4 6	0 0 turn@1
8	init 2 5 6	@2
9	one 2	0 0 turn@2
10	add 2 4 9	@3
11	add 2 5 9	0 0 turn@3
12	ite 2 3 4 10	@4
13	ite 2 -3 5 11	0 1 turn@4
14	next 2 4 12	@5
15	next 2 5 13	0 1 turn@5
16	constd 2 3	@6
17	eq 1 4 16	0 0 turn@6
18	eq 1 5 16	
19	and 1 17 18	
20	bad 19	

**Fig. 3.** Example C program with corresponding BTOR2 model and witness.

BTOR2 witness for the violated property (right). The BTOR2 model defines one bad property ( $a == 3 \ \&\& \ b == 3$ ), which is satisfied in frame 6. The corresponding witness identifies this property as bad property ‘b0’ (first bad property defined in the model). All states are initialized, hence ‘#0’ is empty, and ‘@0’ to ‘@6’ indicate the assignments of input 0 (**turn**, the first input defined in the model) in frames 0 to 6, e.g., **turn** = 1 at  $t = 0$ , **turn** = 0 at  $t = 1$  and so on. In frame 6, both states **a** and **b** reach value 3, and therefore property ‘b0’ is satisfied.

## 4 Tools

We provide a generic stand-alone parser for BTOR2, which features basic type checking and consists of approx. 1,500 lines of C code. We implemented a reference bounded model checker BtorMC, which currently supports checking safety (aka. bad state) properties for models with registers and memories and produces witnesses for satisfiable properties. Unrolling the model is performed by symbolic simulation, i.e., symbolic substitution of current state expressions into next state functions, and incremental SMT solving. We also implemented a simulator for randomly simulating BTOR2 models. It further supports checking BTOR2 witnesses. The model checker is tightly integrated into our SMT solver Boolector [18], an award-winning SMT solver for the theory of fixed-size bit-vectors with arrays and uninterpreted functions. Since the last major version [18], we extended Boolector with several new features. Most notably, Boolector 3.0 now comes with support for quantified bit-vectors [24] and two different local search strategies for quantifier-free bit-vector formulas that don’t rely on but can be combined with bit-blasting [19, 21, 22]. It further provides support for BTOR2. In contrast to previous versions of Boolector, Boolector 3.0 and all BTOR2 tools

are released under the MIT open source license and the source code is hosted on GitHub<sup>1</sup>.

## 5 Experiments

We collected ten real-world (System)Verilog designs with safety properties from various open source projects [11, 26–28]. The majority of these designs include memories. We used the open synthesis suite Yosys [29] to synthesize these designs into BTOR2 and SMT-LIB. For BTOR2, Yosys directly generates the models from a circuit description. For SMT-LIB, since the language does not support describing model checking problems, we used Yosys in combination with Yosys-SMTBMC to produce unrolled (incremental) problems.

We compared BtorMC against the most recent versions of Boolector (3.0) and Yices [10] (2.5.4), the two best solvers of the QF\_ABV division of the SMT competition 2017. The BTOR2 models serve as input for BtorMC, and the incremental SMT-LIB benchmarks serve as input for Boolector and Yices. All benchmarks, synthesis scripts, generated files, log files and the source code of our tools for this evaluation are available at <http://fmv.jku.at/cav18-btor2>.

The results in Table 2 show that our flow using BTOR2 as intermediate format is competitive with simple unrolling. Note that our model checker BtorMC issues incremental calls to Boolector. However, in Boolector, sophisticated word-level rewriting is currently disabled in incremental mode. We expect a major performance boost by fully supporting incremental word-level preprocessing.

**Table 2.** BtorMC/BTOR2 vs. unrolled SMT-LIB with a time limit of 3600 s, where  $k$  is the bound and #bad is the number of bad properties.

Benchmark	$k$	#bad	BtorMC time[s]	Boolector time[s]	Yices time[s]
picorv32-check	30	23	<b>4.8</b>	18.9	10.8
picorv32-pregs	20	3	<b>63.0</b>	293.0	TO
ponylink-slaveTXlen-sat	230	1	305.5	406.8	<b>145.6</b>
ponylink-slaveTXlen-unsat	231	1	183.8	131.4	<b>71.4</b>
VexRiscv-regch0-15	17	2	<b>9.6</b>	48.3	12.2
VexRiscv-regch0-20	22	2	528.8	<b>520.7</b>	2232.2
VexRiscv-regch0-30	32	2	TO	TO	TO
zipcpu-busdelay	100	50	<b>157.0</b>	287.0	181.2
zipcpu-pfcache	100	39	<b>17.4</b>	19.9	32.5
zipcpu-zipmmu	30	57	86.0	412.9	<b>46.5</b>

<sup>1</sup> <https://github.com/boolector>.

## 6 Conclusion

We propose BTOR2, a new word-level model-checking and witness format. For this format we provide a generic parser implementation, a simulator that also checks witnesses, and a reference bounded model checker BtorMC, which is tightly integrated with our SMT solver Boolector. These open source tools are evaluated on new real-world benchmarks, which we synthesized from open source hardware (System) Verilog models into BTOR2 and SMT-LIB with Yosys. The tool Verilog2SMV [14] translates Verilog into model-checking problems in several formats, including nuXmv [7] and BTOR. However, its translation to BTOR is incomplete and development discontinued.

We plan to provide a translator from BTOR2 into SALLY [25], and VMT [8], which are both extensions of SMT-LIB to model symbolic transition systems. It might also be interesting to translate incremental SMT-LIB benchmarks and horn clause models (as handled by, e.g.,  $\mu Z$  [13]) into BTOR2 and vice versa. We hope other compilers and model checkers such as SAL [9], EBMC [15] and ABC [12, 16] will provide support to produce and read BTOR2 models. We want to extend the format to other logics, in particular to support lambdas as in [23]. There is also a need for fuzzing [20] and delta-debugging tools [17].

Last but not least, we want to use this format to bootstrap a word-level model checking competition, which of course needs more benchmarks.

## References

1. Barrett, C., Fontaine, P., Tinelli, C.: The SMT-LIB Standard: Version 2.6. Technical report, Department of Computer Science, The University of Iowa (2017). [www.SMT-LIB.org](http://www.SMT-LIB.org)
2. Biere, A.: The AIGER And-Inverter Graph (AIG) format version 20071012. Technical report, FMV Reports Series, Institute for Formal Models and Verification, Johannes Kepler University, Altenbergerstr 69, 4040 Linz, Austria (2007)
3. Biere, A., van Dijk, T., Heljanko, K.: Hardware model checking competition 2017. In: Stewart, D., Weissenbacher, G. (eds.) 2017 Formal Methods in Computer Aided Design, FMCAD 2017, Vienna, Austria, 2–6 October 2017, p. 9. IEEE (2017). <https://doi.org/10.23919/FMCAD.2017.8102233>
4. Biere, A., Heljanko, K., Wieringa, S.: AIGER 1.9 and beyond. Technical report, FMV Reports Series, Institute for Formal Models and Verification, Johannes Kepler University, Altenbergerstr 69, 4040 Linz, Austria (2011)
5. Brummayer, R., Biere, A., Lonsing, F.: BTOR: bit-precise modelling of word-level problems for model checking. In: Proceedings of the Joint Workshops of the 6th International Workshop on Satisfiability Modulo Theories and 1st International Workshop on Bit-Precise Reasoning, SMT 2008/BPR 2008, pp. 33–38. ACM, New York, USA (2008). <http://doi.acm.org/10.1145/1512464.1512472>
6. Cabodi, G., Loiacono, C., Palena, M., Pasini, P., Patti, D., Quer, S., Vendraminetto, D., Biere, A., Heljanko, K.: Hardware model checking competition 2014: an analysis and comparison of solvers and benchmarks. *J. Satisf. Boolean Model. Comput.* **9**, 135–172 (2014). Published 2016

7. Cavada, R., et al.: The nuXMV symbolic model checker. In: Biere, A., Bloem, R. (eds.) CAV 2014. LNCS, vol. 8559, pp. 334–342. Springer, Cham (2014). [https://doi.org/10.1007/978-3-319-08867-9\\_22](https://doi.org/10.1007/978-3-319-08867-9_22)
8. Cimatti, A., Roveri, M., Griggio, A., Irfan, A.: Verification modulo theories. <http://es.fbk.eu/projects/vmt-lib/>
9. De Moura, L., Owre, S., Shankar, N.: The SAL language manual. Technical report CSL-01-01, Computer Science Laboratory, SRI International, Menlo Park (2003)
10. Dutertre, B.: Yices 2.2. In: Biere, A., Bloem, R. (eds.) CAV 2014. LNCS, vol. 8559, pp. 737–744. Springer, Cham (2014). [https://doi.org/10.1007/978-3-319-08867-9\\_49](https://doi.org/10.1007/978-3-319-08867-9_49)
11. Gisselquist, D.: ZipCPU. <https://github.com/ZipCPU/zipcpu>
12. Ho, Y., Mishchenko, A., Brayton, R.K.: Property directed reachability with word-level abstraction. In: FMCAD, pp. 132–139. IEEE (2017)
13. Hoder, K., Bjørner, N., de Moura, L.:  $\mu Z$  - an efficient engine for fixed points with constraints. In: Gopalakrishnan, G., Qadeer, S. (eds.) CAV 2011. LNCS, vol. 6806, pp. 457–462. Springer, Heidelberg (2011). [https://doi.org/10.1007/978-3-642-22110-1\\_36](https://doi.org/10.1007/978-3-642-22110-1_36)
14. Irfan, A., Cimatti, A., Griggio, A., Roveri, M., Sebastiani, R.: Verilog2SMV: a tool for word-level verification. In: DATE, pp. 1156–1159. IEEE (2016)
15. Kroening, D.: Computing over-approximations with bounded model checking. *Electr. Notes Theor. Comput. Sci.* **144**(1), 79–92 (2006)
16. Long, J., Ray, S., Sterin, B., Mishchenko, A., Brayton, R.K.: Enhancing ABC for stabilization verification of systemverilog/VHDL models. In: Proceedings of the CEUR Workshop DIFTS@FMCAD, vol. 832. [CEUR-WS.org](http://CEUR-WS.org) (2011)
17. Niemetz, A., Biere, A.: ddSMT: a delta debugger for the SMT-LIB v2 format. In: Bruttomesso, R., Griggio, A. (eds.) Proceedings of the 11th International Workshop on Satisfiability Modulo Theories, SMT 2013, Affiliated with the 16th International Conference on Theory and Applications of Satisfiability Testing, SAT 2013, Helsinki, Finland, 8–9 July 2013, pp. 36–45 (2013)
18. Niemetz, A., Preiner, M., Biere, A.: Boolector 2.0. *JSAT* **9**, 53–58 (2015)
19. Niemetz, A., Preiner, M., Biere, A.: Precise and complete propagation based local search for satisfiability modulo theories. In: Chaudhuri, S., Farzan, A. (eds.) CAV 2016. LNCS, vol. 9779, pp. 199–217. Springer, Cham (2016). [https://doi.org/10.1007/978-3-319-41528-4\\_11](https://doi.org/10.1007/978-3-319-41528-4_11)
20. Niemetz, A., Preiner, M., Biere, A.: Model-based API testing for SMT solvers. In: Brain, M., Hadarean, L. (eds.) Proceedings of the 15th International Workshop on Satisfiability Modulo Theories, SMT 2017, Affiliated with the 29th International Conference on Computer Aided Verification, CAV 2017, Heidelberg, Germany, 24–28 July 2017, p. 10 (2017)
21. Niemetz, A., Preiner, M., Biere, A.: Propagation based local search for bit-precise reasoning. *Formal Methods Syst. Des.* **51**(3), 608–636 (2017). <https://doi.org/10.1007/s10703-017-0295-6>
22. Niemetz, A., Preiner, M., Biere, A., Fröhlich, A.: Improving local search for bit-vector logics in SMT with path propagation. In: Proceedings of the Fourth International Workshop on Design and Implementation of Formal Tools and Systems, Austin, USA, 26–27 September 2015, pp. 1–10 (2015)
23. Preiner, M., Niemetz, A., Biere, A.: Lemmas on demand for lambdas. In: Proceedings of the CEUR Workshop DIFTS@FMCAD, vol. 1130. [CEUR-WS.org](http://CEUR-WS.org) (2013)
24. Preiner, M., Niemetz, A., Biere, A.: Counterexample-guided model synthesis. In: Legay, A., Margaria, T. (eds.) TACAS 2017. LNCS, vol. 10205, pp. 264–280. Springer, Heidelberg (2017). [https://doi.org/10.1007/978-3-662-54577-5\\_15](https://doi.org/10.1007/978-3-662-54577-5_15)



25. SRI International's Computer Science Laboratory: Sally - a model checker for infinite-state systems. <https://github.com/SRI-CSL/sally>
26. Wolf, C.: PicoRV32. <https://github.com/cliffordwolf/picorv32>
27. Wolf, C.: PonyLink. <https://github.com/cliffordwolf/PonyLink>
28. Wolf, C.: riscv-formal. <https://github.com/cliffordwolf/riscv-formal>
29. Wolf, C.: Yosys. <https://github.com/YosysHQ/yosys>

**Open Access** This chapter is licensed under the terms of the Creative Commons Attribution 4.0 International License (<http://creativecommons.org/licenses/by/4.0/>), which permits use, sharing, adaptation, distribution and reproduction in any medium or format, as long as you give appropriate credit to the original author(s) and the source, provide a link to the Creative Commons license and indicate if changes were made.

The images or other third party material in this chapter are included in the chapter's Creative Commons license, unless indicated otherwise in a credit line to the material. If material is not included in the chapter's Creative Commons license and your intended use is not permitted by statutory regulation or exceeds the permitted use, you will need to obtain permission directly from the copyright holder.

