Intel® Open Source HD Graphics and Intel Iris™ Plus Graphics

Programmer's Reference Manual

For the 2016 - 2017 Intel Core™ Processors, Celeron™ Processors, and Pentium™ Processors based on the "Kaby Lake" Platform

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Part 2 – Registers M through Z

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Main Graphic Arbiter Error Report

ERROR - Main Graphic Arbiter Error Report

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	040A0h

This register is used to report different error conditions. Error bits are writable.

DWord	Bit	Description
0	31	**Reserved Error Bits 31** Default Value: 0b Access: R/W Future Use.
	30	**Reserved Error Bits 30** Default Value: 0b Access: R/W Future Use.
	29	**Reserved Error Bits 29** Default Value: 0b Access: R/W Future Use.
	28	**Reserved Error Bits 28** Default Value: 0b Access: R/W Future Use.
	27	**Reserved Error Bits 27** Default Value: 0b Access: R/W Future Use.
	26	**Reserved Error Bits 26** Default Value: 0b Access: R/W Future Use.

ERROR - Main Graphic Arbiter Error Report

	25	**Reserved Error Bits 25** Default Value: 0b Access: R/W Future Use.
	24	**Reserved Error Bits 24** Default Value: 0b Access: R/W Future Use.
	23	**Reserved Error Bits 23** Default Value: 0b Access: R/W Future Use.
	22	**Reserved Error Bits 22** Default Value: 0b Access: R/W Future Use.
	21	**Reserved Error Bits 21** Default Value: 0b Access: R/W Future Use.
	20	**Reserved Error Bits 20** Default Value: 0b Access: R/W Future Use.
	19	**Reserved Error Bits 19** Default Value: 0b Access: R/W Future Use.
	18	**Reserved Error Bits 18** Default Value: 0b

ERROR - Main Graphic Arbiter Error Report

	Access:	R/W
	Future Use.	
17	**Reserved Error Bits 17**	
	Default Value:	0b
	Access:	R/W
	Future Use.	
16	**Reserved Error Bits 16**	
	Default Value:	0b
	Access:	R/W
	Future Use.	
15	**Reserved Error Bits 15**	
	Default Value:	0b
	Access:	R/W
	ctx_fault_ctxt_not_prsmt_err - The Present (P) field in the context-entry used to process the DMA request is Clear.	
14	**Reserved Error Bits 14**	
	Default Value:	0b
	Access:	R/W
	ctx_fault_root_not_prsmt_err - The present (UP/LP) field in the root-entry used to process the untranslated request with PASID is 0.	
13	**Reserved Error Bits 13**	
	Default Value:	0b
	Access:	R/W
	ctx_fault_pasid_not_prsnt_err - PASID Table entry to be used does not have the PRESENT flag set. This means the PASID entry is not valid.	
12	**Reserved Error Bits 12**	
	Default Value:	0b
	Access:	R/W
	ctx_fault_pasid_ovflw_err - PASID Table size in extended context entry defines the number of PASIDs that will be supported. If hardware receives a PASID number outside the supported boundary, report as an error.	
11	**Reserved Error Bits 11**	

ERROR - Main Graphic Arbiter Error Report

	Default Value:	0b
	Access:	R/W
	ctx_fault_pasid_dis_err - Submission of advanced context where the PASID field is not enabled in the extended context entry.	
10	**Reserved Error Bits 10**	
	Default Value:	0b
	Access:	R/W
	rstrm_fault_nowb_atomic_err - All page table accesses in advanced context with A/D bits are considered as atomic operations in WB space. However if the memory type for the page table accesses come out as anything but WB, that is an error.	
9	**Reserved**	
8	**Unloaded PD Error**	
	Default Value:	0b
	Access:	R/W
	The Cache Line containing a PD entry being accessed, was marked as invalid in the last PD load cycle.	
7	**Reserved Error Bits 7**	
	Default Value:	0b
	Access:	R/W
	Future Use.	
6	**Reserved**	
5	**Reserved**	
4	**Reserved**	
3	**Reserved**	
2	**Invalid Page Directory Entry Error**	
	Default Value:	0b
	Access:	R/W
	PD entry's valid bit is 0.	
1	**Reserved**	
0	**TLB Page Fault Error**	
	Default Value:	0b
	Access:	R/W
	A TLB Page's GTT translation generated a page fault (GTT entry not valid).	

Main Graphic Arbiter Error Report 2

<table>
<tr><th colspan="3">ERROR_2 - Main Graphic Arbiter Error Report 2</th></tr>
<tr><td colspan="3">Register Space: MMIO: 0/2/0
Default Value: 0x00000000
Size (in bits): 32</td></tr>
<tr><td colspan="3">Address: 040A4h</td></tr>
<tr><th>DWord</th><th>Bit</th><th>Description</th></tr>
<tr><td>0</td><td>31:0</td><td>Main Graphic Arbiter Error Report 2
<table><tr><td>Default Value:</td><td>00000000h</td></tr><tr><td>Access:</td><td>RO</td></tr></table>Bit [31:6] - Reserved.
Bit [5:0] - tlbpend_reg_faultcnt[5:0].</td></tr>
</table>

Main Graphic Arbiter Error Report 3

ERROR_3 - Main Graphic Arbiter Error Report 3

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000 [KBL]
Size (in bits):	32
Address:	040A8h

This register is used to report different error conditions. Error bits are writable.

DWord	Bit	Description
0	31:16	**Reserved** Default Value: 0000h Access: RO
	15	**Error3 Bits 15** Default Value: 0b Access: R/W Future Use.
	14	**Error3 Error Bits 14** Default Value: 0b Access: R/W Future Use.
	13	**Error3 Error Bits 13** Default Value: 0b Access: R/W Future Use.
	12	**Error3 Error Bits 12** Default Value: 0b Access: R/W Future Use.
	11	**Error3 Error Bits 11** Default Value: 0b Access: R/W invalid_varmtrr_overlap_memtype_rd.
	10	**Error3 Error Bits 10**

ERROR_3 - Main Graphic Arbiter Error Report 3

		Default Value: 0b Access: R/W invalid_varmtrr_overlap_memtype_wr.
	9	**Error3 Error Bits 9** Default Value: 0b Access: R/W invalid_default_memtype_value_rd.
	8	**Error3 Error Bits 8** Default Value: 0b Access: R/W invalid_default_memtype_value_wr.
	7	**Error3 Error Bits 7** Default Value: 0b Access: R/W invalid_varmtrr_memtype_value_rd.
	6	**Error3 Error Bits 6** Default Value: 0b Access: R/W invalid_varmtrr_memtype_value_wr.
	5	**Error3 Error Bits 5** Default Value: 0b Access: R/W invalid_fixedmtrr_memtype_value_rd.
	4	**Error3 Error Bits 4** Default Value: 0b Access: R/W invalid_fixedmtrr_memtype_value_wr.
	3	**Error3 Error Bits 3** Default Value: 0b Access: R/W gttc_internal_error.

ERROR_3 - Main Graphic Arbiter Error Report 3

	2	**Error3 Error Bits 2** Default Value: 0b Access: R/W
	1	**Error3 Error Bits 1** Default Value: 0b Access: R/W tlbpend_internal_error.
	0	**Error3 Error Bits 0** Default Value: 0b Access: R/W reg_wrid_internal_error.

MASTER_INT_CTL

MASTER_INT_CTL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W, RO
Size (in bits):	32
Address:	44200h-44203h
Name:	Master Interrupt Control
ShortName:	MASTER_INT_CTL
Power:	PG0
Reset:	soft

This register has the master enable for graphics interrupts and gives an overview of what interrupts are pending.
An interrupt pending bit will read 1b while one or more interrupts of that category are set (IIR) and enabled (IER).
All Pending Interrupts are ORed together to generate the combined interrupt.
The combined interrupt is ANDed with the Master Interrupt enable to create the master enabled interrupt.
The master enabled interrupt goes to PCI device 2 interrupt processing.
The master interrupt enable must be set before any of these interrupts will propagate to PCI device 2 interrupt processing.

DWord	Bit	Description
0	31	**Master Interrupt Enable** Access: R/W This is the master control for graphics interrupts. This must be enabled for any of these interrupts to propagate to PCI device 2 interrupt processing. Value / Name: 0b – Master interrupt disable 1b – Master interrupt enable
	30	**PCU Interrupts Pending** Access: RO This field indicates if interrupts of this category are pending.
	29:25	**Reserved**
	24	**Audio Codec Interrupts Pending** Access: RO This field indicates if interrupts of this category are pending.
	23	**DE PCH Interrupts Pending**

MASTER_INT_CTL

		Access: RO This field indicates if interrupts of this category are pending. The PCH Display interrupt is configured through the SDE interrupt registers.
	22	**DE Misc Interrupts Pending** Access: RO This field indicates if interrupts of this category are pending.
	21	**Reserved**
	20	**DE Port Interrupts Pending** Access: RO This field indicates if interrupts of this category are pending.
	19	**Reserved**
	18	**DE Pipe C Interrupts Pending** Access: RO This field indicates if interrupts of this category are pending.
	17	**DE Pipe B Interrupts Pending** Access: RO This field indicates if interrupts of this category are pending.
	16	**DE Pipe A Interrupts Pending** Access: RO This field indicates if interrupts of this category are pending.
	15:8	**Reserved**
	7	**Reserved**
	6	**VEBox Interrupts Pending** Access: RO This field indicates if interrupts of this category are pending.
	5	**Reserved**
	4	**GTPM Interrupts Pending** Access: RO This field indicates if interrupts of this category are pending.
	3	**VCS2 Interrupts Pending** Access: RO

MASTER_INT_CTL

		This field indicates if interrupts of this category are pending.
	2	**VCS1 Interrupts Pending** Access: RO This field indicates if interrupts of this category are pending.
	1	**Blitter Interrupts Pending** Access: RO This field indicates if interrupts of this category are pending.
	0	**Render Interrupts Pending** Access: RO This field indicates if interrupts of this category are pending.

Master Latency Timer

MLT2_0_2_0_PCI - Master Latency Timer		
Register Space:	PCI: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	8	
Address:	0000Dh	
The IGD does not support the programmability of the master latency timer because it does not perform bursts.		
DWord	**Bit**	**Description**
0	7:0	**Master Latency Timer Count Value** Default Value: 00000000b Access: RO Hardwired to 0s.

Master start timer

MASTIMER - Master start timer		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000001	
Size (in bits):	32	
Address:	0B438h	
DWord	**Bit**	**Description**
0	31:0	**Master start timer value** Default Value: 00000000000000000000000000000001b Access: R/W Master Start Timer (MSTSTTMR). lpconf_lpfc_master_start_timer [31:0]. So many clocks are expired before starting the rest of the counters. Time to wait is 256 * value clocks. Value for this register cannot be 0.

Maximum Latency

MAXLAT_0_2_0_PCI - Maximum Latency		
Register Space:	PCI: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	8	
Address:	0003Fh	
The Integrated Graphics Device has no requirement for the settings of Latency Timers.		
DWord	**Bit**	**Description**
0	7:0	**Maximum Latency Value** Default Value: 00000000b Access: RO Hardwired to 0s because the IGD has no specific requirements for how often it needs to access the PCI bus.

Max Outstanding Pending TLB Requests 0

GFX_PEND_TLB_0 - Max Outstanding Pending TLB Requests 0

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	04034h

DWord	Bit	Description
0	31	**TEX Limit Enable Bit** Default Value: 0b Access: R/W This bit is used to enable the pending TLB requests limitation function for the Texture Cache. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.
	30	**Reserved** Default Value: 0b Access: RO
	29:24	**TEX TLB Limit Count** Default Value: 000000b Access: R/W This is the MAX number of Allowed internal pending read requests which require a TLB read.
	23	**DC Limit Enable Bit** Default Value: 0b Access: R/W This bit is used to enable the pending TLB requests limitation function for the Instruction Cache. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.
	22	**Reserved** Default Value: 0b Access: RO
	21:16	**DC TLB Limit Count** Default Value: 000000b Access: R/W This is the MAX number of Allowed internal pending read requests which require a TLB read.

GFX_PEND_TLB_0 - Max Outstanding Pending TLB Requests 0

15	**VF Limit Enable Bit** Default Value: 0b Access: R/W This bit is used to enable the pending TLB requests limitation function for the Vertex Fetch. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.
14	**Reserved** Default Value: 0b Access: RO
13:8	**VF TLB Limit Count** Default Value: 000000b Access: R/W This is the MAX number of Allowed internal pending read requests which require a TLB read.
7	**VMC Limit Enable bit** Default Value: 0b Access: R/W This bit is used to enable the pending TLB requests limitation function for the Video Motion Compensation. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.
6	**Reserved** Default Value: 0b Access: RO
5:0	**VMC TLB Limit Count** Default Value: 000000b Access: R/W This is the MAX number of Allowed internal pending read requests which require a TLB read.

Max Outstanding Pending TLB Requests 1

GFX_PEND_TLB_1 - Max Outstanding Pending TLB Requests 1

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	04038h

DWord	Bit	Description
0	31	**SOL Limit Enable Bit** Default Value: 0b Access: R/W This bit is used to enable the pending TLB requests limitation function for the SOL. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.
	30	**Reserved** Default Value: 0b Access: RO
	29:24	**SOL TLB Limit Count** Default Value: 000000b Access: R/W This is the MAX number of Allowed internal pending read requests which require a TLB read.
	23	**L3 Limit Enable Bit** Default Value: 0b Access: R/W This bit is used to enable the pending TLB requests limitation function for the L3. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.
	22	**Reserved** Default Value: 0b Access: RO
	21:16	**L3 TLB Limit Count** Default Value: 000000b Access: R/W This is the MAX number of Allowed internal pending read requests which require a TLB read.

GFX_PEND_TLB_1 - Max Outstanding Pending TLB Requests 1

	15	**RCZ Limit Enable Bit** Default Value: 0b Access: R/W This bit is used to enable the pending TLB requests limitation function for the Render Depth Cache. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.
	14	**Reserved** Default Value: 0b Access: RO
	13:8	**RCZ TLB Limit Count** Default Value: 000000b Access: R/W RCZ TLB Limit Count Project: All Format: U6 This is the MAX number of Allowed internal pending read requests which require a TLB read.
	7	**RCC Limit Enable bit** Default Value: 0b Access: R/W This bit is used to enable the pending TLB requests limitation function for the Render Color Cache. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.
	6	**Reserved** Default Value: 0b Access: RO
	5:0	**RCC TLB Limit Count** Default Value: 000000b Access: R/W This is the MAX number of Allowed internal pending read requests which require a TLB read.

Max Outstanding Pending TLB Requests 2

GFX_PEND_TLB_2 - Max Outstanding Pending TLB Requests 2

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	04048h

DWord	Bit	Description
0	31:24	**Reserved** Default Value: 00000000b Access: R/W
	23	**Reserved**
	22	**Reserved** Default Value: 0b Access: R/W
	21:16	**Reserved**
	15	**BLT Limit Enable Bit** Default Value: 0b Access: R/W This bit is used to enable the pending TLB requests limitation function for the Blitter engine. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.
	14	**Reserved** Default Value: 0b Access: R/W
	13:8	**BLT TLB Limit Count** Default Value: 000000b Access: R/W BLT TLB Limit Count Project: All Format: U6 This is the MAX number of Allowed internal pending read requests which require a TLB read.
	7	**Reserved**
	6	**Reserved** Default Value: 0b Access: R/W
	5:0	**Reserved**

Max Outstanding Pending TLB Requests 3

GFX_PEND_TLB_3 - Max Outstanding Pending TLB Requests 3

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0403Ch

DWord	Bit	Description
0	31	**VEBX Limit Enable Bit** Default Value: 0b Access: R/W This bit is used to enable the pending TLB requests limitation function for the VEBX engine. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.
	30	**Reserved** Default Value: 0b Access: R/W
	29:24	**VEBX TLB Limit Count** Default Value: 000000b Access: R/W This is the MAX number of Allowed internal pending read requests which require a TLB read.
	23	**MFX1 Limit Enable Bit** Default Value: 0b Access: R/W This bit is used to enable the pending TLB requests limitation function for the Media1 engine. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.
	22	**Reserved** Default Value: 0b Access: R/W
	21:16	**MFX1 TLB Limit Count** Default Value: 000000b Access: R/W This is the MAX number of Allowed internal pending read requests which require a TLB read.

GFX_PEND_TLB_3 - Max Outstanding Pending TLB Requests 3

	15	**MFX0 Limit Enable Bit** Default Value: 0b Access: R/W This bit is used to enable the pending TLB requests limitation function for the Media0 engine. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.
	14	**Reserved** Default Value: 0b Access: R/W
	13:8	**MFX0 TLB Limit Count** Default Value: 000000b Access: R/W MFX0 TLB Limit Count Project: All Format: U6 This is the MAX number of Allowed internal pending read requests which require a TLB read.
	7	**GFX Limit Enable bit** Default Value: 0b Access: R/W This bit is used to enable the pending TLB requests limitation function for the Render engine. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.
	6	**Reserved** Default Value: 0b Access: R/W
	5:0	**GFX TLB Limit Count** Default Value: 000000b Access: R/W This is the MAX number of Allowed internal pending read requests which require a TLB read.

MAX Requests Allowed - GAM

GFX_MAX_REQ_COUNT - MAX Requests Allowed - GAM

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x43F20101
Size (in bits):	32
Address:	04AA4h

Programmable Request Count - GAM

DWord	Bit	Description
0	31:26	**GAP Writes Max Request Limit Count** Default Value: 010000b Access: R/W This is the MAX number of Allowed Write Requests Count - These counters keep track of the accepted write requests from all GAP clients (RCZ, HiZ, Stc, RCC, L3). Minimum count value must be = 1.
	25:20	**CVS Max Request Limit Count** Default Value: 111111b Access: R/W This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each client. Requests are counted, regardless of kind of cycle (Miss/Hit/Present). Minimum count value must be = 1.
	19	**Reserved** Default Value: 0b Access: RO
	18:13	**L3 Max Request Limit Count** Default Value: 010000b Access: R/W This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each client. Requests are counted, regardless of kind of cycle (Miss/Hit/Present). Minimum count value must be = 1.
	12	**Reserved** Default Value: 0b Access: RO
	11:6	**Z Request Limit Count**

GFX_MAX_REQ_COUNT - MAX Requests Allowed - GAM

		Default Value: 000100b Access: R/W This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each client. Requests are counted, regardless of kind of cycle (Miss/Hit/Present). Minimum count value must be = 1.
	5:0	**RCC Request Limit Count** Default Value: 000001b Access: R/W This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each client. Requests are counted, regardless of kind of cycle (Miss/Hit/Present). Minimum count value must be = 1.

MAX Requests Allowed - MFX

MEDIA_MAX_REQ_COUNT - MAX Requests Allowed - MFX

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x10201020
Size (in bits):	32
Address:	04AA0h

Programmable Request Count - MFX

DWord	Bit	Description
0	31:24	**GFX Max Request Limit Count** Default Value: 00010000b Access: R/W This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (Miss/Hit/Present). Minimum count value must be = 1.
	23:16	**MFX Max Request Limit Count** Default Value: 00100000b Access: R/W This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (Miss/Hit/Present). Minimum count value must be = 1.
	15:14	**Reserved** Default Value: 00b Access: RO
	13:8	**VLF Max Request Limit Count** Default Value: 010000b Access: R/W This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each client. Requests are counted, regardless of kind of cycle (Miss/Hit/Present). Minimum count value must be = 1.
	7:6	**Reserved** Default Value: 00b Access: RO
	5:0	**MFX Max Request Limit Count**

MEDIA_MAX_REQ_COUNT - MAX Requests Allowed - MFX

		Default Value: 100000b Access: R/W This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each client. Requests are counted, regardless of kind of cycle (Miss/Hit/Present). Minimum count value must be = 1.

MAX Requests Allowed - VEBX and BLT

VEBX_BLIT_MAX_REQ_COUNT - MAX Requests Allowed - VEBX and BLT

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x08080020
Size (in bits):	32
Address:	04AA8h

Programmable Request Count - VEBX and BLT

DWord	Bit	Description
0	31:24	**BLT Max Request Limit Count** Default Value: 00001000b Access: R/W This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (Miss/Hit/Present).
	23:16	**VEBX Max Request Limit Count** Default Value: 00001000b Access: R/W This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (Miss/Hit/Present).
	15:8	**Reserved** Default Value: 00000000b Access: RO
	7:0	**MFX1 Max Request Limit Count** Default Value: 00100000b Access: R/W This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (Miss/Hit/Present).

MBC Control Register

MBCTL - MBC Control Register		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00020000	
Size (in bits):	32	
Address:	0907Ch	
MBC Control Register		
DWord	**Bit**	**Description**
0	31:18	**ECORSVD** Access: R/W ECO purposes Reserved
	17	**U2C Global PMON Enable Override** Default Value: 1b Access: R/W U2C Performance Monitor Global Enable Override 0 - U2C Global PMON needs to be enabled for performance monitors to be enabled (default) 1 - Overrride U2C Global PMON Enable is ignored ine baled performance monitor counters
	16	**VCR Fuse Writes as Posted** Access: R/W Non-posted fuse fetching is NOT supported starting. Only posted is allowed (the default). 0 - MBCunit sends VCR Fuse Writes as Non-posted. 1 - MBCunit sends VCR Fuse Writes as posted. Fuse writes to VCR will be default sent as non-posted cycle
	15:8	**RSVD** Access: RO
	7	**Disable Wait for SQemtpy in MAE** Access: R/W 0 - Wait for SQempty for MAE update Flow. 1 - MBC MAE update FSM does not wait for the SQempty to complete the FSM.
	6	**Reserved**
	5	**RSVD** Access: RO
	4	**MBC Driver Boot Enable** Access: R/W

MBCTL - MBC Control Register

		Config bit for driver managed boot kick off. 1 - Enable Boot Fetch without any PM interaction. 0 - Default (no action). This Bit is cleared by the Hardware once the Boot fetch is complete.
	3	**Context Fetch Needed** Access: R/W Context Fetch Needed for Power Exits. 0 - Context Fetch Not Needed. 1 - Context Fetch Needed for Power Exits (CPD Entry).
	2	**BME Update Enable** Access: R/W BME update Enable: 0 - Default BME Update is not Enabled. MBC ignores all the BME updates from SA. 1- BME update is Enabled.
	1	**MAE Update Enable** Access: R/W MAE update Enable: 0 - Default MAE Update is not Enabled. MBC ignores all the MAE updates from SA. 1 - MAE update is Enabled. MBC responds to the MAE updates.
	0	**RSVD** Access: RO

ME Data Registers Valid

ME_DATA_STATUS - ME Data Registers Valid		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	RO Variant	
Size (in bits):	32	
Address:	0C0F4h	
HW uses this register to reflect the status of the incoming writes into ME_DATA and ME_CTRL from the ME.		
DWord	**Bit**	**Description**
0	31	**Clear** A write to this bit clears the contents of the ME_DATA[0-7] registers and ME_CTRL register. It also resets the Data Valid bits below.
	30:9	**Reserved** Format: MBZ
	8:0	**Reserved**

Media0 MOCS Register0

MFX0_MOCS_0 - Media0 MOCS Register0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030 [KBL]
Size (in bits):	32
Address:	0C900h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_0 - Media0 MOCS Register0

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register1

MFX0_MOCS_1 - Media0 MOCS Register1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034 [KBL]
Size (in bits):	32
Address:	0C904h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_1 - Media0 MOCS Register1

6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register2

MFX0_MOCS_2 - Media0 MOCS Register2

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038 [KBL]
Size (in bits):	32
Address:	0C908h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_2 - Media0 MOCS Register2

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register3

MFX0_MOCS_3 - Media0 MOCS Register3

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031 [KBL]
Size (in bits):	32
Address:	0C90Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_3 - Media0 MOCS Register3

6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register4

MFX0_MOCS_4 - Media0 MOCS Register4

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032 [KBL]
Size (in bits):	32
Address:	0C910h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_4 - Media0 MOCS Register4

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register5

MFX0_MOCS_5 - Media0 MOCS Register5

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036 [KBL]
Size (in bits):	32
Address:	0C914h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_5 - Media0 MOCS Register5

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register6

MFX0_MOCS_6 - Media0 MOCS Register6

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A [KBL]
Size (in bits):	32
Address:	0C918h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_6 - Media0 MOCS Register6

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register7

MFX0_MOCS_7 - Media0 MOCS Register7

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033 [KBL]
Size (in bits):	32
Address:	0C91Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_7 - Media0 MOCS Register7

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register8

MFX0_MOCS_8 - Media0 MOCS Register8

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037 [KBL]
Size (in bits):	32
Address:	0C920h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_8 - Media0 MOCS Register8

6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register9

MFX0_MOCS_9 - Media0 MOCS Register9

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B [KBL]
Size (in bits):	32
Address:	0C924h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_9 - Media0 MOCS Register9

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register10

MFX0_MOCS_10 - Media0 MOCS Register10

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032 [KBL]
Size (in bits):	32
Address:	0C928h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_10 - Media0 MOCS Register10

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register11

MFX0_MOCS_11 - Media0 MOCS Register11

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036 [KBL]
Size (in bits):	32
Address:	0C92Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_11 - Media0 MOCS Register11

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register12

MFX0_MOCS_12 - Media0 MOCS Register12

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A [KBL]
Size (in bits):	32
Address:	0C930h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_12 - Media0 MOCS Register12

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register13

MFX0_MOCS_13 - Media0 MOCS Register13

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033 [KBL]
Size (in bits):	32
Address:	0C934h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_13 - Media0 MOCS Register13

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register14

MFX0_MOCS_14 - Media0 MOCS Register14

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037 [KBL]
Size (in bits):	32
Address:	0C938h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_14 - Media0 MOCS Register14

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register15

MFX0_MOCS_15 - Media0 MOCS Register15

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B [KBL]
Size (in bits):	32
Address:	0C93Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_15 - Media0 MOCS Register15

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register16

MFX0_MOCS_16 - Media0 MOCS Register16

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030 [KBL]
Size (in bits):	32
Address:	0C940h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_16 - Media0 MOCS Register16

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register17

MFX0_MOCS_17 - Media0 MOCS Register17

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034 [KBL]
Size (in bits):	32
Address:	0C944h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_17 - Media0 MOCS Register17

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register18

MFX0_MOCS_18 - Media0 MOCS Register18

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038 [KBL]
Size (in bits):	32
Address:	0C948h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_18 - Media0 MOCS Register18

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register19

MFX0_MOCS_19 - Media0 MOCS Register19

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031 [KBL]
Size (in bits):	32
Address:	0C94Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_19 - Media0 MOCS Register19

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register20

MFX0_MOCS_20 - Media0 MOCS Register20

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032 [KBL]
Size (in bits):	32
Address:	0C950h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_20 - Media0 MOCS Register20

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register21

MFX0_MOCS_21 - Media0 MOCS Register21

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036 [KBL]
Size (in bits):	32
Address:	0C954h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_21 - Media0 MOCS Register21

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register22

MFX0_MOCS_22 - Media0 MOCS Register22

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A [KBL]
Size (in bits):	32
Address:	0C958h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_22 - Media0 MOCS Register22

6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register23

MFX0_MOCS_23 - Media0 MOCS Register23

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033 [KBL]
Size (in bits):	32
Address:	0C95Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_23 - Media0 MOCS Register23

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register24

MFX0_MOCS_24 - Media0 MOCS Register24

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037 [KBL]
Size (in bits):	32
Address:	0C960h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_24 - Media0 MOCS Register24

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register25

MFX0_MOCS_25 - Media0 MOCS Register25

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B [KBL]
Size (in bits):	32
Address:	0C964h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_25 - Media0 MOCS Register25

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register26

MFX0_MOCS_26 - Media0 MOCS Register26

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032 [KBL]
Size (in bits):	32
Address:	0C968h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_26 - Media0 MOCS Register26

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register27

MFX0_MOCS_27 - Media0 MOCS Register27

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036 [KBL]
Size (in bits):	32
Address:	0C96Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_27 - Media0 MOCS Register27

6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register28

MFX0_MOCS_28 - Media0 MOCS Register28

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A [KBL]
Size (in bits):	32
Address:	0C970h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_28 - Media0 MOCS Register28

6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register29

MFX0_MOCS_29 - Media0 MOCS Register29

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033 [KBL]
Size (in bits):	32
Address:	0C974h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_29 - Media0 MOCS Register29

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register30

MFX0_MOCS_30 - Media0 MOCS Register30

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037 [KBL]
Size (in bits):	32
Address:	0C978h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_30 - Media0 MOCS Register30

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register31

MFX0_MOCS_31 - Media0 MOCS Register31

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B [KBL]
Size (in bits):	32
Address:	0C97Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_31 - Media0 MOCS Register31

6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register32

MFX0_MOCS_32 - Media0 MOCS Register32

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030 [KBL]
Size (in bits):	32
Address:	0C980h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_32 - Media0 MOCS Register32

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register33

MFX0_MOCS_33 - Media0 MOCS Register33

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034 [KBL]
Size (in bits):	32
Address:	0C984h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_33 - Media0 MOCS Register33

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register34

MFX0_MOCS_34 - Media0 MOCS Register34

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038 [KBL]
Size (in bits):	32
Address:	0C988h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_34 - Media0 MOCS Register34

6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register35

MFX0_MOCS_35 - Media0 MOCS Register35

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031 [KBL]
Size (in bits):	32
Address:	0C98Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_35 - Media0 MOCS Register35

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register36

MFX0_MOCS_36 - Media0 MOCS Register36

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032 [KBL]
Size (in bits):	32
Address:	0C990h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_36 - Media0 MOCS Register36

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register37

MFX0_MOCS_37 - Media0 MOCS Register37

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036 [KBL]
Size (in bits):	32
Address:	0C994h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_37 - Media0 MOCS Register37

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register38

MFX0_MOCS_38 - Media0 MOCS Register38

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A [KBL]
Size (in bits):	32
Address:	0C998h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_38 - Media0 MOCS Register38

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register39

MFX0_MOCS_39 - Media0 MOCS Register39

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033 [KBL]
Size (in bits):	32
Address:	0C99Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_39 - Media0 MOCS Register39

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register40

MFX0_MOCS_40 - Media0 MOCS Register40

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037 [KBL]
Size (in bits):	32
Address:	0C9A0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_40 - Media0 MOCS Register40

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register41

MFX0_MOCS_41 - Media0 MOCS Register41

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B [KBL]
Size (in bits):	32
Address:	0C9A4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_41 - Media0 MOCS Register41

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register42

MFX0_MOCS_42 - Media0 MOCS Register42

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032 [KBL]
Size (in bits):	32
Address:	0C9A8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_42 - Media0 MOCS Register42

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register43

MFX0_MOCS_43 - Media0 MOCS Register43

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036 [KBL]
Size (in bits):	32
Address:	0C9ACh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_43 - Media0 MOCS Register43

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register44

MFX0_MOCS_44 - Media0 MOCS Register44

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A [KBL]
Size (in bits):	32
Address:	0C9B0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_44 - Media0 MOCS Register44

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register45

MFX0_MOCS_45 - Media0 MOCS Register45

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033 [KBL]
Size (in bits):	32
Address:	0C9B4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_45 - Media0 MOCS Register45

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register46

MFX0_MOCS_46 - Media0 MOCS Register46

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037 [KBL]
Size (in bits):	32
Address:	0C9B8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_46 - Media0 MOCS Register46

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register47

MFX0_MOCS_47 - Media0 MOCS Register47

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B [KBL]
Size (in bits):	32
Address:	0C9BCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_47 - Media0 MOCS Register47

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register48

MFX0_MOCS_48 - Media0 MOCS Register48

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030 [KBL]
Size (in bits):	32
Address:	0C9C0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_48 - Media0 MOCS Register48

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register49

MFX0_MOCS_49 - Media0 MOCS Register49

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034 [KBL]
Size (in bits):	32
Address:	0C9C4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_49 - Media0 MOCS Register49

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register50

MFX0_MOCS_50 - Media0 MOCS Register50

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038 [KBL]
Size (in bits):	32
Address:	0C9C8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_50 - Media0 MOCS Register50

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register51

MFX0_MOCS_51 - Media0 MOCS Register51

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031 [KBL]
Size (in bits):	32
Address:	0C9CCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_51 - Media0 MOCS Register51

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register52

MFX0_MOCS_52 - Media0 MOCS Register52

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032 [KBL]
Size (in bits):	32
Address:	0C9D0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_52 - Media0 MOCS Register52

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register53

MFX0_MOCS_53 - Media0 MOCS Register53

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036 [KBL]
Size (in bits):	32
Address:	0C9D4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_53 - Media0 MOCS Register53

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register54

MFX0_MOCS_54 - Media0 MOCS Register54

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A [KBL]
Size (in bits):	32
Address:	0C9D8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_54 - Media0 MOCS Register54

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register55

MFX0_MOCS_55 - Media0 MOCS Register55

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033 [KBL]
Size (in bits):	32
Address:	0C9DCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_55 - Media0 MOCS Register55

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register56

MFX0_MOCS_56 - Media0 MOCS Register56

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037 [KBL]
Size (in bits):	32
Address:	0C9E0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_56 - Media0 MOCS Register56

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register57

MFX0_MOCS_57 - Media0 MOCS Register57

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B [KBL]
Size (in bits):	32
Address:	0C9E4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_57 - Media0 MOCS Register57

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register58

MFX0_MOCS_58 - Media0 MOCS Register58

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032 [KBL]
Size (in bits):	32
Address:	0C9E8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_58 - Media0 MOCS Register58

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register59

MFX0_MOCS_59 - Media0 MOCS Register59

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036 [KBL]
Size (in bits):	32
Address:	0C9ECh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_59 - Media0 MOCS Register59

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register60

MFX0_MOCS_60 - Media0 MOCS Register60

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A [KBL]
Size (in bits):	32
Address:	0C9F0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_60 - Media0 MOCS Register60

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register61

MFX0_MOCS_61 - Media0 MOCS Register61

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033 [KBL]
Size (in bits):	32
Address:	0C9F4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_61 - Media0 MOCS Register61

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register62

MFX0_MOCS_62 - Media0 MOCS Register62

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037 [KBL]
Size (in bits):	32
Address:	0C9F8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_62 - Media0 MOCS Register62

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media0 MOCS Register63

MFX0_MOCS_63 - Media0 MOCS Register63

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B [KBL]
Size (in bits):	32
Address:	0C9FCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX0_MOCS_63 - Media0 MOCS Register63

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register0

MFX1_MOCS_0 - Media1 MOCS Register0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030 [KBL]
Size (in bits):	32
Address:	0CA00h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_0 - Media1 MOCS Register0

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register1

MFX1_MOCS_1 - Media1 MOCS Register1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034 [KBL]
Size (in bits):	32
Address:	0CA04h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_1 - Media1 MOCS Register1

6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register2

MFX1_MOCS_2 - Media1 MOCS Register2

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038 [KBL]
Size (in bits):	32
Address:	0CA08h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_2 - Media1 MOCS Register2

6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register3

MFX1_MOCS_3 - Media1 MOCS Register3

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031 [KBL]
Size (in bits):	32
Address:	0CA0Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_3 - Media1 MOCS Register3

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register4

MFX1_MOCS_4 - Media1 MOCS Register4

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032 [KBL]
Size (in bits):	32
Address:	0CA10h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_4 - Media1 MOCS Register4

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register5

MFX1_MOCS_5 - Media1 MOCS Register5

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036 [KBL]
Size (in bits):	32
Address:	0CA14h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_5 - Media1 MOCS Register5

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register6

MFX1_MOCS_6 - Media1 MOCS Register6

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A [KBL]
Size (in bits):	32
Address:	0CA18h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_6 - Media1 MOCS Register6

6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register7

MFX1_MOCS_7 - Media1 MOCS Register7

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033 [KBL]
Size (in bits):	32
Address:	0CA1Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_7 - Media1 MOCS Register7

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register8

MFX1_MOCS_8 - Media1 MOCS Register8

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037 [KBL]
Size (in bits):	32
Address:	0CA20h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_8 - Media1 MOCS Register8

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register9

MFX1_MOCS_9 - Media1 MOCS Register9

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B [KBL]
Size (in bits):	32
Address:	0CA24h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_9 - Media1 MOCS Register9

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register10

MFX1_MOCS_10 - Media1 MOCS Register10

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032 [KBL]
Size (in bits):	32
Address:	0CA28h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_10 - Media1 MOCS Register10

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register11

MFX1_MOCS_11 - Media1 MOCS Register11

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036 [KBL]
Size (in bits):	32
Address:	0CA2Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_11 - Media1 MOCS Register11

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register12

MFX1_MOCS_12 - Media1 MOCS Register12

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A [KBL]
Size (in bits):	32
Address:	0CA30h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_12 - Media1 MOCS Register12

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register13

MFX1_MOCS_13 - Media1 MOCS Register13

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033 [KBL]
Size (in bits):	32
Address:	0CA34h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_13 - Media1 MOCS Register13

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register14

MFX1_MOCS_14 - Media1 MOCS Register14

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037 [KBL]
Size (in bits):	32
Address:	0CA38h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_14 - Media1 MOCS Register14

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register15

MFX1_MOCS_15 - Media1 MOCS Register15

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B [KBL]
Size (in bits):	32
Address:	0CA3Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_15 - Media1 MOCS Register15

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register16

MFX1_MOCS_16 - Media1 MOCS Register16

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030 [KBL]
Size (in bits):	32
Address:	0CA40h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_16 - Media1 MOCS Register16

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register17

MFX1_MOCS_17 - Media1 MOCS Register17

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034 [KBL]
Size (in bits):	32
Address:	0CA44h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_17 - Media1 MOCS Register17

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register18

MFX1_MOCS_18 - Media1 MOCS Register18

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038 [KBL]
Size (in bits):	32
Address:	0CA48h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_18 - Media1 MOCS Register18

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register19

MFX1_MOCS_19 - Media1 MOCS Register19

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031 [KBL]
Size (in bits):	32
Address:	0CA4Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_19 - Media1 MOCS Register19

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register20

MFX1_MOCS_20 - Media1 MOCS Register20

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032 [KBL]
Size (in bits):	32
Address:	0CA50h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_20 - Media1 MOCS Register20

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register21

MFX1_MOCS_21 - Media1 MOCS Register21

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036 [KBL]
Size (in bits):	32
Address:	0CA54h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_21 - Media1 MOCS Register21

6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register22

MFX1_MOCS_22 - Media1 MOCS Register22

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A [KBL]
Size (in bits):	32
Address:	0CA58h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_22 - Media1 MOCS Register22

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register23

MFX1_MOCS_23 - Media1 MOCS Register23

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033 [KBL]
Size (in bits):	32
Address:	0CA5Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_23 - Media1 MOCS Register23

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register24

MFX1_MOCS_24 - Media1 MOCS Register24

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037 [KBL]
Size (in bits):	32
Address:	0CA60h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_24 - Media1 MOCS Register24

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register25

MFX1_MOCS_25 - Media1 MOCS Register25

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B [KBL]
Size (in bits):	32
Address:	0CA64h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_25 - Media1 MOCS Register25

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register26

MFX1_MOCS_26 - Media1 MOCS Register26

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032 [KBL]
Size (in bits):	32
Address:	0CA68h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_26 - Media1 MOCS Register26

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register27

MFX1_MOCS_27 - Media1 MOCS Register27

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036 [KBL]
Size (in bits):	32
Address:	0CA6Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_27 - Media1 MOCS Register27

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register28

MFX1_MOCS_28 - Media1 MOCS Register28

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A [KBL]
Size (in bits):	32
Address:	0CA70h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_28 - Media1 MOCS Register28

6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register29

MFX1_MOCS_29 - Media1 MOCS Register29

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033 [KBL]
Size (in bits):	32
Address:	0CA74h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_29 - Media1 MOCS Register29

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register30

MFX1_MOCS_30 - Media1 MOCS Register30

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037 [KBL]
Size (in bits):	32
Address:	0CA78h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_30 - Media1 MOCS Register30

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register31

MFX1_MOCS_31 - Media1 MOCS Register31

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B [KBL]
Size (in bits):	32
Address:	0CA7Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_31 - Media1 MOCS Register31

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register32

MFX1_MOCS_32 - Media1 MOCS Register32

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030 [KBL]
Size (in bits):	32
Address:	0CA80h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_32 - Media1 MOCS Register32

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register33

MFX1_MOCS_33 - Media1 MOCS Register33

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034 [KBL]
Size (in bits):	32
Address:	0CA84h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_33 - Media1 MOCS Register33

6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register34

MFX1_MOCS_34 - Media1 MOCS Register34

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038 [KBL]
Size (in bits):	32
Address:	0CA88h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_34 - Media1 MOCS Register34

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register35

MFX1_MOCS_35 - Media1 MOCS Register35

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031 [KBL]
Size (in bits):	32
Address:	0CA8Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_35 - Media1 MOCS Register35

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register36

MFX1_MOCS_36 - Media1 MOCS Register36

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032 [KBL]
Size (in bits):	32
Address:	0CA90h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_36 - Media1 MOCS Register36

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register37

MFX1_MOCS_37 - Media1 MOCS Register37

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036 [KBL]
Size (in bits):	32
Address:	0CA94h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_37 - Media1 MOCS Register37

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register38

MFX1_MOCS_38 - Media1 MOCS Register38

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A [KBL]
Size (in bits):	32
Address:	0CA98h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_38 - Media1 MOCS Register38

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register39

MFX1_MOCS_39 - Media1 MOCS Register39

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033 [KBL]
Size (in bits):	32
Address:	0CA9Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_39 - Media1 MOCS Register39

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register40

MFX1_MOCS_40 - Media1 MOCS Register40

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037 [KBL]
Size (in bits):	32
Address:	0CAA0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_40 - Media1 MOCS Register40

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register41

MFX1_MOCS_41 - Media1 MOCS Register41

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B [KBL]
Size (in bits):	32
Address:	0CAA4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_41 - Media1 MOCS Register41

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register42

MFX1_MOCS_42 - Media1 MOCS Register42

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032 [KBL]
Size (in bits):	32
Address:	0CAA8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_42 - Media1 MOCS Register42

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register43

MFX1_MOCS_43 - Media1 MOCS Register43

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036 [KBL]
Size (in bits):	32
Address:	0CAACh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_43 - Media1 MOCS Register43

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register44

MFX1_MOCS_44 - Media1 MOCS Register44

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A [KBL]
Size (in bits):	32
Address:	0CAB0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_44 - Media1 MOCS Register44

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register45

MFX1_MOCS_45 - Media1 MOCS Register45

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033 [KBL]
Size (in bits):	32
Address:	0CAB4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_45 - Media1 MOCS Register45

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register46

MFX1_MOCS_46 - Media1 MOCS Register46

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037 [KBL]
Size (in bits):	32
Address:	0CAB8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_46 - Media1 MOCS Register46

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register47

MFX1_MOCS_47 - Media1 MOCS Register47

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B [KBL]
Size (in bits):	32
Address:	0CABCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_47 - Media1 MOCS Register47

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register48

MFX1_MOCS_48 - Media1 MOCS Register48

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030 [KBL]
Size (in bits):	32
Address:	0CAC0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_48 - Media1 MOCS Register48

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register49

MFX1_MOCS_49 - Media1 MOCS Register49

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034 [KBL]
Size (in bits):	32
Address:	0CAC4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_49 - Media1 MOCS Register49

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register50

MFX1_MOCS_50 - Media1 MOCS Register50

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038 [KBL]
Size (in bits):	32
Address:	0CAC8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_50 - Media1 MOCS Register50

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register51

MFX1_MOCS_51 - Media1 MOCS Register51

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031 [KBL]
Size (in bits):	32
Address:	0CACCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_51 - Media1 MOCS Register51

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register52

MFX1_MOCS_52 - Media1 MOCS Register52

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032 [KBL]
Size (in bits):	32
Address:	0CAD0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_52 - Media1 MOCS Register52

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register53

MFX1_MOCS_53 - Media1 MOCS Register53

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036 [KBL]
Size (in bits):	32
Address:	0CAD4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_53 - Media1 MOCS Register53

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register54

MFX1_MOCS_54 - Media1 MOCS Register54

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A [KBL]
Size (in bits):	32
Address:	0CAD8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_54 - Media1 MOCS Register54

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register55

MFX1_MOCS_55 - Media1 MOCS Register55

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033 [KBL]
Size (in bits):	32
Address:	0CADCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_55 - Media1 MOCS Register55

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register56

MFX1_MOCS_56 - Media1 MOCS Register56

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037 [KBL]
Size (in bits):	32
Address:	0CAE0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_56 - Media1 MOCS Register56

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register57

MFX1_MOCS_57 - Media1 MOCS Register57

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B [KBL]
Size (in bits):	32
Address:	0CAE4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_57 - Media1 MOCS Register57

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register58

MFX1_MOCS_58 - Media1 MOCS Register58

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032 [KBL]
Size (in bits):	32
Address:	0CAE8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_58 - Media1 MOCS Register58

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register59

MFX1_MOCS_59 - Media1 MOCS Register59

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036 [KBL]
Size (in bits):	32
Address:	0CAECh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_59 - Media1 MOCS Register59

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register60

MFX1_MOCS_60 - Media1 MOCS Register60

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A [KBL]
Size (in bits):	32
Address:	0CAF0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_60 - Media1 MOCS Register60

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register61

MFX1_MOCS_61 - Media1 MOCS Register61

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033 [KBL]
Size (in bits):	32
Address:	0CAF4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_61 - Media1 MOCS Register61

6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register62

MFX1_MOCS_62 - Media1 MOCS Register62

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037 [KBL]
Size (in bits):	32
Address:	0CAF8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_62 - Media1 MOCS Register62

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media1 MOCS Register63

MFX1_MOCS_63 - Media1 MOCS Register63

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B [KBL]
Size (in bits):	32
Address:	0CAFCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

MFX1_MOCS_63 - Media1 MOCS Register63

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

Media 1 PFET control register with lock

PFETCTL - Media 1 PFET control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0004001E [KBL]
Size (in bits):	32
Address:	24088h

DWord	Bit	Description
0	31	**PFET Control Lock** Access: R/W Lock 0 = Bits of MEDIA1 PGFETCTL register are R/W 1 = All bits of MEDIA1 PGFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (that is, writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:21	**Reserved** Access: RO Reserved
	20	**Power Well Status** Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (that is, writing a 0 will not clear the lock). These bits are not reset on FLR.
	19	**Powergood timer error** Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (that is, writing a 0 will not clear the lock). These bits are not reset on FLR.
	18:16	**Delay from enabling secondary PFETs to power good.** Access: R/W Lock Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns 3'b010: 160ns 3'b011: 320ns

PFETCTL - Media 1 PFET control register with lock

3'b100: 640ns
3'b101: 1280ns
3'b110: 2560ns
3'b111: 5120ns

Value	Name
100b	**[Default]**

15:13 **Time period last primay pfet strobe to secondary pfet strobe**

Access:	R/W Lock

Time period last primay pfet strobe to secondary pfet strobe
3'b000: 10ns (or 1 bclk)
3'b001: 20ns (or 2 bclk)
3'b010: 30ns (or 3 bclk)
3'b111: 80ns (or 8 bclk)

12:10 **Time period b/w two adjacent strobes**

Access:	R/W Lock

Time period b/w two adjacent strobes to the primary FETs
3'b000: 10ns (or 1 bclk)
3'b001: 20ns (or 2 bclk)
3'b010: 30ns (or 3 bclk)
3'b111: 80ns (or 8 bclk)

9:7 **FET setup margin from enable to strobe**

Access:	R/W Lock

Setup margin in design before sampling enable event at the first pre-charge sequencer/shift register flop
3'b000: 10ns (or 1 bclk)
3'b001: 20ns (or 2 bclk)
3'b010: 30ns (or 3 bclk)
3'b111: 80ns (or 8 bclk)

6:0 **Number of flops to enable primary FETs**

Access:	R/W Lock

Number of flops to enable primary FETs. For a setting of N there will be N+1 total strobes generated
7'b0000000: 10 Flops to be strobed
7'b0000001: 11 Flops to be strobed
7'b0000010: 12 Flops to be strobed
7'b0001111: 26 Flops to be strobed

Value	Name
0011110b	**[Default]**

Media 1 Power Context Save request

PGCTXREQ - Media 1 Power Context Save request

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	24084h

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO Message Mask bits for lower 16 bits
	15:10	**Reserved** Access: RO Reserved
	9	**Power context save request** Access: R/W Set Power Context Save Request 1'b0 : Power context save is not being requested 1'b1 : Power context save is being requested CPUnit self-clears this bit upon sampling.
	8:0	**Power Context Save request crdit count** Access: R/W QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

Media 1 Power Down FSM control register with lock

POWERDNFSMCTL - Media 1 Power Down FSM control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000088
Size (in bits):	32
Address:	24090h

DWord	Bit	Description
0	31	**power down control Lock** Access: R/W Lock 0 = Bits of MEDIA1 POWERDNFSMCTL register are R/W 1 = All bits of MEDIA1 POWERDNFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (that is, writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:13	**Reserved** Access: RO Reserved
	12	**Leave firewall disabled** Access: R/W Lock When this bit is set, SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM. Encodings: 0 = Default mode, that is, firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, that is,dont firewall the gated domain, but complete logical flow
	11	**Leave reset de-asserted** Access: R/W Lock When this bit is set, SPC will not assert reset for power off flow. But it will pretend to complete the flow with PM. Encodings: 0 = Default mode, that is, assert resets during power down flows 1 = Leave reset de-asserted mode, that is,dont assert reset, but complete logical flow
	10	**Leave CLKs ON** Access: R/W Lock

POWERDNFSMCTL - Media 1 Power Down FSM control register with lock

		When this bit is set, SPC will not gate clks for power off flow. But it will pretend to complete the flow with PM. Encodings: 0 = Default mode, that is, gate clocks during power down flows 1 = Leave CLKS ON mode, that is,dont clock gate, but complete logical flow
	9	**Leave FET On** Access: R/W Lock When this bit is set, SPC will not turn off the PFET even though it will complete the flow with PM. Encodings: 0 = Default mode, that is, power off fets during power down flows 1 = Leave ON mode, that is,dont power off pfet, but complete logical flow **Programming Notes** This bit should be programmed before the powerup sequence is initiated for the Media1.
	8:6	**Power Down state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Gate Clocks
	5:3	**Power Down state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default: Firewall ON
	2:0	**Power Down state 1** Default Value: 000b Access: R/W Lock This will be the 1st state before power is turned OFF in the well

POWERDNFSMCTL - Media 1 Power Down FSM control register with lock		
		Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default: Assert Reset

Media 1 Power Gate Control Request

PGCTLREQ - Media 1 Power Gate Control Request		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	24080h	
Clock Gating Messages Register		
DWord	**Bit**	**Description**
0	31:16	**Message Mask** Access: RO Message Mask To write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:2	**Reserved** Access: RO Reserved
	1	**CLK RST FWE Request** Access: R/W Media1 CLK RST FWE request: '0' : Initiate Power Down sequence (clk/rst/fwe) '1' : Initiate Power Up sequence (clk/rst/fwe)
	0	**Power Gate Request** Access: R/W Media1 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

Media 1 Power on FSM control register with lock

POWERUPFSMCTL - Media 1 Power on FSM control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000088
Size (in bits):	32
Address:	2408Ch

DWord	Bit	Description
0	31	**power up control Lock** Access: R/W Lock 0 = Bits of MEDIA1 POWERUPFSMCTL register are R/W 1 = All bits of MEDIA1 POWERUPFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (that is, writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:9	**Reserved** Access: RO Reserved
	8:6	**Power UP state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - De-assert resets 3'b000: 10ns (or 1 bclk)
	5:3	**Power UP state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF

POWERUPFSMCTL - Media 1 Power on FSM control register with lock

		010 = De-assert resets 1xx = Rsvd for future Default - Firewall OFF
	2:0	**Power UP state 1** Default Value: 000b Access: R/W Lock This will be the 1st state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Clock Ungate

Media 1 TLB Control Register

M1TCR - Media 1 TLB Control Register

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	04264h

DWord	Bit	Description
0	31:1	**Reserved** Default Value: 00000000000000000000000000000000b Access: RO
	0	**Invalidate TLBs on the corresponding Engine** Default Value: 0b Access: R/W SW writes 1 to invalidate the TLBs for the associated engine and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs. This bit is self clear.

Media 2 PFET control register with lock

PFETCTL - Media 2 PFET control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0004001E
Size (in bits):	32
Address:	24108h

DWord	Bit	Description
0	31	**PFET Control Lock** Access: R/W Lock 0 = Bits of MEDIA2 PFETCTL register are R/W 1 = All bits of MEDIA2 PFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:21	**Reserved** Access: RO Reserved
	20	**Power Well Status** Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	19	**Powergood timer error** Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	18:16	**Delay from enabling secondary PFETs to power good.** Default Value: 100b Access: R/W Lock Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns

PFETCTL - Media 2 PFET control register with lock

		3'b010: 160ns 3'b011: 320ns 3'b100: 640ns 3'b101: 1280ns 3'b110: 2560ns 3'b111: 5120ns
	15:13	**Time period last primay pfet strobe to secondary pfet strobe** Access: R/W Lock Time period last primay pfet strobe to secondary pfet strobe 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	12:10	**Time period b/w two adjacent strobes** Access: R/W Lock Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	9:7	**FET setup margin from enable to strobe** Access: R/W Lock Setup margin in design before sampling enable event at the first pre-charge sequencer/shift register flop 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	6:0	**Number of flops to enable primary FETs** Default Value: 0011110b Access: R/W Lock Number of flops to enable primary FETs. For a setting of N there will be N+1 total strobes generated 7'b0000000: 10 Flops to be strobed 7'b0000001: 11 Flops to be strobed 7'b0000010: 12 Flops to be strobed 7'b0001111: 26 Flops to be strobed

Media 2 Power Context Save request

PGCTXREQ - Media 2 Power Context Save request

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	24104h

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO Message Mask bots for lower 16 bits
	15:10	**Reserved** Access: RO Reserved
	9	**Power context save request** Access: R/W Set Power Context Save Request 1’b0 : Power context save is not being requested 1’b1 : Power context save is being requested CPUnit self-clears this bit upon sampling.
	8:0	**Power Context Save request crdit count** Access: R/W QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

Media 2 Power Down FSM control register with lock

POWERDNFSMCTL - Media 2 Power Down FSM control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000088
Size (in bits):	32
Address:	24110h

DWord	Bit	Description
0	31	**power down control Lock** Access: R/W Lock 0 = Bits of MEDIA2 POWERDNFSMCTL register are R/W 1 = All bits of MEDIA2 POWERDNFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:13	**Reserved** Access: RO Reserved
	12	**Leave firewall disabled** Access: R/W Lock When This bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, i.e dont firewall the gated domain, but complete logical flow
	11	**Leave reset de-asserted** Access: R/W Lock When This bit is set SPC will not assert reset for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e assert resets during power down flows 1 = Leave reset de-asserted mode, i.e dont assert reset, but complete logical flow
	10	**Leave CLKs ON** Access: R/W Lock

POWERDNFSMCTL - Media 2 Power Down FSM control register with lock

		When This bit is set SPC will not gate clks for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e gate clocks during power down flows 1 = Leave CLKS ON mode, i.e dont clock gate, but complete logical flow
	9	**Leave FET On** Access: R/W Lock When This bit is set SPC will not turn off the PFET eventhough it will complete the flow with PM Encodings: 0 = Default mode, i.e power off fets during power down flows 1 = Leave ON mode, i.e dont power off pfet, but complete logical flow Programming note : This bit should be programmed before the powerup sequence is initiated Media2
	8:6	**Power Down state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Gate Clocks
	5:3	**Power Down state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default :Firewall ON
	2:0	**Power Down state 1** Default Value: 000b Access: R/W Lock This will be the 1st state before power is turned OFF in the well

POWERDNFSMCTL - Media 2 Power Down FSM control register with lock		
		Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Assert Reset

Media 2 Power Gate Control Request

PGCTLREQ - Media 2 Power Gate Control Request		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	24100h	
Clock Gating Messages Register		
DWord	**Bit**	**Description**
0	31:16	**Message Mask** Access: RO Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:2	**Reserved** Access: RO Reserved
	1	**CLK RST FWE Request** Access: R/W Media2 CLK RST FWE request: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**Power Gate Request** Access: R/W Media2 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

Media 2Power on FSM control register with lock

POWERUPFSMCTL - Media 2Power on FSM control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000088
Size (in bits):	32
Address:	2410Ch

DWord	Bit	Description
0	31	**power up control Lock** Access: R/W Lock 0 = Bits of MEDIA2 POWERUPFSMCTL register are R/W 1 = All bits of MEDIA2 POWERUPFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:9	**Reserved** Access: RO Reserved
	8:6	**Power UP state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - De-assert resets 3'b000: 10ns (or 1 bclk)
	5:3	**Power UP state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF

POWERUPFSMCTL - Media 2Power on FSM control register with lock

		010 = De-assert resets 1xx = Rsvd for future Default - Firewall OFF
	2:0	**Power UP state 1** Default Value: 000b Access: R/W Lock This will be the 1st state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Clock Ungate

Media 2 TLB Control Register

M2TCR - Media 2 TLB Control Register

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	04268h

DWord	Bit	Description
0	31:1	**Reserved** Default Value: 00000000000000000000000000000000b Access: RO
	0	**Invalidate TLBs on the corresponding Engine** Default Value: 0b Access: R/W SW writes 1 to invalidate the TLBs for the associated engine and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs. This bit is self clear.

Media Control Surface Cache Invalidate

MCSCI - Media Control Surface Cache Invalidate

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04AACh

DWord	Bit	Description
0	31:16	**Bit Masks** Default Value: 0000h Access: R/W Mask Bits act as Write Enables for the bits[15:0] of this register
	15	**Disable H/W based RCP$/WCP$ cache invalidate** Default Value: 0b Access: R/W Disable H/W based end of context detection Bit[15] Disable H/W based RCP$/WCP$ cache invalidation 1'b1 : Disable the h/w based end of context detection to clear the contents of RCP$ and WCP$ 1'b0 : Does not disable the h/w based end of context detection
	14	**Reserved bits for future** Default Value: 0b Access: R/W
	13	**Reserved bits for future** Default Value: 0b Access: R/W
	12	**Reserved bits for future** Default Value: 0b Access: R/W
	11	**Reserved bits for future** Default Value: 0b Access: R/W
	10	**Reserved bits for future** Default Value: 0b Access: R/W

MCSCI - Media Control Surface Cache Invalidate

	9	**Reserved bits for future** Default Value: 0b Access: R/W
	8	**Reserved bits for future** Default Value: 0b Access: R/W
	7	**Reserved bits for future** Default Value: 0b Access: R/W
	6	**Reserved bits for future** Default Value: 0b Access: R/W
	5	**Reserved bits for future** Default Value: 0b Access: R/W
	4	**Reserved**
	3	**Invalidate Media#1 WCP$/RCP$ entries** Default Value: 0b Access: R/W Hardware Clear Invalidate Media#1 WCP$/RCP$ entries Bit[3] Clear Media#1 engine enqueued entries from WCP$/RCP$ 1'b0 : Enqueued entries from WCP$/RCP$ are not cleared; 1'b1 : Enqueued entries from WCP$/RCP$ are cleared This event is instantaneous This bit is write-to-clear
	2	**Invalidate Media#0 WCP$/RCP$ entries** Default Value: 0b Access: R/W Hardware Clear Invalidate Media#0 WCP$/RCP$ entries Bit[2] Clear Media#0 engine enqueued entries from WCP$/RCP$ 1'b0 : Enqueued entries from WCP$/RCP$ are not cleared; 1'b1 : Enqueued entries from WCP$/RCP$ are cleared This event is instantaneous This bit is write-to-clear

MCSCI - Media Control Surface Cache Invalidate

	1	**Invalidate VEBOX WCP$/RCP$ entries** Default Value: 0b Access: R/W Hardware Clear Invalidate VEBOX WCP$/RCP$ entries Bit[1] Clear VEBOX engine enqueued entries from WCP$/RCP$ 1'b0 : Enqueued entries from WCP$/RCP$ are not cleared; 1'b1 : Enqueued entries from WCP$/RCP$ are cleared This event is instantaneous This bit is write-to-clear
	0	**Invalidate Render(When used for Media) WCP$/RCP$ entries** Default Value: 0b Access: R/W Hardware Clear Invalidate Render WCP$/RCP$ entries Bit[0] Clear Render engine enqueued entries from WCP$/RCP$ 1'b0 : Enqueued entries from WCP$/RCP$ are not cleared; 1'b1 : Enqueued entries from WCP$/RCP$ are cleared This event is instantaneous This bit is write-to-clear

Message Address

MA_0_2_0_PCI - Message Address

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	000B0h

This register contains the Message Address for MSIs sent by the device.

DWord	Bit	Description
0	31:2	**Message Address** Default Value: 00000000000000000000000000000000b Access: R/W Used by system software to assign an MSI address to the device. The device handles an MSI by writing the padded contents of the MD register to this address.
	1:0	**Force Dword Align** Default Value: 00b Access: RO Hardwired to 0 so that addresses assigned by system software are always aligned on a DWORD address boundary.

Message Control

MC_0_2_0_PCI - Message Control

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	16
Address:	000AEh

Message Signaled Interrupt control register. System software can modify bits in this register, but the device is prohibited from doing so. If the device writes the same message multiple times, only one of those messages is guaranteed to be serviced. If all of them must be serviced, the device must not generate the same message again until the driver services the earlier one.

DWord	Bit	Description
0	7	**64 Bit Capable** Default Value: 0b Access: RO Hardwired to 0 to indicate that the function does not implement the upper 32 bits of the Message address register and is incapable of generating a 64-bit memory address.
	6:4	**Multiple Message Enable** Default Value: 000b Access: R/W System software programs this field to indicate the actual number of messages allocated to this device. This number will be equal to or less than the number actually requested. Value: Number of requests 000: 1 001: 2 010: 4 011: 8 100: 16 101: 32 110: Reserved 111: Reserved
	3:1	**Multiple Message Capable** Default Value: 000b Access: RO System Software reads this field to determine the number of messages being requested by this device. Hardwired to 000b to indicate number of requests is 1.

MC_0_2_0_PCI - Message Control

	0	**MSI Enable** Default Value: 0b Access: R/W Controls the ability of this device to generate MSIs.

Message Data

MD_0_2_0_PCI - Message Data		
Register Space:	PCI: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	16	
Address:	000B4h	
This register contains the Message Data for MSIs sent by the device.		
DWord	**Bit**	**Description**
0	15:0	**Message Data** Default Value: 0000000000000000b Access: R/W Base message data pattern assigned by system software and used to handle an MSI from the device. When the device must generate an interrupt request, it writes a 32-bit value to the memory address specified in the MA register. The upper 16 bits are always set to 0. The lower 16 bits are supplied by this register.

Message Register

MSGREG - Message Register

Register Space:	MMIO: 0/2/0
Default Value:	0x00000001
Size (in bits):	32
Address:	040D4h

DWord	Bit	Description
0	31:16	**Mask Bits** Default Value: 0000h Access: RO Reserved.
	15	**GO_PROTOCOL_GAM_REQUEST15** Default Value: 0b Access: R/W Reserved.
	14	**GO_PROTOCOL_GAM_REQUEST14** Default Value: 0b Access: R/W Reserved.
	13	**GO_PROTOCOL_GAM_REQUEST13** Default Value: 0b Access: R/W Reserved.
	12	**GO_PROTOCOL_GAM_REQUEST12** Default Value: 0b Access: R/W Reserved.
	11	**GO_PROTOCOL_GAM_REQUEST11** Default Value: 0b Access: R/W Reserved.

MSGREG - Message Register

	10	**GO_PROTOCOL_GAM_REQUEST10** Default Value: 0b Access: R/W Reserved.
	9	**GO_PROTOCOL_GAM_REQUEST9** Default Value: 0b Access: R/W Reserved.
	8	**GO_PROTOCOL_GAM_REQUEST8** Default Value: 0b Access: R/W Reserved.
	7	**GO_PROTOCOL_GAM_REQUEST7** Default Value: 0b Access: R/W Reserved.
	6	**GO_PROTOCOL_GAM_REQUEST6** Default Value: 0b Access: R/W Reserved.
	5	**GO_PROTOCOL_GAM_REQUEST5** Default Value: 0b Access: R/W Reserved.
	4	**GO_PROTOCOL_GAM_REQUEST4** Default Value: 0b Access: R/W Reserved.
	3	**GO_PROTOCOL_GAM_REQUEST3** Default Value: 0b Access: R/W Reserved.

MSGREG - Message Register

	2	**GO_PROTOCOL_GAM_REQUEST2** Default Value: 0b Access: R/W Reserved.
	1	**GO_PROTOCOL_GAM_REQUEST1** Default Value: 0b Access: R/W Reserved.
	0	**GO_PROTOCOL_GAM_REQUEST0** Default Value: 1b Access: R/W 0 - GPM to GAM Busy Ack Indication. 1 - GPM to GAM Idle Ack Indication.

Message Signaled Interrupts Capability ID

MSI_CAPID_0_2_0_PCI - Message Signaled Interrupts Capability ID

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x0000D005
Size (in bits):	16
Address:	000ACh

When a device supports MSI it can generate an interrupt request to the processor by writing a predefined data item (a message) to a predefined memory address.

DWord	Bit	Description
0	15:8	**Pointer to Next Capability** Default Value: 11010000b Access: RO This is a hardwired pointer to the next item in the capabilities list which is the Power Management capability.
	7:0	**Capability ID** Default Value: 00000101b Access: RO This field is hardwired to the value 05h to identify the CAP_ID as being for MSI registers.

Messaging Register for GPMunit

MSG_GPM - Messaging Register for GPMunit

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	00C00h

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].
To set bit0, for example, the data would be 0x0001_0001.
To clear bit0, for example, the data would be 0x0001_0000.
Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO
	15	**GPM Messages Bit 15** Access: R/W Placeholder for GPM Messsages. RPMunit could self-clear these bits upon sampling.
	14	**GPM Messages Bit 14** Access: R/W Placeholder for GPM Messsages. RPMunit could self-clear these bits upon sampling.
	13	**GPM Messages Bit 13** Access: R/W Placeholder for GPM Messsages. RPMunit could self-clear these bits upon sampling.
	12	**GPM Messages Bit 12** Access: R/W Placeholder for GPM Messsages. RPMunit could self-clear these bits upon sampling.
	11	**GPM Messages Bit 11** Access: R/W Placeholder for GPM Messsages. RPMunit could self-clear these bits upon sampling.
	10	**GPM Messages Bit 10** Access: R/W Placeholder for GPM Messsages. RPMunit could self-clear these bits upon sampling.

MSG_GPM - Messaging Register for GPMunit

	9	**GPM Messages Bit 9** Access: R/W Placeholder for GPM Messsages. RPMunit could self-clear these bits upon sampling.
	8	**GPM Messages Bit 8** Access: R/W Placeholder for GPM Messsages. RPMunit could self-clear these bits upon sampling.
	7	**Media PowerGate License Request** Access: R/W GPMunit Media PG License Level Request 1'b1 : Media PG ON License Request 1'b0 : Media PG OFF License Request
	6:5	**ICCP Low Level Request** Access: R/W GPMunit IccP License Level Request 2'b00 : Low IccP License Request (default) 2'b01 : High IccP License Request
	4	**Request to send CPD Exit Ack Message on EventBus (U2C)** Access: R/W Request from GPMunit for RPMunit to send CPD_EXIT_ACK message on the Eventbus. RPMunit self-clears this bit upon sampling.
	3	**Request to send CPD Enter Ack Message on EventBus (U2C)** Access: R/W Request from GPMunit for RPMunit to send CPD_ENTER_ACK message on the Eventbus. RPMunit self-clears this bit upon sampling.
	2	**Request to send Credit Active Deassert Message on EventBus (U2C)** Access: R/W Request from GPMunit for RPMunit to send CREDIT_ACTIVE_DEASSERT message on the Eventbus. RPMunit self-clears this bit upon sampling.
	1	**Request to send Credit Active Assert Message on EventBus (U2C)** Access: R/W Request from GPMunit for RPMunit to send CREDIT_ACTIVE_ASSERT message on the Eventbus. RPMunit self-clears this bit upon sampling.
	0	**Request to send IDI Shutdown Ack Message on EventBus (U2C)** Access: R/W Request from GPMunit for RPMunit to send IDI_SHUTDOWN_ACK message on the Eventbus. RPMunit self-clears this bit upon sampling.

Messaging Register for MDRBunit

MSG_MDRB - Messaging Register for MDRBunit

Register Space:	MMIO: 0/2/0
Default Value:	0x00000001
Size (in bits):	32
Address:	00C08h

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].
To set bit0, for example, the data would be 0x0001_0001.
To clear bit0, for example, the data would be 0x0001_0000.
Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO
	15:2	**MDRB Messages** Access: R/W Placeholder for MDRB Messsages. MDRBunit could self-clear these bits upon sampling.
	1	**RFO Enable/Disable Ack for RPM (internal) RFO Request** Access: R/W RFO Enable/Disable Ack for Internal RFO Request. Enable Ack = 1'b1 Disable Ack = 1'b0
	0	**RFO Enable/Disable Ack for U2C (Evtentbus) RFO Request** Default Value: 1b Access: R/W RFO Enable/Disable Ack for U2C RFO Request. Enable Ack = 1'b1 Disable Ack = 1'b0

Messaging Register for MGSRunit

MSG_MGSR - Messaging Register for MGSRunit

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	00C04h

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].
To set bit0, for example, the data would be 0x0001_0001.
To clear bit0, for example, the data would be 0x0001_0000.
Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO
	15:0	**MGSR Messages** Access: R/W Placeholder for MGSR Messsages. MGSRunit could self-clear these bits upon sampling.

Messaging Register for SPCunit

MSG_SPC - Messaging Register for SPCunit

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	00C10h

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].
To set bit0, for example, the data would be 0x0001_0001.
To clear bit0, for example, the data would be 0x0001_0000.
Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description
0	31:1	**Reserved** Access: RO
	0	**SPC GTI PGCTL ACK** Access: R/W SPC PowerGate Control Ack Message 1'b0 : PowerDown Ack (default). 1'b1 : PowerUp Ack (default).

MFC_AVC_CABAC_INSERTION_COUNT

AVC_CABAC_INSERTION_COUNT - MFC_AVC_CABAC_INSERTION_COUNT	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	128ACh

This register stores the count in bytes of **CABAC ZERO_WORD insertion. It is primarily provided for statistical data gathering.**

DWord	Bit	Description
0	31:0	**MFC AVC Cabac Insertion Count** Total number of bytes in the bitstream output before for the CABAC zero word insertion. This count is updated each time when the insertion count is incremented.

MFC_AVC Bitstream Decoding Front-End Parsing Logic Error Counter

MFC_VIN_AVD_ERROR_CNTR - MFC_AVC Bitstream Decoding Front-End Parsing Logic Error Counter

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	12804h

DWord	Bit	Description
0 avd_error_flagsR[31:0]	31:0	**Reserved** Format: MBZ

MFC Image Status Control

MFC_IMAGE_STATUS_CONTROL - MFC Image Status Control		
Register Space:	MMIO: 0/2/0	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	128B8h	
This register stores the suggested data for next frame in multi-pass.		
DWord	**Bit**	**Description**
0	31:24	**Cumulative slice delta QP**
	23:16	**QP Value** suggested slice QP delta value for frame level Rate control. This value can be +ve or -ve
	15	**QP-Polarity Change** Cumulative slice delta QP polarity change.
	14:13	**Num-Pass Polarity Change** Number of passes after cumulative slice delta QP polarity changes.
	12	**Reserved**
	11:8	**Total Num-Pass**
	7:4	**Reserved** Format: MBZ
	3	**Missing Huffman Code** Jpeg HW encoder reports if Huffman table entry is missing.
	2	**Panic** Panic triggered to avoid too big packed file.
	1	**Frame Bit Count** Frame Bit count over-run/under-run flag
	0	**Max Conformance Flag** Max Macroblock conformance flag or Frame Bit count over-run/under-run

MFC Image Status Mask

MFC_IMAGE_STATUS_MASK - MFC Image Status Mask		
Register Space:	MMIO: 0/2/0	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	128B4h	
This register stores the image status(flags).		
DWord	**Bit**	**Description**
0	31:0	**Control Mask** Control Mask for dynamic frame repeat.

MFC QP Status Count

MFC_QUP_CT - MFC QP Status Count		
Register Space:	MMIO: 0/2/0	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	128BCh	
This register stores the suggested QP COUNTS in multi-pass.		
DWord	**Bit**	**Description**
0	31:24	**Cumulative QP Adjust** Format: U8 Cumulative QP adjustment after multiple passes. If there is no need to multi-pass, this value would be zero. (This is in sign magnitude form).
	23:0	**Cumulative QP** Format: U24 Cumulative QP for all MB of a Frame (Can be used for computing average QP).

MFD Error Status

MFD_ERROR_STATUS - MFD Error Status	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12800h
Address:	1C800h

This register stores the error status flags and count reports by the bit-stream decoder.
This register is not part of hardware context save and restore. Driver should read the content prior to starting a new batch/frame.

DWord	Bit	Description
0	31:20	**Reserved** Format: MBZ This field is currently reserved
	19:16	**AVC Short Format Error Flags** Exists If: // AVC Short Format == Ture Bit-stream error detected by VLD short format bit-stream decoder**.** These flags are reset at the beginning of a frame and updated until starting of another frame. [19] – Slice Type SE Error Flag – Invalid Slice Type SE [18] – MMCO SE Error Flag – Invalid memory management control operation SE. MMCO Loop does not end (mmco control != 0) even after all MMCO SEs are decoded OR MMCO SEs are still being decoded and MMCO SE loop end (mmco control == 0) is hit [17] – Reordering IDC Error Flag – Syntax Element modification_of_pic_nums_idc >= 6 OR modification_of_pic_nums_idc != 3 (end of reordering loop) but reordering count has already hit maximum value [16] – Premature bitstream end is hit before finishing slice header decode
	15:0	**Bit-stream Error flags** Exists If: // AVC CAVLC, AVC CABAC, VC1 and MPEG2 == True Bitstream error detected by the VLD bit-steram decoder. These flags are reset at the beginning of a frame and updated until starting of another frame. AVC CAVLC: Please refer to AVC CAVLC table for each bit field AVC CABAC: Please refer to AVC CABAC table for each bit field VC1: Please refer to VC1 table for each bit field MPEG2: Please refer to MPEG2 table for each bit field

MFD Picture Parameter

MFD_PICTURE_PARAM - MFD Picture Parameter		
Register Space:	MMIO: 0/2/0	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	12820h	
Address:	1C820h	
DWord	**Bit**	**Description**
0	31:0	**Reserved** Format: MBZ

MFX_Memory_Latency_Count1

MFX_LAT_CT1 - MFX_Memory_Latency_Count1	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12870h
Address:	1C870h

This register stores the max and min memory latency counts reported on reference read requests.
This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:24	**Max Request Count** This field indicates the maximum number of requests allowed by the memory sub-system channel.
	23:16	**Current Request Count** This field indicates the number of requests currently outstanding in the memory sub-system. This field should report with a value of zero at the end of frame; otherwise the motion compensation engine is most likely hung waiting for read data to be returned from sub-system.
	15:8	**MFX Reference picture read request - Max Latency Count in 8xMedia clock cycles** This field reports the maximum memory latency count on all reference reads requested by the motion compensation engine.
	7:0	**MFX Reference picture read request - Min Latency Count in 8xMedia clock cycles** This field reports the minimum memory latency count on all reference reads requested by the motion compensation engine.

MFX0 Context Element Descriptor (High Part)

MFX0_CTX_EDR_H - MFX0 Context Element Descriptor (High Part)

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	04444h

DWord	Bit	Description
0	31:0	**MFX0 Context Element Descriptor (High Part)** Default Value: 00000000h Access: R/W

MFX0 Context Element Descriptor (Low Part)

MFX0_CTX_EDR_L - MFX0 Context Element Descriptor (Low Part)		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000009	
Size (in bits):	32	
Address:	04440h	
DWord	**Bit**	**Description**
0	31:0	**MFX0 Context Element Descriptor (Low Part)** Default Value: 00000009h Access: R/W

MFX0 Fault Counter

MFX0_FAULT_CNTR - MFX0 Fault Counter		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	045A8h	
DWord	**Bit**	**Description**
0	31:0	**MFX0 Fault Counter** Default Value: 00000000h Access: RO This counter only applies to advance context when fault and stream mode is selected.

MFX0 Fixed Counter

MFX0_FIXED_CNTR - MFX0 Fixed Counter		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	045ACh	
DWord	**Bit**	**Description**
0	31:0	**MFX0 Fixed Counter** Default Value: 00000000h Access: RO This counter only applies to advance context when fault and stream mode is selected.

MFX0 PDP0/PML4/PASID Descriptor (High Part)

MFX0_CTX_PDP0_H - MFX0 PDP0/PML4/PASID Descriptor (High Part)

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0444Ch

DWord	Bit	Description
0	31:0	**MFX0 PDP0/PML4/PASID Descriptor (High Part)** Default Value: 00000000h Access: R/W

MFX0 PDP0/PML4/PASID Descriptor (Low Part)

MFX0_CTX_PDP0_L - MFX0 PDP0/PML4/PASID Descriptor (Low Part)

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	04448h

DWord	Bit	Description
0	31:0	**MFX0 PDP0/PML4/PASID Descriptor (Low Part)** Default Value: 00000000h Access: R/W

MFX0 PDP1 Descriptor Register (High Part)

MFX0_CTX_PDP1_H - MFX0 PDP1 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04454h	
DWord	**Bit**	**Description**
0	31:0	**MFX0 PDP1 Descriptor Register (High Part)** Default Value: 00000000h Access: R/W

MFX0 PDP1 Descriptor Register (Low Part)

MFX0_CTX_PDP1_L - MFX0 PDP1 Descriptor Register (Low Part)		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04450h	
DWord	**Bit**	**Description**
0	31:0	**MFX0 PDP1 Descriptor Register (Low Part)** Default Value: 00000000h Access: R/W

MFX0 PDP2 Descriptor Register (High Part)

MFX0_CTX_PDP2_H - MFX0 PDP2 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0445Ch	
DWord	**Bit**	**Description**
0	31:0	**MFX0 PDP2 Descriptor Register (High Part)** Default Value: 00000000h Access: R/W

MFX0 PDP2 Descriptor Register (Low Part)

MFX0_CTX_PDP2_L - MFX0 PDP2 Descriptor Register (Low Part)

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	04458h

DWord	Bit	Description
0	31:0	**MFX0 PDP2 Descriptor Register (Low Part)** Default Value: 00000000h Access: R/W

MFX0 PDP3 Descriptor Register (High Part)

MFX0_CTX_PDP3_H - MFX0 PDP3 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04464h	
DWord	**Bit**	**Description**
0	31:0	**MFX0 PDP3 Descriptor Register (High Part)** Default Value: 00000000h Access: R/W

MFX0 PDP3 Descriptor Register (Low Part)

MFX0_CTX_PDP3_L - MFX0 PDP3 Descriptor Register (Low Part)		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04460h	
DWord	**Bit**	**Description**
0	31:0	**MFX0 PDP3 Descriptor Register (Low Part)** Default Value: 00000000h Access: R/W

MFX1 Context Element Descriptor (High Part)

MFX1_CTX_EDR_H - MFX1 Context Element Descriptor (High Part)

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	04484h

DWord	Bit	Description
0	31:0	**MFX1 Context Element Descriptor (High Part)** Default Value: 00000000h Access: R/W

MFX1 Context Element Descriptor (Low Part)

MFX1_CTX_EDR_L - MFX1 Context Element Descriptor (Low Part)

Register Space:	MMIO: 0/2/0
Default Value:	0x00000009
Size (in bits):	32
Address:	04480h

DWord	Bit	Description
0	31:0	**MFX1 Context Element Descriptor (Low Part)** Default Value: 00000009h Access: R/W

MFX1 Fault Counter

MFX1_FAULT_CNTR - MFX1 Fault Counter		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	045B0h	

DWord	Bit	Description
0	31:0	**MFX1 Fault Counter** Default Value: 00000000h Access: RO This counter only applies to advance context when fault and stream mode is selected.

MFX1 Fixed Counter

MFX1_FIXED_CNTR - MFX1 Fixed Counter		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	045B4h	
DWord	**Bit**	**Description**
0	31:0	**MFX1 Fixed Counter** Default Value: 00000000h Access: RO This counter only applies to advance context when fault and stream mode is selected.

MFX1 PDP0/PML4/PASID Descriptor (High Part)

MFX1_CTX_PDP0_H - MFX1 PDP0/PML4/PASID Descriptor (High Part)

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0448Ch

DWord	Bit	Description
0	31:0	**MFX1 PDP0/PML4/PASID Descriptor (High Part)** Default Value: 00000000h Access: R/W

MFX1 PDP0/PML4/PASID Descriptor (Low Part)

MFX1_CTX_PDP0_L - MFX1 PDP0/PML4/PASID Descriptor (Low Part)

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	04488h

DWord	Bit	Description
0	31:0	**MFX1 PDP0/PML4/PASID Descriptor (Low Part)** Default Value: 00000000h Access: R/W

MFX1 PDP1 Descriptor Register (High Part)

MFX1_CTX_PDP1_H - MFX1 PDP1 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04494h	
DWord	**Bit**	**Description**
0	31:0	**MFX1 PDP1 Descriptor Register (High Part)** Default Value: 00000000h Access: R/W

MFX1 PDP1 Descriptor Register (Low Part)

MFX1_CTX_PDP1_L - MFX1 PDP1 Descriptor Register (Low Part)

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	04490h

DWord	Bit	Description
0	31:0	**MFX1 PDP1 Descriptor Register (Low Part)** Default Value: 00000000h Access: R/W

MFX1 PDP2 Descriptor Register (High Part)

MFX1_CTX_PDP2_H - MFX1 PDP2 Descriptor Register (High Part)

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0449Ch

DWord	Bit	Description
0	31:0	**MFX1 PDP2 Descriptor Register (High Part)** Default Value: 00000000h Access: R/W

MFX1 PDP2 Descriptor Register (Low Part)

MFX1_CTX_PDP2_L - MFX1 PDP2 Descriptor Register (Low Part)

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	04498h

DWord	Bit	Description
0	31:0	**MFX1 PDP2 Descriptor Register (Low Part)** Default Value: 00000000h Access: R/W

MFX1 PDP3 Descriptor Register (High Part)

MFX1_CTX_PDP3_H - MFX1 PDP3 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	044A4h	
DWord	**Bit**	**Description**
0	31:0	**MFX1 PDP3 Descriptor Register (High Part)** Default Value: 00000000h Access: R/W

MFX1 PDP3 Descriptor Register (Low Part)

MFX1_CTX_PDP3_L - MFX1 PDP3 Descriptor Register (Low Part)

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	044A0h

DWord	Bit	Description
0	31:0	**MFX1 PDP3 Descriptor Register (Low Part)** Default Value: 00000000h Access: R/W

MFX Frame BitStream SE/BIN Count

MFX_SE-BIN_CT - MFX Frame BitStream SE/BIN Count	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1286Ch
Address:	1C86Ch
This register stores the number of BINs (AVC CABAC) and SEs (CAVLD, VLD) decoded in a frame. This register is not part of hardware context save and restore.	

DWord	Bit	Description
0	31:0	**MFX Frame Bit-stream SE/BIN Count** Total number of BINs/SEs decoded in current frame. This number is used with frame performance count to derive Bin/clk or SE/clk.

MFX Frame Macroblock Count

MFX_MB_COUNT - MFX Frame Macroblock Count

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12868h
Address:	1C868h

This register stores the number of Macro-blocks decoded/encoded in current frame.
This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:20	**MBZ** Exists If: // JPEG == True Format: MBZ This field is currently reserved
	31:16	**Intra MB Count** Exists If: // AVC CAVLC, AVC CABAC, VC1 and MPEG2 == True Format: U16
	19:0	**JPEG Block Count** Exists If: // JPEG == True Format: U20 This 20-bit field indicates the number of 8x8 blocks within the JPEG frame. This field is clear at the start of decoding a new frame.
	15:0	**Number of MB Concealment** Exists If: // AVC CAVLC, AVC CABAC, VC1 and MPEG2 == True This 16-bit field indicates the number of MB is concealed by hardware. This field is clear at the start of decoding a new frame.

MFX Frame Motion Comp Miss Count

MFX_MISS_CT - MFX Frame Motion Comp Miss Count	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12888h
Address:	1C888h

This register stores the total number of cacheline hits occurred in the motion compensation cache per frame.
This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:0	**MFX Frame Motion Comp cache miss Count** Format: U32 Total number of CL misses occurred in the 12KB cache of the motion compensation engine per frame. This number is used along with **MFX Frame Motion Comp Read Count** to derive motion comp cache miss/hit ratio.

MFX Frame Motion Comp Read Count

MFX_READ_CT - MFX Frame Motion Comp Read Count		
Register Space:	MMIO: 0/2/0	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	12884h	
Address:	1C884h	
This register stores the total number of reference picture read requests made by the Motion Compensation engine per frame. This register is not part of hardware context save and restore.		
DWord	**Bit**	**Description**
0	31:0	**MFX Frame Motion Comp CL read request Count** Total number of reference picture read requests by the motion compensation engine per frame.

MFX Frame Performance Count

MFX_FRAME_PERFORMANCE_CT - MFX Frame Performance Count	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12860h
Address:	1C860h

This register stores the number of clock cycles spent decoding/encoding the current frame.
This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:0	**MFX Frame Performance Counter** Total number of clocks between frame start and frame end. This counter is incremented on cmclk

MFX Frame Row-Stored/BitStream Read Count

MFX_ROW-PER-BS_COUNT - MFX Frame Row-Stored/BitStream Read Count

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12880h

This register stores the total number of row-stored/bit-stream read requests made by the pre-fetch engine per frame.
This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:0	**MFX row-stored/bit-stream read request Count** Total number of row-stored/bit-stream read requests sent by the memory pre-fetch engine per frame.

MFX LRA 0

MFX_LRA_0 - MFX LRA 0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x7F403F00
Size (in bits):	32
Address:	04A50h

DWord	Bit	Description
0	31:24	**MFX LRA1 Max** Default Value: 01111111b Access: R/W Maximum value of programmable LRA1.
	23:16	**MFX LRA1 Min** Default Value: 01000000b Access: R/W Minimum value of programmable LRA1.
	15:8	**MFX LRA0 Max** Default Value: 00111111b Access: R/W Maximum value of programmable LRA0.
	7:0	**MFX LRA0 Min** Default Value: 00000000b Access: R/W Minimum value of programmable LRA0.

MFX LRA 1

MFX_LRA_1 - MFX LRA 1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0xFFC0BF80	
Size (in bits):	32	
Address:	04A54h	
DWord	**Bit**	**Description**
0	31:24	**MFX LRA3 Max** Default Value: 11111111b Access: R/W Maximum value of programmable LRA3.
	23:16	**MFX LRA3 Min** Default Value: 11000000b Access: R/W Minimum value of programmable LRA3.
	15:8	**MFX LRA2 Max** Default Value: 10111111b Access: R/W Maximum value of programmable LRA2.
	7:0	**MFX LRA2 Min** Default Value: 10000000b Access: R/W Minimum value of programmable LRA2.

MFX LRA 2

MFX_LRA_2 - MFX LRA 2

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x000002D3
Size (in bits):	32
Address:	04A58h

DWord	Bit	Description
0	31:12	**Reserved** Default Value: 00000h Access: RO
	11:10	**VMXRA LRA** Default Value: 00b Access: R/W Which LRA should VMXRA use.
	9:8	**BSP LRA** Default Value: 10b Access: R/W Which LRA should BSP use.
	7:6	**VCS LRA** Default Value: 11b Access: R/W Which LRA should VCS use.
	5:4	**VMX LRA** Default Value: 01b Access: R/W Which LRA should VMX use.
	3:2	**VMC LRA** Default Value: 00b Access: R/W Which LRA should VMC use.
	1:0	**VCR LRA** Default Value: 11b Access: R/W Which LRA should VCR use.

MFX LRA SL1 0

MFX_LRA_SL1_0 - MFX LRA SL1 0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x7F403F00	
Size (in bits):	32	
Address:	04A60h	
DWord	**Bit**	**Description**
0	31:24	**MFX SL1 LRA1 Max** Default Value: 01111111b Access: R/W Maximum value of programmable LRA1.
	23:16	**MFX SL1 LRA1 Min** Default Value: 01000000b Access: R/W Minimum value of programmable LRA1.
	15:8	**MFX SL1 LRA0 Max** Default Value: 00111111b Access: R/W Maximum value of programmable LRA0.
	7:0	**MFX SL1 LRA0 Min** Default Value: 00000000b Access: R/W Minimum value of programmable LRA0.

MFX LRA SL1 1

MFX_LRA_SL1_1 - MFX LRA SL1 1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0xFFC0BF80	
Size (in bits):	32	
Address:	04A64h	

DWord	Bit	Description
0	31:24	**MFX SL1 LRA3 Max** Default Value: 11111111b Access: R/W Maximum value of programmable LRA3.
	23:16	**MFX SL1 LRA3 Min** Default Value: 11000000b Access: R/W Minimum value of programmable LRA3.
	15:8	**MFX SL1 LRA2 Max** Default Value: 10111111b Access: R/W Maximum value of programmable LRA2.
	7:0	**MFX SL1 LRA2 Min** Default Value: 10000000b Access: R/W Minimum value of programmable LRA2.

MFX LRA SL1 2

MFX_LRA_SL1_2 - MFX LRA SL1 2	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x000002D3
Size (in bits):	32
Address:	04A68h

DWord	Bit	Description
0	31:12	**Reserved** Default Value: 00000h Access: RO
	11:10	**VMXRASL1 LRA** Default Value: 00b Access: R/W Which LRA should VMXRASL1 use.
	9:8	**BSPSL1 LRA** Default Value: 10b Access: R/W Which LRA should BSPSL1 use.
	7:6	**VCSSL1 LRA** Default Value: 11b Access: R/W Which LRA should VCSSL1 use.
	5:4	**VMXSL1 LRA** Default Value: 01b Access: R/W Which LRA should VMXSL1 use.
	3:2	**VMCSL1 LRA** Default Value: 00b Access: R/W Which LRA should VMCSL1 use.
	1:0	**VCRSL1 LRA** Default Value: 11b Access: R/W Which LRA should VCRSL1 use.

MFX Memory Latency Count2

MFX_LAT_CT2 - MFX Memory Latency Count2

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12874h
Address:	1C874h

This register stores the accumulative memory latency count on reference picture read requests.
This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:26	**Reserved** Format: MBZ
	25:0	**MFX Reference picture read request - Accumulative Memory Latency Count for the entire frame in 8xMedia clock cycles** The accumulative memory latency count of all reference reads requested by motion compensative engine per frame. This number is used with **MFX Frame Motion Comp Read Count** to derive average memory latency.

MFX Memory Latency Count3

MFX_LAT_CT3 - MFX Memory Latency Count3	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12878h
Address:	1C878h

This register stores the max and min memory latency counts reported on row-stored/bit-stream read requests. Max and current requests into memory sub-system engine.
This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:24	**Max Request Count** This field indicates the maximum number of requests allowed by the memory sub-system channel.
	23:16	**Current Request Count** This field indicates the number of requests currently outstanding in the memory sub-system. This field should report with a value of zero at the end of frame; otherwise the pre-fetch engine most likely hung waiting for read data to be returned from sub-system.
	15:8	**MFX row-stored/bit-stream read request - Max Latency Count in 8xMedia clock cycles** This field reports the maximum memory latency count on all row-stored/bit-stream reads requested by the memory pre-fetch engine.
	7:0	**MFX row-stored/bit-stream read request - Min Latency Count in 8xMedia clock cycles** This field reports the minimum memory latency count on all row-stored/bit-stream reads requested by the memory pre-fetch engine.

MFX Memory Latency Count4

MFX_LAT_CT4 - MFX Memory Latency Count4

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1287Ch
Address:	1C87Ch

This register stores the accumulative memory latency count on row-stored/bit-stream read requests.
This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:26	**Reserved** Format: MBZ
	25:0	**MFX row-stored/bit-stream read request - Accumulative Memory Latency Count for the entire frame in 8xMedia clock cycles** The accumulative memory latency count of all row-stored/bit-stream reads requested by pre-fetch engine per frame. This number is used with **Frame row-stored/bit-stream memory read count** to derive average memory latency.

MFX Pipeline Status Flags

MFX_STATUS_FLAGS - MFX Pipeline Status Flags

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12838h
Address:	1C838h

This register stores the various pipeline status flags.
This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:17	**Reserved** Format: MBZ
	16	**MFX Active** Frame decoding/encoding is in progress. Set on frame_start; clear on frame_end.
	15:10	**Reserved** Format: MBZ
	9	**Streamout Enable**
	8	**Reserved**
	7	**Post Deblocking Mode Enable**
	6	**Pre Deblocking Mode Enable**
	5	**Decoder Mode Select** Value: 0 — Name: Configure the MFD Engine for VLD Mode Value: 1 — Name: Configure the MFD Engine for IT Mode
	4	**Codec Select** Value: 0 — Name: Decode Value: 1 — Name: Encode
	3:2	**Video Mode** Value: 00b — Name: MPEG2

MFX_STATUS_FLAGS - MFX Pipeline Status Flags

		01b: VC1 10b: AVC 11b: JPEG
	1	**Decoder Short Format Mode** 0: AVC/VC1 Short Format Mode is in use 1: AVC/VC1 Long Format Mode is in use
	0	**Stitch Mode** 0b: Not in Stitch Mode 1b: In the Special Stitch Mode

MFX SFC LOCK Request

MFX_SFC_LOCK_REQUEST - MFX SFC LOCK Request		
Register Space:	MMIO: 0/2/0	
Source:	VideoEnhancementCS	
Default Value:	0x00000000	
Access:	WO	
Size (in bits):	32	
Address:	1288Ch	
DWord	**Bit**	**Description**
0	31:1	**Reserved** Format: MBZ
	0	**MFX_SFC_Forced_Lock** Format: U1 This bit can only be set by driver and it has to be clear by driver as well. Driver should set this bit before issuing the software (watchdog timer) reset. It tells MFX that a software reset is going to happen. MFX then issues a forced lock to SFC. If SFC is currently locked to MFX, SFC should not unlock itself from MFX. If SFC is NOT currently locked to MFX, SFC should not accept the lock request from MFX. Driver needs to clear this bit after the software reset sequence is complete.

MFX SFC LOCK Status

MFX_SFC_LOCK_STATUS - MFX SFC LOCK Status

Register Space:	MMIO: 0/2/0
Source:	VideoEnhancementCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	12890h

DWord	Bit	Description
0	31:2	**Reserved** Format: MBZ
	1	**MFX_SFC_Forced_Act** Format: U1 This bit can only be set by hardware and it has to be clear by hardware as well. This bit is going to be polled by driver. This bit indicates that MFX has received MFX_SFC_Forced_Lock from driver and it has sent that signal to SFC. Once this bit is set, it indicates SFC status (lock or unlock) will not be changed anymore. Driver will be safe to start the reset process after this bit is set. Hardware has to de-assert this bit after driver de-assert MFX_SFC_Forced_Lock as well.
	0	**MFX_SFC_Usage** Format: U1 This bit can only be set by hardware and it has to be clear by hardware as well. This bit indicates SFC is currently locked to MFX. This bit should be set after SFC accepts the lock request from MFX. This bit should be clear once SFC finishes the workload and unlocked from MFX. In case a reset happens on MFX, this bit must be reset once a new workload is received

MFX Slice Performance Count

MFX_SLICE_PERFORM_CT - MFX Slice Performance Count	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12864h
Address:	1C864h

This register stores the number of clock cycles spent decoding/encoding the current slice.
This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:0	**MFX Frame Performance Count** Total number of clocks between slice start and slice end. This count is incremented on crm_clk

MGSR2GAM Message Register

MGSR2GAM_MSGREG - MGSR2GAM Message Register

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	040D8h

DWord	Bit	Description
0	31:16	**Mask Bits** Default Value: 0000h Access: RO Mask Bits act as Write Enables for the bits[15:0] of this register.
	15	**MGSR2GAM Message Register 15** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	14	**MGSR2GAM Message Register 14** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	13	**MGSR2GAM Message Register 13** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	12	**MGSR2GAM Message Register 12** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	11	**MGSR2GAM Message Register 11** Default Value: 0b Access: R/W For Future Use. This bit is self clear.

MGSR2GAM_MSGREG - MGSR2GAM Message Register

	10	**MGSR2GAM Message Register 10** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	9	**MGSR2GAM Message Register 9** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	8	**MGSR2GAM Message Register 8** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	7	**MGSR2GAM Message Register 7** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	6	**MGSR2GAM Message Register 6** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	5	**MGSR2GAM Message Register 5** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	4	**MGSR2GAM Message Register 4** Default Value: 0b Access: R/W For Future Use. This bit is self clear.

MGSR2GAM_MSGREG - MGSR2GAM Message Register

	3	**MGSR2GAM Message Register 3** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	2	**MGSR2GAM Message Register 2** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	1	**MGSR2GAM Message Register 1** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	0	**MGSR2GAM Message Register 0** Default Value: 0b Access: R/W Bit0 - Tail Update Ack Message. This bit is self clear.

MGSR Control Register 1

SHADOWREG1 - MGSR Control Register 1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000002
Size (in bits):	32
Address:	00E04h-00E07h

DWord	Bit	Description
0	31:16	**Mask Bits** Access: RO Mask bits applied to [15:0] of same register. If mask is set to 1, corresponding bit in [15:0] is written. If mask is set to 0, corresponding bit in [15:0] is unaffected.
	15:9	**Reserved** Access: RO
	8	**Force Wake** Default Value: 0b Access: R/WC block GT wakeup
	7:4	**Reserved** Access: RO
	3	**RENDER unblock** Default Value: 0b Access: R/WC RENDER unblock (1) or block (0)
	2	**MEDIA unblock** Default Value: 0b Access: R/WC MEDIA unblock (1) or block (0)
	1	**RC6 model** Default Value: 1b Access: R/WC Set RC6 mode (1) or CPD(0)

SHADOWREG1 - MGSR Control Register 1		
	0	**GT unblock** Default Value: 0b Access: R/WC GT unblock (1) or block (0)

MGSR Program Register 1

SHADOWREG119 - MGSR Program Register 1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x10000000
Size (in bits):	32
Address:	00FDCh-00FDFh

DWord	Bit	Description
0	31:29	**Reserved** Access: RO
	28	**MULTICAST** Default Value: 1b Access: R/W Value in this register determines the multicast value driven to MCR during C0. 0 - not multicast 1 - multicast This register is not reset on FLR.
	27:26	**SLICEID** Default Value: 00b Access: R/W Value in this register determines the slice ID driven to MCR during C0. 00 - slice 0, 01 - slice 1, 10 - slice 2 11 - not used The usage model should be to set this register to the appropriate value, read the multicast register and then set it back to 0b00. When slice 0 is disabled (when fuse reflection MMADR 0x9120[25] = 0), this field must be set to a valid slice (slice 1 or slice 2) before issuing a read to a register in a slice unit. This register is not reset on FLR.
	25:24	**SUBSLICEID** Default Value: 00b Access: R/W Value in this register determines the subslice ID driven to MCR during C0. 00 - subslice 0 (or l3_bank0) 01 - subslice 1 (or l3_bank1) 10 - subslice 2 (or l3_bank2) 11 - rsvd (or l3_bank3) This register is not reset on FLR.

SHADOWREG119 - MGSR Program Register 1

	23:20	**RESERVED** Access: RO
	19:0	**ADDR1** Default Value: 00000h Access: R/W Programmable shadow register address. Program additional address to shadow in this register. source : IA This register is not reset on FLR.

MGSR Program Register 2

SHADOWREG120 - MGSR Program Register 2		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00FE0h-00FE3h	
DWord	**Bit**	**Description**
0	31:25	**Reserved2** Default Value: 0000000b Access: R/W
	24	**Reserved**
	23:20	**Reserved** Access: RO
	19:0	**ADDR2** Default Value: 00000h Access: R/W Programmable shadow register address. Program additional address to shadow in this register. source : PCH

MGSR Program Register 3

SHADOWREG121 - MGSR Program Register 3		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00FE4h-00FE7h	
DWord	**Bit**	**Description**
0	31:20	**Reserved** Access: RO
	19:0	**ADDR3** Default Value: 00000h Access: R/W Programmable shadow register address. Program additional address to shadow in this register. Source : IA

MGSR Program Register 4

SHADOWREG122 - MGSR Program Register 4		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00FE8h-00FEBh	
DWord	**Bit**	**Description**
0	31:20	**Reserved** Access: RO
	19:0	**ADDR4** Default Value: 00000h Access: R/W Programmable shadow register address. Program additional address to shadow in this register. source : IA

Minimum Grant

MINGNT_0_2_0_PCI - Minimum Grant		
Register Space:	PCI: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	8	
Address:	0003Eh	
The Integrated Graphics Device has no requirement for the settings of Latency Timers.		
DWord	**Bit**	**Description**
0	7:0	**Minimum Grant Value** Default Value: 00000000b Access: RO Hardwired to 0s because the IGD does not burst as a PCI compliant master.

Mirror of Base Data of Stolen Memory

BDSM_0_2_0_PCI - Mirror of Base Data of Stolen Memory

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	0005Ch

Mirror of BSDM_0_0_0_PCI.
This register contains the base address of graphics data stolen DRAM memory.

DWord	Bit	Description
0	31:20	**Graphics Base of Stolen Memory** Default Value: 000000000000b Access: RO This register contains bits 31 to 20 of the base address of stolen DRAM memory. BIOS determines the base of graphics stolen memory by subtracting the graphics stolen memory size (PCI Device 0 offset 52 bits 6:4) from TOLUD (PCI Device 0 offset BC bits 31:20).
	19:1	**Reserved** Format: MBZ
	0	**Lock** Default Value: 0b Access: RO This bit will lock all writeable settings in this register, including itself.

Mirror of Capabilities A

CAPID0_A_0_2_0_PCI - Mirror of Capabilities A

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	00044h

Mirror of CAPID0_A_0_0_0_PCI.

DWord	Bit	Description	
0	31	**Display HD Audio Disable**	
		Access:	RO
	30	**PEG12 Disable**	
		Default Value:	0b
		Access:	RO
	29	**PEG11 Disable**	
		Default Value:	0b
		Access:	RO
	28	**PEG10 Disable**	
		Default Value:	0b
		Access:	RO
	27	**PCI Express Link Width Upconfig Disable**	
		Default Value:	0b
		Access:	RO
	26	**DMI Width**	
		Default Value:	0b
		Access:	RO
	25	**ECC Disable**	
		Default Value:	0b
		Access:	RO
	24	**Force DRAM ECC Enabled**	
		Default Value:	0b
		Access:	RO
	23	**VTd Disable**	
		Default Value:	0b
		Access:	RO

CAPID0_A_0_2_0_PCI - Mirror of Capabilities A

		0: Enable VTd 1: Disable VTd
	22	**DMI Gen 2 Disable** Default Value: 0b Access: RO
	21	**PEG Gen 2 Disable** Default Value: 0b Access: RO
	20:19	**DDR Size** Default Value: 00b Access: RO
	18	**SPARE18** Default Value: 0b Access: RO
	17	**Disable 1N Mode** Default Value: 0b Access: RO
	16	**Full ULT Fuse Read Disable** Default Value: 0b Access: RO
	15	**Camarillo Device Disable** Default Value: 0b Access: RO
	14	**2 DIMMS per Channel Disable** Default Value: 0b Access: RO
	13	**X2APIC Enabled** Default Value: 0b Access: RO
	12	**Performance Dual Channel Disable** Default Value: 0b Access: RO
	11	**Internal Graphics Disable** Default Value: 0b Access: RO

CAPID0_A_0_2_0_PCI - Mirror of Capabilities A

		0b: There is a graphics engine within this CPU. Internal Graphics Device (Device 2) is enabled and all of its memory and I/O spaces are accessable. Configuration cycles to Device 2 will be completed within the CPU. All non-SMM memory and IO accesses to VGA will be handled based on Memory and IO enables of Device 2 and IO registers within Device 2 and VGA Enable of the PCI to PCI bridge control (If PCI Express GFX attach is supported). A selected amount of Graphics Memory space is pre-allocated from the main memory based on Graphics Mode Select (GMS in the GGC Register). Graphics Memory is pre-allocated above TSEG Memory. 1b: There is no graphics engine within this CPU. Internal Graphics Device (Device 2) and all of its memory and I/O functions are disabled. Configuration cycle targeted to Device 2 will be passed on. All non-SMM memory and IO accesses to VGA will be handled based on VGA Enable of the PCI to PCI bridge control. Device 2 is disabled and hidden.
	10	**Reserved**
	9	**Reserved**
	8	**SPARE8** Default Value: 0b Access: RO
	7:4	**Compatibility Rev ID** Default Value: 0000b Access: RO This is an 8-bit value that indicates the revision identification number for the Host Device 0.
	3	**DDR Overclocking** Default Value: 0b Access: RO
	2	**IA Overclocking Enabled by DSKU** Default Value: 0b Access: RO
	1	**DDR Write VRef** Default Value: 0b Access: RO
	0	**DDR3L Enable** Default Value: 0b Access: RO

Mirror of Capabilities B

CAPID0_B_0_2_0_PCI - Mirror of Capabilities B

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	00048h

Mirror of CAPID0_B_0_0_0_PCI.

DWord	Bit	Description	
0	31	**IMGU Disable**	
		Default Value:	0b
		Access:	RO
	30	**SPARE30**	
		Default Value:	0b
		Access:	RO
	29	**IA Overclocking Enable**	
		Default Value:	0b
		Access:	RO
	28	**SMT Capability**	
		Default Value:	0b
		Access:	RO
	27:25	**Cache Size Capability**	
		Default Value:	000b
		Access:	RO
	24	**SPARE24**	
		Default Value:	0b
		Access:	RO
	23:21	**DDR3 Maximum Frequency Capability with 100 Memory**	
		Default Value:	000b
		Access:	RO
	20	**Gen3 Disable Fuse for PCIe PEG Controllers**	
		Default Value:	0b
		Access:	RO

CAPID0_B_0_2_0_PCI - Mirror of Capabilities B

	19	**Package Type** Default Value: 0b Access: RO
	18	**Additive Graphics Enabled** Default Value: 0b Access: RO 0 - Additive Graphics Disabled 1- Additive Graphics Enabled
	17	**Additive Graphics Capable** Default Value: 0b Access: RO 0 - Capable of Additive Graphics 1 - Not capable of Additive Graphics
	16	**Primary PEG Port x16 Disable** Default Value: 0b Access: RO
	15	**DMIG3 Disable** Default Value: 0b Access: RO
	14:12	**SPARE14_12** Default Value: 000b Access: RO
	11	**Reserved**
	10:9	**SPARE10_9** Default Value: 00b Access: RO
	8	**GMM Disable** Default Value: 0b Access: RO
	7	**Reserved**
	6:4	**DDR3 Maximum Frequency Capability** Default Value: 000b Access: RO

CAPID0_B_0_2_0_PCI - Mirror of Capabilities B

	3	**SPARE3** Default Value: 0b Access: RO
	2	**DDR4 DSKU Enable** Default Value: 0b Access: RO
	1	**Dual PEG Force x1 when VGA Enabled** Default Value: 0b Access: RO
	0	**Single PEG Force x1 when VGA Enabled** Default Value: 0b Access: RO

Mirror of Device Enable

DEVEN0_0_2_0_PCI - Mirror of Device Enable

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x000084BF
Size (in bits):	32
Address:	00054h

Mirror of DEVEN_0_0_0_PCI.

DWord	Bit	Description
0	15	**Device 8 Enable** Default Value: 1b Access: RO
	14	**Chap Enable** Default Value: 0b Access: RO
	13	**Device 6 Enable** Default Value: 0b Access: RO
	12:11	**Reserved** Format: MBZ
	10	**Device 5 Enable** Default Value: 1b Access: RO
	9:8	**Reserved** Format: MBZ
	7	**Device 4 Enable** Default Value: 1b Access: RO
	6	**Reserved** Format: MBZ
	5	**Device 3 enable for Display HD Audio** Default Value: 1b Access: RO

DEVEN0_0_2_0_PCI - Mirror of Device Enable

	4	**Internal Graphics Engine** Default Value: 1b Access: RO 0: Bus 0 Device 2 is disabled and hidden 1: Bus 0 Device 2 is enabled and visible This bit will be set to 0b and remain 0b if Device 2 capability is disabled.
	3	**PEG10 Enable** Default Value: 1b Access: RO
	2	**PEG11 Enable** Default Value: 1b Access: RO
	1	**PEG12 Enable** Default Value: 1b Access: RO
	0	**Host Bridge** Default Value: 1b Access: RO

Mirror of DSMBASE

DSMB - Mirror of DSMBASE		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	090A0h	
DSM Base		
DWord	**Bit**	**Description**
0	31:20	**DSM Base Lower 32 Bits** Access: RO This register contains bits 31 to 20 of the base address of stolen DRAM memory. BIOS determines the base of graphics stolen memory by subtracting the graphics stolen memory size (PCI Device 0 offset 52 bits 6:4) from TOLUD (PCI Device 0 offset BC bits 31:20).
	19:0	**Spares** Access: RO

Mirror of EMRR Base LSB

EMRRBASE_LSB - Mirror of EMRR Base LSB		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	09200h	
Mirror of EMRR Base		
DWord	**Bit**	**Description**
0	31:12	**EMRR Base LSB** Access: RO EMRR Base Value.
	11:0	**Spares** Access: RO

Mirror of EMRR Base MSB

EMRRBASE_MSB - Mirror of EMRR Base MSB			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	09204h		
Mirror of EMRR Base			
DWord	**Bit**	**Description**	
0	31:7	**Spares**	
		Access:	RO
	6:0	**EMRR Base MSB**	
		Access:	RO
		EMRR Base Value.	

Mirror of EU Disable Fuses - Register0

MIRROR_EU_DISABLE0 - Mirror of EU Disable Fuses - Register0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000 [KBL]	
Size (in bits):	32	
Address:	09134h	
DWord	**Bit**	**Description**
0	31:0	**EU Disable Fuses** Access: RO Slice0 - Subslice0 = Register0[7:0] Slice0 - Subslice1 = Register0[15:8] Slice0 - Subslice2 = Register0[23:16] Slice0 - Subslice3 = Register0[31:24]

Mirror of EU Disable Fuses - Register1

MIRROR_EU_DISABLE1 - Mirror of EU Disable Fuses - Register1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000 [KBL]	
Size (in bits):	32	
Address:	09138h	
DWord	**Bit**	**Description**
0	31:0	**EU Disable Fuses** Access: RO Slice1 - Subslice0 = Register1[7:0] Slice1 - Subslice1 = Register1[15:8] Slice1 - Subslice2 = Register1[23:16] Slice1 - Subslice3 = Register1[31:24]

Mirror of EU Disable Fuses - Register2

MIRROR_EU_DISABLE2 - Mirror of EU Disable Fuses - Register2		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000 [KBL]	
Size (in bits):	32	
Address:	0913Ch	
DWord	**Bit**	**Description**
0	31:0	**EU Disable Fuses** Access: RO Slice2 - Subslice0 = Register2[7:0] Slice2 - Subslice1 = Register2[15:8] Slice2 - Subslice2 = Register2[23:16] Slice1 - Subslice3 = Register2[31:24]

Mirror of FUSE1 Control DW

FUSE1 - Mirror of FUSE1 Control DW

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	0911Ch

DWord	Bit	Description	
0	31:25	**Spares**	
		Access:	RO
	24	**EU DP DISABLE**	
		Access:	RO
	23	**Reserved**	
	22	**Reserved**	
	21	**Reserved**	
	20	**Reserved**	
	19	**Reserved**	
	18	**Reserved**	
	17:16	**Spares1**	
		Access:	RO
	15	**Authentication Bypass**	
		Access:	RO
	14	**Reserved**	
	13	**Spares2**	
		Access:	RO
	12	**Reserved**	
	11	**Render Disable**	
		Access:	RO
	10:9	**Spares3**	
		Access:	RO
	8	**VME IME Enable**	
		Access:	RO
	7	**VME CRE Enable**	
		Access:	RO

FUSE1 - Mirror of FUSE1 Control DW		
	6:5	**Media Decode** Access: RO Applicable to Media - Fuse to disable VIN from processing media_objs or turn off the entire crclk tree trunk.
	4	**Disable GT3 Slice Shutdown** Access: RO N/A -- Not used by GT hardware: This fuse is actually enforced by the PCU; it is reflected here for driver information only.
	3	**Reserved**
	2	**Spares4** Access: RO
	1:0	**Media Encode** Access: RO Applicable to Media - One fuse to disable VIN from processing Pak_obj. Second fuse to disable VME.

Mirror of FUSE2 Control DW

FUSE2 - Mirror of FUSE2 Control DW

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	09120h

FUSE2 Control DW

DWord	Bit	Description
0	31:29	**GT SKU Fuse** Access: RO GT SKU Fuse Bits See project specific configuration table for possible values.
	28	**Spares** Access: RO
	27:25	**GT Slice Enable Fuse** Access: RO Slice Enables Bit25 - Slice0 Enable Bit26 - Slice1 Enable Bit27 - Slice2 Enable See project specific configuration table for possible values.
	24	**Spares1** Access: RO
	23:20	**GT Subslice Disable Fuse** Access: RO Subslice Disable Bits Bit 20 - Subslice0 Disable Bit 21 - Subslice1 Disable Bit 22 - Subslice2 Disable Bit 23 - Subslice3 Disable See project specific configuration table for possible values.
	19:18	**GT VDBox and VEBox Configuration Fuse** Access: RO VDBox and VEbox Configurations: 00b = Both VDBOXes and VEBOXes enabled 01b = VDBOX1 and VEBOX1 enabled (GT1,2) 10b = VDBOX0 and VEBOX0 enabled (GT1,2) See project specific configuration table for possible values.

FUSE2 - Mirror of FUSE2 Control DW		
	17:16	**Spares3** Access: RO
	15:0	**Capability Fuse** Fixed Definitions within Capability Fuse: Bit 2: Pre-production/post-production fuse. 0b : Pre-Production. Pre or Post Production quality FW will run 1b : Post Production.only Production quality FW will run Other bits defined by SW PDT. Please refer to Project Specific SW PDT for definition/values for these bits.

Mirror of Global Command Register

GCMD - Mirror of Global Command Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	090CCh

DWord	Bit	Description
0	31	**Translation Enable** Access: RO Software writes to this field to request hardware to enable/disable DMA-remapping hardware. 0: Disable DMA-remapping hardware. 1: Enable DMA-remapping hardware. Hardware reports the status of the translation enable operation through the TES field in the Global Status register. Before enabling (or re-enabling) DMA-remapping hardware through this field, software must: • Setup the DMA-remapping structures in memory. • Flush the write buffers (through WBF field), if write buffer flushing is reported as required. • Set the root-entry table pointer in hardware (through SRTP field). • Perform global invalidation of the context-cache and global invalidation of IOTLB • If advanced fault logging supported, setup fault log pointer (through SFL field) and enable advanced fault logging (through EAFL field). Refer to Section 9 for detailed software requirements. There may be active DMA requests in the platform when software updates this field. Hardware must enable or disable remapping logic only at deterministic transaction boundaries, so that any in-flight transaction is either subject to remapping or not at all. Hardware implementations supporting DMA draining must drain any in-flight translated DMA read/write requests queued within the root complex before completing the translation enable command and reflecting the status of the command through the TES field in the GSTS_REG. Value returned on read of this field is undefined.
	30	**Set Root Table Pointer** Access: RO Software sets this field to set/update the root-entry table pointer used by hardware. The root-entry table pointer is specified through the Root-entry Table Address register. Hardware reports the status of the "root table pointer set" operation through the RTPS field in the Global Status register. The root table pointer set operation must be performed before enabling or re-enabling (after disabling) DMA remapping through the TE field. After a "root table pointer set" operation, software must globally invalidate the context cache and

GCMD - Mirror of Global Command Register

		then globally invalidate the IOTLB. This is required to ensure hardware uses only the remapping structures referenced by the new root table pointer, and not any stale cached entries. While DMA remapping is active, software may update the root table pointer through this field. However, to ensure valid in-flight DMA requests are deterministically remapped, software must ensure that the structures referenced by the new root table pointer are programmed to provide the same remapping results as the structures referenced by the previous root-table pointer. Clearing this bit has no effect. The value returned on a read of this field is undefined.
	29	**Set Fault Log** Access: RO This field is valid only for implementations supporting advanced fault logging. Software sets this field to request hardware to set/update the fault-log pointer used by hardware. The fault-log pointer is specified through Advanced Fault Log register. Hardware reports the status of the fault log set operation through the FLS field in the Global Status register. The fault log pointer must be set before enabling advanced fault logging (through EAFL field). Once advanced fault logging is enabled, the fault log pointer may be updated through this field while DMA remapping is active. Clearing this bit has no effect. The value returned on read of this field is undefined.
	28	**Enable Fault Logging** Access: RO This field is valid only for implementations supporting advanced fault logging. Software writes to this field to request hardware to enable or disable advanced fault logging. 0: Disable advanced fault logging. In this case, translation faults are reported through the Fault Recording registers. 1: Enable use of memory-resident fault log. When enabled, translation faults are recorded in the memory-resident log. The fault log pointer must be set in hardware (through SFL field) before enabling advanced fault logging. Hardware reports the status of the advanced fault logging enable operation through the AFLS field in the Global Status register. Value returned on read of this field is undefined.
	27	**Write Buffer Flush** Access: RO This bit is valid only for implementations requiring write buffer flushing. Software sets this field to request hardware to flush the root-complex internal write buffers. This is done to ensure any updates to the memory-resident remapping structures are not held in any internal write posting buffers. Refer to Section 11.1 for details on write-buffer flushing requirements. Hardware reports the status of the write buffer flushing operation through the WBFS field in the Global Status register. Clearing this bit has no effect. Value returned on read of this field is undefined.

GCMD - Mirror of Global Command Register

	26	**Queued Invalidation Enable** Access: RO This field is valid only for implementations supporting queued invalidations. Software writes to this field to enable or disable queued invalidations. 0: Disable queued invalidations. 1: Enable use of queued invalidations. Hardware reports the status of queued invalidation enable operation through QIES field in the Global Status register. Refer to Section 6.2.2 for software requirements for enabling/disabling queued invalidations. The value returned on a read of this field is undefined.
	25	**Interrupt Remapping Enable** Access: RO This field is valid only for implementations supporting interrupt remapping. 0: Disable interrupt-remapping hardware 1: Enable interrupt-remapping hardware Hardware reports the status of the interrupt remapping enable operation through the IRES field in the Global Status register. There may be active interrupt requests in the platform when software updates this field. Hardware must enable or disable interrupt-remapping logic only at deterministic transaction boundaries, so that any in-flight interrupts are either subject to remapping or not at all. Hardware implementations must drain any in-flight interrupts requests queued in the Root-Complex before completing the interrupt-remapping enable command and reflecting the status of the command through the IRES field in the Global Status register. The value returned on a read of this field is undefined.
	24	**Set Interrupt Remap Table Pointer** Access: RO This field is valid only for implementations supporting interrupt-remapping. Software sets this field to set/update the interrupt remapping table pointer used by hardware. The interrupt remapping table pointer is specified through the Interrupt Remapping Table Address register. Hardware reports the status of the interrupt remapping table pointer set operation through the IRTPS field in the Global Status register. The interrupt remap table pointer set operation must be performed before enabling or re-enabling (after disabling) interrupt-remapping hardware through the IRE field. After an interrupt remap table pointer set operation, software must globally invalidate the interrupt entry cache. This is required to ensure hardware uses only the interrupt-remapping entries referenced by the new interrupt remap table pointer, and not any stale cached entries. While interrupt remapping is active, software may update the interrupt remapping table pointer through this field. However, to ensure valid in-flight interrupt requests are deterministically remapped, software must ensure that the structures referenced by the new interrupt remap table pointer are programmed to provide the same remapping results as the structures referenced by the previous interrupt remap table pointer. Clearing this bit has no effect. The value returned on a read of this field is undefined.

GCMD - Mirror of Global Command Register

	23	**Compatibility Format Interrupt** Access: RO This field is valid only for Intel(R)64 implementations supporting interrupt-remapping. Software writes to this field to enable or disable Compatibility Format interrupts on Intel(R)64 platforms. The value in this field is effective only when interrupt-remapping is enabled and Legacy Interrupt Mode is active. 0: Block Compatibility format interrupts. 1: Process Compatibility format interrupts as pass-through (bypass interrupt remapping). Hardware reports the status of updating this field through the CFIS field in the Global Status register. Refer to Section 5.4.1 for details on Compatibility Format interrupt requests. The value returned on a read of this field is undefined. This field is not implemented on Itanium(TM) implementations.
	22:0	**Spares** Access: RO

Mirror of GMCH Graphics Control

MGGC0_0_2_0_PCI - Mirror of GMCH Graphics Control

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000500
Size (in bits):	16
Address:	00050h

Mirror of GGC_0_0_0_PCI.
All the bits in this register are Intel TXT lockable.

DWord	Bit	Description
0	15:8	**Graphics Mode Select** Default Value: 00000101b Access: RO This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled. BIOS Requirement: BIOS must not set this field to 0h if IVD (bit 1 of this register) is 0. BIOS Requirement: Given new sizes allow down to 8MB allocation, BIOS has to ensure there is sufficient space for WOPCM and basic GFX Stolen functions. 00h:0MB 01h:32MB 02h:64MB 03h:96MB 04h:128MB 05h:160MB (default) 06h:192MB 07h:224MB 08h:256MB 09h:288MB 0Ah:320MB 0Bh:352MB 0Ch:384MB 0Dh:416MB 0Eh:448MB 0Fh:480MB 10h:512MB 11h - 1Fh: Reserved 20h:1024MB 21h - 2Fh: Reserved 30h:1536MB

MGGC0_0_2_0_PCI - Mirror of GMCH Graphics Control

		31h - 3Fh: Reserved 40h: 2048MB 41h - EFh: Reserved F0h: 4MB F1h: 8MB F2h: 12MB F3h: 16MB F4h: 20MB F5h: 24MB F6h: 28MB F7h: 32MB F8h: 36MB F9h: 40MB FAh: 44MB FBh: 48MB FCh: 52MB FDh: 56MB FEh: 60MB FFh: Reserved Hardware functionality in case of programming this value to Reserved is not guaranteed.
	7:6	**GTT Graphics Memory Size** Default Value: 00b Access: RO This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. GSM is assumed to be a contiguous physical DRAM space with DSM, and BIOS needs to allocate a contiguous memory chunk. Hardware will derive the base of GSM from DSM only using the GSM size programmed in the register. Hardware functionality in case of programming this value to Reserved is not guaranteed. 0x0: No Preallocated Memory 0x1: 2MB of Preallocated Memory 0x2: 4MB of Preallocated Memory 0x3: 8MB of Preallocated Memory
	5:3	**Reserved** Format: MBZ
	2	**Versatile Acceleration Mode Enable** Default Value: 0b Access: RO Enables the use of the iGFX engines for Versatile Acceleration. 1 - iGFX engines are in Versatile Acceleration Mode. Device 2 Class Code is 048000h. 0 - iGFX engines are in iGFX Mode. Device 2 Class Code is 030000h.

MGGC0_0_2_0_PCI - Mirror of GMCH Graphics Control

	1	**IGD VGA Disable** Default Value: 0b Access: RO 0: Enable. Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00. 1: Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub- Class Code field within Device 2 function 0 Class Code register is 80. BIOS Requirement: BIOS must not set this bit to 0 if the GMS field pre-allocates no memory. This bit MUST be set to 1 if Device 2 is disabled either via a fuse or fuse override (CAPID0_A[IGD] = 1) or via a register (DEVEN[3] = 0).
	0	**GGC Lock** Default Value: 0b Access: RO When set to 1b, this bit will lock all bits in this register.

Mirror of GMCH Graphics Control Register

MGGC - Mirror of GMCH Graphics Control Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000300
Size (in bits):	32
Address:	09094h

Mirror of GMCH Graphics Control Register

DWord	Bit	Description
0	31:16	**Spares** Access: RO
	15:8	**Graphics Mode Select** Default Value: 3h Access: RO This field selects the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. 0h: No memory pre-allocated. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub-Class Code field within Device 2 function 0 Class Code register is 80. 1h-4h: Reserved. 5h-Dh: DVMT (UMA) mode, memory pre-allocated for frame buffer, in quantities as shown in the Encoding table. Eh-Fh: Reserved. NOTE: This register is locked and becomes Read Only when the D_LCK bit in the SMRAMC register is set. This register is also LT lockable. Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled. BIOS Requirement: BIOS must not set this field to 0h if IVD (bit 1 of this register) is 0.
	7:6	**GTT Graphics Memory Size** Access: RO This field selects the amount of Main Memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. GSM is assumed to be a contiguous physical DRAM space with DSM, and BIOS needs to allocate a contiguous memory chunk. Hardware derives the base of GSM from DSM only using the GSM size programmed in the register. 0h: No memory pre-allocated. GTT cycles (Mem and IO) are not claimed. 1h: 2 MB of memory pre-allocated for GTT. 2h: 4 MB of memory pre-allocated for GTT.

MGGC - Mirror of GMCH Graphics Control Register

		3h: 8 MB of memory pre-allocated for GTT. Hardware functionality in case of programming this value to Reserved is not guaranteed. This register is locked and becomes Read Only when the D_LCK bit in the SMRAMC register is set.
	5:3	**Spares2** Access: RO
	2	**Versatile Acceleration Mode Enable** Access: RO Enables the use of the iGFX engines for Versatile Acceleration. 1 - iGFX engines are in Versatile Acceleration Mode. Device 2 Class Code is 048000h. 0 - iGFX engines are in iGFX Mode. Device 2 Class Code is 030000h.
	1	**IGD VGA Disable** Access: RO 0: Enable. Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00. 1: Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub-Class Code field within Device 2 function 0 Class Code register is 80. BIOS Requirement: BIOS must not set this bit to 0 if the GMS field (bits 6:4 of this register) pre-allocates no memory. This bit MUST be set to 1 if Device 2 is disabled either via a fuse or fuse override (CAPID0[46] = 1) or via a register (DEVEN[3] = 0). This register is locked by LT lock.
	0	**Spares3** Access: RO

Mirror of Graphics Translation Table and Memory Mapped Range Address

GTTMMADR_LSB - Mirror of Graphics Translation Table and Memory Mapped Range Address

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	09124h

This register requests allocation for the combined Graphics Translation Table Modification Range and Memory Mapped Range. The range requires 4 MB combined for MMIO and Global GTT aperture, with 2MB of that used by MMIO and 2MB used by GTT. GTTADR begins at (GTTMMADR + 2 MB) while the MMIO base address is the same as GTTMMADR.

For the Global GTT, this range is defined as a memory BAR in graphics device config space. It is an alias into which software is required to write Page Table Entry values (PTEs). Software may read PTE values from the global Graphics Translation Table (GTT). PTEs cannot be written directly into the global GTT memory area.

The device snoops writes to this region in order to invalidate any cached translations within the various TLBs implemented on-chip. There are some exceptions to this - see GTT-TLB in the Programming Interface chapter.

The allocation is for 4MB and the base address is defined by bits [38:22].

DWord	Bit	Description
0	31:22	**Memory Base Address (LSB - 31:22 of 38:22)** Access: RO Set by the OS, these bits correspond to address signals [38:22]. 4MB combined for MMIO and Global GTT table aperture (2MB for MMIO and 2 MB for GTT).
	21:4	**Spares** Access: RO
	3	**Prefetchable Memory** Access: RO Hardwired to 0 to prevent prefetching.
	2:1	**Memory Type** Access: RO 00b: To indicate 32 bit base address. 01b: Reserved. 10b: To indicate 64 bit base address. 11b: Reserved.

GTTMMADR_LSB - Mirror of Graphics Translation Table and Memory Mapped Range Address

	0	**Memory I/O Space** Access: RO Hardwired to 0 to indicate memory space.

Mirror of Graphics Translation Table and Memory Mapped Range Address UDW

GTTMMADR_MSB - Mirror of Graphics Translation Table and Memory Mapped Range Address UDW

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	09128h

This register requests allocation for the combined Graphics Translation Table Modification Range and Memory Mapped Range. The range requires 4 MB combined for MMIO and Global GTT aperture, with 2MB of that used by MMIO and 2MB used by GTT. GTTADR begins at (GTTMMADR + 2 MB) while the MMIO base address is the same as GTTMMADR.

For the Global GTT, this range is defined as a memory BAR in graphics device config space. It is an alias into which software is required to write Page Table Entry values (PTEs). Software may read PTE values from the global Graphics Translation Table (GTT). PTEs cannot be written directly into the global GTT memory area.

The device snoops writes to this region in order to invalidate any cached translations within the various TLBs implemented on-chip. There are some exceptions to this - see GTT-TLB in the Programming Interface chapter.

The allocation is for 4MB and the base address is defined by bits [38:22].

DWord	Bit	Description
0	31:7	**Spares** Access: RO
	6:0	**Memory Base Address (MSB - 38:32 of 38:22)** Access: RO Set by the OS, these bits correspond to address signals [38:22]. 4MB combined for MMIO and Global GTT table aperture (2MB for MMIO and 2 MB for GTT).

Mirror of GSMBASE

GSMB - Mirror of GSMBASE

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	090A4h

This register contains the base address of stolen DRAM memory for the GTT. BIOS determines the base of GTT stolen memory by subtracting the GTT graphics stolen memory size (PCI Device 0 offset 52 bits 11:8) from the Graphics Base of Data Stolen Memory (PCI Device 0 offset B0 bits 31:20).

DWord	Bit	Description
0	31:20	**GSM Base** Access: RO This register contains the base address of stolen DRAM memory for the GTT. BIOS determines the base of GTT stolen memory by subtracting the GTT graphics stolen memory size (PCI Device 0 offset 52 bits 11:8) from the Graphics Base of Data Stolen Memory (PCI Device 0 offset B0 bits 31:23).
	19:0	**Spares** Access: RO

Mirror of PCICMD MAE/BME

PCICMD - Mirror of PCICMD MAE/BME

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	0912Ch

DWord	Bit	Description
0	31:11	**Spare** Access: R/W
	10	**Interrupt Disable** Access: R/W This bit disables the device from asserting INTx#. 0: Enable the assertion of this device's INTx# signal. 1: Disable the assertion of this device's INTx# signal. DO_INTx messages are not sent to DMI. GSA Implementation: When 1, blocks the sending of an MSI interrupt and blocks the sending of a Line interrupt. (The interrupt status is not blocked from being reflected in the INTSTS bit.) When 0, permits the sending of an MSI interrupt or Line interrupt.
	9	**Fast Back to Back** Access: R/W Not Implemented. Hardwired to 0.
	8	**SERR Enable** Access: R/W Not Implemented. Hardwired to 0.
	7	**Address/Data Stepping Enable** Access: R/W Not Implemented. Hardwired to 0.
	6	**Parity Error Enable** Access: R/W Not Implemented. Hardwired to 0. Since the IGD belongs to the category of devices that does not corrupt programs or data in system memory or hard drives, the IGD ignores any parity error that it detects and continues with normal operation.
	5	**Video Pallete Snooping** Access: R/W This bit is hardwired to 0 to disable snooping.

PCICMD - Mirror of PCICMD MAE/BME

	4	**Memory Write and Invalidate Enable** Access: R/W Hardwired to 0. The IGD does not support memory write and invalidate commands.
	3	**Special Cycle Enable** Access: R/W This bit is hardwired to 0. The IGD ignores Special cycles.
	2	**Bus Master Enable** Access: R/W 0: Disable IGD bus mastering. 1: Enable the IGD to function as a PCI compliant master. GSA Implementation: When 0, blocks the sending of MSI interrupts. When 1, permits the sending of above. (Note: See descriptions of the INTDIS, MSE, and INTSTS bits.)
	1	**Memory Access Enable** Access: R/W This bit controls the IGD's response to memory space accesses. 0: Disable. 1: Enable.
	0	**I/O Access Enable** Access: R/W This bit controls the IGD's response to I/O space accesses. 0: Disable. 1: Enable.

Misc Clocking / Reset Control Registers

MISCCPCTL - Misc Clocking / Reset Control Registers

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000002 [KBL]
Size (in bits):	32
Address:	09424h

Miscellaneous Clocking / Reset Control Registers.

DWord	Bit	Description
0	31:11	**Bonus ECO bits** Access: R/W Bonus ECO bits
	10	**DOP clock gating enable for Media ampler clks** Access: R/W Controls the Enabling of the DOP-level Media sampler (scmsclk) Clock Gating via PM event messages 1 - Clock gating is enabled 0 - Clock gating is disabled
	9	**DOP clock gating enable for SFC media2 clks** Access: R/W Controls the Enabling of the DOP-level SFC (csfcclk) Clock Gating in media2 via PM event messages 1 - Clock gating is enabled 0 - Clock gating is disabled
	8	**DOP clock gating enable for SFC media1 clks** Access: R/W Controls the Enabling of the DOP-level SFC (csfcclk) Clock Gating in media1 via PM event messages 1 - Clock gating is enabled 0 - Clock gating is disabled
	7	**DOP clock gating enable for VEbox clks** Access: R/W Controls the Enabling of the DOP-level Vebox (cvclk) Clock Gating via PM event messages 1 - Clock gating is enabled 0 - Clock gating is disabled

MISCCPCTL - Misc Clocking / Reset Control Registers

	6	**DOP clock gating enable for Media clocks** Access: R/W Controls the Enabling of the DOP-level Media (cmclk) Clock Gating via PM event messages 1 - Clock gating is enabled 0 - Clock gating is disabled
	5	**DOp clock gate enable for Media1 Clocks** Access: R/W Controls the Enabling of the DOP-level Render (cmclk for 2nd media block) Clock Gating via PM event messages 1 - Clock gating is enabled 0 - Clock gating is disabled
	4	**Reserved**
	3	**Reserved**
	2	**DOP clock gating Enable for Fix clocks (cfclk)** Access: R/W Controls the Enabling of the DOP-level Render (cfclk/cf2xclk) Clock Gating via PM event messages 1 - Clock gating is enabled 0 - Clock gating is disabled
	1	**L1 Clock Ungate Enabling Control During Reset** Default Value: 1b Access: R/W Control to enable/disable L1 clock gating during soft resets and FLR reset processing ‘1' : disable L1 clock gating during soft resets and FLR ‘0' : enable L1 clock gating during soft resets and FLR (default op)
	0	**DOP Clock Gating Enable for Render Clocks** Access: R/W Controls the Enabling of the DOP-level Render (crclk/cr2xclk) Clock Gating via PM event messages 1 - Clock gating is enabled 0 - Clock gating is disabled

MISC CTX control register

MISCCTXCTL - MISC CTX control register		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0942Ch	
DWord	**Bit**	**Description**
0	31:1	**Reserved** Access: RO
	0	**Context Restore ACk indication from Csunit** Access: R/W Set Context Restore ACk indication from Csunit 1'b1 : Csunit has completed restoring CPunits adress space Once set, CPunit hardware clears this bit after sending the ctx save ack done message to CS 1'b0 : Csunit has NOT completed restoring CPunits adress space

Misc Reset Control Register

RSTCTL - Misc Reset Control Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	09420h

Miscellaneous reset control registers.

DWord	Bit	Description
0	31:4	**Reserved** Access: RO Reserved
	3:2	**Reset Staggering Period Control** Access: R/W Reset assertion staggering period between reset domains during FLR and soft-resets: 00: 6 csclk staggering reset assertion staggering 01: 12 cs clocks 10: 18 cs clocks 11: 24 cs clocks
	1:0	**Reset Residency Control** Access: R/W Reset assertion residency period for FLR and soft-resets. 00 : 8 cs clocks 01 : 16 cs clocks 10 : 32 cs clocks 11 : 64 cs clocks

MMCD Misc Control

MMCD_MISC_CTRL - MMCD Misc Control

Register Space:	MMIO: 0/2/0
Source:	BSpec
	0x8000003C
Size (in bits):	32
Address:	04DDCh

This register contains control bits for permute control line address, page faulting mode and cache control bits

DWord	Bit	Description
0	31	**Permute Compressed Line Address** Default Value: 1b Access: R/W Controls where the compressed line is written in memory 1'b0: Write to lower CL address, i.e bit[X]=0 1'b1: Write based on the hash selection as indicated by bit[27] (default)
	30	**Reserved**
	29	**Reserved**
	28	**Reserved**
	27	**Hash Select for Compressed Read/Write Address calculation** Default Value: 0b Access: R/W 1'b0: Legacy mode : Read/Write address computation will be done using a hash of Virtual address bits 6 to 11 bit[X] = bit[X] XOR bit[11] XOR bit[10] XOR bit[9] XOR bit[8] XOR bit[7] XOR bit[6] 1'b1: LLC/eLLC hot spotting avoidance mode : Read/Write address computation will be done using a hash of Virtual address bits 17 to 21 bit[X] = bit[X+1] XOR bit[17] XOR bit[18] XOR bit[19] XOR bit[20] XOR bit[21] Software needs to guarantee that the base address of the resource is aligned to 4MB or ensure that the virtual address is not changed between the passes for compressed surface handling
	26:14	**Reserved_1** Default Value: 0b Access: R/W
	13:11	**Page Faulting Mode** Default Value: 0b Access: R/W this field controls page faulting mode that will be used in the memory interface block for the given request coming from this surface 3'b000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved

MMCD_MISC_CTRL - MMCD Misc Control

	10:7	**Reserved_2** Default Value: 0b Access: R/W
	6	**Don't allocate on Miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM) 1'b0: Allocate on miss 1'b1: Do Not allocate on miss
	5:4	**Cache Replcament management** Default Value: 3h Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. If a particular allocation is done at youngest age 3 it tends to stay longer in cache as compared to older age allocation - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches 2'b11: Good chance of generating hits 2'b10: Poor chance of generating hits 2'b01: Don't change the LRU if it is a HIT 2'b00: Reserved
	3:2	**Target Cache** Default Value: 3h Access: R/W This field allows the choice of LLC vs eLLC for caching 2'b00: eLLC only 2'b01: LLC only 2'b10: LLC/eLLC allowed 2'b11: LLC/eLLC allowed
	1:0	**LLC/eDRAM Cacheability control** Default Value: 0b Access: R/W Memory type information used in LLC/eDRAM 2'b00: Use cacheability controls from page table/ UC with fence (if coherent cycle) 2'b01: Uncacheable(UC) - non-cacheable 2'b10: Writethrough (WT) 2'b11: Writeback (WB)

Mode Register for GAB

GAB_MODE - Mode Register for GAB

Register Space:	MMIO: 0/2/0
Source:	BlitterCS
Default Value:	0x00000000
Access:	r/w
Size (in bits):	32
Address:	220A0h-220A3h

The GAB_MODE register
contains information that controls configurations in the GAB.

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask
	15:6	**Reserved** Read/Write
	5:3	**BLB Arbitration Priority** Format: U3
	2:0	**BCS Arbitration Priority** Format: U3

Mode Register for GAC

GAC_MODE - Mode Register for GAC

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000 [KBL]
Access:	r/w
Size (in bits):	32
Address:	120A0h-120A3h
ShortName:	GAC_MODE

The GAC_MODE register contains information that controls configurations in the GAC.

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask
	15:1	**Reserved** Access: r/w
	0	**GACunit VCS Fence Performance fix Override** Format: Disable

Value	Name	Description
0	**[Default]**	Performance fix **enabled** to block client credits until VCS fence advances.
1		Performance fix to block credits until VCS fence advances, **disabled.** Fence will not block input traffic from clients and will advance only after ingress FIFOs are empty (Legacy behavior.)

Mode Register for GAFS

GAFS_MODE - Mode Register for GAFS

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	r/w
Size (in bits):	32
Trusted Type:	1
Address:	0212Ch

DWord	Bit	Description
0	31:16	**Mask Bits** Access: WO Format: Mask Masks: These bits serve as write enables for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.
	15:11	**Reserved** Format: PBC
	10	**Reserved** Format: PBC
	9	**Reserved**
	8:2	**Reserved** Format: PBC
	1:0	**Reserved** Format: PBC

Mode Register for Software Interface

MI_MODE - Mode Register for Software Interface

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	r/w
Size (in bits):	32
Address:	0209Ch-0209Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_RCSUNIT
Address:	1209Ch-1209Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_VCSUNIT0
Address:	1A09Ch-1A09Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_VECSUNIT
Address:	1C09Ch-1C09Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_VCSUNIT1
Address:	2209Ch-2209Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_BCSUNIT

The MI_MODE register contains information that controls software interface aspects of the Memory Interface function.

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask A 1 in a bit in this field allows the modification of the corresponding bit in Bits 15:0
	15	**Suspend Flush** Format: U1 Value 0h: No Delay **[Default]** — HW will not delay flush, this bit will get cleared by MI_SUSPEND_FLUSH as well

MI_MODE - Mode Register for Software Interface

1h	Delay Flush	Suspend flush is active

Programming Notes
This should only be written to from the ring using MI_SUSPEND_FLUSH. It is considered undefined if written by software through MMIO

14 **Reserved**

Source:	VideoCS, VideoCS2, VideoEnhancementCS, PositionCS
Exists If:	//VCS, VECS, POCS, BCS
Format:	PBC

14 **Reserved**

Source:	RenderCS
Format:	PBC

13 **Reserved**

Format:	PBC

12 **Reserved**

Format:	PBC

11 **Invalidate UHPTR enable**

Source:	RenderCS, VideoCS, VideoCS2, VideoEnhancementCS
Exists If:	//RCS, VCS, VECS, BCS
Format:	Enable

If bit set H/W clears the valid bit of UHPTR (2134h, bit 0) when current active head pointer is equal to UHPTR.

10 **Atomic Read Return for MI_COPY_MEM_MEM**

Format:	U1

Value	Name	Description
0h	Disable **[Default]**	Hardware does a regular memory fence write to complete the write to the destination address before moving to the next instruction.
1h	Enable	Hardware does Atomic Move with Read Return to complete the write to the destination address before moving to the next instruction.

9 **Rings Idle**

Format:	U1

Read Only Status bit

Value	Name	Description
0h	Not Idle **[Default]**	Parser not Idle or Ring Arbiter not Idle.
1h	Idle	Parser Idle and Ring Arbiter Idle.

MI_MODE - Mode Register for Software Interface

Programming Notes
Writes to this bit are not allowed.

8 Stop Rings

Format:	U1

Value	Name	Description
0h	**[Default]**	Normal Operation.
1h		Parser is turned off and Ring arbitration is turned off.

Programming Notes
Software must set this bit to force the Rings and Command Parser to Idle. Software must read a 1 in the Ring Idle bit after setting this bit to ensure that the hardware is idle.
Software must clear this bit for Rings to resume normal operation.

7:5 Reserved

Format:	PBC

4:2 Reserved

Source:	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS
Format:	PBC

4:1 Predicate Enable

Source:	RenderCS

This field gets set when "MI_SET_PREDICATE" command is parsed by render command streamer. Predicate Disable is the default mode of operation.

Value	Name	Description
0h	Predicate Disable	Predication is Disabled and RCS will process commands as usual.
1h	Predicate on Result2 clear	Following Commands will be NOOPED by RCS only if the MI_PREDICATE_RESULT_2 is clear.
2h	Predicate on Result2 set	Following Commands will be NOOPED by RCS only if the MI_PREDICATE_RESULT_2 is set.
3h	Predicate on Result clear	Following Commands will be NOOPED by RCS only if the MI_PREDICATE_RESULT is clear.
4h	Predicate on Result set	Following Commands will be NOOPED by RCS only if the MI_PREDICATE_RESULT is set.
5h	Predicate when two or more slices enabled	Following Commands will be NOOPED by RCS only when one slice is enabled, NOOPED when more than one slice is enabled.
6h	Predicate when one	Following Commands will be Executed by RCS only when two

MI_MODE - Mode Register for Software Interface

	or three slices enabled	slices are enabled, NOOPED when one or three slices are enabled.
7h	Predicate when one or two slices enabled	Following Commands will be Executed by RCS only when all the three slices are enabled, NOOPED when less than three slices are enabled.
8h, 9h, Ah	Reserved	
Bh, Ch, Dh, Eh	Reserved	
Fh	Predicate Always	Following Commands will be NOOPED by RCS unconditionally.

Programming Notes
SW must use MI_SET_PREDICATE instead of MMIO access.

1 **Reserved**

Source:	VideoCS, VideoCS2, VideoEnhancementCS
Format:	PBC

1 **Bypass Fence Write**

Source:	BlitterCS

If set, this bit will bypass all writes during flushes, independent of programming. This includes post-sync op bits, the implicit TLB invalidate write (set in GFX_MODE[13]), and sync flush fences. *Note this is only intended for work-arounds*

Value	Name
0	Normal Operation
1	Bypass

0 **Reserved**

Source:	CommandStreamer
Format:	PBC

MTRR Capability Register 0

MTRR_CR_0 - MTRR Capability Register 0

Register Space:	MMIO: 0/2/0
Default Value:	0x0000050A
Size (in bits):	32
Address:	0F100h

Register to define MTRR - range register capabilities.

DWord	Bit	Description
0	31:11	**Reserved** Default Value: 00000000000000000000b Access: RO
	10	**Write Combining Support** Default Value: 1b Access: RO 0: Write Combining (WC) memory type is not supported. 1: Write Combining (WC) memory type is supported. GFX Implementation: More details on memory type section however WC support in GFX looks like streamlining non-cacheable accesses. This is the existing UC concept used in GFX architecture.
	9	**Reserved** Default Value: 0b Access: RO
	8	**Fixed Range MTRRs Support** Default Value: 1b Access: RO 0: No Fixed range MTRRs are supported. 1: Fixed Range MTRRs (IA32_MTRR_FIX64K_00000 through IA32_MTRR_FIX4K_0F8000) are supported.
	7:0	**Variable Range MTRR Count** Default Value: 0Ah Access: RO Indicates the number of variable ranges implemented.

MTRR Capability Register 1

MTRR_CR_1 - MTRR Capability Register 1		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F104h	
Register to define MTRR - range register capabilities		
DWord	**Bit**	**Description**
0	31:0	**MTRR Capability Register 1 Reserved** Default Value: 00000000h Access: RO Bit[63:32]: Reserved.

MTRR Default Type Register 0

MTRR_DT_0 - MTRR Default Type Register 0

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0F108h

Register to define MTRR - range register capabilities.

DWord	Bit	Description
0	31:12	**Reserved** Default Value: 00000000000000000000b Access: RO
	11	**Reserved**
	10	**Fixed Range MTRR Enable/Disable** Default Value: 0b Access: R/W 0: Disable fixed-range MTRRs. 1: Enable fixed-range MTRRs. When the fixed-range MTRRs are enabled, they take priority over the variable-range MTRRs when overlaps in ranges occur. If the fixed-range MTRRs are disabled, the variable range MTRRs can still be used and can map the range ordinarily covered by the fixed-range MTRRs. GFX Implementation: GFX uses this field as a specific enable/disable for fixed range MTRRs.
	9:8	**Reserved** Default Value: 00b Access: RO
	7:0	**Default Memory Type** Default Value: 00h Access: R/W Indicates default memory type used for physical memory address ranges that do not have a memory type specified for them by an MTRR. Legal values for this field are 0, 1, 4, 5, and 6. GFX Implementation: GFX uses this field to assign memory regions that are not assigned as part of the fixed and variable range registers.

MTRR Default Type Register 1

MTRR_DT_1 - MTRR Default Type Register 1		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F10Ch	
Register to define MTRR - range register capabilities.		
DWord	**Bit**	**Description**
0	31:0	**MTRR Default Type Register 1 Reserved** Default Value: 00000000h Access: RO Bit[63:32]: Reserved.

MT Virtual Page Address Registers

MTTLB_VA - MT Virtual Page Address Registers

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	04800h-04803h

DWord	Bit	Description
0	31:12	**Address** Format: GraphicsAddress[31:12] Page virtual address.
	11:0	**Reserved** Format: MBZ

MT Virtual Page Address Registers

MTTLB_VA - MT Virtual Page Address Registers

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	04800h-04803h

DWord	Bit	Description
0	31:12	**Address** Format: GraphicsAddress[31:12] Page virtual address.
	11:0	**Reserved** Format: MBZ

Multi Size Aperture Control

MSAC_0_2_0_PCI - Multi Size Aperture Control

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000001
Size (in bits):	8
Address:	00062h

This register determines the size of the graphics memory aperture (GMADR) in function 0 and in the trusted space, and affects certain bits of the GMADR register.
Bits [4:0] 00000b: 128MB, GMADR[26:4] is hardwired to all 0
Bits [4:0] 00001b: 256MB, GMADR[27:4] overriden to all 0
Bits [4:0] 00010b: illegal (hardware will treat this as 00011b)
Bits [4:0] 00011b: 512MB, GMADR[28:27] overriden to all 0
Bits [4:0] 00100-00110b: illegal (hardware will treat this as 00111b)
Bits [4:0] 00111b: 1024MB, GMADR[29:27] overriden to all 0
Bits [4:0] 01000-01110b: illegal (hardware will treat this as 01111b)
Bits [4:0] 01111b: 2048MB, GMADR[30:27] overriden to all 0
Bits [4:0] 10000-11110b: illegal (hardware will treat this as 11111b)
Bits [4:0] 11111b: 4096MB, GMADR[31:27] overriden to all 0
This register is Intel TXT locked, becomes read-only when trusted environment is launched.

DWord	Bit	Description
0	7:5	**Reserved R/W** Default Value: 000b Access: R/W Scratch Bits
	4	**Untrusted Aperture Size Bit 4** Default Value: 0b Access: R/W Key
	3	**Untrusted Aperture Size Bit 3** Default Value: 0b Access: R/W Key
	2	**Untrusted Aperture Size Bit 2** Default Value: 0b Access: R/W Key
	1	**Untrusted Aperture Size Bit 1** Default Value: 0b Access: R/W Key

MSAC_0_2_0_PCI - Multi Size Aperture Control			
	0	**Untrusted Aperture Size Bit 0**	
		Default Value:	1b
		Access:	R/W Key

NDE_RSTWRN_OPT

NDE_RSTWRN_OPT

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	46408h-4640Bh
Name:	North Display Reset Warn Options
ShortName:	NDE_RSTWRN_OPT
Power:	PG0
Reset:	global

This register is used to control the display behavior on receiving a Reset Warning.

DWord	Bit	Description
0	31:7	**Reserved** Format: MBZ
	6	**Reserved** Format: MBZ
	5	**Reserved**
	4	**RST PCH Handshake En** This field enables the handshake with PCH display when processing the reset. This applies to all types of DE resets. By default it is disabled and the north display will not wait for south display to acknowledge the reset. **Value / Name** 0b: Disable 1b: Enable **Programming Notes** This must be set to 1b as part of the display initialization sequence.
	3:0	**Reserved**

NFADFL Count Current EI

NFADFL_EVENT0 - NFADFL Count Current EI		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00DA4h	
This register mirrors an accumulating count for Unslice Frequency COntrol Event 0. It is enabled by configuration bits in GPMunit and SPMunits. Note that count is never cleared and delta should be calculated by sampling the initial register value at the start and subtracting that value off from the final sample value.		
DWord	**Bit**	**Description**
0	31:0	**NFADFL Event Count in Current EI** Access: RO

NFADFL Count Previous EI

NFADFL_EVENT1 - NFADFL Count Previous EI		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00DA8h	
This register mirrors an accumulating count for Unslice Frequency COntrol Event 0. It is enabled by configuration bits in GPMunit and SPMunits. Note that count is never cleared and delta should be calculated by sampling the initial register value at the start and subtracting that value off from the final sample value.		
DWord	**Bit**	**Description**
0	31:0	**NFADFL Event Count in Previous EI** Access: RO

NOP Identification Register

NOPID - NOP Identification Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Trusted Type:	1
Address:	02094h-02097h
Name:	NOP Identification Register
ShortName:	NOPID_RCSUNIT
Address:	12094h-12097h
Name:	NOP Identification Register
ShortName:	NOPID_VCSUNIT0
Address:	1A094h-1A097h
Name:	NOP Identification Register
ShortName:	NOPID_VECSUNIT
Address:	1C094h-1C097h
Name:	NOP Identification Register
ShortName:	NOPID_VCSUNIT1
Address:	22094h-22097h
Name:	NOP Identification Register
ShortName:	NOPID_BCSUNIT

The NOPID register contains the Noop Identification value specified by the last MI_NOOP instruction that enabled this register to be updated.

DWord	Bit	Description
0	31:22	**Reserved** Format: MBZ
	21:0	**Reserved**

Null Range 0 Base Register

NULL_BASE_0 - Null Range 0 Base Register

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	04050h

DWord	Bit	Description
0	31:21	**Null Range Base Address** Default Value: 00000000000b Access: R/W Lock Base address contents of the Null Range that has to be checked against.
	20:2	**Reserved** Default Value: 00000000000000000b Access: RO
	1	**Null Range Register Lock** Default Value: 0b Access: R/W When set, The null range register is locked. Writes have no impact on the register and reads continue to return the contents. Note that enable and lock can be written in the same cycle, as lock taking effect, the accompanying update to the register will take effect as well.
	0	**Null Range Enable** Default Value: 0b Access: R/W Lock When set, The null range register is enabled. Hardware will detect the accesses falling into null range and treat then as invalid access where writes are dropped and reads are returned with all zero's.

Null Range 1 Base Register

NULL_BASE_1 - Null Range 1 Base Register		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04054h	
DWord	**Bit**	**Description**
0	31:7	**Reserved** Default Value: 00000000000000000000000b Access: RO
	6:0	**Null Range Base Address** Default Value: 0000000b Access: R/W Lock Base address contents of the Null Range that has to be checked against.

OA Interrupt Mask Register

OA_IMR - OA Interrupt Mask Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0xFFFFFFFF
Access:	R/W
Size (in bits):	32
Address:	02B20h

The OAIMR register is used by software to control whether OA generates an interrupt or not.

DWord	Bit	Description
0	31:29	**Reserved** Default Value: 7h Format: PBC
	28	**Mask Bit** 0h – Not Masked – May generate an interrupt 1h – Masked **[Default]** – Will not generate an interrupt
	27:0	**Reserved** Default Value: FFFFFFFh Format: PBC

OA TLB Control Register

OTCR - OA TLB Control Register

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0427Ch

DWord	Bit	Description
0	31:1	**Reserved** Default Value: 00000000000000000000000000000000b Access: RO
	0	**Invalidate TLBs on the corresponding Engine** Default Value: 0b Access: R/W SW writes 1 to invalidate the TLBs for the associated engine and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs. This bit is self clear.

Observation Architecture Buffer

OABUFFER - Observation Architecture Buffer

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000001 [KBL]
Size (in bits):	32
Address:	02B14h
Access:	R/W

This register is used to program the OA unit.

Programming Notes

This MMIO must be set before the OATAILPTR register and set after the OAHEADPTR register. This is to enable proper functionality of the overflow bit.

DWord	Bit	Description
0	31:6	**Report Buffer Offset** Format: GraphicsAddress[31:6] This field specifies 64B aligned GFX MEM address where the chap counter values are reported.
	5:3	**Inter Trigger Report Buffer Size** This field indicates the size of report buffer for time/event-based report trigger mechanisms. This field is programmed in terms of multiple of 128KB.

Value	Name	Description
0h	128 KB **[Default]**	All context considered
1h	256 KB	
2h	512 KB	
3h	1 MB	
4h	2 MB	
5h	4 MB	
6h	8 MB	
7h	16 MB	

	2	**OA Report Trigger Select**

Value	Name	Description
0		Level Report trigger
1		Edge Report trigger

	1	**Disable Overrun Mode** Format: Enable This field defines the mode of reporting for internal trigger/timer based reporting. When this bit

OABUFFER - Observation Architecture Buffer

is set, overrun does not lose reports but stops reporting.
Based on the head and tail pointer, when HW detects room for the report, it would resume reporting to the buffer. This mode would not set the over-run bit in the register.
When this mode bit is reset, buffer overrun can happen and lose the reports while setting the buffer over-run bit.

Value	Name	Description
0h	Disable **[Default]**	Counter gets written out on regular intervals, defined by the Timer Period
1h	Enable	Counter does not get written out on regular interval

0 **Memory Select PPGTT/GGTT Access**

Value	Name
0h	PPGTT
1h	GGTT **[Default]**

Programming Notes
When each context has its own Per Process GTT, this field should be always set to GGTT.

Observation Architecture Control

OACONTROL - Observation Architecture Control

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02B00h

This register controls global OA functionality, report format, interrupt steering and context filtering.

DWord	Bit	Description
0	31:6	**Reserved** Format: PBC
	5	**Interrupt Steering Bit** When set, OACS unit sends interrupt messages to the SHIM through message channel. When reset, OACS unit sends the interrupt message to Display Engine as config writes on GAM interface.
	4:2	**Counter Select** Format: Performance Counter Report Format This field selects which performance counter report format to use, please refer to Performance Counter Report Formats section for more details on the structure of the format.
	1	**Specific Context Enable** Format: Enable **Description** Enables counters to work on a context specific workload. The context is given by bits 31:12. OA unit level clock gating must be ENABLED when using specific ContextID feature. When "Specific Context Enable" bit is set to '1' in OACONTROL register, Boolean/Threshold report trigger function gets enabled only for the selected context. When "Specific Context Enable" bit is set to '0' in OACONTROL register, Boolean/Threshold report trigger function gets enabled for all contexts. When "Specific Context Enable" bit is set to '1' in OACONTROL register, Timer based report trigger function gets enabled only for the selected context. When "Specific Context Enable" bit is set to '0' in OACONTROL register, Timer based report trigger function gets enabled for all contexts. **Value** / **Name** / **Description** 0h / Disable **[Default]** / All contexts are considered

OACONTROL - Observation Architecture Control

		1h	Enable	Only the contexts with the Select Context ID field in OACTXID are considered
	0	**Performance Counter Enable**		
		Format:		Enable
		Global performance counter enable. If clear, no counting will occur. MI_REPORT_PERF_COUNT is undefined when clear.		
		Programming Notes		
		When this bit is set, OABUFFER, OAHEADPTR and OATAILPTR must be programmed correctly to ensure report triggers due to Context Switch and GO transition happen correctly.		

Observation Architecture Control Context ID

OACTXID - Observation Architecture Control Context ID	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02364h

This register has the context details when Specific context Enable is set. This register is implemented in render command streamer and render context save/restored. This register should be initialized by SW appropriately on the very first submission of a context when OA is enabled.

DWord	Bit	Description
0	31:0	**Select Context ID** Specifies the context ID of the one context that affects the performance counters when "Specific Context Enable" bit is set. All other contexts are ignored. **Ring Buffer Mode of Scheduling:** Bits[31:12] represent the CCID and bits [11:0] must be zero. **Execlist mode of scheduling:** Bits[31:0] represent the context id.

Observation Architecture Control per Context

OACTXCONTROL - Observation Architecture Control per Context

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02360h

This register is implemented in render command streamer and render context save/restored.
This register should be initialized by SW appropriately on the very first submission of a context when OA is enabled.

DWord	Bit	Description
0	31	**Slice Shutdown In Progress** Access: RO This bit indicates the status of the Slice Shutdown hapenning in render engine. Value / Name / Description: 0 — Indicates there is no slice shutdown hapenning in render engine. 1 — Indicates there is an slice shutdown hapenning in render engine.
	30:8	**Reserved** Format: PBC
	7:2	**Timer Period** Format: Select Specifies the period of the timer strobe as a function of the minimum TIME_STAMP resolution. The period is determined by selecting a specified bit from the TIME_STAMP register as follows: StrobePeriod = MinimumTimeStampPeriod * 2 **(TimerPeriod + 1)** The exponent is defined by this field. **Note:** The TIME_STAMP is not reset at start time so the phase of the strobe is not synchronized with the enable of the OA unit. This could result in approximately a full StrobePeriod elapsing prior to the first trigger. Usage for this mechanism should be time based periodic triggering, typically.
	1	**Timer Enable** Format: Enable Description: This field enables the timer logic to output a periodic strobe, as defined by the Timer Period. When disabled the timer output is not asserted. Users should be aware that the timer-based report logic and the Boolean report trigger logic are logically OR'd together with no buffering of

OACTXCONTROL - Observation Architecture Control per Context

report triggers. This implies that only one performance counter report will be generated for clocks where both the timer-based report logic and the Boolean report trigger logic trigger a performance counter report.

When "Specific Context Enable" bit is set to '1' in OACONTROL register, Timer based report trigger function gets enabled only for the selected context.
When "Specific Context Enable" bit is set to '0' in OACONTROL register, Timer based report trigger function gets enabled for all contexts.

Value	Name	Description
0h	Disable **[Default]**	Counter does not get written out on regular interval
1h	Enable	Counter gets written out on regular intervals, defined by the Timer Period

0

Counter Stop-Resume Mechanism

Format:	Select

Value	Name	Description
1h		resume counting for all counters

Observation Architecture Head Pointer

OAHEADPTR - Observation Architecture Head Pointer		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02B0Ch	
This register allows SW to program head pointer.		
DWord	**Bit**	**Description**
0	31:6	**Head Pointer** Virtual address of the internal trigger based buffer that is updated by software after consuming reports from the report buffer. This pointer must be updated by SW only when using time or event-based report triggering. **Programming Notes** SW must ensure that Head Pointer and the Tail Pointer match before enabling internally triggered performance counter reporting.
	5:0	**Reserved** Format: PBC

Observation Architecture Report Trigger 2

OAREPORTTRIG2 - Observation Architecture Report Trigger 2

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02744h

Description

This register controls some of the Boolean logic defining Boolean/threshold report trigger 0. The bit definitions in this register refer to the stages in the report trigger block diagram in the Performance Counter Reporting section.

Report triggers generated from OAREPORTTRIG 1-4 and OAREPORTTRIG 5-8 are ORed to form a new report trigger. Report trigger behavior can be derived by programming these two sets of OA REPORT registers with the same value. Users should be aware that while programming Timer based and Threshold Counter based triggers simultaneously for internal reporting, they should be programmed such way that they are not consecutively triggered. If programmed simultaneously, RTL pulse detection logic will have problem when these triggers occur in consecutive clock cycles.

DWord	Bit	Description
0	31	**Report Trigger Enable** Format: Enable **Description** Enable Boolean/threshold report trigger 0. Users should be aware that the timer-based report logic and the Boolean report trigger logic are logically OR'd together with no buffering of report triggers. This implies that only one performance counter report will be generated for clocks where both the timer-based report logic and the Boolean report trigger logic trigger a performance counter report. When "Specific Context Enable" bit set to '1' in OACONTROL register, Boolean/Threshold report trigger function gets enabled only for the selected context. When "Specific Context Enable" bit set to '0' in OACONTROL register, Boolean/Threshold report trigger function gets enabled for all contexts.
	30:24	**Reserved** Format: PBC
	23	**Threshold Enable** Format: Enable Enable the threshold compare logic within the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).

OAREPORTTRIG2 - Observation Architecture Report Trigger 2

	22	**Invert D Enable 0** Format: Enable Invert the specified signal at the D stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	21	**Invert C Enable 1** Format: Enable Invert the specified signal at the C stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	20	**Invert C Enable 0** Format: Enable Invert the specified signal at the C stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	19	**Invert B Enable 3** Format: Enable Invert the specified signal at the B stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	18	**Invert B Enable 2** Format: Enable Invert the specified signal at the B stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	17	**Invert B Enable 1** Format: Enable Invert the specified signal at the B stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	16	**Invert B Enable 0** Format: Enable Invert the specified signal at the B stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	15	**Invert A Enable 15** Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).

OAREPORTTRIG2 - Observation Architecture Report Trigger 2

	14	**Invert A Enable 14** Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	13	**Invert A Enable 13** Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	12	**Invert A Enable 12** Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	11	**Invert A Enable 11** Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	10	**Invert A Enable 10** Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	9	**Invert A Enable 9** Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	8	**Invert A Enable 8** Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	7	**Invert A Enable 7** Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).

OAREPORTTRIG2 - Observation Architecture Report Trigger 2

	6	**Invert A Enable 6** Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	5	**Invert A Enable 5** Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	4	**Invert A Enable 4** Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	3	**Invert A Enable 3** Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	2	**Invert A Enable 2** Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	1	**Invert A Enable 1** Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	0	**Invert A Enable 0** Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).

Observation Architecture Report Trigger 6

OAREPORTTRIG6 - Observation Architecture Report Trigger 6

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02754h

Description

This register controls some of the Boolean logic defining Boolean/threshold report trigger 1. Note that Boolean report triggers 0 and 1 are logically OR'd together without buffering, this implies that only one performance counter report will be generated for clocks where both Boolean report triggers evaluate true. The bit definitions in this register refer to the stages in the report trigger block diagram in the Performance Counter Reporting section.

Report triggers generated from OAREPORTTRIG 1-4 and OAREPORTTRIG 5-8 are ORed to form a new report trigger. Report trigger behavior can be derived by programming these two sets of OA REPORT registers with the same value. Users should be aware that while programming Timer based and Threshold Counter based triggers simultaneously for internal reporting, they should be programmed such way that they are not consecutively triggered. If programmed simultaneously, RTL pulse detection logic will have problem when these triggers occur in consecutive clock cycles.

DWord	Bit	Description
0	31	**Report Trigger Enable** **Description** Enable Boolean/threshold report trigger 0. Users should be aware that the timer-based report logic and the Boolean report trigger logic are logically OR'd together with no buffering of report triggers. This implies that only one performance counter report will be generated for clocks where both the timer-based report logic and the Boolean report trigger logic trigger a performance counter report. When "Specific Context Enable" bit set to '1' in OACONTROL register, Boolean/Threshold report trigger function gets enabled only for the selected context. When "Specific Context Enable" bit set to '0' in OACONTROL register, Boolean/Threshold report trigger function gets enabled for all contexts.
	30:24	**Reserved** Format: PBC
	23	**Threshold Enable** Enable the threshold compare logic within the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	22	**Invert D Enable 0** Invert the specified signal at the D stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).

OAREPORTTRIG6 - Observation Architecture Report Trigger 6		
	21	**Invert C Enable 1** Invert the specified signal at the C stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	20	**Invert C Enable 0** Invert the specified signal at the C stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	19	**Invert B Enable 3** Invert the specified signal at the B stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	18	**Invert B Enable 2** Invert the specified signal at the B stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	17	**Invert B Enable 1** Invert the specified signal at the B stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	16	**Invert B Enable 0** Invert the specified signal at the B stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	15	**Invert A Enable 15** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	14	**Invert A Enable 14** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	13	**Invert A Enable 13** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	12	**Invert A Enable 12** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	11	**Invert A Enable 11** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	10	**Invert A Enable 10** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	9	**Invert A Enable 9** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	8	**Invert A Enable 8** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).

OAREPORTTRIG6 - Observation Architecture Report Trigger 6		
	7	**Invert A Enable 7** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	6	**Invert A Enable 6** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	5	**Invert A Enable 5** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	4	**Invert A Enable 4** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	3	**Invert A Enable 3** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	2	**Invert A Enable 2** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	1	**Invert A Enable 1** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	0	**Invert A Enable 0** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).

Observation Architecture Report Trigger Counter

OARPTTRIG_COUNTER - Observation Architecture Report Trigger Counter

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02B1Ch

This register provides status of report trigger threshold count 1 and 2. This register is for HW internal purpose and power context save/restored. This register must not be programmed by SW.

DWord	Bit	Description
0	31:16	**Report Trig Threshold Count 1 Status** **Programming Notes** This field is for HW internal use to context save/restore rpt trigger threshold count 1. It always indicates current value of HW's internal report trigger count. SW should not program these bits.
	15:0	**Report Trig Threshold count 2 status** **Programming Notes** This field is for HW internal use to context save/restore rpt trigger threshold count 2. It always indicates current value of HW's internal report trigger count. SW should not program these bits.

Observation Architecture Start Trigger 5

OASTARTTRIG5 - Observation Architecture Start Trigger 5

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02720h

This register provides the threshold value optionally used to define the start trigger for B7-B4 counters. Note that the value in this register must match the value in OASTARTTRIG1 to have B7-B0 start at the same time. The bit definition in this register refers to the stages in the start trigger block diagram in the Performance Counter Reporting section.

DWord	Bit	Description
0	31:16	**Reserved** Format: PBC
	15:0	**Threshold Value** Format: U16 **Programming Notes** Threshold value for the compare logic within the start trigger logic for B7-B4 counters.

Observation Architecture Start Trigger Counter

OASTARTTRIG_COUNTER - Observation Architecture Start Trigger Counter

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02B18h

This register provides status of start trigger threshold count 1 and 2. This register is for HW internal purpose.

DWord	Bit	Description
0	31:16	**Start Trig Threshold Count 1 Status** **Programming Notes** This field is for HW internal use to context save/restore start trigger threshold count 1. It always indicates current value of HW's internal start trigger count. SW should not program these bits.
	15:0	**Start Trig Threshold count 2 status** **Programming Notes** : This field is for HW internal use to context save/restore start trigger threshold count 2. It always indicates current value of HW's internal start trigger count. SW should not program these bits.

Observation Architecture Status Register

OASTATUS - Observation Architecture Status Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00030000
Access:	R/W
Size (in bits):	32
Address:	02B08h

This register provides status of report buffer and overflow conditions as well as status of some flags which hardware needs for internal purpose.
Software should not program these status bits.

DWord	Bit	Description
0	31:22	**Reserved** Default Value: 0 Format: PBC
	21	**Start Trigger Flag 1** 0 – **[Default]** 1 **Programming Notes**: This bit is for HW internal use to context save /restore Start Trigger 1 occurrence On RC6 entry. Software should not program this bit.
	20	**Start Trigger Flag 2** 0 – **[Default]** 1 **Programming Notes**: This bit is for HW internal use to context save /restore Start Trigger 2 occurrence On RC6 entry. Software should not program this bit.
	19	**Report Trigger Flag 1** 0 – **[Default]** 1 **Programming Notes**

OASTATUS - Observation Architecture Status Register

	This bit is for HW internal use to context save /restore Report Trigger 1 occurrence On RC6 entry. Software should not program this bit.
18	**Report Trigger Flag 2** Value: 0 — **[Default]** Value: 1 **Programming Notes**: This bit is for HW internal use to context save /restore Report Trigger 2 occurrence On RC6 entry. Software should not program this bit.
17	**Tail Pointer Wrap Flag** Format: U1 Value: 0 Value: 1 — **[Default]** **Programming Notes**: This bit is for HW internal use to context save /restore Tail Pointer Wrap Flag. SW should not program this bit. This bit gets programmed only when Tail Pointer Wrap Mask bit is set.
16	**Head Pointer Wrap Flag** Format: U1 Value: 0 Value: 1 — **[Default]** **Programming Notes**: This bit is for HW internal use to context save /restore Head Pointer Wrap Flag. SW should not program this bit. This bit gets programmed only when Head Pointer Wrap Mask bit is set.
15:6	**Reserved** Default Value: 0 Format: PBC
5	**Reserved** Default Value: 0 Format: PBC
4	**Reserved**

OASTATUS - Observation Architecture Status Register

	Default Value:	0
	Format:	PBC

3 Reserved

2 Counter Overflow

Format:	Select

This bit is set if any of the counters overflows. This bit can be reset by SW by either soft reset or writing a 1 to it.

Value	Name
0	**[Default]**
1	

1 Buffer Overflow

This bit is set when the Tail-pointer - Head pointer > max internal trigger buffer size

Value	Name
0h	**[Default]**
1	

0 Report Lost Error

Format:	Enable

This bit is set if the Report Trigger due to "Internal Report Trigger-1", "Internal Report Trigger-2" or "Timer Triggered" to write out the counter values is dropped, while there is an ongoing report in progress.

The report request is ignored and the counter continue to count.

Value	Name
0	**[Default]**
1	

Programming Notes
This bit can be reset by SW by either soft reset or writing a 1 to it.

Observation Architecture Tail Pointer

OATAILPTR - Observation Architecture Tail Pointer

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02B10h

This register allows software to program tail pointer and also indicates current tail pointer value.

DWord	Bit	Description
0	31:6	**Tail Pointer** Virtual address of the internal trigger based buffer that is updated for every 64B cacheline write to memory when reporting via internal report trigger. This pointer will not be updated for MI_REPORT_PERF_COUNT command based writes. **Programming Notes** Before enabling internally triggered performance counter reporting, SW must ensure that this address matches the Report Buffer Offset programmed in OABUFFER register (i.e. tail pointer must start at the beginning of the report buffer). SW must ensure that Tail pointer and the Head Pointer match before enabling internally triggered performance counter reporting.
	5:0	**Reserved** Format: PBC

Outstanding Page Request Allocation

OPRA_0_2_0_PCI - Outstanding Page Request Allocation

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	0030Ch

DWord	Bit	Description
0	31:0	**Outstanding Page Request Allocation** Default Value: 00000000000000000000000000000000b Access: R/W This register contains the number of outstanding page request messages the associated Page Request Interface is allowed to issue.

Outstanding Page Request Capacity

OPRC_0_2_0_PCI - Outstanding Page Request Capacity

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00008000
Size (in bits):	32
Address:	00308h

DWord	Bit	Description
0	31:0	**Outstanding Page Request Capacity** Default Value: 00000000000000001000000000000000b Access: RO This register contains the number of outstanding page request messages the associated Page Request Interface physically supports. This is the upper limit on the number of pages that can be usefully allocated to the Page Request Interface. Hardwired to 32,768 requests.

Page Directory Pointer Descriptor - PDP0/PML4/PASID

PDP0 - Page Directory Pointer Descriptor - PDP0/PML4/PASID

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64

PDP0/PML4/PASID: This register can contain three values which depend on the element descriptor definition.
PASID[19:0]: Populated in the first 20bits of the register and selected when Advanced Context flag is set in the element descriptor in execlist mode of submission. This is not valid in ring buffer mode of scheduling.
PML4[38:12]: Pointer to base address of PML4 and selected when Legacy Context flag is set and 64b address support is selected.
PDP0[38:12]: Pointer to one of the four page directory pointer (lowest) and defines the first 0-1GB of memory mapping. This is valid when Legacy Context Flag is set and 64bit virtual addressing is not supported.
Note: This is a guest physical address.

Programming Notes

Execlist Based Scheduling: SW should update PDP0/12/3 registers in context image with proper values before submitting the context to HW in execlist mode of scheduling. HW restores these registers as part of context restore to set the PPGTT access accordingly. PPGTT is always enabled in advanced context mode of execlist based scheduling and can be disabled only in legacy context mode. Privilege Access Bit in Element Descriptor controls the PPGTT enabling in legacy context mode.

Ring Buffer Based Scheduling: A write via MMIO to PDP0_DESCRIPROR (lower Dword) triggers the Page Directory Restore in HW when PPGTT is enabled. SW should ensure PDP1/2/3 registers are programmed appropriately prior to programming PDP0. PDP0_DESCRIPTOR lower dword should be programmed at the end. Per-Process GTT Enable Bit in GFX_MODE register controls the PPGTT enabling and disabling. Programming Per-Process GTT Enable Bit in GFX_MODE register doesn't enable/disable the PPGTT translation of memory access immediately; the change comes in to affect only when the Page Directory registers are programmed. Programming Per-Process GTT Enable Bit in GFX_MODE register bit must be followed by programming Page Directory Registers in order to enable or disable the PPGTT translation of memory access. PDP* DESCRIPTOR registers must always be programmed through MI_LOAD_REGISTER_IMMEDIATE command in ring buffer with PDP0_DESCRIPRTOR lower dword written at the end. PDP0/12/3 registers are context save restored. PDP descriptors are context save restored per render context in RCS and must be programmed following MI_SET_CONTEXT command, in case of PDP descriptors programmed without context set (MI_SET_CONTEXT) will get lost on C6 entry/exit. PDP descriptors are context save restored in VCS, BCS and VECS engines and must be programmed following setup of CCID register, in case of PDP descriptors programmed without CCID set will get lost on C6 entry/exit. PDP descriptor registers should be programmed after ensuring the pipe is completely flushed and TLB's invalidated.

DWord	Bit	Description
0	63	**PD Load Busy** Access: RO Format: Valid

PDP0 - Page Directory Pointer Descriptor - PDP0/PML4/PASID		
		This read-only field gets set when PDP0 is written to indicating Page Directory Restore activity is in progress and will get reset once the activity is completed.
	62:0	**PDP0 Descriptor**

Page Directory Pointer Descriptor - PDP1

PDP1 - Page Directory Pointer Descriptor - PDP1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64

PDP1[38:12]: Pointer to one of the four page directory pointer (lowest+1) and defines the first 1-2GB of memory mapping. This is valid when Legacy Context Flag is set and 64bit virtual addressing is not supported. *Note: This is a guest physical address.*

DWord	Bit	Description
0	63:0	**PDP1 Descriptor**

Page Directory Pointer Descriptor - PDP2

PDP2 - Page Directory Pointer Descriptor - PDP2	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64

PDP2[38:12]: Pointer to one of the four page directory pointer (lowest+2) and defines the first 2-3GB of memory mapping. This is valid when Legacy Context Flag is set and 64bit virtual addressing is not supported. *Note: This is a guest physical address.*

DWord	Bit	Description
0	63:0	**PDP2 Descriptor**

Page Directory Pointer Descriptor - PDP3

PDP3 - Page Directory Pointer Descriptor - PDP3	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64

PDP3[38:12]: Pointer to one of the four page directory pointer (lowest+3) and defines the first 3-4GB of memory mapping. This is valid when Legacy Context Flag is set and 64bit virtual addressing is not supported. *Note: This is a guest physical address.*

DWord	Bit	Description
0	63:0	**PDP3 Descriptor**

Page Request Control

PR_CTRL_0_2_0_PCI - Page Request Control

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	16
Address:	00304h

DWord	Bit	Description
0	1	**Reset** Default Value: 0b Access: RO When the Enable field is clear, or is being cleared in the same register update that sets this field, writing a 1b to this field, clears the associated implementation dependent page request credit Counter and pending request state for the associated Page Request Interface. No action is initiated if this field is written to 0b or if this field is written with any value when the PRE field is set. Processor graphics does not use this field, and hardwires it as read-only (0).
	0	**Page-Request Enable** Default Value: 0b Access: R/W When Set, indicates that the page request interface on the endpoint is allowed to make page requests. If both this field and the Stopped field in Page Request Status register are Clear, then the Page request interface will not issue new page requests, but has outstanding page requests for which page responses have not yet been received. When this field transitions from 0 to 1, all the status fields in the Page-Request Status register are cleared. Enabling a page request interface that has not successfully stopped has indeterminate results.

Page Request Extended Capability Header

PR_EXTCAP_0_2_0_PCI - Page Request Extended Capability Header

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00010013
Size (in bits):	32
Address:	00300h

Page Request Extended Capability reports support for page-faults on Device-2, compliant to PCI-Express ATS 1.1 Specification

DWord	Bit	Description
0	31:20	**Next Capability Offset** Default Value: 000000000000b Access: RO **Description**: This is a hardwired pointer to the next item in the capabilities list. Value 000h indicates that this is the end of the PCI-Express Extended capability Linked List.
	19:16	**Version** Default Value: 0001b Access: RO Hardwired to capability version 1.
	15:0	**Capability ID** Default Value: 0000000000010011b Access: RO Hardwired to the Page Request Extended Capability ID

Page Request Queue Address Register 0

PAGEREQ_QADDR_0 - Page Request Queue Address Register 0

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0F0D0h

Register to configure the base address and size of the page request queue.

DWord	Bit	Description
0	31:12	**Page Request Queue Base Register** Default Value: 00000h Access: R/W This field points to the base of 4KB aligned invalidation request queue. Hardware may ignore and not implement bits 63:HAW, where HAW is the host address width. Reads of this field return the value that was last programmed to it.
	11:3	**Reserved** Default Value: 000000000b Access: RO
	2:0	**Queue Size** Default Value: 000b Access: R/W This field specifies the size of the page request queue. A value of X in this field indicates a page request queue of (2X) 4KB pages. The number of entries in the invalidation queue is 2(X+8).

Page Request Queue Address Register 1

PAGEREQ_QADDR_1 - Page Request Queue Address Register 1		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F0D4h	
Register to configure the base address and size of the page request queue.		
DWord	**Bit**	**Description**
0	31:0	**Page Request Queue Base Register** Default Value: 00000000h Access: R/W This field points to the base of 4KB aligned invalidation request queue. Hardware may ignore and not implement bits 63:HAW, where HAW is the host address width. Reads of this field return the value that was last programmed to it.

Page Request Queue Head Register 0

PAGEREQ_QHEAD_0 - Page Request Queue Head Register 0

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	0F0C0h

Register indicating the page request queue head.

DWord	Bit	Description
0	31:19	**Reserved** Default Value: 0000000000000b Access: RO
	18:4	**Queue Head** Default Value: 000000000000000b Access: R/W Specifies the offset (128-bit aligned) to the page request queue for the command that is processed next by software. GFX implementation: GFX has to read the content of the Head pointer as tail pointer gets close to it to prevent overflows in page request queue.
	3:0	**Reserved** Default Value: 0h Access: RO

Page Request Queue Head Register 1

PAGEREQ_QHEAD_1 - Page Request Queue Head Register 1		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F0C4h	
Register indicating the page request queue head.		
DWord	**Bit**	**Description**
0	31:0	**Page Request Queue Head Register 1 Reserved** Default Value: 00000000h Access: RO Bit[63:32]: Reserved.

Page Request Queue Tail Register 0

PAGEREQ_QTAIL_0 - Page Request Queue Tail Register 0		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000 [KBL]	
Size (in bits):	32	
Address:	0F0C8h	
Register indicating the page request queue tail.		
DWord	**Bit**	**Description**
0	31:1	**Queue Tail** Default Value: 00000000000000000000000000000000b Access: R/W Bit[31:19]: Reserved. Bit[18:4]: Specifies the offset (128-bit aligned) to the page request queue for the request that is written next by hardware. GFX Implementation: GT manages the tail pointer value as part of page requests. The value can be acquired as part of the RC6 exit. Bit[3:1]: Reserved.
	0	**Valid Bit** Default Value: 0b Access: R/W This bit can only be cleared by SW, which also clears the other fields.

Page Request Queue Tail Register 1

PAGEREQ_QTAIL_1 - Page Request Queue Tail Register 1		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000 [KBL]	
Size (in bits):	32	
Address:	0F0CCh	
Register indicating the page request queue tail.		
DWord	**Bit**	**Description**
0	31:0	**Page Request Queue Tail Register 1 Reserved** Default Value: 00000000h Access: RO Bit[63:32]: Reserved.

Page Request Status

PR_STATUS_0_2_0_PCI - Page Request Status

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00008000
Size (in bits):	16
Address:	00306h

DWord	Bit	Description
0	15	**PRG Response PASID Required** Default Value: 1b Access: RO If set, the Function expects a PASID TLP Prefix on PRG Response Messages when the corresponding page requests had a PASID TLP Prefix. If Clear, the function does not expect PASID TLP Prefixes on any PRG Response Message. Function behavior is undefined if this bit is Clear and the Function receives a PRG Response Message with a PASID TLP Prefix. Function behavior is undefined if this bit is Set and the Function receives a PRG Response Message with no PASID TLP Prefix when the corresponding Page Requests had a PASID TLP Prefix. This bit is RsvdZ if the Function does not support the PASID TLP Prefix.
	14:9	**Reserved** Format: MBZ
	8	**Stopped** Default Value: 0b Access: RO When this field is Set, the associated page request interface has stopped issuing additional Page requests and that all previously issued Page requests have completed. When this field is clear the associate Page request interface either has not stopped or has stopped issuing new Page requests but has outstanding Page requests.
	7:2	**Reserved** Format: MBZ
	1	**Unexpected Page Request Group Index** Default Value: 0b Access: R/W One Clear When Set, indicates the function received a PRG response message containing a PRG index that has no matching request, a response failure. This field is Set by the Function and cleared when a 1b is written to the field.

PR_STATUS_0_2_0_PCI - Page Request Status

		Processor graphics Sets this field when it receives a page_grp_resp_dsc with PRG Index that does not match PRG index in any outstanding page_grp_req_dsc. Such page_grp_resp_dsc is ignored. When Page-Request Enable (PRE) field in the Page-request Control register transitions from 0 to 1, this field is cleared.
	0	**Response Failure** Default Value: 0b Access: R/W One Clear When Set, indicates the function received a PRG response message indicating a response failure. The function expects no further response from the host(any received are ignored). This field is Set by the Function and cleared when a 1b is written to this field. Processor graphics Sets this field when it receives a page_grp_resp_dsc or page_stream_resp_dsc with Response Code of Response Failure (1111b). The advanced context corresponding to the PASID in such response is terminated with error. When Page-Request Enable (PRE) field in the Page-request control register transitions from 0 to 1, this field is cleared.

PAK_Stream-Out Report (Errors)

PAK_ERR - PAK_Stream-Out Report (Errors)		
Register Space:	MMIO: 0/2/0	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	128E8h	

DWord	Bit	Description
0	31:22	**Reserved** Format: MBZ
	21	**Incorrect IntraMBFlag in I-slice(AVCf)**
	20	**Out of Range Symbol Code(AVC/mpeg2)**
	19	**Incorrect MBType(AVC/mpeg2**
	18	**Motion Vectors are not inside the frame boundary(mpeg2)**
	17	**Scale code is zero(mpeg2)**
	16	**Incorrect DCTtype for given motionType(mpeg2)**
	15:8	**MB Y-position** This field indicates Macro Block(MB) Y- position where an error occured while encoding.
	7:0	**MB X-position** This field indicates Macro Block(MB) X- position where an error occured while encoding.

PAK_Stream-Out Report (Warnings)

PAK_WARN - PAK_Stream-Out Report (Warnings)		
Register Space:	MMIO: 0/2/0	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	128E4h	
DWord	**Bit**	**Description**
0	31:22	**Reserved** Format: MBZ
	21	**Skip Run > 8192 (AVC)**
	20	**Incorrect SkipMB (AVC and mpeg2)**
	19	**Incorrect MV difference for dual-prime MB (mpeg2)**
	18	**End of Slice signal missing on last MB of a Row(mpeg2)**
	17	**Incorrect DCT type for field picture**
	16	**MVs are not within defined range by fcode**
	15:8	**MB Y-position**
	7:0	**MB X-position**

PAK Report Running Status

PAK_REPORT_STAT - PAK Report Running Status

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	128ECh

DWord	Bit	Description
0	31:1	**Reserved**
	0	**PAK Status** Value / Name / Description 0 / / PAK engine is IDLE 1 / / PAK engine is currently generating bit stream.

PAL_EXT_GC_MAX

PAL_EXT_GC_MAX

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0007FFFF, 0x0007FFFF, 0x0007FFFF
Access:	R/W
Size (in bits):	96

Address:	4A420h-4A42Bh
Name:	Pipe Extended Gamma Correction Max
ShortName:	PAL_EXT_GC_MAX_A
Power:	PG1
Reset:	soft

Address:	4AC20h-4AC2Bh
Name:	Pipe Extended Gamma Correction Max
ShortName:	PAL_EXT_GC_MAX_B
Power:	PG2
Reset:	soft

Address:	4B420h-4B42Bh
Name:	Pipe Extended Gamma Correction Max
ShortName:	PAL_EXT_GC_MAX_C
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31:19	**Reserved** Format: MBZ
	18:0	**Red Ext Max GC Point** Default Value: 11111111111111111b Format: U3.16 The extended point for red color channel gamma correction. This value is represented in a 3.16 format with 3 integer and 16 fractional bits.
1	31:19	**Reserved** Format: MBZ
	18:0	**Green Ext Max GC Point** Default Value: 11111111111111111b Format: U3.16 The extended point for green color channel gamma correction. This value is represented in a 3.16 format with 3 integer and 16 fractional bits.

PAL_EXT_GC_MAX		
2	31:19	**Reserved** Format: MBZ
	18:0	**Blue Ext Max GC Point** Default Value: 11111111111111111b Format: U3.16 The extended point for blue color channel gamma correction. This value is represented in a 3.16 format with 3 integer and 16 fractional bits.

PAL_GC_MAX

PAL_GC_MAX

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00010000, 0x00010000, 0x00010000
Access:	R/W
Size (in bits):	96

Address:	4A410h-4A41Bh
Name:	Pipe Gamma Correction Max
ShortName:	PAL_GC_MAX_A
Power:	PG1
Reset:	soft

Address:	4AC10h-4AC1Bh
Name:	Pipe Gamma Correction Max
ShortName:	PAL_GC_MAX_B
Power:	PG2
Reset:	soft

Address:	4B410h-4B41Bh
Name:	Pipe Gamma Correction Max
ShortName:	PAL_GC_MAX_C
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31:17	**Reserved** Format: MBZ
	16:0	**Red Max GC Point** Default Value: 10000000000000000b Format: U1.16 The 513th entry for the red color channel of the 12 bit interpolated gamma correction. This value is represented in a 1.16 format with 1 integer and 16 fractional bits. **Restriction** Restriction : The value should always be programmed to be less than or equal to 1.0.
1	31:17	**Reserved** Format: MBZ

PAL_GC_MAX

	16:0	**Green Max GC Point** Default Value: 10000000000000000b Format: U1.16 The 513th entry for the green color channel of the 12 bit interpolated gamma correction. This value is represented in a 1.16 format with 1 integer and 16 fractional bits. **Restriction** Restriction : The value should always be programmed to be less than or equal to 1.0.
2	31:17	**Reserved** Format: MBZ
	16:0	**Blue Max GC Point** Default Value: 10000000000000000b Format: U1.16 The 513th entry for the blue color channel of the 12 bit interpolated gamma correction. This value is represented in a 1.16 format with 1 integer and 16 fractional bits. **Restriction** Restriction : The value should always be programmed to be less than or equal to 1.0.

PAL_LGC

PAL_LGC	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	4A000h-4A3FFh
Name:	Pipe A Legacy Palette
ShortName:	PAL_LGC_A_*
Power:	PG1
Reset:	soft
Address:	4A800h-4ABFFh
Name:	Pipe B Legacy Palette
ShortName:	PAL_LGC_B_*
Power:	PG2
Reset:	soft
Address:	4B000h-4B3FFh
Name:	Pipe C Legacy Palette
ShortName:	PAL_LGC_C_*
Power:	PG2
Reset:	soft

There are 256 instances of this register format per display pipe.

Restriction

Restriction : This register must be written only as a full 32 bit dword. Byte or word writes are not supported.

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:16	**Red Legacy Palette Entry** Default Value: UUh Red legacy palette entry value.
	15:8	**Green Legacy Palette Entry** Default Value: UUh Green legacy palette entry value.

PAL_LGC		
	7:0	**Blue Legacy Palette Entry** Default Value: UUh Blue legacy palette entry value.

PAL_PREC_DATA

PAL_PREC_DATA	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	4A404h-4A407h
Name:	Pipe Precision Palette Data
ShortName:	PAL_PREC_DATA_A
Power:	PG1
Reset:	soft
Address:	4AC04h-4AC07h
Name:	Pipe Precision Palette Data
ShortName:	PAL_PREC_DATA_B
Power:	PG2
Reset:	soft
Address:	4B404h-4B407h
Name:	Pipe Precision Palette Data
ShortName:	PAL_PREC_DATA_C
Power:	PG2
Reset:	soft

These are the precision palette entries used for the 10 bpc, split, and 12 bpc gamma.
The Precision Palette Index Value indicates the precision palette location to be accessed through this register.

Programming Notes

For 10 bpc, program with the color 10 bit palette entry fraction value.
For 12 bpc gamma odd indexes, program with the upper 10 bits of the color palette entry fraction value.
For 12 bpc gamma even indexes, program the MSbs with the lower 6 bits of the color palette entry fraction value, then program all 0s in the LSbs.
For split gamma indexes 0 to 511, program with the first gamma (before CSC) color 10 bit palette entry fraction value.
For split gamma indexes 512 to 1023, program with the second gamma (after CSC) color 10 bit palette entry fraction value.

Restriction

Restriction : This register must be written only as a full 32 bit dword. Byte or word writes are not supported.

DWord	Bit	Description

PAL_PREC_DATA		
0	31:30	**Reserved**
	29:20	**Red Precision Palette Entry** Default Value: UUUUUUUUUUb Red precision palette entry value.
	19:10	**Green Precision Palette Entry** Default Value: UUUUUUUUUUb Green precision palette entry value.
	9:0	**Blue Precision Palette Entry** Default Value: UUUUUUUUUUb Blue precision palette entry value.

PAL_PREC_INDEX

PAL_PREC_INDEX

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	4A400h-4A403h
Name:	Pipe Precision Palette Index
ShortName:	PAL_PREC_INDEX_A
Power:	PG1
Reset:	soft
Address:	4AC00h-4AC03h
Name:	Pipe Precision Palette Index
ShortName:	PAL_PREC_INDEX_B
Power:	PG2
Reset:	soft
Address:	4B400h-4B403h
Name:	Pipe Precision Palette Index
ShortName:	PAL_PREC_INDEX_C
Power:	PG2
Reset:	soft

This index controls access to the array of precision palette data values.

DWord	Bit	Description
0	31	**Precision Palette Format** This field selects the format of the precision palette data. **Value** / **Name** / **Description** 0b / Non-split / 10 bpc or 12 bpc gamma format 1b / Split / Split gamma format **Restriction** Restriction : It must be set when reading or writing precision palette entries for split gamma mode. It must be cleared before programming the legacy palette.
	30:16	**Reserved** Format: MBZ

PAL_PREC_INDEX

15 — Index Auto Increment

This field enables the index auto increment.

Value	Name	Description
0b	No Increment	Do not automatically increment the index value.
1b	Auto Increment	Increment the index value with each read or write to the data register.

14:10 — Reserved

Format:	MBZ

9:0 — Index Value

This field indicates the data location to be accessed through the data register.

This value can be automatically incremented by a read or a write to the data register if the index auto increment bit is set.

When automatically incrementing, the current automatically calculated index value can be read here, and the index will roll over to 0 after reaching the end of the allowed range.

Value	Name
[0,1023]	

PASID Capability

PASID_CAP_0_2_0_PCI - PASID Capability

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00001402
Size (in bits):	16
Address:	00104h

PASID capability reports support for Process Address Space ID(PASID) on Device-2, compliant to PCI-Express PASID ECN.

DWord	Bit	Description
0	12:8	**Maximum PASID Width** Default Value: 10100b Access: RO Indicates the width of the PASID field supported by the Endpoint. Hardwired to 14h to indicate support for all PASID values (20 bits).
	7:3	**Reserved** Format: MBZ
	2	**Privilege Mode Supported** Default Value: 0b Access: RO Hardwired to 0, the Endpoint supports operating in Non-privileged mode only, and will never request privileged mode in requests-with-PASID.
	1	**Execute Permission Supported** Default Value: 1b Access: RO Hardwired to 1, the Endpoint supports requests-with-PASID that requests execute permission.
	0	**Reserved** Format: MBZ

PASID Control

PASID_CTRL_0_2_0_PCI - PASID Control

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	8
Address:	00106h

Process Address Space ID (PASID) control for Device-2.

DWord	Bit	Description
0	2	**Privileged Mode Enable** Default Value: 0b Access: RO Hardwired to 0, the Endpoint is not permitted to request privileged mode in requests-with-PASID.
	1	**Execute Permission Enable** Default Value: 0b Access: R/W If Set, the Endpoint is permitted to request execute permission in requests-with-PASID. If Clear, the Endpoint is not permitted to do so. Behavior is undefined if this bit changes value when ATS Enable field in ATS Capability is Set. Processor graphics does not use this field. Software is expected to Set this field before configuring extended-context-entry for Device-2 with the Execute Request Enable field Set.
	0	**PASID Enable** Default Value: 0b Access: R/W If Set, the Endpoint is permitted to generate requests-with-PASID. If Clear, the Endpoint is not permitted to do so. Behavior is undefined if this bit changes value when ATS Enable field in ATS Capability is Set. If Priviliged Mode Supported field in PASID Capability register is Clear, then this field is treated as Reserved(0). Processor graphics does not use this field. Software is expected to Set this field before configuring extended-context-entry for Device-2 with Supervisor Request Enable field Set. For compatibility reasons, this field is implemented as RW.

PASID Extended Capability Header

PASID_EXTCAP_0_2_0_PCI - PASID Extended Capability Header

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x2001001B
Size (in bits):	32
Address:	00100h

PASID capability reports support for Process Address Space ID(PASID) on Device-2, compliant to PCI-Express PASID ECN.

DWord	Bit	Description
0	31:20	**Next Capability Offset** Default Value: 001000000000b Access: RO This is a hardwired pointer to the next item in the capabilities list.
	19:16	**Version** Default Value: 0001b Access: RO Hardwired to capability version 1.
	15:0	**Capability ID** Default Value: 0000000000011011b Access: RO Hardwired to the PASID Extended Capability ID

PAT Index

PAT_INDEX - PAT Index

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000003
Access:	R/W
Size (in bits):	32

DWord	Bit	Description
0	31:10	**Reserved** Default Value: 00000000000000000000b
	9:8	**Class of Service** Default Value: 00b This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec 00: Class0 01: Class1 10: Class2 11: Class3
	7:6	**Reserved** Default Value: 00b
	5:4	**LRU AGE** Default Value: 00b 00: Take the age value from Uncore CRs 01: Assign the age of "0" 10: Do not change the age on a hit 11: Assign the age of "3"
	3:2	**Target Cache** Default Value: 00b 00: eLLC only 01: LLC only 10: LLC/eLLC allowed 11: LLC/eLLC allowed
	1:0	**Mem Type** Default Value: 11b 00: Uncacheable(UC) 01: Write Combining(WC) 10: Write through(WT) 11: Write back(WB)

PAT Index High

PAT_INDEX_H - PAT Index High		
Register Space:	MMIO: 0/2/0	
Default Value:	0x03030303	
Size (in bits):	32	
Address:	040E4h	

DWord	Bit	Description
0	31:0	**PAT Index High** Default Value: 03030303h Access: R/W

PAT Index Low

PAT_INDEX_L - PAT Index Low		
Register Space:	MMIO: 0/2/0	
Default Value:	0x03030303	
Size (in bits):	32	
Address:	040E0h	
DWord	**Bit**	**Description**
0	31:0	**PAT Index Low** Default Value: 03030303h Access: R/W

PCI Command

PCICMD_0_2_0_PCI - PCI Command

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	16
Address:	00004h

This 16-bit register provides basic control over the IGD's ability to respond to PCI cycles. The PCICMD Register in the IGD disables the IGD PCI compliant master accesses to main memory.

DWord	Bit	Description
0	10	**Interrupt Disable** Default Value: 0b Access: R/W This bit disables the device from asserting INTx#. 0: Enable the assertion of this device's INTx# signal. 1: Disable the assertion of this device's INTx# signal. DO_INTx messages will not be sent to DMI.
	9	**Fast Back-to-Back** Default Value: 0b Access: RO Not Implemented. Hardwired to 0.
	8	**SERR Enable** Default Value: 0b Access: RO Not Implemented. Hardwired to 0.
	7	**Wait Cycle Control** Default Value: 0b Access: RO Not Implemented. Hardwired to 0.
	6	**Parity Error Enable** Default Value: 0b Access: RO Not Implemented. Hardwired to 0. Since the IGD belongs to the category of devices that does not corrupt programs or data in system memory or hard drives, the IGD ignores any parity error that it detects and continues with normal operation.

PCICMD_0_2_0_PCI - PCI Command

	5	**Video Palette Snooping** Default Value: 0b Access: RO This bit is hardwired to 0 to disable snooping.
	4	**Memory Write and Invalidate Enable** Default Value: 0b Access: RO Hardwired to 0. The IGD does not support memory write and invalidate commands.
	3	**Special Cycle Enable** Default Value: 0b Access: RO This bit is hardwired to 0. The IGD ignores Special cycles.
	2	**Bus Master Enable** Default Value: 0b Access: R/W 0: Disable IGD bus mastering. 1: Enable the IGD to function as a PCI compliant master.
	1	**Memory Access Enable** Default Value: 0b Access: R/W This bit controls the IGD's response to memory space accesses. 0: Disable. 1: Enable.
	0	**I/O Access Enable** Default Value: 0b Access: R/W This bit controls the IGD's response to I/O space accesses. 0: Disable. 1: Enable.

PCI Express Capability

PCIECAP_0_2_0_PCI - PCI Express Capability

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000092
Size (in bits):	16
Address:	00072h

PCI Express Capability

DWord	Bit	Description
0	13:9	**Interrupt Message Number** Default Value: 00000b Access: RO This field indicates which MSI vector is used for the interrupt message generated in association with any of the status bits of this Capability structure. Since this device only supports one MSI vector, this field is hardwired to 0.
	8	**Slot Implemented** Default Value: 0b Access: RO This field is hardwired to 0 for an endpoint device.
	7:4	**Device Port Type** Default Value: 1001b Access: RO This field is hardwired to 9h to indicate a Root Complex Integrated Endpoint.
	3:0	**Capability Version** Default Value: 0010b Access: RO This field is hardwired to 2h to indicate Functions compliant to PCI Express 3.0 Base Specification.

PCI Express Capability Header

PCIECAPHDR_0_2_0_PCI - PCI Express Capability Header

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x0000AC10
Size (in bits):	16
Address:	00070h

PCI Express Capability Header

DWord	Bit	Description
0	15:8	**Next Capability Pointer** Default Value: 10101100b Access: RO This field is hardwired to point to the next PCI Capability structure, the MSI Capabilities at ACh.
	7:0	**Capability Identifier** Default Value: 00010000b Access: RO This field is hardwired to 10h to indicate that this is a PCI Express Capability structure.

PCI Express Device Capabilities

DEVICECAP_0_2_0_PCI - PCI Express Device Capabilities

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x10008000
Size (in bits):	32
Address:	00074h

PCI Express Device Capabilities

DWord	Bit	Description
0	28	**Function Level Reset Capability** Default Value: 1b Access: RO Hardwired to 1b to indicate the Function supports the optional Function Level Reset mechanism.
	27:26	**Captured Slot Power Limit Scale** Default Value: 00b Access: RO Not applicable for a Root Complex integrated Endpoint with no Link or Slot. Hardwired to 00b.
	25:18	**Captured Slot Power Limit Value** Default Value: 00000000b Access: RO Not applicable for a Root Complex integrated Endpoint with no Link or Slot. Hardwired to 00h.
	17:16	**Reserved** Format: MBZ
	15	**Role-Based Error Reporting** Default Value: 1b Access: RO When Set, this bit indicates that the Function implements the functionality originally defined in the Error Reporting ECN for PCI Express Base Specification, Revision 1.0a, and later incorporated into PCI Express Base Specification, Revision 1.1. This bit must be Set by all Functions conforming to the ECN, PCI Express Base Specification, Revision 1.1, or subsequent PCI Express Base Specification revisions.
	14:12	**Reserved** Format: MBZ

DEVICECAP_0_2_0_PCI - PCI Express Device Capabilities

11:9	**Endpoint L1s Acceptable Latency** Default Value: 000b Access: RO This field indicates the acceptable total latency that an Endpoint can withstand due to the transition from the L1 state to the L0 state. This does not apply to the integrated graphics device, soit is hardwired to 000b (Maximum of 1 us).
8:6	**Endpoint L0s Acceptable Latency** Default Value: 000b Access: RO This field indicates the acceptable total latency that an Endpoint can withstand due to the transition from the L0s state to the L0 state. This does not apply to the integrated graphics device, so tit is hardwired to 000b (Maximum of 64 ns).
5	**Extended Tag Field Supported** Default Value: 0b Access: RO This bit indicates the maximum supported size of the Tag field as a Requester. This does not apply to the integrated graphics device, so it is hardwired to the default value of 0b (5-bit Tag field supported).
4:3	**Phantom Functions Supported** Default Value: 00b Access: RO This field indicates the support for use of unclaimed Function Numbers to extend the number of outstanding transactions for PCIe devices. This does not apply to the integrated graphics device, so it is hardwired to 00b to indicate no Function Number bits are used for Phantom Functions.
2:0	**Max Payload Size Supported** Default Value: 000b Access: RO This field indicates the maximum payload size that the Function can support for TLPs. Hardwired to 000b to represent 128 bytes, the minimum allowed value.

PCI Express Device Control

DEVICECTL_0_2_0_PCI - PCI Express Device Control

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	16
Address:	00078h

This register controls device specific capabilities.

DWord	Bit	Description
0	15	**Initiate Function Level Reset** Default Value: 0b Access: R/W Set A write of 1b initiates Function Level Reset (FLR). FLR requirements are defined in the PCI Express Base Specification. Registers and state information that do not apply to conventional PCI are exempt from the FLR requirements given there. Once written 1, FLR will be initiated. During FLR, a read will return 1's since device 2 reads abort. Once FLR completes, hardware will clear the bit to 0. If a local panel is powered on and configured to power down on reset, the FLR will typically take several hundred milliseconds to complete. The worst possible, although unrealistic, delay is 5 seconds.
	14:12	**Max Read Request Size** Default Value: 000b Access: RO Functions that do not generate Read Requests larger than 128 bytes and Functions that do not generate Read Requests on their own behalf are permitted to implement this field as Read Only (RO) with a value of 000b.
	11	**Enable No Snoop** Default Value: 0b Access: RO This bit is permitted to be hardwired to 0b if a Function would never Set the No Snoop attribute in transactions it initiates. The graphics device never generates a PCI Express TLP.
	10	**Aux Power PM Enable** Default Value: 0b Access: RO Functions that do not implement this capability hardwire this bit to 0b.

DEVICECTL_0_2_0_PCI - PCI Express Device Control

9	**Phantom Functions Enable**	
	Default Value:	0b
	Access:	RO
	Functions that do not implement this capability hardwire this bit to 0b.	
8	**Extended Tag Field Enable**	
	Default Value:	0b
	Access:	RO
	Functions that do not implement this capability hardwire this bit to 0b.	
7:5	**Max Payload Size**	
	Default Value:	000b
	Access:	RO
	Functions that support only the 128-byte max payload size are permitted to hardwire this field to 000b.	
4	**Enable Relaxed Ordering**	
	Default Value:	0b
	Access:	RO
	A Function is permitted to hardwire this bit to 0b if it never sets the Relaxed Ordering attribute in transactions it initiates as a Requester. The graphics device never generates a PCI Express TLP.	
3	**Unsupported Request Response Enable**	
	Default Value:	0b
	Access:	RO
	A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b.	
2	**Fatal Error Enable**	
	Default Value:	0b
	Access:	RO
	A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b.	
1	**Non-Fatal Error Enable**	
	Default Value:	0b
	Access:	RO
	A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b.	

DEVICECTL_0_2_0_PCI - PCI Express Device Control

	0	**Correctable Error Enable** Default Value: 0b Access: RO A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b.

PCI Express Device Status

DEVICESTS_0_2_0_PCI - PCI Express Device Status

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	16
Address:	0007Ah

This register shows the status of the PCIe Device.

DWord	Bit	Description
0	5	**Transactions Pending** Default Value: 0b Access: RO 1: The Function has issued one or more non-posted transactions which have not been completed, including non-posted transactions that a target has terminated with Retry. Must be cleared ipon completion of FLR. 0: All non-posted transactions have been completed.
	4	**AUX Power Detected** Default Value: 0b Access: RO Functions that require Aux power report this bit as Set if Aux power is detected by the Function. The integrated graphics device does not require Aux power.
	3	**Unsupported Request Detected** Default Value: 0b Access: RO This bit indicates the Function received an Unsupported Request. The Root Complex Integrated Endpoint graphics device does not use the PCI Express error reporting mechanism.
	2	**Fatal Error Detected** Default Value: 0b Access: RO This bit indicates the status of Fatal errors detected. The Root Complex Integrated Endpoint graphics device does not use the PCI Express error reporting mechanism.
	1	**Non-Fatal Error Detected** Default Value: 0b Access: RO This bit indicates the status of Non-Fatal errors detected. The Root Complex Integrated Endpoint graphics device does not use the PCI Express error reporting mechanism.

DEVICESTS_0_2_0_PCI - PCI Express Device Status

	0	**Correctable Error Detected** Default Value: 0b Access: RO This bit indicates the status of Correctable errors detected. The Root Complex Integrated Endpoint graphics device does not use the PCI Express error reporting mechanism.

PCI Status

PCISTS2_0_2_0_PCI - PCI Status

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000010
Size (in bits):	16
Address:	00006h

PCISTS is a 16-bit status register that reports the occurrence of a PCI compliant master abort and PCI compliant target abort. PCISTS also indicates the DEVSEL# timing that has been set by the IGD.

DWord	Bit	Description
0	15	**Detected Parity Error** Default Value: 0b Access: RO Since the IGD does not detect parity, this bit is always hardwired to 0.
	14	**Signaled System Error** Default Value: 0b Access: RO The IGD never asserts SERR#, therefore this bit is hardwired to 0.
	13	**Received Master Abort Status** Default Value: 0b Access: RO The IGD never gets a Master Abort, therefore this bit is hardwired to 0.
	12	**Received Target Abort Status** Default Value: 0b Access: RO The IGD never gets a Target Abort, therefore this bit is hardwired to 0.
	11	**Signaled Target Abort Status** Default Value: 0b Access: RO Hardwired to 0. The IGD does not use target abort semantics.
	10:9	**DEVSEL Timing** Default Value: 00b Access: RO Hardwired to 00.

PCISTS2_0_2_0_PCI - PCI Status

8	**Master Data Parity Error Detected** Default Value: 0b Access: RO Since Parity Error Response is hardwired to disabled, and the IGD does not do any parity detection, this bit is hardwired to 0.
7	**Fast Back-to-Back** Default Value: 0b Access: RO Hardwired to 0.
6	**User Defined Format** Default Value: 0b Access: RO Hardwired to 0.
5	**66 MHz PCI Capable** Default Value: 0b Access: RO Hardwired to 0.
4	**Capability List** Default Value: 1b Access: RO This bit is hardwired to 1 to indicate that the register at 34h provides an offset into the function's PCI Configuration Space containing a pointer to the location of the first item in the list.
3	**Interrupt Status** Default Value: 0b Access: RO Variant This bit reflects the state of the interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the devices INTx# signal be asserted.
2:0	**Reserved** Format: MBZ

PCU Interrupt Definition

PCU Interrupt Definition	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	444E0h-444EFh
Name:	PCU Interrupts
ShortName:	PCU_INTERRUPT
Power:	PG0
Reset:	soft

This table indicates which events are mapped to each bit of the PCU Interrupt registers.
0x444E0 = ISR
0x444E4 = IMR
0x444E8 = IIR
0x444EC = IER

DWord	Bit	Description
0	31:26	**Unused_Int_31_26** These interrupts are currently unused.
	25	**PCU_Pcode2driver_Mailbox_Event**
	24	**PCU_Thermal_Event**
	23:0	**Unused_Int_23_0** These interrupts are currently unused.

Pending Head Pointer Register

UHPTR - Pending Head Pointer Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02134h-02137h
Name:	Pending Head Pointer Register
ShortName:	UHPTR_RCSUNIT
Address:	12134h-12137h
Name:	Pending Head Pointer Register
ShortName:	UHPTR_VCSUNIT0
Address:	1A134h-1A137h
Name:	Pending Head Pointer Register
ShortName:	UHPTR_VECSUNIT
Address:	1C134h-1C137h
Name:	Pending Head Pointer Register
ShortName:	UHPTR_VCSUNIT1
Address:	22134h-22137h
Name:	Pending Head Pointer Register
ShortName:	UHPTR_BCSUNIT

Programming Notes	Source
Once SW uses UHPTR to preempt the existing workload, should explicitly program MI_SET_CONTEXT to save the preempted context status before submitting the new workload. In case SW doesn't want to save the state of the preempted context, it should at the minimum program RS_PREEMPT_STATUS to 0x0 so that the register status doesn't interfere with the new workloads.	RenderCS

DWord	Bit	Description
0	31:3	**Head Pointer Address** Format: GraphicsAddress[31:3] **Description** This register represents the GFX address offset where execution should continue in the ring buffer following execution of a Preemptable Command. Refer to the Preemption section for the list of preemptable commands supported in ring buffer mode of scheduling.

UHPTR - Pending Head Pointer Register

	2:1	**Reserved** Format: MBZ
	0	**Head Pointer Valid** **Description** This bit is set by the software to request a pre-emption. It is reset by hardware when a Preemptable command is parsed by the command streamer. The hardware uses the head pointer programmed in this register at the time the reset is generated. Refer to the Preemption section for the list of preemptable commands supported in ring buffer mode of scheduling. This bit is treated as set by command streamer only when arbitration is not disabled using MI_ARB_ON_OFF command. Preemption will not occur on MI_ARB_CHEK command when UHPTR is valid if the arbitration is disabled using MI_ARB_ON_OFF command.

Value	Name	Description
0	InValid	No valid updated head pointer register, resume execution at the current location in the ring buffer
1	Valid	Indicates that there is an updated head pointer programmed in this register

Performance Counter 1 LSB

PERFCNT1_LSB - Performance Counter 1 LSB		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	091B8h	
GT implements 2 general purpose counters each with 44-bits, each counter can be programmed to count one main event out of set of events (see the event list). Some events are simple duration events and some are edge detects (0=>1 transition is counted). The nature of the event is also programmed to the register that allocates the counter value.		
DWord	**Bit**	**Description**
0	31:0	**Counter Value (LSB - 31:0 of 43:0)** Access: RO The Counter Value: This is the field where the counter value can be observed via a simple read to the register.

Performance Counter 1 MSB

PERFCNT1_MSB - Performance Counter 1 MSB		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	091BCh	
GT implements 2 general purpose counters each with 44-bits, each counter can be programmed to count one main event out of set of events (see the event list). Some events are simple duration events and some are edge detects (0=>1 transition is counted). The nature of the event is also programmed to the register that allocates the counter value.		
DWord	**Bit**	**Description**
0	31	**Counter 1 Enable** Access: R/W Counter#1 Enable. 0: Counter is disabled. The count value is not deterministic. 1: Counter is enabled. Once enabled, the counter is activated if the global enable (from NCU) is also asserted.
	30	**Overflow Enable** Access: R/W Overflow Enable. 0: Overflow reporting is enabled. 1: Overflow reporting is disabled.
	29	**Edge Detect** Access: R/W Edge Detect: 0: Edge detect is enabled. 1: Edge detect is disabled.
	28	**Counter Clear** Access: R/W Counter Clear.
	27:20	**Event Selection** Access: R/W Event Selection: The event list (see attached). Used as a MUX control to select the event to Counter.

PERFCNT1_MSB - Performance Counter 1 MSB

	19:12	**RSVD** Access: RO
	11:0	**Counter Value (MSB - 43:32 of 43:0)** Access: RO The Counter Value: This is the field where the counter value can be observed via a simple read to the register.

Performance Counter 2 LSB

PERFCNT2_LSB - Performance Counter 2 LSB		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	091C0h	
GT implements 2 general purpose counters each with 44-bits, each counter can be programmed to count one main event out of set of events (see the event list). Some events are simple duration events and some are edge detects (0=>1 transition is counted). The nature of the event is also programmed to the register that allocates the counter value.		
DWord	**Bit**	**Description**
0	31:0	**Counter Value (LSB - 31:0 of 43:0)** Access: RO The Counter Value: This is the field where the counter value can be observed via a simple read to the register.

Performance Counter 2 MSB

PERFCNT2_MSB - Performance Counter 2 MSB		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	091C4h	
GT implements 2 general purpose counters each with 44-bits, each counter can be programmed to count one main event out of set of events (see the event list). Some events are simple duration events and some are edge detects (0=>1 transition is counted). The nature of the event is also programmed to the register that allocates the counter value.		
DWord	**Bit**	**Description**
0	31	**Counter 2 Enable** Access: R/W Counter#2 Enable. 0: Counter is disabled. The count value is not deterministic. 1: Counter is enabled. Once enabled, the counter is activated if the global enable (from NCU) is also asserted.
	30	**Overflow Enable** Access: R/W Overflow Enable. 0: Overflow reporting is enabled. 1: Overflow reporting is disabled.
	29	**Edge Detect** Access: R/W Edge Detect. 0: Edge detect is enabled. 1: Edge detect is disabled.
	28	**Counter Clear** Access: R/W Counter Clear.
	27:20	**Event Selection** Access: R/W Event Selection: The event list (see attached). Used as a MUX control to select the event to Counter.

PERFCNT2_MSB - Performance Counter 2 MSB		
	19:12	**RSVD** Access: RO
	11:0	**Counter Value (MSB - 43:32 of 43:0)** Access: RO The Counter Value: This is the field where the counter value can be observed via a simple read to the register.

Performance Matrix Events LSB

PERFMATRIX_LSB - Performance Matrix Events LSB		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	091C8h	
Performance Matrix Events		
DWord	**Bit**	**Description**
0	31	**NONE - No Details as to Snoop related infor** Access: R/W NONE - No Details as to Snoop related infor.
	30	**NID7** Access: R/W NID 7.
	29	**NID 6** Access: R/W NID 6.
	28	**NID 5** Access: R/W NID 5.
	27	**NID 4** Access: R/W NID 4.
	26	**NID 3** Access: R/W NID 3.
	25	**NID 2** Access: R/W NID 2.

PERFMATRIX_LSB - Performance Matrix Events LSB

	24	**NID1** Access: R/W NID 1.
	23	**NID0** Access: R/W NID 0.
	22	**Local Node** Access: R/W Local Node.
	21	**F-STATE** Access: R/W F-STATE.
	20	**S-State** Access: R/W S-STATE.
	19	**E-STATE** Access: R/W E-STATE.
	18	**M-STATE** Access: R/W M-STATE.
	17	**No Supplier Details** Access: R/W No Supplier Details.
	16	**Snoop Response from Uncore** Access: R/W Account for any snoop response from Uncore.
	15	**IDI requests** Access: R/W Any - any requests that crosses IDI.

PERFMATRIX_LSB - Performance Matrix Events LSB

	14:12	**ECORSVD** Access: R/W ECORSVD - For future changes.
	11	**WCIL AND WCILF** Access: R/W Write Combining.
	10	**LOCK** Access: R/W Locks - count locks & split lock requests.
	9	**MLC Prefetch to LLC - Code** Access: R/W MLC prefetch to LLC - Code.
	8	**LLCRFO** Access: R/W MLC prefetch to LLC - RFO.
	7	**MLC Prefetch to LLC - Data** Access: R/W MLC prefetch to LLC - Load (exclude LRUhints).
	6	**MPL RFOs** Access: R/W PF Ifetch = MPL Fetches.
	5	**PF Ifetch** Access: R/W PF Ifetch = MPL Fetches.
	4	**MPL Reads** Access: R/W PF Data Rd = MPL Reads.
	3	**Write Back** Access: R/W Writeback = MLC_EVICT/DCUWB.

PERFMATRIX_LSB - Performance Matrix Events LSB		
	2	**Demand Ifetch** Access: R/W Demand Ifetch = IFU Fetches.
	1	**Demand RFO** Access: R/W Demand RFO = DCU RFOs.
	0	**Demand Data Rd** Access: R/W Demand Data Rd = DCU reads (exclude partials).

Performance Matrix Events MSB

PERFMATRIX_MSB - Performance Matrix Events MSB

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	091CCh

Performance Matrix Events

DWord	Bit	Description
0	31:6	**RSVD** Access: RO
	5	**NON Dram** Access: R/W Non Dram - Target was non-DRAM system address.
	4	**Hit Modified** Access: R/W A snoop was needed and it HitMed in local or remote cache. HitM denotes a cache-line was modified before snoop effect. This includes: • Snoop HitM w/ Invalidation and WB (LLC miss, CRD/DRD) • Snoop Forward Modified w/ Invalidation (LLC Hit/Miss, RFO) • Snoop MtoS (LLC Hit, CRD/DRD)
	3	**Hit with Forward** Access: R/W A snoop was needed and data was Forwarded from a remote socket: • Snoop Forward Clean, Left Shared (LLC Miss, CRD/DRD)
	2	**Hit No Forward** Access: R/W A snoop was needed and it Hits in at least one snooped cache. Hit denotes a cache-line was valid before snoop effect. This includes: • Snoop Hit w/ Invalidation (LLC Hit, RFO) • Snoop Hit, Left Shared (LLC Hit/Miss, CRD/DRD) • Snoop Forward Clean w/ Invalidation (LLC Miss, RFO)

PERFMATRIX_MSB - Performance Matrix Events MSB		
	1	**SNOOP Miss** Access: R/W A snoop was need and it missed all snooped caches: • For LLC Hit, ReslHitI was returned by all cores • For LLC Miss, RspI was returned by all sockets
	0	**NO Snoop Was needed** Access: R/W No snoop was neeeded to satisfy the request.

Per-process GTT Page Directory Pointer 0

PDP0 - Per-process GTT Page Directory Pointer 0	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	02270h-02277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_RCSUNIT
Address:	0C3C0h-0C3C7h
Address:	12270h-12277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VCSUNIT0
Address:	1A270h-1A277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VECSUNIT
Address:	1C270h-1C277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VCSUNIT1
Address:	22270h-22277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_BCSUNIT
The bitwise definition of this register matches the PDP0/PML4/PASI Descriptor register in GAM	

DWord	Bit	Description
0	63:0	**PDP0 Descriptor** PDP0/PML4/PASID: This register can contain three values which depend on the element descriptor definition. PASID[19:0]: Populated in the first 20bits of the register and selected when Advanced Context flag is set. PML4[38:12]: Pointer to base address of PML4 and selected when Legacy Context flag is set and 64b address support is selected PDP0[38:12]: Pointer to one of the four page directory pointer (lowest) and defines the first 0-1GB of memory mapping *Note: This is a guest physical address* (unused bits need to be populated as 0's)

Per-process GTT Page Directory Pointer 1

PDP1 - Per-process GTT Page Directory Pointer 1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	02278h-0227Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_RCSUNIT
Address:	0C3C8h-0C3CFh
Address:	12278h-1227Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_VCSUNIT0
Address:	1A278h-1A27Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_VECSUNIT
Address:	1C278h-1C27Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_VCSUNIT1
Address:	22278h-2227Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_BCSUNIT

The bitwise definition of this register matches the PDP1 Descriptor register in GAM

DWord	Bit	Description
0	63:0	**PDP1 Descriptor** Format: GraphicsAddress[63:0] PDP1 [63:12]: Pointer to one of the four page directory pointer (lowest+1) and defines the first 1-2GB of memory mapping *Note: This is a guest physical address* (unused bits need to be populated as 0's)

Per-process GTT Page Directory Pointer 2

PDP2 - Per-process GTT Page Directory Pointer 2	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	02280h-02287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_RCSUNIT
Address:	0C3D0h-0C3D7h
Address:	12280h-12287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VCSUNIT0
Address:	1A280h-1A287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VECSUNIT
Address:	1C280h-1C287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VCSUNIT1
Address:	22280h-22287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_BCSUNIT

The bitwise definition of this register matches the PDP2 Descriptor register in GAM

DWord	Bit	Description
0	63:0	**PDP2 Descriptor** Format: GraphicsAddress[63:0] PDP2 [63:12]: Pointer to one of the four page directory pointer (lowest+2) and defines the first 2-3GB of memory mapping *Note: This is a guest physical address* (unused bits need to be populated as 0's)

Per-process GTT Page Directory Pointer 3

PDP3 - Per-process GTT Page Directory Pointer 3	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	02288h-0228Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_RCSUNIT
Address:	0C3D8h-0C3DFh
Address:	12288h-1228Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VCSUNIT0
Address:	1A288h-1A28Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VECSUNIT
Address:	1C288h-1C28Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VCSUNIT1
Address:	22288h-2228Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_BCSUNIT

The bitwise definition of this register matches the PDP3 Descriptor register in GAM

DWord	Bit	Description
0	63:0	**PDP3 Descriptor** Format: GraphicsAddress[63:0] PDP3 [63:12]: Pointer to one of the four page directory pointer (lowest+3) and defines the first 3-4GB of memory mapping *Note: This is a guest physical address* (unused bits need to be populated as 0's)

PIPE_BOTTOM_COLOR

PIPE_BOTTOM_COLOR

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank OR pipe disabled

Address:	70034h-70037h
Name:	Pipe Bottom Color
ShortName:	PIPE_BOTTOM_COLOR_A
Power:	PG1
Reset:	soft

Address:	71034h-71037h
Name:	Pipe Bottom Color
ShortName:	PIPE_BOTTOM_COLOR_B
Power:	PG2
Reset:	soft

Address:	72034h-72037h
Name:	Pipe Bottom Color
ShortName:	PIPE_BOTTOM_COLOR_C
Power:	PG2
Reset:	soft

There is one instance of this register format per each pipe A/B/C.
This register sets the color that appears underneath the bottom most plane in the pipe blender Z-order.
The value for each color channel is represented in an unsigned 0.10 format with 0 integer and 10 fractional bits.

DWord	Bit	Description
0	31	**Pipe Gamma Enable** This bit enables pipe gamma correction for the bottom color. Value: 0b — Name: Disable Value: 1b — Name: Enable

PIPE_BOTTOM_COLOR

	30	**Pipe CSC Enable** This bit enables pipe color space conversion for the bottom color. **Value** / **Name** 0b – Disable 1b – Enable
	29:20	**V R Bottom Color** Format: U0.10 This field sets the bottom color for the V or Red channel.
	19:10	**Y G Bottom Color** Format: U0.10 This field sets the bottom color for the Y or Green channel.
	9:0	**U B Bottom Color** Format: U0.10 This field sets the bottom color for the U or Blue channel.

PIPE_FLIPCNT

PIPE_FLIPCNT	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	70044h-70047h
Name:	Pipe Flip Count
ShortName:	PIPE_FLIPCNT_A
Power:	PG1
Reset:	soft
Address:	71044h-71047h
Name:	Pipe Flip Count
ShortName:	PIPE_FLIPCNT_B
Power:	PG2
Reset:	soft
Address:	72044h-72047h
Name:	Pipe Flip Count
ShortName:	PIPE_FLIPCNT_C
Power:	PG2
Reset:	soft

There is one instance of this register format per each pipe A/B/C.

DWord	Bit	Description
0	31:0	**Pipe Flip Counter** **Description** This field provides read back of the display pipe flip counter. The counter increments on the start of each flip to plane 1 of this pipe. The start of flip is when the plane surface address is updated, not when the flip completes. The flip can be through command streamer asynchronous and synchronous flips or MMIO writes to the plane 1 surface address. It rolls over back to 0 after (2^32)-1 flips.

PIPE_FLIPTMSTMP

PIPE_FLIPTMSTMP	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	7004Ch-7004Fh
Name:	Pipe Flip Time Stamp
ShortName:	PIPE_FLIPTMSTMP_A
Power:	PG1
Reset:	soft
Address:	7104Ch-7104Fh
Name:	Pipe Flip Time Stamp
ShortName:	PIPE_FLIPTMSTMP_B
Power:	PG2
Reset:	soft
Address:	7204Ch-7204Fh
Name:	Pipe Flip Time Stamp
ShortName:	PIPE_FLIPTMSTMP_C
Power:	PG2
Reset:	soft

There is one instance of this register format per each pipe A/B/C.

DWord	Bit	Description
0	31:0	**Pipe Flip Time Stamp** **Description** This field provides read back of the display pipe flip time stamp. The time stamp value is sampled on the start of each flip to plane 1 of this pipe. The start of flip is when the plane surface address is updated, not when the flip completes. The flip can be through command streamer asynchronous and synchronous flips or MMIO writes to the plane 1 surface address. The TIMESTAMP_CTR register has the current time stamp value.

PIPE_FRMCNT

PIPE_FRMCNT	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	70040h-70043h
Name:	Pipe Frame Count
ShortName:	PIPE_FRMCNT_A
Power:	PG1
Reset:	soft
Address:	71040h-71043h
Name:	Pipe Frame Count
ShortName:	PIPE_FRMCNT_B
Power:	PG2
Reset:	soft
Address:	72040h-72043h
Name:	Pipe Frame Count
ShortName:	PIPE_FRMCNT_C
Power:	PG2
Reset:	soft

There is one instance of this register format per each pipe A/B/C.

DWord	Bit	Description
0	31:0	**Pipe Frame Counter** Provides read back of the display pipe frame counter. This counter increments on every start of vertical blank and rolls over back to 0 after (2^32)-1 frames.

PIPE_FRMTMSTMP

PIPE_FRMTMSTMP	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	70048h-7004Bh
Name:	Pipe Frame Time Stamp
ShortName:	PIPE_FRMTMSTMP_A
Power:	PG1
Reset:	soft
Address:	71048h-7104Bh
Name:	Pipe Frame Time Stamp
ShortName:	PIPE_FRMTMSTMP_B
Power:	PG2
Reset:	soft
Address:	72048h-7204Bh
Name:	Pipe Frame Time Stamp
ShortName:	PIPE_FRMTMSTMP_C
Power:	PG2
Reset:	soft

There is one instance of this register format per each pipe A/B/C.

DWord	Bit	Description
0	31:0	**Pipe Frame Time Stamp** This field provides read back of the display pipe frame time stamp. The time stamp value is sampled at every start of vertical blank. The TIMESTAMP_CTR register has the current time stamp value.

PIPE_MISC

PIPE_MISC	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank OR pipe disabled
Address:	70030h-70033h
Name:	Pipe Miscellaneous
ShortName:	PIPE_MISC_A
Power:	PG1
Reset:	soft
Address:	71030h-71033h
Name:	Pipe Miscellaneous
ShortName:	PIPE_MISC_B
Power:	PG2
Reset:	soft
Address:	72030h-72033h
Name:	Pipe Miscellaneous
ShortName:	PIPE_MISC_C
Power:	PG2
Reset:	soft

There is one instance of this register format per each pipe A/B/C.

DWord	Bit	Description
0	31:30	**Stereo Mask Pipe Int** This field controls which pipe vertical timing (vertical blank, scan line, and vertical sync) events will be reported in interrupts during stereo 3D mode.

Value	Name	Description
00b	Mask None	No masking. Report both the left and right eye vertical events.
01b	Mask Left	Mask the left eye vertical events. Only report right eye events.
10b	Mask Right	Mask the right eye vertical events. Only report left eye events.
11b	Reserved	Reserved

Restriction

PIPE_MISC

		Restriction : This field must be programmed prior to enabling stereo 3D mode and must not be changed while stereo 3D is enabled. In the stacked frame mode the vertical sync is not generated in the gap between left and right eye images, and the scan line count increments across the entire tall frame, so masking may cause unexpected behavior for those events.
	29:28	**Stereo Mask Pipe Render** This field controls which pipe vertical timing (vertical blank, scan line, and vertical sync) events will be reported in render responses during stereo 3D mode.

Value	Name	Description
00b	Mask None	No masking. Report both the left and right eye vertical events.
01b	Mask Left	Mask the left eye vertical events. Only report right eye events.
10b	Mask Right	Mask the right eye vertical events. Only report left eye events.
11b	Reserved	Reserved

Restriction
Restriction : This field must be programmed prior to enabling stereo 3D mode and must not be changed while stereo 3D is enabled. In the stacked frame mode the vertical sync is not generated in the gap between left and right eye images, and the scan line count increments across the entire tall frame, so masking may cause unexpected behavior for those events.

	27:26	**Reserved**
	25:24	**Reserved**
	23:22	**Reserved**
	21	**Change Mask for Register Write** This field controls change tracking for the pipe register write. Change tracking can be used by PSR/SRD and WD.

Value	Name
0b	Not Masked
1b	Masked

	20	**Change Mask for Vblank Vsync Int** This field controls change tracking for the vblank or vsync interrupt enable. Change tracking can be used by PSR/SRD and WD.

Value	Name
0b	Not Masked
1b	Masked

	19	**Reserved**
	18	**Reserved**
	17	**Reserved**
	16	**Reserved**

PIPE_MISC

15:14 Rotation Info

This field indicates to internal KVMR screen capture that the display has been rotated through software or hardware rotation.

Select the closest value if the rotation is not an exact multiple of 90 degrees.

Hardware rotation of the display output is controlled through the plane control registers, not through this field.

Value	Name	Description
00b	None	No rotation on this pipe
01b	90	90 degree rotation on this pipe
10b	180	180 degree rotation on this pipe
11b	270	270 degree rotation on this pipe

Restriction
Restriction : This field must be programmed in order for internal KVMR screen capture to work correctly when display is rotated by software or hardware.

13:12 Reserved

Format:	MBZ

11 Pipe output color space select

This field indicates the output color space.

This field affects the values of the pipe border and some capture functions.

This field does not affect the planes, pipe CSC, or ports.

Value	Name
0b	RGB
1b	YUV

Restriction
Restriction : This field must be set to match the color space that will be output from the pipe CSC or output from the planes if they pipe CSC is bypassed.

10 xvYCC Color Range Limit

This field limits the color range of the pipe output to 1 to 254 for 8-bit components, 4 to 1019 for 10bit components, and 16 to 4079 for 12-bit components.

Values outside of the range will be clamped to fit within the range.

Value	Name	Description
0b	Full	Do not limit the range
1b	Limit	Limit range

9:8 Reserved

Format:	MBZ

PIPE_MISC

7:5 Dithering BPC

This field selects the number of bits per color to be used in dithering.

Value	Name	Description
000b	8 bpc	8 bits per color
001b	10 bpc	10 bits per color
010b	6 bpc	6 bits per color
Others	Reserved	Reserved

Programming Notes
When dithering is enabled, the value selected here should match the bits per color selected in the Transcoder DDI Function Control register attached to this pipe.

4 Dithering enable

This field enables dithering.

Value	Name
0b	Disable
1b	Enable

3:2 Dithering type

This field selects the dithering type.

Value	Name	Description
00b	Spatial	Spatial
01b	ST1	Spatio-Temporal 1
10b	ST2	Spatio-Temporal 2
11b	Temporal	Temporal

1 Reserved

Format:	MBZ

0 BFI enable

This field enables black frame insertion.

Value	Name
0b	Disable
1b	Enable

PIPE_SCANLINE

PIPE_SCANLINE

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	RO
Size (in bits):	32

Address:	70000h-70003h
Name:	Pipe Scan Line
ShortName:	PIPE_SCANLINE_A
Power:	PG1
Reset:	soft

Address:	71000h-71003h
Name:	Pipe Scan Line
ShortName:	PIPE_SCANLINE_B
Power:	PG2
Reset:	soft

Address:	72000h-72003h
Name:	Pipe Scan Line
ShortName:	PIPE_SCANLINE_C
Power:	PG2
Reset:	soft

This register enables the read back of the pipe vertical line counter.
The value increments at the leading edge of HSYNC.
The value resets to line zero at the first active line of the display.
In interlaced display timings, the scan line counter provides the current line in the field. One field can have a total number of lines that is one greater than the other field.

DWord	Bit	Description
0	31	**Current Field** This is an indication of the current display field.

Value	Name	Description
0b	Odd	First field (odd field)
1b	Even	Second field (even field)

DWord	Bit	Description
	30:13	**Reserved**

PIPE_SCANLINE		
	12:0	**Line Counter for Display** This is an indication of the current display scan line. **Programming Notes** The line count value is from the display output timing generator, representing the scan line currently being output to a receiver. Due to buffering within the display engine, the line being fetched (read) from the frame buffer is not directly linked to the line being output. It is possible for the fetched line to be hundreds of lines ahead of the timing generator output line.

PIPE_SCANLINECOMP

PIPE_SCANLINECOMP	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	70004h-70007h
Name:	Pipe Scan Line Compare
ShortName:	PIPE_SCANLINECOMP_A
Power:	PG1
Reset:	soft
Address:	71004h-71007h
Name:	Pipe Scan Line Compare
ShortName:	PIPE_SCANLINECOMP_B
Power:	PG2
Reset:	soft
Address:	72004h-72007h
Name:	Pipe Scan Line Compare
ShortName:	PIPE_SCANLINECOMP_C
Power:	PG2
Reset:	soft

This register is used to initiate a display scan line compare. This MMIO driven scan line compare can not be used at the same time as the command streamer driven scan line compare on the same pipe. When this register is written with the Initiate Compare bit set to 1b, the Display Engine (DE) will start comparing the display pipe or plane (selectable) current scan line value (current scan line) with the start scan line value (current scan line >= start scan line) and the end scan line value (current scan line <= end scan line) to decide if the pipe scan line is inside or outside the scan line window of interest. DE will wait until the current scan line is either outside (Inclusive mode) or inside (Exclusive mode) the scan line window, then trigger a scan line event and stop any further comparing. The scan line event can cause display to send a scan line compare response to the command streamer, (used for releasing a MI_WAIT_FOR_EVENT on scan line window), if unmasked in the DERRMR mask register 0x44050. The scan line event can also cause display to generate a scan line compare interrupt, if the interrupt registers are configured for that. The value programmed should be the desired value - 1, so for scan line 0, the value programmed is vertical total, and for scan line 1, the value programmed is 0. The programmable range can include the vertical blank. In interlaced display timings, the current scan line is the current line of the current interlaced field. Either MMIO or a MI_LOAD_REGISTER_IMM command can be used to unmask the scan line render response 0x44050. That can be done anytime before programming this register. There is one instance of this register per pipe.

PIPE_SCANLINECOMP

Restriction
Restriction : A new scan line compare must not be started until after the previous compare has finished. The end scan line value must be greater than or equal to the start scan line value. When using LRI care must be taken to follow all the programming rules for LRI targetting the display engine.

DWord	Bit	Description
0	31	**Initiate Compare** This field initiates the scan line compare. When this register is written with this bit set to 1b, the display engine will do one complete comparison cycle, trigger a scan line event, then stop comparing. **Value / Name** 0b – Do nothing 1b – Initiate compare **Restriction** Restriction : Do not write this register again until after any previous scan line compare has completed.
	30	**Inclusive Exclusive Select** This field selects whether the scan line compare is done in inclusive mode, where display triggers the scan line event when outside the scan line window, or inclusive mode, where display triggers when inside the window. **Value / Name / Description** 0b – Exclusive – Exclusive mode: trigger scan line event when inside the scan line window 1b – Inclusive – Inclusive mode: trigger scan line event when outside the scan line window
	29	**Counter Select** This field selects whether the scan line compare is done using the pipe timing generator scanline counter or a plane scanline counter. The pipe timing generator counts the scanlines being output from display. The plane counts the scan lines being fetched from the frame buffer. **Value / Name / Description** 0b – Timing generator – Use the scanline count from the pipe timing generator 1b – Plane 1 – Use the scanline count from plane 1 **Programming Notes** Due to buffering within the display engine, the line being fetched from the frame buffer is not directly linked to the line being output. It is possible for the fetched line to be hundreds of lines ahead of the timing generator output line. The plane scan line count more closely represents what data is currently being fetched by the plane.
	28:16	**Start Scan Line** This field specifies the starting scan line number of the scan line window.

PIPE_SCANLINECOMP

	15	**Render Response Destination** This bit indicates what destination to send the scan line event render response to. Value / Name / Description 0b / CS / Send scan line event response to CS 1b / BCS / Send scan line event response to BCS
	14:13	**Reserved**
	12:0	**End Scan Line** This field specifies the ending scan line number of the scan line window.

PIPE_SRCSZ

PIPE_SRCSZ	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank
Address:	6001Ch-6001Fh
Name:	Pipe Source Image Size
ShortName:	PIPE_SRCSZ_A
Power:	PG1
Reset:	soft
Address:	6101Ch-6101Fh
Name:	Pipe Source Image Size
ShortName:	PIPE_SRCSZ_B
Power:	PG2
Reset:	soft
Address:	6201Ch-6201Fh
Name:	Pipe Source Image Size
ShortName:	PIPE_SRCSZ_C
Power:	PG2
Reset:	soft

There is one instance of this register for each pipe.

Programming Notes

In VGA display mode, this register is ignored and the VGA size from the VGA registers is used instead.

DWord	Bit	Description
0	31:29	**Reserved** Format: MBZ
	28:16	**Horizontal Source Size** This field specifies Horizontal Source Size. This determines the horizontal size of the image created by the display planes. This field is programmed to the number of pixels desired minus one. **Restriction** Restriction : This register must always be programmed to the same value as the Horizontal Active, except

PIPE_SRCSZ

		when panel fitting is enabled. Horizontal source sizes larger than 4096 pixels can not be used when Frame Buffer Compression or Panel Fitting are enabled. Horizontal source size should be atleast 8 pixels when panel fitting is enabled.
	15:12	**Reserved** Format: MBZ
	11:0	**Vertical Source Size** This field specifies Vertical Source Size. This determines the vertical size of the image created by the display planes. This field is programmed to the number of lines desired minus one. **Restriction** Restriction : Vertical source sizes larger than 4096 lines are not supported. This register must always be programmed to the same value as the Vertical Active, except when panel fitting is enabled. Vertical source size should be atleast 8 lines when panel fitting is enabled.

PLANE_AUX_DIST

PLANE_AUX_DIST	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled; after armed
Double Buffer Armed By:	Write to PLANE_SURF or plane not enabled
Address:	701C0h-701C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_1_A
Power:	PG1
Reset:	soft
Address:	702C0h-702C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_2_A
Power:	PG1
Reset:	soft
Address:	703C0h-703C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_3_A
Power:	PG1
Reset:	soft
Address:	711C0h-711C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_1_B
Power:	PG2
Reset:	soft
Address:	712C0h-712C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_2_B
Power:	PG2
Reset:	soft

PLANE_AUX_DIST

Address:	713C0h-713C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_3_B
Power:	PG2
Reset:	soft

Address:	721C0h-721C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_1_C
Power:	PG2
Reset:	soft

Address:	722C0h-722C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_2_C
Power:	PG2
Reset:	soft

Address:	723C0h-723C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_3_C
Power:	PG2
Reset:	soft

This register is used to specify the distance from the main surface base address and the stride of the auxiliary surface.
Unlike the surface base address, this register value cannot be updated through flips.

DWord	Bit	Description
0	31:12	**Auxiliary Surface Distance** **Description** This offset specifies the distance (in multiple of 4K bytes) of the Auxiliary surface from the main surface. When using YUV planar formats this field represents the distance of UV surface. When using compressed surface this field represents the distance of control surface. In the graphics address space, the auxiliary surface should always be allocated after the main surface, and the programmed auxiliary surface distance must not be negative. **Restriction** It must be 4K page aligned.Allocate an extra 136 Page Table Entries (PTEs) beyond the end of the displayed surface. If 180 or 270 plane rotation capability is required, allocate an exra 136 PTEs before the begining of the surface. When address range limits are reached, wrap around to finish allocating the extra PTEs. Only the PTEs will be used, not the pages themselves. The end of the surface cannot be within 136 PTEs of the end of the graphics memory.

PLANE_AUX_DIST		
	11:10	**Reserved**
	9:0	**Auxiliary Surface Stride** **Description** This field specifies the stride of the auxiliary surface. Refer to PLANE_STRIDE register for stride programming details. When using YUV planar formats this field represents the stride of UV surface. When using compressed surface this field represents the stride of the control surface. Restriction : When using render compressed surfaces, the programmed auxiliary surface stride should not exceed 8 (8 * 128 = 1024 bytes).

PLANE_BUF_CFG

PLANE_BUF_CFG	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank, plane not enabled, or pipe not enabled
Double Buffer Armed By:	Write to PLANE_SURF or plane not enabled
Address:	7017Ch-7017Fh
Name:	Cursor Buffer Config
ShortName:	CUR_BUF_CFG_A
Power:	PG1
Reset:	soft
Address:	70278h-7027Bh
Name:	Plane NV12 Buffer Config
ShortName:	PLANE_NV12_BUF_CFG_1_A
Power:	PG1
Reset:	soft
Address:	7027Ch-7027Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_1_A
Power:	PG1
Reset:	soft
Address:	70378h-7037Bh
Name:	Plane NV12 Buffer Config
ShortName:	PLANE_NV12_BUF_CFG_2_A
Power:	PG1
Reset:	soft
Address:	7037Ch-7037Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_2_A
Power:	PG1
Reset:	soft

PLANE_BUF_CFG

Address:	70478h-7047Bh
Name:	Plane NV12 Buffer Config
ShortName:	PLANE_NV12_BUF_CFG_3_A
Power:	PG1
Reset:	soft
Address:	7047Ch-7047Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_3_A
Power:	PG1
Reset:	soft
Address:	7117Ch-7117Fh
Name:	Cursor Buffer Config
ShortName:	CUR_BUF_CFG_B
Power:	PG2
Reset:	soft
Address:	71278h-7127Bh
Name:	Plane NV12 Buffer Config
ShortName:	PLANE_NV12_BUF_CFG_1_B
Power:	PG2
Reset:	soft
Address:	7127Ch-7127Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_1_B
Power:	PG2
Reset:	soft
Address:	71378h-7137Bh
Name:	Plane NV12 Buffer Config
ShortName:	PLANE_NV12_BUF_CFG_2_B
Power:	PG2
Reset:	soft
Address:	7137Ch-7137Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_2_B
Power:	PG2
Reset:	soft

PLANE_BUF_CFG	
Address:	71478h-7147Bh
Name:	Plane NV12 Buffer Config
ShortName:	PLANE_NV12_BUF_CFG_3_B
Power:	PG2
Reset:	soft
Address:	7147Ch-7147Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_3_B
Power:	PG2
Reset:	soft
Address:	7217Ch-7217Fh
Name:	Cursor Buffer Config
ShortName:	CUR_BUF_CFG_C
Power:	PG2
Reset:	soft
Address:	72278h-7227Bh
Name:	Plane NV12 Buffer Config
ShortName:	PLANE_NV12_BUF_CFG_1_C
Power:	PG2
Reset:	soft
Address:	7227Ch-7227Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_1_C
Power:	PG2
Reset:	soft
Address:	72378h-7237Bh
Name:	Plane NV12 Buffer Config
ShortName:	PLANE_NV12_BUF_CFG_2_C
Power:	PG2
Reset:	soft
Address:	7237Ch-7237Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_2_C
Power:	PG2
Reset:	soft

PLANE_BUF_CFG

Address:	72478h-7247Bh
Name:	Plane NV12 Buffer Config
ShortName:	PLANE_NV12_BUF_CFG_3_C
Power:	PG2
Reset:	soft

Address:	7247Ch-7247Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_3_C
Power:	PG2
Reset:	soft

Programming Notes

Buffer programming instructions are documented separately. For YUV planar (NV12 or P0xx) plane formats, the UV buffer allocation must be programmed in the Plane Buffer Config register and the Y buffer allocation must be programmed in the Plane NV12 Buffer Config register.

DWord	Bit	Description
0	31:26	**Reserved**
	25:16	**Buffer End** Default Value: 000h This field contains the buffer end position for this plane.
	15:10	**Reserved**
	9:0	**Buffer Start** Default Value: 000h This field contains the buffer start position for this plane.

PLANE_CTL

PLANE_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled; after armed
Double Buffer Armed By:	Write to PLANE_SURF or plane not enabled
Address:	70180h-70183h
Name:	Plane Control
ShortName:	PLANE_CTL_1_A
Power:	PG1
Reset:	soft
Address:	70280h-70283h
Name:	Plane Control
ShortName:	PLANE_CTL_2_A
Power:	PG1
Reset:	soft
Address:	70380h-70383h
Name:	Plane Control
ShortName:	PLANE_CTL_3_A
Power:	PG1
Reset:	soft
Address:	71180h-71183h
Name:	Plane Control
ShortName:	PLANE_CTL_1_B
Power:	PG2
Reset:	soft
Address:	71280h-71283h
Name:	Plane Control
ShortName:	PLANE_CTL_2_B
Power:	PG2
Reset:	soft

PLANE_CTL

Address:	71380h-71383h
Name:	Plane Control
ShortName:	PLANE_CTL_3_B
Power:	PG2
Reset:	soft

Address:	72180h-72183h
Name:	Plane Control
ShortName:	PLANE_CTL_1_C
Power:	PG2
Reset:	soft

Address:	72280h-72283h
Name:	Plane Control
ShortName:	PLANE_CTL_2_C
Power:	PG2
Reset:	soft

Address:	72380h-72383h
Name:	Plane Control
ShortName:	PLANE_CTL_3_C
Power:	PG2
Reset:	soft

The pipe scaler can be attached to a plane to scale the plane output before blending.

Restriction
Restriction : Refer to 'Plane Capability and Interoperability' page for plane capabilities and restrictions.

DWord	Bit	Description
0	31	**Plane Enable** When this bit is set, the plane will generate pixels for display. When cleared to zero, plane memory fetches cease and plane output is transparent. Value: 0b = Disable; 1b = Enable
	30	**Pipe Gamma Enable** This bit enables pipe gamma correction for the plane pixel data. Value: 0b = Disable; 1b = Enable

PLANE_CTL

29 **Remove YUV Offset**

This field controls whether the plane removes or preserves the 1/2 offset on U and V components when the source pixel format is YUV and the plane YUV to RGB CSC is disabled.

This bit has no effect on RGB source pixel formats

Value	Name	Description
0b	Remove	Remove 1/2 offset on UV components
1b	Preserve	Preserve 1/2 offset on UV compontents

28 **YUV Range Correction Disable**

Setting this bit disables the YUV range correction logic inside the plane.

The range correction logic is used to expand the compressed range YUV to full range YUV.

The Y channel is expanded from the 8 bit +16 to +235 range to full range. The U and V channels are expanded from the 8 bit -112 to +112 range to full range.

Extended range values will be preserved after the expansion.

This bit has no effect on RGB source pixel formats since they automatically bypass range correction.

Value	Name
0b	Enable
1b	Disable

27:24 **Source Pixel Format**

This field selects the source pixel format for the plane. Before entering the blender, each source format is converted to the pipe pixel format. The 8-bpp indexed format will always use the pipe palette. In planar YUV formats Y samples appear first in memory followed by interleaved UV samples. YUV 4:2:2 byte order is programmed separately. YUV 4:2:0 and YUV 4:4:4 byte order is not programmable. RGB color order is programmed separately for some formats.

Value	Name	Description
0000b	YUV 16-bit 4:2:2	YUV 16-bit 4:2:2 packed
0001b	NV12 YUV 4:2:0	NV12 YUV 4:2:0 Planar
0010b	RGB 32-bit 2:10:10:10	RGB 32-bit 2:10:10:10
0100b	RGB 32-bit 8:8:8:8	RGB 32-bit 8:8:8:8
0110b	RGB 64-bit 16:16:16:16 Float	RGB 64-bit 16:16:16:16 Floating Point
1000b	YUV 32-bit 4:4:4	YUV 32-bit 4:4:4 packed (8:8:8:8 MSB-X:Y:U:V)
1010b	RGB 32-bit XR_BIAS 10:10:10	RGB 32-bit Extended Range Bias RGBX (2:10:10:10 MSB-X:B:G:R)
1100b	Indexed 8-bit	Indexed 8-bit
1110b	RGB 16-bit 5:6:5	RGB 16-bit (5:6:5 MSB-R:G:B)

Restriction
Restriction : Plane scaling is not compatible with the Indexed 8-bit, XR_BIAS, and Floating Point source pixel

PLANE_CTL

formats, or any pixel values less than 0 or greater than 1. NV12 is supported only on plane 1 and plane 2 of pipe A and pipe B. NV12 format requires the Plane scaling to be enabled .

23 Pipe CSC Enable

Description
This bit enables pipe color space conversion for the plane pixel data. This is separate from the color conversion logic within the plane.

Value	Name
0b	Disable
1b	Enable

22:21 Key Enable

This field enables color keying.

The key color, range, channel enables, and mask are programmed in PLANE_KEYVAL, PLANE_KEYMSK, and PLANE_KEYMAX.

Value	Name	Description
00b	Disable	Disable keying for this plane.
01b	Source Key Enable	This plane's pixels will be checked for a key match. The blend between this plane and the plane below will treat the key matched pixels as transparent.
10b	Destination Key Enable	This plane's pixels will be checked for a key match. The blend between this plane and the plane above will treat the pixels above as opaque only where this plane is key matched and the plane above is opaque. When plane gamma is enabled, the gamma processing may shift the pixel color values sent to blender and may cause it to not match the key color as desired. The recommendation is to use the pipe gamma when destination keying is enabled.
11b	Source Key Window Enable	This plane's pixels will be checked for a key match. The blend between this plane and the plane below will treat the key matched pixels as transparent only where the plane below is opaque.

Restriction
Restriction : Plane color keying is not compatible with the Indexed 8-bit pixel format. Destination key/Source Key Window should be enabled only on one set (a pair) of planes, per pipe, at a time. Source key and Source Key Window must not be enabled on the bottom most active plane. Destination key must not be enabled on the top most active plane.

20 RGB Color Order

This field is used to select the color order when using RGB data formats, except RGB 32-bit XR_BIAS 10:10:10 and 16-bit BGRX 5:6:5.

For other formats, this field is ignored.

PLANE_CTL

Value	Name	Description
0b	BGRX	BGRX (MSB-X:R:G:B)
1b	RGBX	RGBX (MSB-X:B:G:R)

19 **Plane YUV to RGB CSC Dis**

This bit controls the plane internal YUV to RGB color space conversion.
RGB source pixel formats automatically bypass the plane internal color space conversion.

Value	Name	Description
0b	Enable	YUV pixel data goes through the plane color conversion
1b	Disable	YUV pixel data bypasses the plane color conversion

18 **Plane YUV to RGB CSC Format**

This bit specifies the source YUV format for the plane internal YUV to RGB color space conversion operation.
This field is ignored when source data is RGB.

Value	Name	Description
0b	BT.601	ITU-R Recommendation BT.601
1b	BT.709	ITU-R Recommendation BT.709

17:16 **YUV 422 Byte Order**

This field is used to select the byte order when using YUV 4:2:2 data formats.
For other formats, this field is ignored.

Value	Name	Description
00b	YUYV	YUYV (8:8:8:8 MSB-V:Y2:U:Y1)
01b	UYVY	UYVY (8:8:8:8 MSB-Y2:V:Y1:U)
10b	YVYU	YVYU (8:8:8:8 MSB-U:Y2:V:Y1)
11b	VYUY	VYUY (8:8:8:8 MSB-Y2:U:Y1:V)

15 **Render Decomp**

This bit enables the Display decompression of Render compressed surfaces.

Value	Name
0b	Disable
1b	Enable

Restriction
Restriction : Color Clear is not supported.
Restriction : Only the Left-right cache-line pair decompression is supported. The compressed surface should be Y (Legacy) or Y F Tiled. Decompression is not supported with 90/270 degree rotation.
Restriction : Decompression is supported only with RGB8888 format.
Restriction : Decompression is supported only on plane 1 and plane 2 of pipe A and pipe B.
Restriction : When render decompression is enabled, hardware internally converts the Async

PLANE_CTL

	flips to Sync flips.
14	**Trickle Feed Enable** 0b: Enable 1b: Disable Restriction : Do not program this field to 1b.
13	**Plane Gamma Disable** This bit controls plane internal gamma correction. 1b: Disable 0b: Enable
12:10	**Tiled Surface** This field indicates that the surface data is in tiled memory. This bit may be updated through MMIO writes or through a command streamer initiated synchronous flip. 000b: Linear memory 001b: Tile X memory 100b: Tile Y (Legacy) memory 101b: Tile Y F memory Restriction : Interlaced mode is not supported with Y Tiling. Tile Y S is not supported.
9	**Async Address Update Enable** This bit will enable asynchronous updates of the plane surface address when written by MMIO (MMIO asynchronous flips). The surface address will change as soon as possible. 0b: Sync - Surface Address MMIO writes will update synchronous to start of vertical blank 1b: Async - Surface Address MMIO writes will update asynchronous to start of vertical blank Restriction

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	Restriction : No command streamer (ring) flips to this plane are allowed when this bit is enabled. Each surface address write must be followed by a wait for flip done indication before writing the surface address register again. Not supported with linear memory.
8	**Reserved** Format: MBZ
7:6	**Stereo Surface Vblank Mask** This field controls which vertical blank (left eye, right eye, or both) will be used for the plane surface address double-buffering during stereo 3D mode. This field is ignored when not in stereo 3D mode.

Value	Name	Description
00b	Mask None	Both the left and right eye vertical blanks will be used.
01b	Mask Left	Mask the left eye vertical blank. Only the right eye vertical blank will be used.
10b	Mask Right	Mask the right eye vertical blank. Only the left eye vertical blank will be used.

Alpha Mode

This field controls how the plane will use per pixel alpha data from frame buffer. Constant plane alpha is defined in PLANE_KEYMSK and PLANE_KEYMAX registers.

Value	Name	Description
00b	Disable	Alpha channel ignored.
10b	Enable with SW pre-multiply	Alpha channel used. Color channels should be pre-multiplied with alpha by software.
11b	Enable with HW pre-multiply	Alpha channel used. Color channels will be pre-multiplied with alpha by hardware.

Restriction
Restriction : Per pixel alpha is supported only with RGB8888 pixel formats. FBC is not compatible with per pixel alpha.

3	**Allow Double Buffer Update Disable** Access: R/W This field controls whether double buffer updates are allowed to be disabled for this plane. The DOUBLE_BUFFER_CTL register can be configured to globally disable double buffer updates for resources that allow them to be disabled. This field applies only to the plane registers that supports double buffering. Scaler registers used for plane scaling purposes are not included in this. Restriction : When plane scaling is enabled, the S/W must ensure that the plane size/plane

PLANE_CTL

scaler programming gets applied to the same frame by completing the programming early in the active region; programming these registers close to vblank may result in partial incorrect programming leading to screen corruption.

Value	Name
0b	Not Allowed
1b	Allowed

2 **Reserved**

Format:	MBZ

1:0 **Plane Rotation**

This field controls hardware rotation of the plane.

Value	Name
00b	No rotation
01b	90 degree rotation
10b	180 degree rotation
11b	270 degree rotation

Programming Notes
Hardware does not change the plane position when rotation is enabled. Software may need to adjust the plane position to match the physical orientation of the display.

Restriction
Restriction : 90/270 degree rotation requires the surface to be Y Tiled. Interlaced mode is not supported with 90/270 degree rotation. Render-Display decompression is not supported with 90/270 degree rotation.

PLANE_GAMC

PLANE_GAMC	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000, 0x04010040, 0x08020080, 0x0C0300C0, 0x10040100, 0x14050140, 0x18060180, 0x1C0701C0, 0x20080200, 0x24090240, 0x280A0280, 0x2C0B02C0, 0x300C0300, 0x340D0340, 0x380E0380, 0x3C0F03C0
Access:	R/W
Size (in bits):	512
Address:	701D0h-7020Fh
Name:	Plane Gamma
ShortName:	PLANE_GAMC_1_A
Power:	PG1
Reset:	soft
Address:	702D0h-7030Fh
Name:	Plane Gamma
ShortName:	PLANE_GAMC_2_A
Power:	PG1
Reset:	soft
Address:	703D0h-7040Fh
Name:	Plane Gamma
ShortName:	PLANE_GAMC_3_A
Power:	PG1
Reset:	soft
Address:	711D0h-7120Fh
Name:	Plane Gamma
ShortName:	PLANE_GAMC_1_B
Power:	PG2
Reset:	soft
Address:	712D0h-7130Fh
Name:	Plane Gamma
ShortName:	PLANE_GAMC_2_B
Power:	PG2
Reset:	soft
Address:	713D0h-7140Fh

PLANE_GAMC

Name:	Plane Gamma
ShortName:	PLANE_GAMC_3_B
Power:	PG2
Reset:	soft

Address:	721D0h-7220Fh
Name:	Plane Gamma
ShortName:	PLANE_GAMC_1_C
Power:	PG2
Reset:	soft

Address:	722D0h-7230Fh
Name:	Plane Gamma
ShortName:	PLANE_GAMC_2_C
Power:	PG2
Reset:	soft

Address:	723D0h-7240Fh
Name:	Plane Gamma
ShortName:	PLANE_GAMC_3_C
Power:	PG2
Reset:	soft

These registers are used to determine the characteristics of the gamma correction for the plane pixel data before blending.

Additional gamma correction can be done in the display pipe gamma if desired.

The gamma correction curve is represented by specifying a set of gamma entry reference points spaced equally along the curve for values between -1 and 1.

For extended values there is an extended gamma entry reference point at the maximum alowed input value.

All input values are clamped to the greater than -3.0 and less than 3.0 range before the gamma calculation.

* For input values greater than or equal to 0 and less than 1.0, the input value is used to linearly interpolate between two adjacent points of the first 17 gamma entries to create the result value.

The first 16 entries are stored in PLANE_GAMC with 10 bits per color in an unsigned 0.10 format with 0 integer and 10 fractional.

The 17th entry is stored in the PLANE_GAMC16 register with 11 bits per color in an unsigned 1.10 format with 1 integer and 10 fractional bits.

* For input values greater than or equal to 1.0 and less than 3.0, the input value is used to linearly interpolate between the 17th and 18th gamma entries to create the result value.

The 18th entry is stored in the PLANE_GAMC17 register with 12 bits per color in an unsigned 2.10 format with 2 integer and 10 fractional bits.

* For negative input values, gamma is mirrored along the X-axis, giving the same result as positive input values, except for a negative sign

When gamma input may be negative, the first gamma point should be programmed to a value of 0.0 in order to have a symmetric mirroring.

PLANE_GAMC

Gamma correction can be enabled or disabled through the plane control register.
See Pipe Gamma for an example gamma curve diagram.

Programming Notes

To program the gamma correction entries, calculate the desired gamma curve for inputs from 0 to 3.0.
For inputs of 0 to 1.0, multiply the input value by 16 to find the gamma entry number, then store the desired gamma result in that entry.
For inputs greater than 1.0 and less than or equal to 3.0, store the result for an input of 3.0 in the 18th gamma entry (PLANE_GAMC17).

Restriction

Restriction : The gamma curve must be flat or increasing, never decreasing.
The gamma correction registers should only be updated when the plane is off, otherwise screen artifacts may show temporarily.

DWord	Bit	Description
0	31:30	**Reserved** Format: MBZ
	29:20	**Red** Default Value: 00 0000 0000b Format: U0.10
	19:10	**Green** Default Value: 00 0000 0000b Format: U0.10
	9:0	**Blue** Default Value: 00 0000 0000b Format: U0.10
1	31:30	**Reserved** Format: MBZ
	29:20	**Red** Default Value: 00 0100 0000b Format: U0.10
	19:10	**Green** Default Value: 00 0100 0000b Format: U0.10
	9:0	**Blue** Default Value: 00 0100 0000b Format: U0.10

PLANE_GAMC		
2	31:30	**Reserved** Format: MBZ
	29:20	**Red** Default Value: 00 1000 0000b Format: U0.10
	19:10	**Green** Default Value: 00 1000 0000b Format: U0.10
	9:0	**Blue** Default Value: 00 1000 0000b Format: U0.10
3	31:30	**Reserved** Format: MBZ
	29:20	**Red** Default Value: 00 1100 0000b Format: U0.10
	19:10	**Green** Default Value: 00 1100 0000b Format: U0.10
	9:0	**Blue** Default Value: 00 1100 0000b Format: U0.10
4	31:30	**Reserved** Format: MBZ
	29:20	**Red** Default Value: 01 0000 0000b Format: U0.10
	19:10	**Green** Default Value: 01 0000 0000b Format: U0.10
	9:0	**Blue** Default Value: 01 0000 0000b Format: U0.10
5	31:30	**Reserved** Format: MBZ

PLANE_GAMC

	29:20	**Red** Default Value: 01 0100 0000b Format: U0.10
	19:10	**Green** Default Value: 01 0100 0000b Format: U0.10
	9:0	**Blue** Default Value: 01 0100 0000b Format: U0.10
6	31:30	**Reserved** Format: MBZ
	29:20	**Red** Default Value: 01 1000 0000b Format: U0.10
	19:10	**Green** Default Value: 01 1000 0000b Format: U0.10
	9:0	**Blue** Default Value: 01 1000 0000b Format: U0.10
7	31:30	**Reserved** Format: MBZ
	29:20	**Red** Default Value: 01 1100 0000b Format: U0.10
	19:10	**Green** Default Value: 01 1100 0000b Format: U0.10
	9:0	**Blue** Default Value: 01 1100 0000b Format: U0.10
8	31:30	**Reserved** Format: MBZ

PLANE_GAMC		
	29:20	**Red** Default Value: 10 0000 0000b Format: U0.10
	19:10	**Green** Default Value: 10 0000 0000b Format: U0.10
	9:0	**Blue** Default Value: 10 0000 0000b Format: U0.10
9	31:30	**Reserved** Format: MBZ
	29:20	**Red** Default Value: 10 0100 0000b Format: U0.10
	19:10	**Green** Default Value: 10 0100 0000b Format: U0.10
	9:0	**Blue** Default Value: 10 0100 0000b Format: U0.10
10	31:30	**Reserved** Format: MBZ
	29:20	**Red** Default Value: 10 1000 0000b Format: U0.10
	19:10	**Green** Default Value: 10 1000 0000b Format: U0.10
	9:0	**Blue** Default Value: 10 1000 0000b Format: U0.10
11	31:30	**Reserved** Format: MBZ

PLANE_GAMC		
	29:20	**Red** Default Value: 10 1100 0000b Format: U0.10
	19:10	**Green** Default Value: 10 1100 0000b Format: U0.10
	9:0	**Blue** Default Value: 10 1100 0000b Format: U0.10
12	31:30	**Reserved** Format: MBZ
	29:20	**Red** Default Value: 11 0000 0000b Format: U0.10
	19:10	**Green** Default Value: 11 0000 0000b Format: U0.10
	9:0	**Blue** Default Value: 11 0000 0000b Format: U0.10
13	31:30	**Reserved** Format: MBZ
	29:20	**Red** Default Value: 11 0100 0000b Format: U0.10
	19:10	**Green** Default Value: 11 0100 0000b Format: U0.10
	9:0	**Blue** Default Value: 11 0100 0000b Format: U0.10
14	31:30	**Reserved** Format: MBZ

PLANE_GAMC		
	29:20	**Red** Default Value: 11 1000 0000b Format: U0.10
	19:10	**Green** Default Value: 11 1000 0000b Format: U0.10
	9:0	**Blue** Default Value: 11 1000 0000b Format: U0.10
15	31:30	**Reserved** Format: MBZ
	29:20	**Red** Default Value: 11 1100 0000b Format: U0.10
	19:10	**Green** Default Value: 11 1100 0000b Format: U0.10
	9:0	**Blue** Default Value: 11 1100 0000b Format: U0.10

PLANE_GAMC16

PLANE_GAMC16	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000400, 0x00000400, 0x00000400
Access:	R/W
Size (in bits):	96
Address:	70210h-7021Bh
Name:	Plane Gamma Point 16
ShortName:	PLANE_GAMC16_1_A
Power:	PG1
Reset:	soft
Address:	70310h-7031Bh
Name:	Plane Gamma Point 16
ShortName:	PLANE_GAMC16_2_A
Power:	PG1
Reset:	soft
Address:	70410h-7041Bh
Name:	Plane Gamma Point 16
ShortName:	PLANE_GAMC16_3_A
Power:	PG1
Reset:	soft
Address:	71210h-7121Bh
Name:	Plane Gamma Point 16
ShortName:	PLANE_GAMC16_1_B
Power:	PG2
Reset:	soft
Address:	71310h-7131Bh
Name:	Plane Gamma Point 16
ShortName:	PLANE_GAMC16_2_B
Power:	PG2
Reset:	soft
Address:	71410h-7141Bh
Name:	Plane Gamma Point 16
ShortName:	PLANE_GAMC16_3_B

PLANE_GAMC16

Power:	PG2
Reset:	soft

Address:	72210h-7221Bh
Name:	Plane Gamma Point 16
ShortName:	PLANE_GAMC16_1_C
Power:	PG2
Reset:	soft

Address:	72310h-7231Bh
Name:	Plane Gamma Point 16
ShortName:	PLANE_GAMC16_2_C
Power:	PG2
Reset:	soft

Address:	72410h-7241Bh
Name:	Plane Gamma Point 16
ShortName:	PLANE_GAMC16_3_C
Power:	PG2
Reset:	soft

These registers are used to determine the 17th reference point (point 16 when counting from 0) for plane gamma correction.
The values are represented in an unsigned 1.10 format with 1 integer and 10 fractional bits.
See PLANE_GAMC for plane gamma programming information.

Restriction

Restriction : The value should always be programmed to be less than or equal to 1.0.

DWord	Bit	Description
0	31:11	**Reserved** Format: MBZ
	10:0	**GAMC16R** Default Value: 00000400h Format: U1.10 This value specifies the 17th reference point that is used for the red color channel gamma correction.
1	31:11	**Reserved** Format: MBZ
	10:0	**GAMC16G** Default Value: 00000400h Format: U1.10

<table>
<tr><th colspan="4">PLANE_GAMC16</th></tr>
<tr><td></td><td></td><td colspan="2">This value specifies the 17th reference point that is used for the green color channel gamma correction.</td></tr>
<tr><td rowspan="2">2</td><td>31:11</td><td colspan="2">Reserved<table><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
<tr><td>10:0</td><td colspan="2">GAMC16B<table><tr><td>Default Value:</td><td>00000400h</td></tr><tr><td>Format:</td><td>U1.10</td></tr></table>This value specifies the 17th reference point that is used for the blue color channel gamma correction.</td></tr>
</table>

PLANE_GAMC17

PLANE_GAMC17	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000C00, 0x00000C00, 0x00000C00
Access:	R/W
Size (in bits):	96
Address:	7021Ch-70227h
Name:	Plane Gamma Point 17
ShortName:	PLANE_GAMC17_1_A
Power:	PG1
Reset:	soft
Address:	7031Ch-70327h
Name:	Plane Gamma Point 17
ShortName:	PLANE_GAMC17_2_A
Power:	PG1
Reset:	soft
Address:	7041Ch-70427h
Name:	Plane Gamma Point 17
ShortName:	PLANE_GAMC17_3_A
Power:	PG1
Reset:	soft
Address:	7121Ch-71227h
Name:	Plane Gamma Point 17
ShortName:	PLANE_GAMC17_1_B
Power:	PG2
Reset:	soft
Address:	7131Ch-71327h
Name:	Plane Gamma Point 17
ShortName:	PLANE_GAMC17_2_B
Power:	PG2
Reset:	soft
Address:	7141Ch-71427h
Name:	Plane Gamma Point 17
ShortName:	PLANE_GAMC17_3_B

PLANE_GAMC17

Power:	PG2
Reset:	soft

Address:	7221Ch-72227h
Name:	Plane Gamma Point 17
ShortName:	PLANE_GAMC17_1_C
Power:	PG2
Reset:	soft

Address:	7231Ch-72327h
Name:	Plane Gamma Point 17
ShortName:	PLANE_GAMC17_2_C
Power:	PG2
Reset:	soft

Address:	7241Ch-72427h
Name:	Plane Gamma Point 17
ShortName:	PLANE_GAMC17_3_C
Power:	PG2
Reset:	soft

These registers are used to determine the 18th reference point (point 17 when counting from 0) for plane gamma correction.
The values are represented in an unsigned 2.10 format with 2 integer and 10 fractional bits.
See PLANE_GAMC for plane gamma programming information.

Restriction

Restriction : The value should always be programmed to be less than or equal to 3.0.

DWord	Bit	Description
0	31:12	**Reserved** Format: MBZ
	11:0	**GAMC17R** Default Value: 00000C00h Format: U2.10 This value specifies the 18th reference point that is used for the red color channel gamma correction.
1	31:12	**Reserved** Format: MBZ
	11:0	**GAMC17G** Default Value: 00000C00h Format: U2.10

<table>
<tr><th colspan="3">PLANE_GAMC17</th></tr>
<tr><td></td><td></td><td>This value specifies the 18th reference point that is used for the green color channel gamma correction.</td></tr>
<tr><td rowspan="2">2</td><td>31:12</td><td>Reserved<table><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
<tr><td>11:0</td><td>GAMC17B<table><tr><td>Default Value:</td><td>00000C00h</td></tr><tr><td>Format:</td><td>U2.10</td></tr></table>This value specifies the 18th reference point that is used for the blue color channel gamma correction.</td></tr>
</table>

PLANE_KEYMAX

PLANE_KEYMAX	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank, pipe not enabled, or plane not enabled
Address:	701A0h-701A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_1_A
Power:	PG1
Reset:	soft
Address:	702A0h-702A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_2_A
Power:	PG1
Reset:	soft
Address:	703A0h-703A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_3_A
Power:	PG1
Reset:	soft
Address:	711A0h-711A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_1_B
Power:	PG2
Reset:	soft
Address:	712A0h-712A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_2_B
Power:	PG2
Reset:	soft
Address:	713A0h-713A3h

PLANE_KEYMAX

Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_3_B
Power:	PG2
Reset:	soft

Address:	721A0h-721A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_1_C
Power:	PG2
Reset:	soft

Address:	722A0h-722A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_2_C
Power:	PG2
Reset:	soft

Address:	723A0h-723A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_3_C
Power:	PG2
Reset:	soft

When plane source is YUV, this register specifies the maximum YUV key value to be used together with the minimum YUV key value and the channel enables to determine if the plane matches the key.
When plane source is RGB, this register is not used.

DWord	Bit	Description
0	31:24	**Plane Alpha Value** Specifies the plane alpha value when plane alpha is enabled in PLANE_KEYMSK register.
	23:16	**V Key Max Value** Specifies the maximum key value for the V channel.
	15:8	**Y Key Max Value** Specifies the maximum key value for the Y channel.
	7:0	**U Key Max Value** Specifies the maximum key value for the U channel.

PLANE_KEYMSK

PLANE_KEYMSK	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank, pipe not enabled, or plane not enabled
Address:	70198h-7019Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_1_A
Power:	PG1
Reset:	soft
Address:	70298h-7029Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_2_A
Power:	PG1
Reset:	soft
Address:	70398h-7039Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_3_A
Power:	PG1
Reset:	soft
Address:	71198h-7119Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_1_B
Power:	PG2
Reset:	soft
Address:	71298h-7129Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_2_B
Power:	PG2
Reset:	soft
Address:	71398h-7139Bh

PLANE_KEYMSK

Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_3_B
Power:	PG2
Reset:	soft

Address:	72198h-7219Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_1_C
Power:	PG2
Reset:	soft

Address:	72298h-7229Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_2_C
Power:	PG2
Reset:	soft

Address:	72398h-7239Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_3_C
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31	**Plane Alpha Enable** Description: Enables the plane alpha. Color channels will be pre-multiplied by hardware with the plane alpha value from PLANE_KEYMAX register. Per-pixel alpha is defined in the PLANE_CTL register. Value 0b: Disable Value 1b: Enable
	30:27	**Reserved** Format: MBZ
	26	**V or R Key Channel Enable** Enables the V/Red channel for key comparison. A disabled channel will be ignored when determining a key match. Value 0b: Disable Value 1b: Enable

PLANE_KEYMSK

	25	**Y or G Key Channel Enable** Enables the Y/Green channel for key comparison. A disabled channel will be ignored when determining a key match. **Value** / **Name** 0b – Disable 1b – Enable
	24	**U or B Key Channel Enable** Enables the U/Blue channel for key comparison. A disabled channel will be ignored when determining a key match. **Value** / **Name** 0b – Disable 1b – Enable
	23:16	**R Key Mask Value** Specifies the key mask for the Red channel. A zero bit in the mask indicates that the corresponding bit will be ignored when determining a key match.
	15:8	**G Key Mask Value** Specifies the key mask for the Green channel. A zero bit in the mask indicates that the corresponding bit will be ignored when determining a key match.
	7:0	**B Key Mask Value** Specifies the key mask for the Blue channel. A zero bit in the mask indicates that the corresponding bit will be ignored when determining a key match.

PLANE_KEYVAL

PLANE_KEYVAL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank, pipe not enabled, or plane not enabled
Address:	70194h-70197h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_1_A
Power:	PG1
Reset:	soft
Address:	70294h-70297h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_2_A
Power:	PG1
Reset:	soft
Address:	70394h-70397h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_3_A
Power:	PG1
Reset:	soft
Address:	71194h-71197h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_1_B
Power:	PG2
Reset:	soft
Address:	71294h-71297h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_2_B
Power:	PG2
Reset:	soft
Address:	71394h-71397h

PLANE_KEYVAL

Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_3_B
Power:	PG2
Reset:	soft

Address:	72194h-72197h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_1_C
Power:	PG2
Reset:	soft

Address:	72294h-72297h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_2_C
Power:	PG2
Reset:	soft

Address:	72394h-72397h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_3_C
Power:	PG2
Reset:	soft

When plane source is YUV, this register specifies the minimum YUV key value to be used together with the maximum YUV key value and the channel enables to determine if the plane matches the key. When plane source is RGB, this register specifies the RGB key value to be used together with the channel masks to determine if the plane matches the key. RGB key matches can only occur for positive pixel values in the 0 to 1 range. Extended range pixel values will not match. MSB bits are used for comparison.

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:16	**V Min or R Key Value** Specifies the minimum key value for the V channel or the compare value for Red channel.
	15:8	**Y Min or G Key Value** Specifies the minimum key value for the Y channel or the compare value for Green channel.
	7:0	**U Min or B Key Value** Specifies the minimum key value for the U channel or the compare value for Blue channel.

PLANE_LEFT_SURF

PLANE_LEFT_SURF	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of left or right eye vertical blank (selectable), pipe not enabled. or plane not enabled; after armed
Double Buffer Armed By:	Write to PLANE_SURF or plane not enabled
Address:	701B0h-701B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_1_A
Power:	PG1
Reset:	soft
Address:	702B0h-702B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_2_A
Power:	PG1
Reset:	soft
Address:	703B0h-703B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_3_A
Power:	PG1
Reset:	soft
Address:	711B0h-711B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_1_B
Power:	PG2
Reset:	soft
Address:	712B0h-712B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_2_B
Power:	PG2
Reset:	soft

PLANE_LEFT_SURF

Address:	713B0h-713B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_3_B
Power:	PG2
Reset:	soft

Address:	721B0h-721B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_1_C
Power:	PG2
Reset:	soft

Address:	722B0h-722B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_2_C
Power:	PG2
Reset:	soft

Address:	723B0h-723B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_3_C
Power:	PG2
Reset:	soft

Restriction

Restriction : This register must be programmed with a valid address prior to enabling stereo 3D on this pipe.

DWord	Bit	Description
0	31:12	**Left Surface Base Address** Format: GraphicsAddress[31:12] This address specifies the stereo 3D left eye surface base address bits 31:12. **Restriction** Restriction : This surface must have the same stride, tiling, and panning offset parameters as the right eye surface and meet all the same restrictions.
	11:0	**Reserved**

PLANE_OFFSET

PLANE_OFFSET	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank, pipe not enabled, or plane not enabled
Address:	701A4h-701A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_1_A
Power:	PG1
Reset:	soft
Address:	701C4h-701C7h
Name:	Plane Auxiliary Offset
ShortName:	PLANE_AUX_OFFSET_1_A
Power:	PG1
Reset:	soft
Address:	702A4h-702A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_2_A
Power:	PG1
Reset:	soft
Address:	702C4h-702C7h
Name:	Plane Auxiliary Offset
ShortName:	PLANE_AUX_OFFSET_2_A
Power:	PG1
Reset:	soft
Address:	703A4h-703A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_3_A
Power:	PG1
Reset:	soft
Address:	703C4h-703C7h

PLANE_OFFSET	
Name:	Plane Auxiliary Offset
ShortName:	PLANE_AUX_OFFSET_3_A
Power:	PG1
Reset:	soft
Address:	711A4h-711A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_1_B
Power:	PG2
Reset:	soft
Address:	711C4h-711C7h
Name:	Plane Auxiliary Offset
ShortName:	PLANE_AUX_OFFSET_1_B
Power:	PG2
Reset:	soft
Address:	712A4h-712A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_2_B
Power:	PG2
Reset:	soft
Address:	712C4h-712C7h
Name:	Plane Auxiliary Offset
ShortName:	PLANE_AUX_OFFSET_2_B
Power:	PG2
Reset:	soft
Address:	713A4h-713A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_3_B
Power:	PG2
Reset:	soft
Address:	713C4h-713C7h
Name:	Plane Auxiliary Offset
ShortName:	PLANE_AUX_OFFSET_3_B
Power:	PG2
Reset:	soft
Address:	721A4h-721A7h

PLANE_OFFSET

Name:	Plane Offset
ShortName:	PLANE_OFFSET_1_C
Power:	PG2
Reset:	soft
Address:	721C4h-721C7h
Name:	Plane Auxiliary Offset
ShortName:	PLANE_AUX_OFFSET_1_C
Power:	PG2
Reset:	soft
Address:	722A4h-722A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_2_C
Power:	PG2
Reset:	soft
Address:	722C4h-722C7h
Name:	Plane Auxiliary Offset
ShortName:	PLANE_AUX_OFFSET_2_C
Power:	PG2
Reset:	soft
Address:	723A4h-723A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_3_C
Power:	PG2
Reset:	soft
Address:	723C4h-723C7h
Name:	Plane Auxiliary Offset
ShortName:	PLANE_AUX_OFFSET_3_C
Power:	PG2
Reset:	soft

This register specifies the panning for the plane surface. The start position is specified in this register as a (x, y) offset from the beginning of the surface. When performing 180 rotation, hardware will internally add the plane size to the offsets so the plane will start displaying from the bottom right corner of the image. When performing 90 rotation, the offset programmed should take the rotation in to consideration. X offset = (Surface height in tiles * tile height) - Y offset - Y Size, Y offset = X offset When performing 270 rotation, use the same programming as 90 rotation. For YUV planar format non-rotate cases, the UV surface offsets should be half of the Y surface offsets when the UV surface is tile row aligned. When the UV surface is not tile row aligned, the UV surface Y offset should also include the lines from the previous nearest tile row aligned address.

PLANE_OFFSET

Restriction
Restriction : The plane size + offset must not exceed the maximum supported plane size.

DWord	Bit	Description
0	31:29	**Reserved** Format: MBZ
	28:16	**Start Y Position** The Start Y Position or the Y Offset is the vertical offset in lines of the beginning of the active display plane relative to the display surface. **Restriction** Restriction : In 90/270 rotation modes, this offset must be even lines aligned for YUV 4:2:2, YUV 4:2:0 formats.
	15:13	**Reserved** Format: MBZ
	12:0	**Start X Position** The Start X Position or the X Offset is the horizontal offset in pixels of the beginning of the active display plane relative to the display surface. **Restriction** Restriction : In 0/180 rotation modes, this offset must be even pixel aligned for YUV 4:2:2, YUV 4:2:0 formats.

PLANE_POS

PLANE_POS	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled; after armed
Double Buffer Armed By:	Write to PLANE_SURF or plane not enabled
Address:	7018Ch-7018Fh
Name:	Plane Position
ShortName:	PLANE_POS_1_A
Power:	PG1
Reset:	soft
Address:	7028Ch-7028Fh
Name:	Plane Position
ShortName:	PLANE_POS_2_A
Power:	PG1
Reset:	soft
Address:	7038Ch-7038Fh
Name:	Plane Position
ShortName:	PLANE_POS_3_A
Power:	PG1
Reset:	soft
Address:	7118Ch-7118Fh
Name:	Plane Position
ShortName:	PLANE_POS_1_B
Power:	PG2
Reset:	soft
Address:	7128Ch-7128Fh
Name:	Plane Position
ShortName:	PLANE_POS_2_B
Power:	PG2
Reset:	soft

PLANE_POS

Address:	7138Ch-7138Fh
Name:	Plane Position
ShortName:	PLANE_POS_3_B
Power:	PG2
Reset:	soft

Address:	7218Ch-7218Fh
Name:	Plane Position
ShortName:	PLANE_POS_1_C
Power:	PG2
Reset:	soft

Address:	7228Ch-7228Fh
Name:	Plane Position
ShortName:	PLANE_POS_2_C
Power:	PG2
Reset:	soft

Address:	7238Ch-7238Fh
Name:	Plane Position
ShortName:	PLANE_POS_3_C
Power:	PG2
Reset:	soft

This register specifies the screen position of the plane.
The origin of the plane position is always the upper left corner of the display pipe source image area.
When plane scaling is not enabled on this plane, this is the position of the plane when blended with other planes on this pipe.
When plane scaling is enabled on this plane, the scaler window position is the position of the plane when blended with other planes on this pipe.
When performing rotation, the plane image is rotated by hardware, but the position is not, so it must be adjusted if it is desired to maintain the same apparent position on a physically rotated display.

Restriction

Restriction : When plane scaling is not enabled on this plane, the plane must be completely contained within the pipe source area. Pipe source size >= plane position + plane size.
When plane scaling is enabled on this plane, the X and Y positions must be programmed to 0.

DWord	Bit	Description
0	31:28	**Reserved** Format: MBZ
	27:16	**Y Position** This specifies the vertical position of the plane upper left corner in lines.

PLANE_POS		
	15:13	**Reserved** Format: MBZ
	12:0	**X Position** This specifies the horizontal position of the plane upper left corner in pixels.

PLANE_SIZE

PLANE_SIZE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled; after armed
Double Buffer Armed By:	Write to PLANE_SURF or plane not enabled
Address:	70190h-70193h
Name:	Plane Size
ShortName:	PLANE_SIZE_1_A
Power:	PG1
Reset:	soft
Address:	70290h-70293h
Name:	Plane Size
ShortName:	PLANE_SIZE_2_A
Power:	PG1
Reset:	soft
Address:	70390h-70393h
Name:	Plane Size
ShortName:	PLANE_SIZE_3_A
Power:	PG1
Reset:	soft
Address:	71190h-71193h
Name:	Plane Size
ShortName:	PLANE_SIZE_1_B
Power:	PG2
Reset:	soft
Address:	71290h-71293h
Name:	Plane Size
ShortName:	PLANE_SIZE_2_B
Power:	PG2
Reset:	soft

PLANE_SIZE

Address:	71390h-71393h
Name:	Plane Size
ShortName:	PLANE_SIZE_3_B
Power:	PG2
Reset:	soft

Address:	72190h-72193h
Name:	Plane Size
ShortName:	PLANE_SIZE_1_C
Power:	PG2
Reset:	soft

Address:	72290h-72293h
Name:	Plane Size
ShortName:	PLANE_SIZE_2_C
Power:	PG2
Reset:	soft

Address:	72390h-72393h
Name:	Plane Size
ShortName:	PLANE_SIZE_3_C
Power:	PG2
Reset:	soft

This register specifies the plane source size, the size of the image fetched from the frame buffer.
When plane scaling is not enabled on this plane, this is the size of the plane when blended with other planes on this pipe.
When plane scaling is enabled on this plane, the scaler window size is the size of the plane when blended with other planes on this pipe.

Restriction

Restriction : When plane scaling is not enabled on this plane, the plane must be completely contained within the pipe source area. Pipe source size >= plane position + plane size.

DWord	Bit	Description
0	31:28	**Reserved** Format: MBZ
	27:16	**Height** This specifies the height of the plane in lines. The value in the register is the height minus one. **Restriction** Restriction : The height must be at least one line. The height is limited to maximum of 4096 lines. When

PLANE_SIZE

		plane scaling is enabled, the height must be atleast 8 lines.
	15:13	**Reserved** Format: MBZ
	12:0	**Width** This specifies the width of the plane in pixels. The value in the register is the width minus one.

Restriction

Restriction :
The width must be even (programmed value odd) when YUV 4:2:2 or YUV 4:2:0 source pixel format is used. The width must be at least one pixel.
The width should be less than or equal to the stride in pixels.

Tiling format	Bytes per pixel	Max Width supported in pixels (with no horizontal panning)
Linear, X Tiling	8	4096
	1, 2, 4	8192
Yb and Yf Tiling	8	2048
	4	4096
	1,2	8192

PLANE_STRIDE

PLANE_STRIDE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled; after armed
Double Buffer Armed By:	Write to PLANE_SURF or plane not enabled
Address:	70188h-7018Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_1_A
Power:	PG1
Reset:	soft
Address:	70288h-7028Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_2_A
Power:	PG1
Reset:	soft
Address:	70388h-7038Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_3_A
Power:	PG1
Reset:	soft
Address:	71188h-7118Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_1_B
Power:	PG2
Reset:	soft
Address:	71288h-7128Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_2_B
Power:	PG2
Reset:	soft

PLANE_STRIDE

Address:	71388h-7138Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_3_B
Power:	PG2
Reset:	soft

Address:	72188h-7218Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_1_C
Power:	PG2
Reset:	soft

Address:	72288h-7228Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_2_C
Power:	PG2
Reset:	soft

Address:	72388h-7238Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_3_C
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31:10	**Reserved**
	9:0	**Stride** This field specifies the stride for the plane. The field is used to determine the line to line increment for the plane. For Linear memory, this field specifies the stride in chunks of 64 bytes (1 cache line). If the programmed value is 100, the actual stride = 100 * 64 = 6400 bytes. For X-Tiled & Y-Tiled memory, this field specifies the stride in number of tiles. For Tile X, if the programmed value is 10, the actual stride = 10 * 512 (X tile width) = 5120 bytes. For Tile Y legacy, if the programmed value is 10, the actual stride = 10 * 128 (Y tile width) = 1280 bytes. This register may be updated through MMIO writes or through command streamer initiated synchronous flips.

Tile Format	Width in bytes
Tile X	512
Tile Y (legacy)	128
Tile YF (8 bpp)	64
Tile YF (16 bpp, 32 bpp, 64 bpp)	128

PLANE_STRIDE

Programming Notes

For YUV planar (NV12 or P0xx) source fomats, the Auxiliary surface (UV surface) stride should be programmed seperately in the PLANE_AUX_DIST register.

Restriction

Restriction :
For YUV planar (NV12 or P0xx) plane pixel formats, the stride calculated in bytes should be equal for the Y and UV surfaces. In Tile Yf format, the stride value programmed for YUV planar - Y surface should be an even number of tiles in the non-rotate mode.
The stride in bytes must not exceed the of the size of 8K pixels and 32K bytes

Tile Format	Pixel Format	Maximum Stride in tiles	YUV Planar Maximum Auxiliary surface stride in tiles	Render Decompression Maximum Auxiliary surface stride in tiles
X Tiling	64 bpp pixel formats	64	NA	NA
	32 bpp pixel format	64	NA	NA
	16 bpp pixel formats	32	NA	NA
	YUV planar	16	16	NA
Y Tiling (Legacy)	64 bpp pixel formats	256	NA	NA
	32 bpp pixel formats	256	NA	8
	16 bpp pixel formats	128	NA	NA
	YUV planar	64	64	NA
YF Tiling	32 bpp pixel formats	256	NA	8
	16 bpp Pixel formats	128	NA	NA

PLANE_STRIDE						
			YUV planar	128	64	NA

PLANE_SURF

PLANE_SURF	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of left or right eye vertical blank (selectable), pipe not enabled, or plane not enabled
Address:	7019Ch-7019Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_1_A
Power:	PG1
Reset:	soft
Address:	7029Ch-7029Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_2_A
Power:	PG1
Reset:	soft
Address:	7039Ch-7039Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_3_A
Power:	PG1
Reset:	soft
Address:	7119Ch-7119Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_1_B
Power:	PG2
Reset:	soft
Address:	7129Ch-7129Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_2_B
Power:	PG2
Reset:	soft
Address:	7139Ch-7139Fh

PLANE_SURF

Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_3_B
Power:	PG2
Reset:	soft

Address:	7219Ch-7219Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_1_C
Power:	PG2
Reset:	soft

Address:	7229Ch-7229Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_2_C
Power:	PG2
Reset:	soft

Address:	7239Ch-7239Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_3_C
Power:	PG2
Reset:	soft

Writes to this register arm primary registers for this pipe. A write to this register is considered a flip and can cause a flip done interrupt if the interrupt registers are configured for that. The values in this register may be updated through MMIO writes or through command streamer initiated flips. Synchronous updates (synchronous command streamer flips or synchronous MMIO writes) will update the plane surface values at the start of the next vertical blank. Asynchronous updates (asynchronous command streamer flips or asynchronous MMIO writes) will update the plane surface values at the next TLB request or at the start of the next vertical blank. Stereo 3D synchronous updates (stereo 3D command streamer flips or synchronous MMIO writes while stereo 3D is enabled) will update at the start of either the left or right eye vertical blank, selectable by the plane control register stereo surface vblank mask.

Asynchronous flip completion time depends greatly on how much data has been prefetched for power savings, and can take up to 1 full frame to complete. For faster flip completion, disable FBC and render compression and allocate a small amount of data buffer for the plane.

DWord	Bit	Description
0	31:12	**Surface Base Address** Format: GraphicsAddress[31:12] This address specifies the surface base address bits 31:12. In stereo 3D mode this is the right eye base address. In non-stereo 3D mode this is the only base address. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. **Restriction**

PLANE_SURF

		The surface base address must be at least 256KB aligned in the Linear or X-tiling modes and must be at least 1MB aligned in the Y-tiling mode. Allocate an extra 136 Page Table Entries (PTEs) beyond the end of the displayed surface. If 180 or 270 plane rotation capability is required, allocate an exra 136 PTEs before the begining of the surface. When address range limits are reached, wrap around to finish allocating the extra PTEs. Only the PTEs will be used, not the pages themselves. For render compression, the padding must be added for both the main surface and the compression control surface. There must be padding between the main and the control surfaces. For planar YUV 420 formats, the padding must be added for both Y and UV surfaces.There must be padding between the Y and UV surfaces.
	11	**Reserved**
	10	**Reserved**
	9	**Reserved**
	8:7	**Reserved**
	6:4	**Reserved**
	3	**Ring Flip Source** This bit indicates if the source of the last ring flip was CS or BCS. This will determine where the flip done response is sent.
	2	**Reserved**
	1:0	**Reserved**

Value	Name
0b	CS
1b	BCS

PLANE_SURFLIVE

PLANE_SURFLIVE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000 [KBL]
Size (in bits):	32
Address:	701ACh-701AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_1_A
Power:	PG1
Reset:	soft
Address:	701BCh-701BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_1_A
Power:	PG1
Reset:	soft
Address:	702ACh-702AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_2_A
Power:	PG1
Reset:	soft
Address:	702BCh-702BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_2_A
Power:	PG1
Reset:	soft
Address:	703ACh-703AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_3_A
Power:	PG1
Reset:	soft
Address:	703BCh-703BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_3_A
Power:	PG1
Reset:	soft

PLANE_SURFLIVE

Address:	711ACh-711AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_1_B
Power:	PG2
Reset:	soft
Address:	711BCh-711BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_1_B
Power:	PG2
Reset:	soft
Address:	712ACh-712AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_2_B
Power:	PG2
Reset:	soft
Address:	712BCh-712BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_2_B
Power:	PG2
Reset:	soft
Address:	713ACh-713AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_3_B
Power:	PG2
Reset:	soft
Address:	713BCh-713BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_3_B
Power:	PG2
Reset:	soft
Address:	721ACh-721AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_1_C
Power:	PG2
Reset:	soft

PLANE_SURFLIVE

Address:	721BCh-721BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_1_C
Power:	PG2
Reset:	soft

Address:	722ACh-722AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_2_C
Power:	PG2
Reset:	soft

Address:	722BCh-722BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_2_C
Power:	PG2
Reset:	soft

Address:	723ACh-723AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_3_C
Power:	PG2
Reset:	soft

Address:	723BCh-723BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_3_C
Power:	PG2
Reset:	soft

There is one instance of this register for each plane.

DWord	Bit	Description
0	31:12	**Live Surface Base Address** Access: RO This gives the live value of the surface base address as being currently used for the plane.
	11	**Reserved** Format: MBZ
	10:9	**Reserved**
	8:6	**Reserved**
	5	**Reserved**
	4	**Reserved**

PLANE_SURFLIVE		
	3:0	**Reserved** Format: MBZ

PLANE_WM

PLANE_WM	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00004007
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank, plane not enabled, or pipe not enabled
Double Buffer Armed By:	Write to PLANE_SURF or plane not enabled
Address:	70140h-7015Fh
Name:	Cursor A Watermarks
ShortName:	CUR_WM_A_*
Power:	PG1
Reset:	soft
Address:	70168h-7016Bh
Name:	Cursor Transition Watermarks
ShortName:	CUR_WM_TRANS_A
Power:	PG1
Reset:	soft
Address:	70240h-7025Fh
Name:	Plane 1 A Watermarks
ShortName:	PLANE_WM_1_A_*
Power:	PG1
Reset:	soft
Address:	70268h-7026Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_1_A
Power:	PG1
Reset:	soft
Address:	70340h-7035Fh
Name:	Plane 2 A Watermarks
ShortName:	PLANE_WM_2_A_*
Power:	PG1
Reset:	soft

PLANE_WM	
Address:	70368h-7036Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_2_A
Power:	PG1
Reset:	soft
Address:	70440h-7045Fh
Name:	Plane 3 A Watermarks
ShortName:	PLANE_WM_3_A_*
Power:	PG1
Reset:	soft
Address:	70468h-7046Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_3_A
Power:	PG1
Reset:	soft
Address:	71140h-7115Fh
Name:	Cursor B Watermarks
ShortName:	CUR_WM_B_*
Power:	PG2
Reset:	soft
Address:	71168h-7116Bh
Name:	Cursor Transition Watermarks
ShortName:	CUR_WM_TRANS_B
Power:	PG2
Reset:	soft
Address:	71240h-7125Fh
Name:	Plane 1 B Watermarks
ShortName:	PLANE_WM_1_B_*
Power:	PG2
Reset:	soft
Address:	71268h-7126Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_1_B
Power:	PG2
Reset:	soft

PLANE_WM	
Address:	71340h-7135Fh
Name:	Plane 2 B Watermarks
ShortName:	PLANE_WM_2_B_*
Power:	PG2
Reset:	soft
Address:	71368h-7136Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_2_B
Power:	PG2
Reset:	soft
Address:	71440h-7145Fh
Name:	Plane 3 B Watermarks
ShortName:	PLANE_WM_3_B_*
Power:	PG2
Reset:	soft
Address:	71468h-7146Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_3_B
Power:	PG2
Reset:	soft
Address:	72140h-7215Fh
Name:	Cursor C Watermarks
ShortName:	CUR_WM_C_*
Power:	PG2
Reset:	soft
Address:	72168h-7216Bh
Name:	Cursor Transition Watermarks
ShortName:	CUR_WM_TRANS_C
Power:	PG2
Reset:	soft
Address:	72240h-7225Fh
Name:	Plane 1 C Watermarks
ShortName:	PLANE_WM_1_C_*
Power:	PG2
Reset:	soft

PLANE_WM

Address:	72268h-7226Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_1_C
Power:	PG2
Reset:	soft

Address:	72340h-7235Fh
Name:	Plane 2 C Watermarks
ShortName:	PLANE_WM_2_C_*
Power:	PG2
Reset:	soft

Address:	72368h-7236Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_2_C
Power:	PG2
Reset:	soft

Address:	72440h-7245Fh
Name:	Plane 3 C Watermarks
ShortName:	PLANE_WM_3_C_*
Power:	PG2
Reset:	soft

Address:	72468h-7246Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_3_C
Power:	PG2
Reset:	soft

Programming Notes

There are eight regular watermarks and a transition watermark per plane/cursor. For YUV planar source formats, only the Y surface watermark value should be programmed. Watermark programming instructions are documented separately.

Restriction

Restriction : For minimum watermark requirements refer to Display Watermark Programming section.

DWord	Bit	Description
0	31	**Enable** This field enables this watermark. All the watermarks at this level for all enabled planes must be enabled before the level will be used.

PLANE_WM

Value	Name
1b	Enable
0b	Disable

30 — **Reserved**

29:19 — **Reserved**

Format:	MBZ

18:14 — **Lines**

Default Value:	01h

Description
This field contains the watermark value in lines. Hardware ignores the lines for the the transition watermark.
Hardware ignores the lines for the level 0 watermark.

13:10 — **Reserved**

9:0 — **Blocks**

Default Value:	007h

This field contains the watermark value in blocks of 8 cachelines.

PORT_CLK_SEL

PORT_CLK_SEL		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
DWord	**Bit**	**Description**
0	31:28	**Reserved**
	27:0	**Reserved** Format: MBZ

Power Clock State Register

PWR_CLK_STATE - Power Clock State Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000088 [KBL]
Access:	R/W
Size (in bits):	32
Address:	020C8h
Name:	Render Power Clock State Register
ShortName:	R_PWR_CLK_STATE
Address:	220C8h
Name:	BCS Power Clock State Register
ShortName:	BCS_PWR_CLK_STATE
Address:	120C8h
Name:	VCS Power Clock State Register
ShortName:	VCS_PWR_CLK_STATE
Address:	1A0C8h
Name:	VECS Power Clock State Register
ShortName:	VECS_PWR_CLK_STATE

This register contains the mode selection for configuring render engine to attain desired performance and power requirements for a given context. This register is render context save/restored. This register must be initialized correctly when the context is submitted for the first time. This register is context save/restored as part of Exec-List context image in both Exec-List and Ring-Buffer mode of scheduling. This register contents are valid only when "Enable" bit [31] of the register is set.

Programming Notes

This register is only functional for RenderCS. This register must not be exercised in VideoCS, BlitterCS and VideoEnhancementCS.

This register must not be programmed directly through CPU MMIO cycle.
Exec-List Scheduling Mode: Every context can have its own required render engine configuration by programming this register appropriately in the logical render context image in memory (LRCA) before submitting the context to the execlist submit port. This register must not be programmed using MI_LOAD_REGISTER_IMM command in ring buffer or in batch buffer, however programming "NON-SLM Indication" field through MI_LOAD_REGISTER_IMM is an exception defined below. If a need arises to change the render configuration for a context being executed in HW, Scheduler must preempt the context and update the desired render configuration in the logical render context image in memory and resubmit the context. Only "NON-SLM Indictaion" field in R_PWR_CLK_STATE register is allowed to be modified through MI_LOAD_REGISTER_IMM command in ring_buffer or privileged_batch_buffer. SW must modify only "NON-SLM Indication" field and must ensure to program other fields with the same value as in LRCA. SW must ensure to

PWR_CLK_STATE - Power Clock State Register

program PIPECONTROl flush command with CS Stall and HDC Flush prior to programming MI_LOAD_REGISTER_IMM command to modify "NON-SLM Indication" in R_PWR_CLK_STATE register.
Example: //R_PWR_CLK_STATE register value in LRCA configured with two slices and NON-SLM indication reset: 0x80005_0000 //SW desires to set NON-SLM Indication filed in ring buffer MI_LOAD_REGISTER_IMM 0x20C8, 0x8005_0100

Ring Buffer Scheduling: This register must be programmed using MI_LOAD_REGISTER_IMM command in the ring buffer. When this register is being programmed to re-configure the number of slices, SW must context save the state before programming this register and restore the state after programming the register via dummy MI_SET_CONTEXT command, this will ensure the existing state is programmed to all the new slices that are powered up, in case of slice shutdown (slice power down) this is not required.
Example:
MI_SET_CONTEXT -> CXTA
MI_BATCH_BUFFER_START
MI_BATCH_BUFFER_START
MI_SET_CONTEXT -> CXTB //Dummy Context to save existing render state to be restored latter.
MI_LOAD_REGISTER_IMM : R_PWR_CLK_STATE (1 Slice to 3 Slices) // Slice configuration done.
MI_STORE_DATA_IMM (Update R_PWR_CLK_STATE value in CTXA context image to modified value)
MI_SET_CONTEXT -> CXTA // Context restore of valid state to all the slices powered up with R_PWR_CLK_STATE restored with modifed value.

DWord	Bit	Description
0	31	**Power Clock State Enable** Format: U1 Value / Name / Description: 0h – Power Clock State Disabled – No specific power state set, bits[30:0] are ignored. 1h – Power Clock State Enabled – Power Clock is set and bit[30:0] are valid and have the desired state.
	30:0	**Power Clock State** Format: Power Clock State Format

Power Context Save

PWRCTXSAVE - Power Context Save

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04A04h

DWord	Bit	Description
0	31:16	**Mask Bits** Default Value: 0000h Access: RO
	15	**Extra Bits15** Default Value: 0b Access: R/W Extra Bits for future use.
	14	**Extra Bits14** Default Value: 0b Access: R/W Extra Bits for future use.
	13	**Extra Bits13** Default Value: 0b Access: R/W Extra Bits for future use.
	12	**Extra Bits12** Default Value: 0b Access: R/W Extra Bits for future use.
	11	**Extra Bits11** Default Value: 0b Access: R/W Extra Bits for future use.

PWRCTXSAVE - Power Context Save

	10	**Extra Bits10** Default Value: 0b Access: R/W Extra Bits for future use.
	9	**Power Context Save Request** Default Value: 0b Access: R/W Power Context Save. Bit[9]. Power Context Save Request. 1'b0: Power context save is not being requested (default). 1'b1: Power context save is being requested. Unit needs to self-clear this bit upon sampling. This bit is self clear.
	8:0	**Power Context Save Quad Word Credits** Default Value: 000000000b Access: R/W Power Context Save. Bits[8:0]. QWord Credits for Power Context Save Request. An initial length packet is required per power context save session, but that packet does not consume a credit. See protocol description for more details. Minimum Credits = 1: Unit may send 1 QWord pair. Maximum Credits = 511: Unit may send 511 QWord pairs. A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Only valid with PWRCTX_SAVE_REQ (Bit9).

Power context Save Register for LPFC

LPCSR - Power context Save Register for LPFC		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B408h	
DWord	**Bit**	**Description**
0	31:10	**Reserved** Access: RO Reserved.
	9:0	**Power context save register command** Access: R/W Hardware Clear Bit[9]. Power Context Save Request. 1'b0: Power context save is not being requested (default). 1'b1: Power context save is being requested. Unit needs to self-clear this bit upon sampling. Bits[8:0]. QWord Credits for Power Context Save Request. Minimum Credits = 1: Unit may send 1 QWord pair (enough for first LRI at least). Maximum Credits = 511: Unit may send 511 QWord pairs. A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

Power Context Save request

PCTXSAVEREQ - Power Context Save request		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	08110h	
DWord	**Bit**	**Description**
0	31:16	**Message Mask** Access: RO Message Mask bits for lower 16 bits
	15:10	**Reserved** Access: RO Reserved
	9	**Power context save** Access: R/W Set Power Context Save Request 1'b0 : Power context save is not being requested 1'b1 : Power context save is being requested CPUnit self-clears this bit upon sampling.
	8:0	**Power Context Save request crdit count** Access: R/W QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

PP_CONTROL

PP_CONTROL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32

Address:	C7204h-C7207h
Name:	Panel Power Control
ShortName:	PP_CONTROL
Power:	Always on
Reset:	soft

DWord	Bit	Description
0	31:16	**Reserved**
	15:9	**Reserved** Format: MBZ
	8:4	**Reserved** Format: MBZ
	3	**VDD Override** This bit is used to force on VDD for the embedded DisplayPort panel so AUX transactions can occur without enabling the panel power sequence. This is intended for panels that require VDD to be asserted before accessing AUX port on the receiver. Value / Name: 0b – Not Force 1b – Force Restriction: Restriction : When software clears this bit from '1' to '0' (disable VDD override) it must ensure that T4 power cycle delay is met before setting this bit to '1' again.
	2	**Backlight Enable** This field enables the backlight when hardware is in the correct panel power sequence state. Value / Name: 0b – Disable 1b – Enable

PP_CONTROL

	1	**Power Down on Reset** This field selects whether the panel will run the power down sequence when a reset is detected **Value** / **Name** 0b – Do not run power down on reset 1b – Run power down on reset **Programming Notes** Setting power down on reset is recommended for panel protection.
	0	**Power State Target** This field sets the panel power state target. It can be written at any time and takes effect at the completion of any current power cycle. **Value** / **Name** / **Description** 0b / Off / If panel power is currently on, the power off sequence starts immediately. If a power on sequence is currently in progress, the power off sequence starts after the power on state is reached, which may include a power cycle delay. 1b / On / If panel power is currently off, the power on sequence starts immediately. If a power off sequence is currently in progress, the power on sequence starts after the power off state is reached and the power cycle delay is met. **Restriction** Restriction : A correct Power Cycle Delay value must be programmed before enabling panel power.

PP_DIVISOR

PP_DIVISOR

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0004AF00
Access:	R/W
Size (in bits):	32
Address:	C7210h-C7213h
Name:	Panel Power Cycle Delay and Reference Divisor
ShortName:	PP_DIVISOR
Power:	Always on
Reset:	soft

This register programs the reference divisor and controls how long the panel must remain in a power off condition once powered down.

DWord	Bit	Description
0	31:8	**Reference divider** Default Value: 0004AFh 24 MHz This field provides the value of the divider used for the creation of the panel timer reference clock. The output of the divider is used as the time base (100 us) for all other timers. The value should be (100 * Ref clock frequency in MHz / 2) - 1. **Restriction** Restriction : The value of zero must not be used.
	7:5	**Reserved** Format: MBZ
	4:0	**Power Cycle Delay** Default Value: 00000b 0mS Power cycle delay. Programmable value of time panel must remain in a powered down state after powering down. This provides the time delay for the eDP T12 time value; the shortest time from panel power disable to power enable. If a panel power on sequence is attempted during this delay, the power on sequence will not commence until the delay is complete. The time unit used is the 100 ms timer. This register needs to be programmed to a "+1" value. For instance to achieve 400mS, program a value of 5. Writing a value of 0 selects no delay or is used to abort the delay if it is active. **Restriction** Restriction : A correct value must be programmed before enabling panel power.

PP_OFF_DELAYS

PP_OFF_DELAYS		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	C720Ch-C720Fh	
Name:	Panel Power Off Sequencing Delays	
ShortName:	PP_OFF_DELAYS	
Power:	Always on	
Reset:	soft	

DWord	Bit	Description
0	31:29	**Reserved** Format: MBZ
	28:16	**Power Down delay** This fields provides the delay during power down. Software programs this field with the time delay for the eDP T10 time value; the time from source ending valid video data to source disabling panel power. Software controls the source valid video data output. The time unit is 100us.
	15:13	**Reserved** Format: MBZ
	12:0	**Backlight Off to Power Down** This field provides the backlight off to power down delay. Software programs this field with the time delay for the eDP T9 time value; the time from backlight disable to source ending valid video data. Software controls the backlight disable and source valid video data output. The time unit is 100us.

PP_ON_DELAYS

PP_ON_DELAYS	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	C7208h-C720Bh
Name:	Panel Power On Sequencing Delays
ShortName:	PP_ON_DELAYS
Power:	Always on
Reset:	soft

DWord	Bit	Description
0	31:29	**Reserved** Format: MBZ
	28:16	**Power Up Delay** This field provides the delay during panel power up. Software programs this field with the delay for eDP T3; the time from enabling panel power to when the sink HPD and AUX channel should be ready. Software controls when AUX channel transactions start. The time unit is 100us.
	15:13	**Reserved** Format: MBZ
	12:0	**Power On to Backlight On** This field provides the power on to backlight enable delay. Software controls the source valid video data output and can enable backlight after this delay has been met. Hardware will not allow the backlight to enable until after the power up delay (eDP T3) and this delay have passed. The time unit is 100us.

PP_STATUS

PP_STATUS

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	C7200h-C7203h
Name:	Panel Power Status
ShortName:	PP_STATUS
Power:	Always on
Reset:	soft

DWord	Bit	Description
0	31	**Panel Power On Status** Value / Name / Description: 0b / Off / Panel power down has completed. A power cycle delay may be currently active. 1b / On / Panel is currently powered up or is currently in the power down sequence. **Programming Notes** Software is responsible for enabling the embedded panel display only at the correct point as defined in the mode set sequence.
	30	**Reserved** Format: MBZ
	29:28	**Power Sequence Progress** Value / Name / Description: 00b / None / Panel is not in a power sequence 01b / Power Up / Panel is in a power up sequence (may include power cycle delay) 10b / Power Down / Panel is in a power down sequence 11b / Reserved / Reserved
	27	**Power Cycle Delay Active** Power cycle delays occur after a panel power down sequence or after a hardware reset. Value / Name: 0b / Not Active **[Default]** 1b / Active
	26:4	**Reserved** Format: MBZ

PP_STATUS		
	3:0	**Reserved**

PPGTT Page Fault Data Registers

PP_PFD[0:31] - PPGTT Page Fault Data Registers

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	04580h

The GTT Page Fault Log entries can be read from these registers.
4580h-4583h: Fault Entry 0
...
45FCh-45FFh: Fault Entry 31

DWord	Bit	Description
0	31:12	**Fault Entry Page Address** Format: GraphicsAddress[31:12] This RO field contains the faulting page address for this Fault Log entry. This field will contain a valid fault address only if the bit in the GTT Page Fault Indication Register corresponding with the address offset of this entry is set.
	11:0	**Reserved** Format: MBZ

Predicate Rendering Data Result

MI_PREDICATE_RESULT - Predicate Rendering Data Result		
Register Space:	MMIO: 0/2/0	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02418h	
DWord	**Bit**	**Description**
0	31:1	**Reserved** Format: PBC
	0	**MI_PREDICATE_RESULT** This bit is the result of the last MI_PREDICATE.

Predicate Rendering Data Result 1

MI_PREDICATE_RESULT_1 - Predicate Rendering Data Result 1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0241Ch-0241Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_RCSUNIT
Address:	1241Ch-1241Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_VCSUNIT0
Address:	1A41Ch-1A41Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_VECSUNIT
Address:	1C41Ch-1C41Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_VCSUNIT1
Address:	2241Ch-2241Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_BCSUNIT

DWord	Bit	Description
0	31:1	**Reserved** Format: PBC
	0	**MI_PREDICATE_RESULT_1** This bit is used to predicate MI_BATCH_BUFFER_START commands in the RCS command stream. Usage Model: MI_MATH command will be used to do some ALU operations over GPR followed by a MI_LOAD_REGISTER_REGISTER to move the result from GPR to MI_PREDICATE_RESULT_1.

Predicate Rendering Data Result 2

MI_PREDICATE_RESULT_2 - Predicate Rendering Data Result 2

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	023BCh-023BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_RCSUNIT
Address:	123BCh-123BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_VCSUNIT0
Address:	1A3BCh-1A3BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_VECSUNIT
Address:	1C3BCh-1C3BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_VCSUNIT1
Address:	223BCh-223BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_BCSUNIT

DWord	Bit	Description
0	31:1	**Reserved** Format: MBZ
	0	**MI_PREDICATE_RESULT_2** This bit must be loaded with by SW based on GT mode of operation. This register must be loaded appropriately before using MI_SET_PREDICATE command. Value / Name / Description 0h / **[Default]** / Indicates GT2 mode and lower slice is disabled. 1h / / Indicates GT3 mode and lower slice is enabled.

Predicate Rendering Data Storage

MI_PREDICATE_DATA - Predicate Rendering Data Storage	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	02410h-02417h

DWord	Bit	Description
0	63:32	**MI_PREDICATE_DATA_UDW** This register is used either as computed value based off the MI_PREDICATE_SRC0 and MI_PREDICATE_SRC1 or a temporary register. See Predicate Rendering section for more details.
	31:0	**MI_PREDICATE_DATA_LDW** This register is used either as computed value based off the MI_PREDICATE_SRC0 and MI_PREDICATE_SRC1 or a temporary register. See Predicate Rendering section for more details.

Predicate Rendering Temporary Register0

MI_PREDICATE_SRC0 - Predicate Rendering Temporary Register0	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	02400h-02407h

DWord	Bit	Description
0	63:0	**MI_PREDICATE_SRC0** This register is a temporary register for Predicate Rendering. See Predicate Rendering section for more details.

Predicate Rendering Temporary Register1

MI_PREDICATE_SRC1 - Predicate Rendering Temporary Register1		
Register Space:	MMIO: 0/2/0	
Source:	RenderCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Address:	02408h-0240Fh	
DWord	**Bit**	**Description**
0	63:0	**MI_PREDICATE_SRC1** This register is a temporary register for Predicate Rendering. See Predicate Rendering section for more details.

Preemption Hint

PREEMPTION_HINT - Preemption Hint	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	024BCh-024BFh
Name:	Preemption Hint
ShortName:	PREEMPTION_HINT_RCSUNIT
Address:	124BCh-124BFh
Name:	Preemption Hint
ShortName:	PREEMPTION_HINT_VCSUNIT0
Address:	1A4BCh-1A4BFh
Name:	Preemption Hint
ShortName:	PREEMPTION_HINT_VECSUNIT
Address:	1C4BCh-1C4BFh
Name:	Preemption Hint
ShortName:	PREEMPTION_HINT_VCSUNIT1
Address:	224BCh-224BFh
Name:	Preemption Hint
ShortName:	PREEMPTION_HINT_BCSUNIT

Description	Source
This register contains the Head pointer offset in to the Ring Buffer or the Dword aligned Graphics address in to the Batch Buffer corresponding to either MI_ARB_CHECK called Preemption Hint Address. When Preemption Hint Address is enabled, RCS will honor UHPTR only on parsing MI_ARB_CHK at Preemption Hint Address.	
This register contains the Head pointer offset into the Ring Buffer or the Dword aligned Graphics address into the Batch Buffer corresponding to the below listed commands in execlist mode of operation • MI_ARB_CHECK • MI_WAIT_FOR_EVENT • MI_SEMAPHORE_WAIT • 3D_PRIMITIVE • GPGPU_WALKER	RenderCS

PREEMPTION_HINT - Preemption Hint

• MEDIA_STATE_FLUSH • PIPE_CONTROL (Only in GPGPU mode of pipeline selection) • MI_ATOMIC (Post Sync Operation set in GPGPU mode of pipeline selection) • MI_SEMAPHORE_SIGNAL (Post Sync Operation set in GPGPU mode of pipeline selection)	
This register contains the Head pointer offset into the Ring Buffer or the Dword aligned Graphics address into the Batch Buffer corresponding to the below listed commands in execlist mode of operation • MI_ARB_CHECK • MI_WAIT_FOR_EVENT • MI_SEMAPHORE_WAIT	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS

Programming Notes

Programming Restriction:
Ring BUffer Mode Of Scheduling: This register must NEVER be programmed in functional mode, this should be used only in validation mode to achieve deterministic behavior of UHPTR being sampled by a given MI_ARB_CHECK in command stream. Programmer has to ensure that RCS Preemption Hint register gets programmed before UHPTR is programmed and well before RCS crosses the corresponding execution point. Preemption hint for both RingBuffer and Batch Buffer can't be enabled simultaneously.

This register must NEVER be programmed in functional mode, this should be used only in validation mode to achieve deterministic behavior of preemption to match behvioral functional models.
User must ensure the Preempted Hint Address programmed matches either Ring Head Offset or Batch Buffer Graphics Virtual Address and not both of them.
User must also ensure the Preempted Hint Address[19:0] programmed matches either Ring Head Offset[19:0] or Batch Buffer Graphics Virtual Address[19:0] and not both of them.

DWord	Bit	Description
0	31:2	**Preempted Hint Address** Format: U30 Format: GraphicsAddress[31:2] This field contains the Head offset in to the Ring Buffer when Preemption Hint is set to Ring Buffer and Dword aligned Graphics Address in to the batch buffer when Preemption Hint is set to Batch Buffer.
	1	**Batch Buffer Preemption Hint** Format: Enabled

Value	Name	Description
0h	Disabled	Preemption hint is disabled in batch buffer.
1h	Enabled	Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Batch Buffer.

PREEMPTION_HINT - Preemption Hint

	0	**Ring Preemption Hint** Format: Enable **Value** / **Name** / **Description** 0h / Disable / Preemption hint is disabled in ring buffer. 1h / Enabled / Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Ring Buffer.

Preemption Hint Upper DWord

PREEMPTION_HINT_UDW - Preemption Hint Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	024C8h-024CBh
Name:	Preemption Hint Upper DWord
ShortName:	PREEMPTION_HINT_UDW_RCSUNIT
Address:	124C8h-124CBh
Name:	Preemption Hint Upper DWord
ShortName:	PREEMPTION_HINT_UDW_VCSUNIT0
Address:	1A4C8h-1A4CBh
Name:	Preemption Hint Upper DWord
ShortName:	PREEMPTION_HINT_UDW_VECSUNIT
Address:	1C4C8h-1C4CBh
Name:	Preemption Hint Upper DWord
ShortName:	PREEMPTION_HINT_UDW_VCSUNIT1
Address:	224C8h-224CBh
Name:	Preemption Hint Upper DWord
ShortName:	PREEMPTION_HINT_UDW_BCSUNIT

This register contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the Batch Buffer corresponding to MI_ARB_CHECK command called Preemption Hint Address.

Programming Notes

This register should NEVER be programmed in functional mode, this should be used only in validation mode to achieve deterministic behavior of UHPTR being sampled by a given MI_ARB_CHK in command stream.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:0	**Preempted Hint Address Upper DWORD** Format: GraphicsAddress[47:32]

Primitives Generated By VF

IA_PRIMITIVES_COUNT - Primitives Generated By VF	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02318h

This register stores the count of primitives generated by VF. This register is part of the context save and restore. More details about the precise event counted by this register are located **here**.

DWord	Bit	Description
0	63:32	**IA Primitives Count Report UDW** Total number of primitives output by the Vertex Fetch (IA) stage. This count is updated for every primitive output by the VF stage, as long as Statistics Enable is set in VF_STATE (see the Vertex Fetch Chapter in the 3D Volume.)
	31:0	**IA Primitives Count Report LDW** Total number of primitives output by the Vertex Fetch (IA) stage. This count is updated for every primitive output by the VF stage, as long as Statistics Enable is set in VF_STATE (see the Vertex Fetch Chapter in the 3D Volume.)

Private PAT

PRIV_PAT - Private PAT		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000003	
Size (in bits):	32	
Address:	040E8h	
DWord	**Bit**	**Description**
0	31:0	**Private PAT** Default Value: 00000003h Access: R/W Bit[31:8]: Reserved.

Private PAT

PRIV_PAT - Private PAT		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	040E8h	
DWord	**Bit**	**Description**
0	31:0	**Private PAT** Default Value: 00000000h Access: R/W Bit[31:16]: Reserved. Bit[15:8]: PPGTT Private PAT. (See bit[7:0] for definition.) Bit[7:6]: Reserved. Bit[5:4]: (See below.) 00b: Age is 0. 01b: Age is 1. 10b: Age is 2. 11b: Age is 3. Bit[3:2]: (See below.) 00b: Override to eLLC Only. (This setting overrides the memory_object_control_state via surface state to be eLLC target only.) 01b: eLLC only. 10b: LLC only. 11b: eLLC/LLC. Bit[1:0]: (see below): 00b: Uncached with fence. 01b: Write Combining (traditional UC). 10b: Write Through. 11b: Write Back.

PS_CTRL

PS_CTRL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank after armed
Double Buffer Armed By:	Write to PS_WIN_SZ
Address:	68180h-68183h
Name:	PS Control 1
ShortName:	PS_CTRL_1_A
Power:	PG1
Reset:	soft
Address:	68280h-68283h
Name:	PS Control 1
ShortName:	PS_CTRL_2_A
Power:	PG1
Reset:	soft
Address:	68980h-68983h
Name:	PS Control 1
ShortName:	PS_CTRL_1_B
Power:	PG2
Reset:	soft
Address:	68A80h-68A83h
Name:	PS Control 1
ShortName:	PS_CTRL_2_B
Power:	PG2
Reset:	soft
Address:	69180h-69183h
Name:	PS Control 1
ShortName:	PS_CTRL_1_C
Power:	PG2
Reset:	soft

PS_CTRL

Description

The pipe scalers are used to scale the output of a display pipe or of a display plane. Pipe A and B have two scalers each and Pipe C has one.
The scaler preserves 8 bits of alpha and 10 bits of each color channel for plane scaling and 12 bits of each color channel for pipe scaling.
The scalers can be assigned to any plane (except cursor) output or the output of the display pipe (after blending and color correction, before dithering and color clamping).
The scalers support horizontal source sizes up to 4096 pixels.
The '7x5' scaler mode supports up to 2.99 in each direction.
The 'Dynamic' scaler mode supports up to 2.99 in both directions when operating on horizontal source sizes up to 2048 pixels. It will only support up to 1.99 in the vertical direction when operating on horizontal source sizes greater than 2048 pixels.
The 'NV12' scaler mode supports up to 1.99 downscaling in each direction.

Programming Notes

Driver is responsible for making sure all the plane, pipe, and scaler size registers are programmed appropriately and gets applied atomically to the same frame since hardware does not ensure an atomic update of plane, scaler, and pipe source size registers.

Restriction

Restriction : Down scaling (scaler input size is larger than scaler window size) can reduce the maximum supported pixel rate for a pipe as well as increase the watermark and data buffer requirements. Refer to the Display Resolution Support page and Watermark Calculations page for detailed calculations.

Restriction :
Scalers must not be enabled when the horizontal source size is greater than 4096 pixels.
Scaler 1 and 2 must not be both scaling the same plane output.
When scaling a pipe, the scaler window size and position must fit within the pipe active size.
When scaling a plane, the plane position must be programmed to 0 and the scaler window size and position must fit within the pipe source size.
When scaling is enabled, the scaler input width should be a minimum of 8 pixels and the height should be minimum of 8 scanlines.
When the plane scaling is used with YUV 420 planar formats, the height should be a minimum of 16 scanlines.
When using down scaling (scaler input size is larger than scaler output size) the maximum supported pixel rate will be reduced by the down scale amount.

DWord	Bit	Description
0	31	**Enable Scaler** This field enables the scaler. Value: 0b — Name: Disable Value: 1b — Name: Enable
	30	**Reserved** Format: MBZ

PS_CTRL

29:28 **Scaler Mode**

Value	Name	Description
00b	Dynamic	Supports 7x5 (HorizontalxVertical) filtering up to 2048 horizontal source sizes and automatically switches to 5x3 filtering for larger sizes.
01b	7x5	Supports 7x5 (HorizontalxVertical) filtering up to 4096 horizontal source sizes. In this mode the other scaler should not be enabled. This mode is supported only in Pipe A and B.
10b	NV12	This mode should be programmed when using plane scaler with the NV12 surface format. This mode uses 5x3 (HorizontalxVertical) filtering.

Restriction
Restriction : 7x5 filtering mode with horizontal source sizes greater than 2048 is supported only with Scaler 1 (PS_CTRL_1_*). And, when the Scaler 1 is used in 7x5 extended mode, the scaler 2 should not be enabled.Exended 7x5 mode is not supported in pipe C.

27:25 **Scaler Binding**

This field selects the where the scaling operation is done.
When scaling a pipe, the pipe source size specifies the input size to the scaler.
When scaling a plane, the PLANE_SIZE specifies the input size to the scaler.
Any border around a scaled plane window will become transparent at the plane blender.

Value	Name
000b	Pipe Scaler
001b	Plane 1 Scaler
010b	Plane 2 Scaler
011b	Plane 3 Scaler
100b	Plane 4 Scaler

Restriction
Restriction : The scaler input size should be atleast 8 scanlines. Plane/Pipe scaling is not compatible with interlaced fetch mode. Plane up and down scaling is not compatible with keying. Keying can be enabled with 1:1 plane scaling. Plane scaling is not compatible with the Indexed 8-bit, XR_BIAS, and Floating Point source pixel formats, or any pixel values less than 0 or greater than 1.

24:23 **FILTER SELECT**

This field selects filter coefficients. The medium coefficients will provide an unfiltered image when the scale factor is 1:1.

Value	Name
00b	Medium

PS_CTRL

		01b	Medium
		10b	Edge Enhance
		11b	Bilinear
	22	**Reserved**	
		Format:	MBZ
	21	**Reserved**	
	20	**Reserved**	
	19:18	**Reserved**	
		Format:	MBZ
	17	**Reserved**	
	16:9	**Reserved**	
		Format:	MBZ
	8	**Reserved**	
	7	**Reserved**	
	6:5	**Reserved**	
	4:0	**Reserved**	
		Format:	MBZ

PS_ECC_STAT

PS_ECC_STAT	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/WC
Size (in bits):	32
Address:	681D0h-681D3h
Name:	PS ECC Status 1
ShortName:	PS_ECC_STAT_1_A
Power:	PG1
Reset:	soft
Address:	682D0h-682D3h
Name:	PS ECC Status 1
ShortName:	PS_ECC_STAT_2_A
Power:	PG1
Reset:	soft
Address:	689D0h-689D3h
Name:	PS ECC Status 1
ShortName:	PS_ECC_STAT_1_B
Power:	PG2
Reset:	soft
Address:	68AD0h-68AD3h
Name:	PS ECC Status 1
ShortName:	PS_ECC_STAT_2_B
Power:	PG2
Reset:	soft
Address:	691D0h-691D3h
Name:	PS ECC Status 1
ShortName:	PS_ECC_STAT_1_C
Power:	PG2
Reset:	soft

Each of these fields is a sticky bit that gives the ECC error status for a particular memory bank.
A '1' in a bit indicates that ECC detected an error. A write of '1' to a bit will clear the bit.
Single errors are corrected by ECC. Double errors are not correctable.

DWord	Bit	Description

PS_ECC_STAT		
0	31:24	**Reserved** Format: MBZ
	23	**Double Error Bank 7**
	22	**Double Error Bank 6**
	21	**Double Error Bank 5**
	20	**Double Error Bank 4**
	19	**Double Error Bank 3**
	18	**Double Error Bank 2**
	17	**Double Error Bank 1**
	16	**Double Error Bank 0**
	15:8	**Reserved** Format: MBZ
	7	**Single Error Bank 7**
	6	**Single Error Bank 6**
	5	**Single Error Bank 5**
	4	**Single Error Bank 4**
	3	**Single Error Bank 3**
	2	**Single Error Bank 2**
	1	**Single Error Bank 1**
	0	**Single Error Bank 0**

PS_HPHASE

PS_HPHASE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of horizontal blank after armed
Double Buffer Armed By:	Write to PS_WIN_SZ
Address:	68194h-68197h
Name:	PS Horizontal Phase 1
ShortName:	PS_HPHASE_1_A
Power:	PG1
Reset:	soft
Address:	68294h-68297h
Name:	PS Horizontal Phase 1
ShortName:	PS_HPHASE_2_A
Power:	PG1
Reset:	soft
Address:	68994h-68997h
Name:	PS Horizontal Phase 1
ShortName:	PS_HPHASE_1_B
Power:	PG2
Reset:	soft
Address:	68A94h-68A97h
Name:	PS Horizontal Phase 1
ShortName:	PS_HPHASE_2_B
Power:	PG2
Reset:	soft
Address:	69194h-69197h
Name:	PS Horizontal Phase 1
ShortName:	PS_HPHASE_1_C
Power:	PG2
Reset:	soft

PS_HPHASE

This register programs the scaler horizontal filtering initial phase.
The initial phase within the -0.5 to 1.5 range is supported. Refer to PS_VPHASE for programming details.

DWord	Bit	Description
0	31:30	**Y Initial HPhase Int** This field specifies the integer part of the Y horizontal filtering initial phase when the scaler is operating on YUV420 hybrid planar formats.This field is ignored for non-YUV420 pixel formats.
	29:17	**Y Initial HPhase Frac** This field specifies the fractional part of the Y horizontal filtering initial phase when the scaler is operating on YUV420 hybrid planar formats.This field is ignored for non-YUV420 pixel formats.
	16	**Y Initial HPhase Trip** This field specifies whether the initial trip, that may occur while applying the initial phase, is used in Y horizontal filtering.This field is ignored for non-YUV420 pixel formats. Value: 1b — Name: Enable Value: 0b — Name: Disable
	15:14	**UV or RGB Initial HPhase Int** This field specifies the integer part of the UV or RGB horizontal filtering initial phase.
	13:1	**UV or RGB Initial HPhase Frac** This field specifies the fractional part of the UV or RGB horizontal filtering initial phase.
	0	**UV or RGB Initial HPhase Trip** This field specifies whether the initial trip, that may occur while applying the initial phase, is used in UV or RGB horizontal filtering. Value: 1b — Name: Enable Value: 0b — Name: Disable

PS_HSCALE

PS_HSCALE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	68190h-68193h
Name:	PS Horizontal Scale 1
ShortName:	PS_HSCALE_1_A
Power:	PG1
Reset:	soft
Address:	68290h-68293h
Name:	PS Horizontal Scale 1
ShortName:	PS_HSCALE_2_A
Power:	PG1
Reset:	soft
Address:	68990h-68993h
Name:	PS Horizontal Scale 1
ShortName:	PS_HSCALE_1_B
Power:	PG2
Reset:	soft
Address:	68A90h-68A93h
Name:	PS Horizontal Scale 1
ShortName:	PS_HSCALE_2_B
Power:	PG2
Reset:	soft
Address:	69190h-69193h
Name:	PS Horizontal Scale 1
ShortName:	PS_HSCALE_1_C
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31:18	**Reserved** Format: MBZ

PS_HSCALE		
	17:15	**HScale Int** Access: RO This field gives the integer part of the horizontal scaling factor divided by the oversampling rate. HSCALE_INT = int(src width/dest width)
	14:0	**HScale Frac** Access: RO This field gives the fractional part of the horizontal scaling factor divided by the oversampling rate. HSCALE_FRAC = int(((src width/dest width)-HSCALE_INT)*2^^15)

PS_PWR_GATE

PS_PWR_GATE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank after armed
Double Buffer Armed By:	Write to PS_WIN_SZ
Address:	68160h-68163h
Name:	Power Gate Control 1
ShortName:	PS_PWR_GATE_1_A
Power:	PG1
Reset:	soft
Address:	68260h-68263h
Name:	Power Gate Control 1
ShortName:	PS_PWR_GATE_2_A
Power:	PG1
Reset:	soft
Address:	68960h-68963h
Name:	Power Gate Control 1
ShortName:	PS_PWR_GATE_1_B
Power:	PG2
Reset:	soft
Address:	68A60h-68A63h
Name:	Power Gate Control 1
ShortName:	PS_PWR_GATE_2_B
Power:	PG2
Reset:	soft
Address:	69160h-69163h
Name:	Power Gate Control 1
ShortName:	PS_PWR_GATE_1_C
Power:	PG2
Reset:	soft

<table>
<tr><th>DWord</th><th>Bit</th><th>Description</th></tr>
<tr><td rowspan="6">0</td><td>31</td><td>Reserved</td></tr>
<tr><td>30:6</td><td>Reserved
Format: MBZ</td></tr>
<tr><td>5</td><td>Reserved
Format: MBZ</td></tr>
<tr><td>4:3</td><td>Settling Time
Time for RAMs in a given filter group to settle after they are powered up.
<table><tr><th>Value</th><th>Name</th></tr><tr><td>00b</td><td>32 cdclks</td></tr><tr><td>01b</td><td>64 cdclks</td></tr><tr><td>10b</td><td>96 cdclks</td></tr><tr><td>11b</td><td>128 cdclks</td></tr></table></td></tr>
<tr><td>2</td><td>Reserved
Format: MBZ</td></tr>
<tr><td>1:0</td><td>SLPEN Delay
Delay between sleep enables of individual banks of RAMs.
<table><tr><th>Value</th><th>Name</th></tr><tr><td>00b</td><td>8 cdclks</td></tr><tr><td>01b</td><td>16 cdclks</td></tr><tr><td>10b</td><td>24 cdclks</td></tr><tr><td>11b</td><td>32 cdclks</td></tr></table></td></tr>
</table>

PS_VPHASE

PS_VPHASE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank after armed
Double Buffer Armed By:	Write to PS_WIN_SZ
Address:	68188h-6818Bh
Name:	PS Vertical Phase 1
ShortName:	PS_VPHASE_1_A
Power:	PG1
Reset:	soft
Address:	68288h-6828Bh
Name:	PS Vertical Phase 1
ShortName:	PS_VPHASE_2_A
Power:	PG1
Reset:	soft
Address:	68988h-6898Bh
Name:	PS Vertical Phase 1
ShortName:	PS_VPHASE_1_B
Power:	PG2
Reset:	soft
Address:	68A88h-68A8Bh
Name:	PS Vertical Phase 1
ShortName:	PS_VPHASE_2_B
Power:	PG2
Reset:	soft
Address:	69188h-6918Bh
Name:	PS Vertical Phase 1
ShortName:	PS_VPHASE_1_C
Power:	PG2
Reset:	soft

PS_VPHASE

This register programs the scaler vertical filtering initial phase.The programming of this register is ignored in the pipe scaler PF/ID fetch mode, and the pipe scaler is responsible for applying the appropriate vertical phase to the proper frame when interlacing.
The initial phase within the -0.5 to 1.5 range is supported.
Programming +ve intital phase:

- Initial Phase Trip = 1b
- Initial Phase Int = Desired Initial Phase Int
- Initial Phase Frac = Desired Initial Phase Frac

Programming -ve initial phase:

- Initial Phase Trip = 0b
- Initial Phase Int = 00b
- Initial Phase Frac = 1 - Desired Initial Phase Frac

For example, -0.25 initial phase should be programmed as

- Initial Phase Trip = 0b
- Initial Phase Int = 00b
- Initial Phase Frac = 1 - 0.25 = 0.75

The following table shows phase programming for frequently used YUV420 to YUV444 chroma upsampling scenarios.

YUV 420 Chroma Siting	H Phase	V Phase	Programmed H Initial Phase	Programmed H Initial Trip	Programmed V Initial Phase	Programmed V Initial Trip
Top Left	0	0	0	0	0	0
Left (MPEG-2)	0	-0.25	0	0	0.75	0
Center (MPEG-1)	-0.25	-0.25	0.75	0	0.75	0

DWord	Bit	Description
0	31:30	**Y Initial VPhase Int** This field specifies the integer part of the Y vertical filtering initial phase when the scaler is operating on YUV420 hybrid planar formats.This field is ignored for non-YUV420 pixel formats.
	29:17	**Y Initial VPhase Frac** This field specifies the fractional part of the Y vertical filtering initial phase when the scaler is operating on YUV420 hybrid planar formats.This field is ignored for non-YUV420 pixel formats.
	16	**Y Initial VPhase Trip** This field specifies the whether the initial trip, that may occur while applying the initial phase, is used in Y vertical filtering.This field is ignored for non-YUV420 pixel formats.

PS_VPHASE

		Value / **Name** 1b — Used 0b — Not Used
	15:14	**UV or RGB Initial VPhase Int** This field specifies the integer part of the UV or RGB vertical filtering initial phase.
	13:1	**UV or RGB Initial VPhase Frac** This field specifies the fractional part of the UV or RGB vertical filtering initial phase.
	0	**UV or RGB Initial VPhase Trip** This field specifies whether the initial trip, that may occur while applying the initial phase, is used in UV or RGB vertical filtering. **Value** / **Name** 1b — Used 0b — Not Used

PS_VSCALE

PS_VSCALE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	68184h-68187h
Name:	PS Vertical Scale 1
ShortName:	PS_VSCALE_1_A
Power:	PG1
Reset:	soft
Address:	68284h-68287h
Name:	PS Vertical Scale 1
ShortName:	PS_VSCALE_2_A
Power:	PG1
Reset:	soft
Address:	68984h-68987h
Name:	PS Vertical Scale 1
ShortName:	PS_VSCALE_1_B
Power:	PG2
Reset:	soft
Address:	68A84h-68A87h
Name:	PS Vertical Scale 1
ShortName:	PS_VSCALE_2_B
Power:	PG2
Reset:	soft
Address:	69184h-69187h
Name:	PS Vertical Scale 1
ShortName:	PS_VSCALE_1_C
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31:18	**Reserved** Format: MBZ

PS_VSCALE		
	17:15	**VScale Int** Access: RO This field gives the integer part of the vertical scale factor. VSCALE_INT = int(src height/(interlace x dest height)) Interlace = 1/2 in interlace modes, 1 in progressive modes.
	14:0	**VScale Frac** Access: RO This field gives the fractional part of the vertical scale factor. VSCALE_FRAC = int((src height/(interlace x dest height)-VSCALE_INT)*2^^15) Interlace = 1/2 in interlace modes, 1 in progressive modes.

PS_WIN_POS

PS_WIN_POS	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank after armed
Double Buffer Armed By:	Write to PS_WIN_SZ
Address:	68170h-68173h
Name:	PS Window Position 1
ShortName:	PS_WIN_POS_1_A
Power:	PG1
Reset:	soft
Address:	68270h-68273h
Name:	PS Window Position 1
ShortName:	PS_WIN_POS_2_A
Power:	PG1
Reset:	soft
Address:	68970h-68973h
Name:	PS Window Position 1
ShortName:	PS_WIN_POS_1_B
Power:	PG2
Reset:	soft
Address:	68A70h-68A73h
Name:	PS Window Position 1
ShortName:	PS_WIN_POS_2_B
Power:	PG2
Reset:	soft
Address:	69170h-69173h
Name:	PS Window Position 1
ShortName:	PS_WIN_POS_1_C
Power:	PG2
Reset:	soft

PS_WIN_POS

Coordinates are determined with a value of (0,0) being the upper left corner of the display device (rotation does not affect this).

Restriction

Restriction : When scaling a pipe, the scaled output must fit inside the pipe active area, so Pipe active size >= PS window position + PS window size.
When scaling a plane, the scaled output must fit inside the pipe source area, so Pipe source size >= PS window position + PS window size.

DWord	Bit	Description
0	31:29	**Reserved** Format: MBZ
	28:16	**XPOS** This field specifies the horizontal coordinate in pixels of the upper left most pixel of the scaled output window.
	15:12	**Reserved** Format: MBZ
	11:0	**YPOS** This field specifies the vertical coordinate in lines of the upper left most pixel of the scaled output window. **Restriction** Restriction : Bit 0 must be zero for interlaced modes.

PS_WIN_SZ

PS_WIN_SZ	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank
Address:	68174h-68177h
Name:	PS Window Size 1
ShortName:	PS_WIN_SZ_1_A
Power:	PG1
Reset:	soft
Address:	68274h-68277h
Name:	PS Window Size 1
ShortName:	PS_WIN_SZ_2_A
Power:	PG1
Reset:	soft
Address:	68974h-68977h
Name:	PS Window Size 1
ShortName:	PS_WIN_SZ_1_B
Power:	PG2
Reset:	soft
Address:	68A74h-68A77h
Name:	PS Window Size 1
ShortName:	PS_WIN_SZ_2_B
Power:	PG2
Reset:	soft
Address:	69174h-69177h
Name:	PS Window Size 1
ShortName:	PS_WIN_SZ_1_C
Power:	PG2
Reset:	soft
This register specifies the size in pixels of the scaled output window. A programmed value of (100, 100) will result in scaled output window of size 100x100 pixels.	

PS_WIN_SZ

Writes to this register arm PS registers on this pipe. After arming, any write to other PS registers will disarm all PS registers. Subsequent write to this register will arm them again.

Restriction
Restriction : When scaling a pipe, the scaled output must fit inside the pipe active area, so Pipe active size >= PS window position + PS window size. When scaling a plane, the scaled output must fit inside the pipe source area, so Pipe source size >= PS window position + PS window size.

DWord	Bit	Description
0	31:29	**Reserved** Format: MBZ
	28:16	**XSIZE** This field specifies the horizontal size in pixels of the scaled output window.
	15:12	**Reserved** Format: MBZ
	11:0	**YSIZE** This field specifies the vertical size in scan lines of the scaled output window. **Restriction** Restriction : Bit 0 must be zero for interlaced modes.

PS Depth Count

PS_DEPTH_COUNT - PS Depth Count	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02350h

This register stores the value of the count of samples that have passed the depth test. This register is part of the context save and restore. Note that the value of this register can be obtained in a pipeline-synchronous fashion without a pipeline flush by using the 3DCONTROL command. See 3D Overview in the 3D volume.
More details about the precise event counted by this register are located **here**.

DWord	Bit	Description
0..1	63:32	**Depth Count UDW** This register reflects the total number of samples that have passed the depth test (i.e., will be visible). All samples are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Samples that pass the depth test but fail the stencil test will not be counted.
	31:0	**Depth Count LDW** This register reflects the total number of samples that have passed the depth test (i.e., will be visible). All samples are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Samples that pass the depth test but fail the stencil test will not be counted.

PS Depth Count for Slice0

PS_DEPTH_COUNT_SLICE0 - PS Depth Count for Slice0	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	022D8h

This register stores the value of the count of pixels that have passed the depth test in Slice0. This register is part of the context save and restore. This register should not be programmed by SW.Note: In GT3 mode there are two slices Slice0 (Upper Slice) and Slice1 (Lower slice).

DWord	Bit	Description
0..1	63:32	**Depth Count UDW** This register reflects the total number of pixels that have passed the depth test in Slice0(i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.
	31:0	**Depth Count LDW** This register reflects the total number of pixels that have passed the depth test in Slice0(i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.

PS Depth Count for Slice1

PS_DEPTH_COUNT_SLICE1 - PS Depth Count for Slice1	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	022F8h

This register stores the value of the count of pixels that have passed the depth test in Slice1. This register is part of the context save and restore. This register should not be programmed by SW.Note: In GT3 mode there are two slices Slice0 (Upper Slice) and Slice1 (Lower slice).

DWord	Bit	Description
0..1	63:32	**Depth Count UDW** This register reflects the total number of pixels that have passed the depth test in Slice1(i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.
	31:0	**Depth Count LDW** This register reflects the total number of pixels that have passed the depth test in Slice1(i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.

PS Depth Count for Slice2

PS_DEPTH_COUNT_SLICE2 - PS Depth Count for Slice2	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02450h

This register stores the value of the count of pixels that have passed the depth test in Slice2. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0..1	63:32	**Depth Count UDW** This register reflects the depth test in slice2 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.
	31:0	**Depth Count LDW** This register reflects the depth test in slice2 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.

PS Depth Count for Slice3

PS_DEPTH_COUNT_SLICE3 - PS Depth Count for Slice3	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02460h

This register stores the value of the count of pixels that have passed the depth test in Slice3. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0..1	63:32	**Depth Count UDW** This register reflects the depth test in slice3 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.
	31:0	**Depth Count LDW** This register reflects the depth test in slice3 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.

PS Invocation Count

PS_INVOCATION_COUNT - PS Invocation Count		
Register Space:	MMIO: 0/2/0	
Source:	RenderCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Trusted Type:	1	
Address:	02348h	
More details about the precise event counted by this register are located **here**.		
DWord	**Bit**	**Description**
0..1	63:32	**PS Invocation Count UDW** Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.
	31:0	**PS Invocation Count LDW** Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PS Invocation Count for Slice0

PS_INVOCATION_COUNT_SLICE0 - PS Invocation Count for Slice0	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	022C8h

This register stores the value of the count of pixels that get shaded in Slice0. This register is part of the context save and restore. This register should not be programmed by SW.Note: In GT3 mode there are two slices Slice0 (Upper Slice) and Slice1 (Lower slice).

DWord	Bit	Description
0..1	63:32	**PS Invocation Count UDW** Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice0. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.
	31:0	**PS Invocation Count LDW** Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice0. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PS Invocation Count for Slice1

PS_INVOCATION_COUNT_SLICE1 - PS Invocation Count for Slice1	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	022F0h

This register stores the value of the count of pixels that get shaded in Slice0. This register is part of the context save and restore. This register should not be programmed by SW.Note: In GT3 mode there are two slices Slice0 (Upper Slice) and Slice1 (Lower slice).

DWord	Bit	Description
0..1	63:32	**PS Invocation Count UDW** Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice1. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.
	31:0	**PS Invocation Count LDW** Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice1. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PS Invocation Count for Slice2

PS_INVOCATION_COUNT_SLICE2 - PS Invocation Count for Slice2	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02448h

This register stores the value of the count of pixels that get shaded in Slice2. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0..1	63:32	**PS Invocation Count UDW** Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice2. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.
	31:0	**PS Invocation Count LDW** Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice2. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PS Invocation Count for Slice3

PS_INVOCATION_COUNT_SLICE3 - PS Invocation Count for Slice3	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02458h

This register stores the value of the count of pixels that get shaded in Slice3. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0..1	63:32	**PS Invocation Count UDW** Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice3. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.
	31:0	**PS Invocation Count LDW** Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice3. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PSR_EVENT

PSR_EVENT

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/WC
Size (in bits):	32
Address:	6F848h-6F84Bh
Name:	Transcoder EDP PSR Event Mask
ShortName:	PSR_EVENT_EDP
Power:	PG1
Reset:	soft

This register captures the event that caused an exit from PSR or PSR2. The exit events will be set by hardware. Software will need to clear these events.

DWord	Bit	Description
0	31:18	**Reserved** Format: MBZ
	17	**PSR2 watch dog timer expire** Access: R/WC This is a sticky bit which is set when the PSR2 watch dog timer expires, causing PSR exit. Clear by writing with a 1. Value: 0b = Condition Not Detected; 1b = Condition Detected
	16	**PSR2 Disable** Access: R/WC This is a sticky bit which is set when the PSR2 is disabled, causing PSR exit. Clear by writing with a 1. Value: 0b = Condition Not Detected; 1b = Condition Detected
	15	**Selective Update Dirty FIFO Underrun** Access: R/WC This is a sticky bit which is set when the selective update dirty/clean FIFO Underruns, causing PSR exit. Clear by writing with a 1. Value / Name

PSR_EVENT

0b	Condition Not Detected
1b	Condition Detected

14 Selective Update CRC FIFO Underrun

Access:	R/WC

This is a sticky bit which is set when the selective update CRC FIFO Underruns, causing PSR exit.
Clear by writing with a 1.

Value	Name
0b	Condition Not Detected
1b	Condition Detected

13 Reserved

Format:	MBZ

12 Graphics Reset

Access:	R/WC

This is a sticky bit which is set when a graphics reset causes PSR exit.
Clear by writing with a 1.

Value	Name
0b	Condition Not Detected
1b	Condition Detected

11 PCH Interrupt

Access:	R/WC

This is a sticky bit which is set when a PCH Interrupt causes PSR exit.
Clear by writing with a 1.

Value	Name
0b	Condition Not Detected
1b	Condition Detected

10 Memory Up

Access:	R/WC

This is a sticky bit which is set when a PCU memup up event causes PSR exit.
Clear by writing with a 1.

Value	Name
0b	Condition Not Detected
1b	Condition Detected

9 Front Buffer Modify

Access:	R/WC

This is a sticky bit which is set when a front buffer modify causes PSR exit.
Clear by writing with a 1.

PSR_EVENT

Value	Name
0b	Condition Not Detected
1b	Condition Detected

8 Watch dog timer expire

Access:	R/WC

This is a sticky bit which is set when the PSR watch dog timer expires, causing PSR exit.
Clear by writing with a 1.

Value	Name
0b	Condition Not Detected
1b	Condition Detected

7 Reserved

Format:	MBZ

6 Pipe Registers Update

Access:	R/WC

This is a sticky bit which is set when a display pipe register update causes PSR exit.
Clear by writing with a 1.

5 Register Update

Access:	R/WC

This is a sticky bit which is set when a non-pipe register update causes PSR exit.
Clear by writing with a 1.

Value	Name
0b	Condition Not Detected
1b	Condition Detected

4 Reserved

3 KVMR session enable

Access:	R/WC

This is a sticky bit which is set when a KVMR session is enabled, causing PSR exit.
Clear by writing with a 1.

Value	Name
0b	Condition Not Detected
1b	Condition Detected

2 VBI enable

Access:	R/WC

This is a sticky bit which is set when vblank or vsync interrupt is enabled, causing PSR exit.
Clear by writing with a 1.

Value	Name

PSR_EVENT

		0b: Condition Not Detected 1b: Condition Detected
	1	**LPSP mode exit** Access: R/WC This is a sticky bit which is set when LPSP mode is exited, causing PSR exit. This bit is reserved for DDIs Clear by writing with a 1. **Value** / **Name** 0b: Condition Not Detected 1b: Condition Detected
	0	**SRD disable** Access: R/WC This is a sticky bit which is set when SRD enable is cleared, causing PSR exit. Clear by writing with a 1. **Value** / **Name** 0b: Condition Not Detected 1b: Condition Detected

PSR_MASK

PSR_MASK	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x04008000
Access:	R/W
Size (in bits):	32
Address:	60860h-60863h
Name:	Transcoder A PSR Event Mask
ShortName:	PSR_MASK_A
Power:	PG2
Reset:	soft
Address:	61860h-61863h
Name:	Transcoder B PSR Event Mask
ShortName:	PSR_MASK_B
Power:	PG2
Reset:	soft
Address:	62860h-62863h
Name:	Transcoder C PSR Event Mask
ShortName:	PSR_MASK_C
Power:	PG2
Reset:	soft
Address:	6F860h-6F863h
Name:	Transcoder EDP PSR Event Mask
ShortName:	PSR_MASK_EDP
Power:	PG1
Reset:	soft

Description

Some of the masking is controlled here and some in the PIPE_MISC register. There is one instance of this register format per each transcoder A/B/C/EDP.

Restriction

Restriction : Only bit 30 (Idle Frame Override) can be changed while PSR or PSR2 is enabled. The other fields must not be changed while PSR or PSR2 is enabled.

DWord	Bit	Description
0	31:30	**Idle Frame Override** This field overrides the entry/exit conditions to force PSR or PSR2 Deep Sleep entry/exit.

PSR_MASK

Value	Name	Description
00b,01b	No Override	Do not override. Use regular entry and exit conditions.
10b	Force Idle Frame	Force Idle Frames to force PSR entry or PSR2 Deep Sleep
11b	Force Non-Idle Frame	Force Non-Idle Frames to force PSR exit or exit from PSR2 Deep Sleep

29 **Reserved**

Format:	MBZ

28 **Mask Max Sleep**

This field controls the mask for the max sleep time event.

Value	Name
0b	Not Masked
1b	Masked

27 **Mask LPSP**

This field controls the mask for the low power single pipe event.
This field is ignored by transcoder A/B/C.

Value	Name
0b	Not Masked
1b	Masked

26 **Mask Memup**

This field controls the mask for the memory up event.

Value	Name	Description
0b	Not Masked	
1b	Masked **[Default]**	Masked - will not be considered in PSR idleness tracking (default)

25 **Mask Hotplug**

This field controls the mask for the hotplug event.Not used in PSR2 Deep Sleep entry/exit.

Value	Name
0b	Not Masked
1b	Masked

24 **Mask FBC Modify**

This field controls the mask for the FBC front buffer modify event.

Value	Name
0b	Not Masked
1b	Masked

23:17 **Reserved**

Format:	MBZ

16 **Mask Display Reg Write**

This field controls the mask for the register write event.

PSR_MASK

		Value / **Name** 0b — Not Masked 1b — Masked
	15	**Exit on Pixel Underrun** This field controls the mask for exit on pixel underrun. 0b — Not Masked 1b — Masked **[Default]**
	14:1	**Reserved** Format: MBZ
	0	**Global Mask** This field is no longer used. The global mask function moved to 0x42084 bit 0. 0b — Not Masked 1b — Masked

PSR2_CTL

PSR2_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00002811
Access:	R/W
Size (in bits):	32
Address:	6F900h-6F903h
Name:	Transcoder EDP PSR2 Control
ShortName:	PSR2_CTL_EDP
Power:	PG1
Reset:	soft

Programming Notes

To use FBC modification tracking for idleness calculations when FBC is disabled, program FBC_CTL CPU Fence Enable, FBC_CONTROL_SA_REGISTER, FBC_CPU_FENCE_OFFSET_REGISTER, FBC_RT_BASE_ADDR_REGISTER, and BLITTER_TRACKING_REGISTER as they are programmed when FBC is enabled.

Restriction

Restriction :
PSR2 is limited to 24bpp 8:8:8, even when using the manual tracking mode.
Only the PSR2 Enable can be changed while PSR2 is enabled. The other fields must not be changed while PSR2 is enabled. Selective Update Tracking Enable must be set before or along with PSR2 enable.

Restriction :
PSR2 is supported for pipe active sizes up to 3640 pixels wide and 2304 lines tall.

DWord	Bit	Description
0	31	**PSR2 Enable** This bit enables Revision 2.0 of the Panel Self Refresh function. Updates will take place at the start of the next vertical blank. The port will send PSR2 VDMs while enabled.

Value	Name
0b	Disable
1b	Enable

Restriction

Restriction : PSR2 must not be enabled when the PSR Setup time from DPCD 00071h is greater than the time for vertical blank minus one line.

Restriction : PSR2 must not be enabled together with Interlacing, Black Frame Insertion (BFI), Compression Mode, or S3D.

PSR2_CTL

30 Selective Update Tracking Enable

Access:	Double Buffered
Double Buffer Update Point:	Start of vertical blank OR transcoder disabled

This field enables the Selective Update Tracking Mechanism.
Updates to this field will take effect at the next vertical blank.

Value	Name
0b	Disable
1b	Enable

Restriction
Restriction : This field must be enabled anytime before or along with PSR2 Enable. It must be disabled along with or anytime after PSR2 disable.

29 Context restore to PSR2 Deep Sleep State

This field restores eDP context to PSR2 Deep Sleep State on a context restore.

Value	Name
0b	Disable
1b	Enable

Restriction
Restriction : This bit should only be used with context save restore.

28:27 Reserved

Format:	MBZ

26 Reserved

25 Reserved

24:20 Max SU Disable Time

Default Value:	00000b Disabled

This field is the maximum time to spend in PSR2 Selective update without fetching a full frame.
It is programmed in increments of sixty frames.
Programming all 1s gives 31x60 frames time.

Restriction
Restriction : Programming all 0s disable the forced fetch of a full frame in SU.

19:15 Reserved

Format:	MBZ

PSR2_CTL

	14:13	**IO buffer Wake** This field selects the number of lines before the Selective Update Region to wake the IO Buffers. **Value** / **Name** 00b: 8 lines 01b: 7 lines **[Default]** 10b: 6 lines 11b: 5 lines
	12:11	**Fast Wake** This field selects the number of lines before the Selective Update Region to send the Fast Wake. **Value** / **Name** 00b: 8 lines 01b: 7 lines **[Default]** 10b: 6 lines 11b: 5 lines
	10	**Reserved** Format: MBZ
	9:8	**TP2 Time** This field selects the TP2 time when training the link on exit from PSR2 DeepSleep (waking). **Value** / **Name** 00b: 500us 01b: 100us 10b: 2.5ms 11b: 50us
	7:4	**Frames Before SU Entry** Default Value: 0001b 1 Frames Before SU Entry This field is the number of frames it takes to enter into Selective Update when PSR2 is enabled.
	3:0	**Idle Frames** Default Value: 0001b 1 idle frame This field is the number of idle frames required before entering PSR2 Deep Sleep.

PSR2_MAN_TRK_CTL

PSR2_MAN_TRK_CTL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank OR transcoder disabled
Address:	6F910h-6F913h
Name:	Transcoder EDP PSR2 Manual Tracking Control
ShortName:	PSR2_MAN_TRK_CTL_EDP
Power:	PG1
Reset:	soft

Programming Notes

The frame is divided into blocks of four scan lines each. SW must provide starting and ending block address of the selective update region.
There can be only one selective update region in a frame.
HW tracking of the selective update region will be disabled when this bit is set.

DWord	Bit	Description
0	31	**PSR2 Manual Tracking Enable** This bit enables the manual tracking mode for PSR2 Selective Update. Value: 0b – Disable; 1b – Enable
	30:21	**SU Region Start Address** This field indicates the starting block address of the selective update region.
	20:11	**SU Region End Address** This field indicates the ending block address of the selective update region.
	10:0	**Reserved** Format: MBZ

PSR2_STATUS

PSR2_STATUS

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	6F940h-6F943h
Name:	Transcoder EDP PSR2 Status
ShortName:	PSR2_STATUS_EDP
Power:	PG1
Reset:	soft

There is one instance of this register format per each transcoder A/B/C/EDP.

DWord	Bit	Description
0	31:28	**PSR2 State** Access: RO This field indicates the live state of PSR2

Value	Name	Description
0000b	IDLE	Reset state
0001b	CAPTURE	Send capture frame
0010b	CPTURE_FS	Fast sleep after capture frame is sent
0011b	SLEEP	Selective Update
0100b	BUFON_FW	Turn Buffer on and Send Fast wake
0101b	ML_UP	Turn Main link up and send SR
0110b	SU_STANDBY	Selective update or Standby state
0111b	FAST_SLEEP	Send Fast sleep
1000b	DEEP_SLEEP	Enter Deep sleep
1001b	BUF_ON	Turn ON IO Buffer
1010b	TG_ON	Turn ON Timing Generator
Others	Reserved	Reserved

	27:26	**Link Status** Access: RO This field indicates the live status of the link.

Value	Name	Description
00b	Full Off	Link is fully off

PSR2_STATUS

01b	Full On	Link is fully on
10b	Standby	Link is in standby
11b	Reserved	Reserved

25 Reserved

Format:	MBZ

24:20 Max Sleep Time Counter

Access:	RO

This field provides the live status of the sleep time counter.

19:16 PSR2 Deep Sleep Entry Count

Access:	RO

The value in this register represents the number of times PSR2 Deep Sleep has been entered. The count will increment with each entry. After reaching the maximum count value the counter will rollover and continue from 0.

15:9 Reserved

Format:	MBZ

8 Sending TP2

Access:	RO

This field indicates if TP2 is currently being sent.

Value	Name	Description
0b	Not Sending	Not sending TP2
1b	Sending	Sending TP2

7 Reserved

6 Reserved

5 PSR2 deep Sleep Entry Completion

Access:	R/WC

This is a sticky bit which is set on PSR2 deep sleep entry completion.Clear this bit by writing a 1b to it.

Value	Name
0b	Not complete
1b	Complete

PSR2_STATUS

	4	**PSR2 SU Entry Completion** Access: R/WC This is a sticky bit which is set on PSR2 SU entry completion.Clear this bit by writing a 1b to it. Value: 0b — Name: Not complete Value: 1b — Name: Complete
	3:0	**Idle Frame Counter** Access: RO This field provides the live status of the idle frame counter.

PSR2_SU_ECC_STAT

PSR2_SU_ECC_STAT	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/WC
Size (in bits):	32
Address:	6FA64h-6FA67h
Name:	PSR2_SU ECC Status
ShortName:	PSR2_SU_ECC_STAT
Power:	PG1
Reset:	soft

Each of these fields is a sticky bit that gives the ECC error status for a particular memory bank.
A '1' in a bit indicates that ECC detected an error. A write of '1' to a bit will clear the bit.
Single errors are corrected by ECC. Double errors are not correctable.

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23	**Double Error Bank 7**
	22	**Double Error Bank 6**
	21	**Double Error Bank 5**
	20	**Double Error Bank 4**
	19	**Double Error Bank 3**
	18	**Double Error Bank 2**
	17	**Double Error Bank 1**
	16	**Double Error Bank 0**
	15:8	**Reserved** Format: MBZ
	7	**Single Error Bank 7**
	6	**Single Error Bank 6**
	5	**Single Error Bank 5**
	4	**Single Error Bank 4**
	3	**Single Error Bank 3**
	2	**Single Error Bank 2**
	1	**Single Error Bank 1**
	0	**Single Error Bank 0**

PSR2_SU_STATUS

PSR2_SU_STATUS	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000, 0x00000000, 0x00000000
Access:	RO
Size (in bits):	96
Address:	6F914h-6F91Fh
Name:	Transcoder EDP PSR2 Selective Update Status
ShortName:	PSR2_SU_STATUS
Power:	PG1
Reset:	soft

A frame is divided into selective update blocks of four scan lines each.
This register provies the count of the number of selective update blocks per frame, for the last eight frames

DWord	Bit	Description
0	31:30	**Reserved** Format: MBZ
	29:20	**Number of SU blocks in frame N - 2** This field indicates the number of selective update blocks in frame N - 1.
	19:10	**Number of SU blocks in frame N - 1** This field indicates the number of selective update blocks in frame N - 1.
	9:0	**Number of SU blocks in frame N** This field indicates the number of selective update blocks in frame N.
1	31:30	**Reserved** Format: MBZ
	29:20	**Number of SU blocks in frame N - 5** This field indicates the number of selective update blocks in frame N - 1.
	19:10	**Number of SU blocks in frame N - 4** This field indicates the number of selective update blocks in frame N - 1.
	9:0	**Number of SU blocks in frame N - 3** This field indicates the number of selective update blocks in frame N.
2	31:20	**Reserved** Format: MBZ
	19:10	**Number of SU blocks in frame N - 7** This field indicates the number of selective update blocks in frame N - 1.
	9:0	**Number of SU blocks in frame N - 6** This field indicates the number of selective update blocks in frame N.

PTE SW Fault Repair High

PTESWC_H - PTE SW Fault Repair High		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04104h	
DWord	**Bit**	**Description**
0	31:0	**PTE SW Fault Repair High** Default Value: 00000000h Access: R/W Fixed PTE entry is written by SW here.

PTE SW Fault Repair Low

PTESWC_L - PTE SW Fault Repair Low		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04100h	
DWord	**Bit**	**Description**
0	31:0	**PTE SW Fault Repair Low** Default Value: 00000000h Access: R/W Fixed PTE entry is written by SW here.

PWR_WELL_CTL

PWR_WELL_CTL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32

Address:	45400h-45403h
Name:	Power Well Control 1
ShortName:	PWR_WELL_CTL1
Power:	PG0
Reset:	global

Address:	45404h-45407h
Name:	Power Well Control 2
ShortName:	PWR_WELL_CTL2
Power:	PG0
Reset:	global

Description

This register is used for display power control. There are multiple instances of this register format to allow software components to have parallel control of the display power.
PWR_WELL_CTL1 is generally used for BIOS to control power.
PWR_WELL_CTL2 is generally used for driver to control power.
The power enable requests from all sources are logically ORd together to enable the power, so the power will only disable after all sources have requested the power to disable.
When a power well is disabled (powered down), access to any registers in the power well will complete, but write data will be dropped and read data will be all zeroes.
The display connections diagram indicates which functional blocks are contained in each power well. The display MMIO register specification has a field for each register to indicate which power well it is in.

This register is on the ungated clock and the chip reset, not the FLR reset.

Restriction

Restriction : The power request field must not be changed for a resource while a power enable/disable for that resource is currently in progress, as indicated by power well state for that resource.

Restriction : Power wells must be enabled and disabled following the display initialization and mode set sequences.

DWord	Bit	Description
0	31	**Power Well 2 Request** Access: R/W

PWR_WELL_CTL

This field requests power well #2 to enable or disable.

Value	Name
0b	Disable
1b	Enable

Restriction
Restriction : Power well #2 must not be enabled until after FUSE_STATUS Fuse PG1 Distribution Status is Done. Power well #2 must not be enabled when Power well #1 is disabled.

30 Power Well 2 State

Access:	RO

This field indicates the status of power well #2.

Value	Name
0b	Disabled
1b	Enabled

29 Power Well 1 Request

Access:	R/W

This field requests power well #1 to enable or disable.

Value	Name
0b	Disable
1b	Enable

Restriction
Restriction : Power well #1 must not be enabled until after FUSE_STATUS Fuse PG0 Distribution Status is Done. Power well #1 must not be disabled when Power well #2 is enabled.

28 Power Well 1 State

Access:	RO

This field indicates the status of power well #1.

Value	Name
0b	Disabled
1b	Enabled

27:26 Reserved

Format:	MBZ

25:24 Reserved

Format:	MBZ

PWR_WELL_CTL

	23:16	**Reserved** Format: MBZ
	15:14	**Reserved** Format: MBZ
	13:12	**Reserved** Format: MBZ
	11:10	**Reserved** Format: MBZ
	9	**DDI D IO Power Request** Access: R/W This field requests power for DDI D IO to enable or disable. Value: 0b — Name: Disable Value: 1b — Name: Enable
	8	**DDI D IO Power State** Access: RO This field indicates the status of power for DDI D IO. Value: 0b — Name: Disabled Value: 1b — Name: Enabled
	7	**DDI C IO Power Request** Access: R/W This field requests power for DDI C IO to enable or disable. Value: 0b — Name: Disable Value: 1b — Name: Enable
	6	**DDI C IO Power State** Access: RO This field indicates the status of power for DDI C IO. Value: 0b — Name: Disabled Value: 1b — Name: Enabled

PWR_WELL_CTL

	5	**DDI B IO Power Request** Access: R/W This field requests power for DDI B IO to enable or disable. 0b: Disable 1b: Enable
	4	**DDI B IO Power State** Access: RO This field indicates the status of power for DDI B IO. 0b: Disabled 1b: Enabled
	3	**DDI A and DDI E IO Power Request** Access: R/W This field requests power for DDI A and DDI E IO to enable or disable. 0b: Disable 1b: Enable
	2	**DDI A and DDI E IO Power State** Access: RO This field indicates the status of power for DDI A and DDI E IO. 0b: Disabled 1b: Enabled
	1	**Misc IO Power Request** Access: R/W This field requests power for Miscellaneous IO to enable or disable. Miscellaneous IO includes the AUX channels, audio pins, and utility pin.
	0	**Misc IO Power State** Access: RO This field indicates the status of power for Miscellaneous IO.

PWRCTXSAVE Message Register for Boot Controller Unit

MSG_PWRCTXSAVE - PWRCTXSAVE Message Register for Boot Controller Unit

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	0850Ch

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].
To set bit0, for example, the data would be 0x0001_0001.
To clear bit0, for example, the data would be 0x0001_0000.
Note that mask bit is the data bit offset + 16.
Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description
0	31:10	**RSVD** Access: RO
	9	**Power Context Save Request** Access: R/W Power Context Save Request 1'b0: Power context save is not being requested (default). 1'b1: Power context save is being requested. Unit needs to self-clear this bit upon sampling.
	8:0	**QWord Credits for Power Context Save Request** Access: R/W QWord Credits for Power Context Save Request. Minimum Credits = 1: Unit may send 1 QWord pair (enough for first LRI at least). Maximum Credits = 511: Unit may send 511 QWord pairs. A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and consume one QWord credit. Only valid with PWRCTXSAVE_REQ (Bit9).

RAM Clock Gating Control 1

RCGCTL1 - RAM Clock Gating Control 1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000100
Size (in bits):	32
Address:	09410h

RAM Clock Gating Control Registers.

DWord	Bit	Description
0	31	**USBunit RAM Clock Gating Disable** Access: R/W USBunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	30	**VLFunit RAM Clock Gating Disable** Access: R/W VLFunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	29	**VISunit RAM Clock Gating Disable** Access: R/W VISunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	28	**STCunit RAM Clock Gating Disable** Access: R/W STCunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	27	**TDSunit RAM Clock Gating Disable** Access: R/W TDSunit RAM Clock Gating Disable Control:

RCGCTL1 - RAM Clock Gating Control 1

		'0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	26	**VMCunit RAM Clock Gating Disable** Access: R/W VMCunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	25	**QRCunit RAM Clock Gating Disable** Access: R/W QRCunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	24	**SCunit RAM Clock Gating Disable** Access: R/W SCunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	23	**SVLunit RAM Clock Gating Disable** Access: R/W SVLunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	22	**VFunit RAM Clock Gating Disable** Access: R/W VFunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	21	**URBunit RAM Clock Gating Disable** Access: R/W URBunit RAM Clock Gating Disable Control:

RCGCTL1 - RAM Clock Gating Control 1

		'0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	20	**GAMWunit RAM Clock Gating Disable** Access: R/W GAMWunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	19	**SVGunit RAM Clock Gating Disable** Access: R/W SVGunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	18	**RCZunit RAM Clock Gating Disable** Access: R/W RCZunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	17	**RCPBEunit RAM Clock Gating Disable** Access: R/W RCPBEunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	16	**RCCunit RAM Clock Gating Disable** Access: R/W RCCunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	15	**PSDunit RAM Clock Gating Disable** Access: R/W PSDunit RAM Clock Gating Disable Control:

RCGCTL1 - RAM Clock Gating Control 1

		'0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	14	**MTunit RAM Clock Gating Disable** Access: R/W MTunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	13	**SBEunit RAM Clock gating Disable** Access: R/W SBEunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	12	**IZunit RAM Clock Gating Disable** Access: R/W IZunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	11	**IECPunit RAM Clock Gating Disable** Access: R/W IECPunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	10	**ICunit RAM Clock Gating Disable** Access: R/W ICunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	9	**HIZunit RAM Clock Gating Disable** Access: R/W HIZunit RAM Clock Gating Disable Control:

RCGCTL1 - RAM Clock Gating Control 1

		'0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	8	**GAMunit RAM Clock Gating Disable** Default Value: 1b Access: R/W GAMunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	7	**BCunit RAM Clock Gating Disable** Access: R/W BCunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	6	**HDCunit RAM Clock Gating Disable** Access: R/W GAFSunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	5	**DMunit RAM Clock Gating Disable** Access: R/W DMunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	4	**WMFEunit RAM Clock Gating Disable** Access: R/W WMFEunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

RCGCTL1 - RAM Clock Gating Control 1

	3	**CSunit RAM Clock Gating Disable** Access: R/W CSunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	2	**BLBunit RAM Clock Gating Disable** Access: R/W BLBunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	1	**MPCunit RAM Clock Gating Disable** Access: R/W MPCunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	0	**BFunit RAM Clock Gating Disable** Access: R/W BFunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

RAM Clock Gating Control 2

RCGCTL2 - RAM Clock Gating Control 2

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0xFFC00000 [KBL]
Size (in bits):	32
Address:	09414h

RAM Clock Gating Control Registers.

DWord	Bit	Description
0	31	**1x2X Assign fub XOR clock gate disable** Default Value: 1b Access: R/W XOR based unit level clock gating disable in 1x2x_asgn fub: '0' : XOR Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : XOR Clock Gating Disabled. (that is, clocks are toggling, always) WorkAround. This bit must be programmed to 1 when a physical 3-slice part has the middle slice (slice 1) fused off.
	30:28	**VMCRunit clock gate disable** Default Value: 111b Access: R/W VMCR unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	27:25	**SMCRunit clock gate disable** Default Value: 111b Access: R/W SMCR unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	24:22	**MCRunit clock gate disable** Default Value: 111b Access: R/W MCR unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for

RCGCTL2 - RAM Clock Gating Control 2

		functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	21	**MUCunit RAM clock gate disable** Access: R/W MUC unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	20	**WVISunit clock gate disable** Access: R/W WVIS unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	19	**WAVM unit RAM clock gate disable** Access: R/W WAVM unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	18	**WHME unit RAM clock gate disable bit** Access: R/W WHME unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	17	**WIME unit RAM clock gate disable** Access: R/W WIME unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	16	**WMPC unit RAM clock gating disable** Access: R/W WMPC unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for

RCGCTL2 - RAM Clock Gating Control 2

		functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	15	**SDEunit RAM clock gate disable** Access: R/W SDE unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	14	**VSHM unit clock gate disable** Access: R/W VSHM unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	13	**DAPRTS unit RAM clock gate disable** Access: R/W DAPRTS unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.
	12	**GS unit RAM clock gate disable** Access: R/W GS unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	11	**Reserved**
	10	**GAMTunit RAM clock gate disable bit** Access: R/W GAMT unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	9	**VCW unit RAM clock gate disable** Access: R/W VCW unit RAM Clock Gating Disable Control:

RCGCTL2 - RAM Clock Gating Control 2

		'0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	8	**VEO unit RAm clock gate disable** Access: R/W VEO unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	7	**IMEunit RAM clock gate disable** Access: R/W IMEunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	6	**CREunit RAM clock gate disable** Access: R/W CREunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	5	**RSunit RAM clock gate disable** Access: R/W RSunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	4	**MSCunit RAM Clock Gating Disable** Access: R/W MSCunit RAM Clock Gating Disable Control '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	3	**VMXunit RAM Clock Gating Disable** Access: R/W VMXunit RAM Clock Gating Disable Control

RCGCTL2 - RAM Clock Gating Control 2

		'0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	2	**GAunit RAM Clock Gating Disable for all EUs** Access: R/W GAunit RAM Clock Gating Disable Control For all EUs in each Row: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	1	**VSunit RAM Clock Gating Disable** Access: R/W VSunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	0	**HSunit RAM Clock Gating Disable** Access: R/W HSunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

RAWCLK_FREQ

RAWCLK_FREQ	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000018
Access:	R/W
Size (in bits):	32
Address:	C6204h-C6207h
Name:	Rawclk Frequency
ShortName:	RAWCLK_FREQ
Power:	Always on
Reset:	soft

These fields are used to generate a divided down clock for miscellaneous timers in display.

DWord	Bit	Description
0	31:10	**Reserved** Format: MBZ
	9:0	**Rawclk frequency** Default Value: 0000011000b 24 MHz Program this field to match the rawclk frequency. Raw Clock = 24 MHz

RC6 Context Base

RC6CTXBASE - RC6 Context Base		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00D48h	
RC6 Location		
DWord	**Bit**	**Description**
0	31:1	**Reserved** Access: RO
	0	**RC6Context Base Register Lock** Access: R/W Lock 1'b0 : All fields of this register are writable (default) 1'b1 : This register is Read Only BIOS must set this bit to prevent further changes

RC6 LOCATION

RC6LOCATION - RC6 LOCATION		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00D40h	
RC6 Location		
DWord	**Bit**	**Description**
0	31	**Reserved** Access: RO
	30:1	**Reserved** Access: RO
	0	**RC6Context Location** Access: R/W 1'b0 : Send context data to C6SRAM (default) 1'b1 : Send context data to DRAM location specified in RC6MEMBASE

RCC LRA 0

RCC_LRA_0 - RCC LRA 0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x03017E00 [KBL]
Size (in bits):	32
Address:	04A40h

DWord	Bit	Description
0	31:27	**Reserved** Default Value: 00000b Access: RO
	26:18	**RCC LRA1 Min** Access: R/W Minimum value of programmable LRA1. Value: 011000000b — Name: **[Default]**
	17:9	**RCC LRA0 Max** Access: R/W Maximum value of programmable LRA0. Value: 010111111b — Name: **[Default]**
	8:0	**RCC LRA0 Min** Default Value: 000000000b Access: R/W Minimum value of programmable LRA0.

RCC LRA 1

RCC_LRA_1 - RCC LRA 1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x6FF616BD [KBL]
Size (in bits):	32
Address:	04A44h

DWord	Bit	Description
0	31	**Reserved** Default Value: 0b Access: RO
	30:22	**RCC LRA2 Max** Access: R/W Maximum value of programmable LRA2. Value: 110111111b — Name: **[Default]**
	21:13	**RCC LRA2 Min** Access: R/W Minimum value of programmable LRA2. Value: 110110000b — Name: **[Default]**
	12:11	**GATR LRA** Default Value: 10b Access: R/W Which LRA should GATR use.
	10:2	**RCC LRA1 Max** Access: R/W Maximum value of programmable LRA1. If RCCLRA2Min == RCCLRA2Max , GATR LRA is disabled, GATR cycles are mapped to RCCLRA0 If RCCLRA2Min == RCCLRA2Max , GATR LRA is disabled, RCCLRA1Max will default to RCCLRA2Max to reuse GATR entries Value: 110101111b — Name: **[Default]**

RCC_LRA_1 - RCC LRA 1

	1	**MSC LRA** Default Value: 0b Access: R/W Which LRA should MSC use.
	0	**RCC LRA** Default Value: 1b Access: R/W Which LRA should RCC use.

RCC Virtual page Address Registers

RCCTLB_VA - RCC Virtual page Address Registers

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	04A00h-04A03h

These registers are directly mapped to the current Virtual Addresses in the RCCTLB (Render Cache for Color TLB).

DWord	Bit	Description
0	31:12	**Address** Format: GraphicsAddress[31:12] Page virtual address.
	11:0	**Reserved** Format: MBZ

RCZ Virtual Page Address Registers

RCZTLB_VA - RCZ Virtual Page Address Registers

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	04B00h-04B03h

These registers are directly mapped to the current Virtual Addresses in the RCZTLB (Render Cache for Z (Depth), Hi Z, and Stencil TLB).

DWord	Bit	Description
0	31:12	**Address** Format: GraphicsAddress[31:12] Page virtual address.
	11:0	**Reserved** Format: MBZ

RCZ Virtual Page Address Registers

RCZTLB_VA - RCZ Virtual Page Address Registers

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	04B00h-04B03h

These registers are directly mapped to the current Virtual Addresses in the RCZTLB (Render Cache for Z (Depth), Hi Z, and Stencil TLB).

DWord	Bit	Description
0	31:12	**Address** Format: GraphicsAddress[31:12] Page virtual address.
	11:0	**Reserved** Format: MBZ

Ready Bit Vector 0 for TLBPEND registers

TLBPEND_RDY0 - Ready Bit Vector 0 for TLBPEND registers		
Register Space:	MMIO: 0/2/0	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	04708h-0470Bh	
This register contains the ready bits for entries 0-31 of TLBPEND structure (Cycles pending TLB translation).		
DWord	**Bit**	**Description**
0	31:0	**Ready bits per entry**

Ready Bit Vector 1 for TLBPEND registers

TLBPEND_RDY1 - Ready Bit Vector 1 for TLBPEND registers		
Register Space:	MMIO: 0/2/0	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	0470Ch-0470Fh	
This register contains the ready bits for entries 32-63 of TLBPEND structure (Cycles pending TLB translation).		
DWord	**Bit**	**Description**
0	31:0	**Ready bits per entry**

Render TLB Control Register

RTCR - Render TLB Control Register

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	04260h

DWord	Bit	Description
0	31:1	**Reserved** Default Value: 00000000000000000000000000000000b Access: RO
	0	**Invalidate TLBs on the corresponding Engine** Default Value: 0b Access: R/W SW writes 1 to invalidate the TLBs for the associated engine and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs. This bit is self clear.

Reported BitRateControl Convergence Status

MFX_VP8_BRC_CONVERGENCE_STATUS - Reported BitRateControl Convergence Status

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	12928h

This register stores BitRateControl Convergence Status.

DWord	Bit	Description
0	31	**Reserved**
	30:28	**Reserved**
	27	**Reserved**
	26:24	**Reserved**
	23	**Reserved**
	22:20	**Reserved**
	19	**Reserved**
	18:16	**Reserved**
	15:12	**Reserved** Format: MBZ
	11:8	**Total Num of Pass** Format: U4 This bit indicates the number of Multipass including current frame. Note that Initial Pass is not counted.
	7:2	**Reserved** Format: MBZ
	1	**Overflow OR Underflow Flag** Format: U1 This bit indicates the current frame has BRC overflow OR underflow.

MFX_VP8_BRC_CONVERGENCE_STATUS - Reported BitRateControl Convergence Status		
	0	**MB Max. Conformance Flag** Format: U1 This contains flag that indicate Inter MB or Intra MB Max. Conformance is not met. This is legacy support and this feature is not validated.

Reported BitRateControl CumulativeDeltaLoopFilter and LoopFilter 01

MFX_VP8_BRC_CUMULATIVE_D_LOOP_FILTER01 - Reported BitRateControl CumulativeDeltaLoopFilter and LoopFilter 01

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	12920h

This register stores per segement Bit Rate Control DeltaLoopFilter.

DWord	Bit	Description
0	31	**Reserved** Format: MBZ
	30:24	**Segment1 CumulativeDeltaLoopFilter** Format: S6 This contains Segment1 CumulativeDeltaLoopFilter in Bit Rate Control. It accumulates all Segment1 DeltaQindices per pass in Multipass. This register is valid after a BRC pass is done.
	23:22	**Reserved** Format: MBZ
	21:16	**Segment1 LoopFilter** Format: U6 This contains Segment1 LoopFilter used in current frame. This register is valid after a BRC pass is done.
	15	**Reserved** Format: MBZ
	14:8	**Segment0 CumulativeDeltaLoopFilter** Format: S6 This contains Segment0 CumulativeDeltaLoopFilter in Bit Rate Control. It accumulates all Segment0 DeltaQindices per pass in Multipass. This register is valid after a BRC pass is done. If Segmentation is not enabled, this field reflects CumulativeDeltaLoopFilter. If Segmentation is enabled, this field reflects Segment0 CumulativeDeltaLoopFilter.

MFX_VP8_BRC_CUMULATIVE_D_LOOP_FILTER01 - Reported BitRateControl CumulativeDeltaLoopFilter and LoopFilter 01

	7:6	**Reserved** Format: MBZ
	5:0	**Segment0 LoopFilter** Format: U6 This contains Segment0 LoopFilter used in current frame. This register is valid after a BRC pass is done. If Segmentation is not enabled, this field reflects LoopFilter. If Segmentation is enabled, this field reflects Segment0 LoopFilter.

Reported BitRateControl CumulativeDeltaLoopFilter and LoopFilter 23

MFX_VP8_BRC_CUMULATIVE_D_LOOP_FILTER23 - Reported BitRateControl CumulativeDeltaLoopFilter and LoopFilter 23

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	12924h

This register stores per segement Bit Rate Control DeltaLoopFilter.

DWord	Bit	Description
0	31	**Reserved** Format: MBZ
	30:24	**Segment3 CumulativeDeltaLoopFilter** Format: S6 This contains Segment3 CumulativeDeltaLoopFilter in Bit Rate Control. It accumulates all Segment3 DeltaQindices per pass in Multipass. This register is valid after a BRC pass is done.
	23:22	**Reserved** Format: MBZ
	21:16	**Segment3 LoopFilter** Format: U6 This contains Segment3 LoopFilter used in current frame. This register is valid after a BRC pass is done.
	15	**Reserved** Format: MBZ
	14:8	**Segment2 CumulativeDeltaLoopFilter** Format: S6 This contains Segment2 CumulativeDeltaLoopFilter in Bit Rate Control. It accumulates all Segment2 DeltaQindices per pass in Multipass. This register is valid after a BRC pass is done.
	7:6	**Reserved** Format: MBZ

MFX_VP8_BRC_CUMULATIVE_D_LOOP_FILTER23 - Reported BitRateControl CumulativeDeltaLoopFilter and LoopFilter 23		
	5:0	**Segment2 LoopFilter** Format: U6 This contains Segment2 LoopFilter used in current frame. This register is valid after a BRC pass is done.

Reported BitRateControl CumulativeDeltaQindex and Qindex 01

MFX_VP8_BRC_CUMULATIVE_DQ_INDEX01 - Reported BitRateControl CumulativeDeltaQindex and Qindex 01

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	12918h
ShortName:	MFX_VP8_BRC_CUMULATIVE_DQ_INDEX01_VB0

This register stores per segement Bit Rate Control CumulativeDeltaQindex.

DWord	Bit	Description
0	31:24	**Segment1 CumulativeDeltaQindex** Format: S7 This contains Segment1 CumulativeDeltaQindex in Bit Rate Control. It accumulates all Segment1 DeltaQindices per pass in Multipass. This register is valid after a BRC pass is done.
	23	**Reserved** Format: MBZ
	22:16	**Segment1 Qindex** Format: U7 This contains Segment1 Qindex used in current frame. This register is valid after a BRC pass is done.
	15:8	**Segment0 CumulativeDeltaQindex** Format: S7 TThis contains Segment0 CumulativeDeltaQindex in Bit Rate Control. It accumulates all Segment0 DeltaQindices per pass in Multipass. This register is valid after a BRC pass is done. If Segmentation is not enabled, this field reflects CumulativeDeltaQindex. If Segmentation is enabled, this field reflects Segment0 CumulativeDeltaQindex.
	7	**Reserved** Format: MBZ

MFX_VP8_BRC_CUMULATIVE_DQ_INDEX01 - Reported BitRateControl CumulativeDeltaQindex and Qindex 01		
	6:0	**Segment0 Qindex** Format: U7 This contains Segment0 Qindex used in current frame. This register is valid after a BRC pass is done. If Segmentation is not enabled, this field reflects Qindex. If Segmentation is enabled, this field reflects Segment0 Qindex.

Reported BitRateControl CumulativeDeltaQindex and Qindex 23

MFX_VP8_BRC_CUMULATIVE_DQ_INDEX23 - Reported BitRateControl CumulativeDeltaQindex and Qindex 23

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	1291Ch
ShortName:	MFX_VP8_BRC_CUMULATIVE_DQ_INDEX23_VB0

This register stores per segement Bit Rate Control CumulativeDeltaQindex and Qindex.

DWord	Bit	Description
0	31:24	**Segment3 CumulativeDeltaQindex** Format: S7 This contains Segment3 CumulativeDeltaQindex in Bit Rate Control. It accumulates all Segment3 DeltaQindices per pass in Multipass. This register is valid after a BRC pass is done.
	23	**Reserved** Format: MBZ
	22:16	**Segment3 Qindex** Format: U7 This contains Segment3 Qindex used in current frame. This register is valid after a BRC pass is done.
	15:8	**Segment2 CumulativeDeltaQindex** Format: S7 This contains Segment2 CumulativeDeltaQindex in Bit Rate Control. It accumulates all Segment2 DeltaQindices per pass in Multipass. This register is valid after a BRC pass is done.
	7	**Reserved** Format: MBZ

MFX_VP8_BRC_CUMULATIVE_DQ_INDEX23 - Reported BitRateControl CumulativeDeltaQindex and Qindex 23		
	6:0	**Segment2 Qindex** Format: U7 This contains Segment2 Qindex used in current frame. This register is valid after a BRC pass is done.

Reported BitRateControl DeltaLoopFilter

MFX_VP8_BRC_D_LOOP_FILTER - Reported BitRateControl DeltaLoopFilter

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12914h
ShortName:	MFX_VP8_BRC_D_LOOP_FILTER_VB0

This register stores per segement Bit Rate Control DeltaLoopFilter.

DWord	Bit	Description
0	31	**Reserved** Format: MBZ
	30:24	**Segment3 DeltaLoopFilter** Format: S6 This contains Segment3 DeltaLoopFilter in Bit Rate Control. This register is valid after a BRC pass is done
	23	**Reserved** Format: MBZ
	22:16	**Segment2 DeltaLoopFilter** Format: S6 This contains Segment2 DeltaLoopFilter in Bit Rate Control. This register is valid after a BRC pass is done
	15	**Reserved** Format: MBZ
	14:8	**Segment1 DeltaLoopFilter** Format: S6 This contains Segment1 DeltaLoopFilter in Bit Rate Control. This register is valid after a BRC pass is done.
	7	**Reserved** Format: MBZ

MFX_VP8_BRC_D_LOOP_FILTER - Reported BitRateControl DeltaLoopFilter

	6:0	**Segment0 DeltaLoopFilter** Format: S6 This contains Segment0 DeltaLoopFilter in Bit Rate Control. This register is valid after a BRC pass is done. If Segmentation is not enabled, this field reflects DeltaLoopFilter. If Segmentation is enabled, this field reflects Segment0 DeltaLoopFilter.

Reported BitRateControl DeltaQindex

MFX_VP8_BRC_DQ_INDEX - Reported BitRateControl DeltaQindex

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12910h
ShortName:	MFX_VP8_BRC_DQ_INDEX_VB0

This register stores per segement Bit Rate Control DeltaQindex.

DWord	Bit	Description
0	31:24	**Segment3 DeltaQindex** Format: S7 This contains Segment3 DeltaQindex in Bit Rate Control. This register is valid after a BRC pass is done
	23:16	**Segment2 DeltaQindex** Format: S7 This contains Segment2 DeltaQindex in Bit Rate Control. This register is valid after a BRC pass is done
	15:8	**Segment1 DeltaQindex** Format: S7 This contains Segment1 DeltaQindex in Bit Rate Control. This register is valid after a BRC pass is done.
	7:0	**Segment0 DeltaQindex** Format: S7 This contains Segment0 DeltaQindex in Bit Rate Control. This register is valid after a BRC pass is done. If Segmentation is not enabled, this field reflects DeltaQindex. If Segmentation is enabled, this field reflects Segment0 DeltaQindex.

Reported BitRateControl parameter Mask

MFX_VP8_CNTRL_MASK - Reported BitRateControl parameter Mask

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12900h
ShortName:	MFX_VP8_CNTRL_MASK_VB0

This register stores the count of bytes of the bitstream output per frame

DWord	Bit	Description
0	31:6	**Reserved** Format: MBZ
	5	**Final Bitstream Buffer Overrun Mask** Format: U1 This is same bit reflected in MFX_VP8_ENC_CFG DW2 bit5. This denotes Final bitstream buffer overrun feature is enabled.
	4	**Intermediate Bitstream Buffer Overrun Mask** Format: U1 This is same bit reflected in MFX_VP8_ENC_CFG DW2 bit4. This denotes intermediate bitstream buffer overrun feature is enabled.
	3	**Intra MB Bit Count Conformance Mask** Format: U1 This is legacy support as AVC for Intra MB Bit Count conformance. This is same bit reflected in MFX_VP8_ENC_CFG DW2 bit3. This feature is not validated.
	2	**Inter MB Bit Count Conformance Mask** Format: U1 This is legacy support as AVC for Inter MB Bit Count conformance. This is same bit reflected in MFX_VP8_ENC_CFG DW2 bit2. This feature is not validated.

MFX_VP8_CNTRL_MASK - Reported BitRateControl parameter Mask

	1	**Frame Bit Rate Overflow Mask** Format: U1 This is same bit reflected in MFX_VP8_ENC_CFG DW2 bit0. It denotes if Frame Bit Rate Overflow is enabled for Bit Rate Control
	0	**Frame Bit Rate Underflow Mask** Format: U1 This is same bit reflected in MFX_VP8_ENC_CFG DW2 bit1. It denotes if Frame Bit Rate Underflow is enabled for Bit Rate Control

Reported BitRateControl parameter Status

MFX_VP8_CNTRL_STATUS - Reported BitRateControl parameter Status

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12904h
ShortName:	MFX_VP8_CNTRL_STATUS_VB0

This register stores the count of bytes of the bitstream output per frame

DWord	Bit	Description
0	31:8	**Reserved** Format: MBZ
	7	**QindexClampHigh Status** Format: U1 This denotes if Qindex is clamped by QindexClampHigh value programmed in MFX_VP8_PIC_STATE.DW7.
	6	**QindexClampLow Status** Format: U1 This denotes if Qindex is clamped by QindexClampLow value programmed in MFX_VP8_PIC_STATE.DW7.
	5	**Final Bitstream Buffer Overrun Status** Format: U1 This denotes if Final bitstream buffer overrun.
	4	**Intermediate Bitstream Buffer Overrun Status** Format: U1 This denotes if any of the Intermediate bitstream buffer overrun. (including FrameHeader, Partition1 to Partition8)
	3	**Intra MB Bit Count Conformance Status** Format: U1 This is legacy support as AVC for Intra MB Bit Count conformance.

MFX_VP8_CNTRL_STATUS - Reported BitRateControl parameter Status

		It denotes if Intra MB Bit Count meets conformance size. This feature is not validated.
	2	**Inter MB Bit Count Conformance Status** Format: U1 This is legacy support as AVC for Inter MB Bit Count conformance. It denotes if Inter MB Bit Count meets conformance size. This feature is not validated.
	1	**Frame Bit Rate Overflow Status** Format: U1 It denotes if Frame Bit Rate Overflow in current frame
	0	**Frame Bit Rate Underflow Status** Format: U1 It denotes if Frame Bit Rate Underflow in current frame

Reported Bitstream Output Bit Count for Syntax Elements Only

HCP_BITSTREAMSE_BITCOUNT_FRAME - Reported Bitstream Output Bit Count for Syntax Elements Only

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1E9A8h

This register stores the count of number of bits in the bitstream due to syntax elements only. This excludes header/ byte alignment /tail/EMU/CABAC-0word/padding bits but includes the stop-one-bit. This register is part of the context save and restore.

DWord	Bit	Description
0	31:0	**HCP Bitstream Syntax Element Only Bit Count** Format: U32 Total number of bits in the bitstream output due to syntax elements only. It includes the data bytes only. This count is updated for every time the internal bitstream counter is incremented and its reset at image start.

Reported Bitstream Output Bit Count for Syntax Elements Only Register

MFC_BITSTREAM_SE_BITCOUNT_FRAME - Reported Bitstream Output Bit Count for Syntax Elements Only Register	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	128A4h

This register stores the count of number of bits in the bitstream due to syntax elements only. This excludes header/ byte alignment /tail/EMU/CABAC-0word/padding bits but includes the stop-one-bit. This register is part of the context save and restore.

DWord	Bit	Description
0	31:0	**MFC Bitstream Syntax Element Only Bit Count** Total number of bits in the bitstream output due to syntax elements only. It includes the data bytes only. This count is updated for every time the internal bitstream counter is incremented and its reset at image start.

Reported Bitstream Output Byte Count per Frame Register

MFC_BITSTREAM_BYTECOUNT_FRAME - Reported Bitstream Output Byte Count per Frame Register	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	128A0h
This register stores the count of bytes of the bitstream output per frame	

DWord	Bit	Description
0	31:0	**MFC Bitstream Byte Count per Frame** Total number of bytes in the bitstream output per frame from the encoder. This includes header/tail/byte alignment/data bytes/EMU (emulation) bytes/cabac-zero word insertion/padding insertion. This count is updated for every time the internal bitstream counter is incremented and its reset at image start.

Reported Bitstream Output CABAC Bin Count Register

MFC_AVC_CABAC_BIN_COUNT_FRAME - Reported Bitstream Output CABAC Bin Count Register	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	128A8h

This register stores the count of number of bins per frame.

DWord	Bit	Description
0	31:0	**MFC AVC Cabac Bin Count** Total number of BINs in the bitstream output per frame from the encoder. This count is updated for every time the bin counter is incremented and its reset at image start.

Reported Bitstream Output CABAC Insertion Count

HCP_CABAC_INSERTION_COUNT - Reported Bitstream Output CABAC Insertion Count

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1E9B0h

This register stores the count in bytes of **CABAC ZERO_WORD insertion. It is primarily provided for statistical data gathering.**

DWord	Bit	Description
0	31:0	**HCP Cabac Insertion Count** Format: U32 Total number of bytes in the bitstream output before for the CABAC zero word insertion. This count is updated each time when the insertion count is incremented.

Reported Final Bitstream Byte Count

MFX_VP8_FRM_BYTE_CNT - Reported Final Bitstream Byte Count

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12908h

This register stores the count of bytes of the bitstream output per frame

DWord	Bit	Description
0	31:0	**Final BitStream Byte Count** Format: U32 This register contains Final Bitstream byte count

Reported Frame Zero Padding Byte Count

MFX_VP8_FRM_ZERO_PAD - Reported Frame Zero Padding Byte Count

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1290Ch
ShortName:	MFX_VP8_FRM_ZERO_PAD_VB0

This register stores Frame Zero Padding Byte Count

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:0	**Frame Zero Padding Byte Count** Format: U16 This register contains Frame Zero Padding byte count This is legacy support. This feature is not validated.

Reported Timestamp Count

TIMESTAMP - Reported Timestamp Count	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	02358h-0235Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_RCSUNIT
Address:	12358h-1235Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VCSUNIT0
Address:	1A358h-1A35Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VECSUNIT
Address:	1C358h-1C35Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VCSUNIT1
Address:	22358h-2235Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_BCSUNIT

Description	Source
This register provides an elapsed real-time value that can be used as a timestamp for GPU events over short periods of time. Note that the value of this register can be obtained in a 3D pipeline-synchronous fashion without a pipeline flush by using the PIPE_CONTROL command. See 3D Geometry Pipeline in the "3D and Media" volume.This register (effectively) counts at a constant frequency by adjusting the increment amount according to the actual reference clock frequency. SW therefore does not need to know the reference clock frequency.	RenderCS
This register provides an elapsed real-time value that can be used as a timestamp.The accumulated value in this register is of the timestamp stamp granularity (base unit) defined in the “Time Stamp Bases” subsection in Power Management chapter.	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS
This register is *not* reset by a graphics reset. It will maintain its value unless a full chipset reset is performed.	

DWord	Bit	Description

TIMESTAMP - Reported Timestamp Count		
0	63:36	**Reserved** Format: MBZ
	35:32	**Timestamp Value UN** Format: U4 This register increment's for every timestamp base unit. The granularity of the time stamp base unit is defined in the "Time Stamp Bases" subsection in Power Management chapter. Note: This is the Upper Nibble of the Timesamp Value, a 36-bit signal.
	31:0	**Timestamp Value LDW** Format: U32 This register increment's for every timestamp base unit. The granularity of the time stamp base unit is defined in the "Time Stamp Bases" subsection in Power Management chapter.

Report Queue CFG HI

RPTQCFGHI - Report Queue CFG HI		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	098ACh	
Config to MCI and DFT Ring		
DWord	**Bit**	**Description**
0	31	**Report fifo cfg hi valid** Access: RO
	30:18	**RSVD_30_18** Access: RO
	17:16	**Report fifo cfg hi bits 9_8** Access: RO
	15:8	**RSVD_15_8** Access: RO
	7:0	**Report fifo cfg hi bits 0_7** Access: RO

Report Queue CFG LO

RPTQCFGLO - Report Queue CFG LO			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	098A8h		
Config to MCI and DFT Ring			
DWord	**Bit**	**Description**	
0	31:0	**Report fifo cfg low**	
		Access:	RO

Reset Control Register

RESET_CTRL - Reset Control Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	r/w
Size (in bits):	32
Address:	020D0h-020D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_RCSUNIT
Address:	120D0h-120D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_VCSUNIT0
Address:	1A0D0h-1A0D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_VECSUNIT
Address:	1C0D0h-1C0D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_VCSUNIT1
Address:	220D0h-220D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_BCSUNIT

Soft reset flow for an engine (Render, Blitter, Video, Video Enhancement) is asynchronous to the context execution in HW. SW needs a deterministic way to ensure it resets the context it intends to. One way to achieve this is to ensure HW doesn't switch out the context while SW is doing a soft reset. This is achieved by having an explicit interface between HW-SW to prepare the engine prior to the soft reset. SW sets the "Request Reset" in RESET_CTRL register of an engine indicating SW wants to initiate a soft reset flow for the corresponding engine. In response to "Request Reset" bit set, HW sets "Ready for Reset" bit of RESET_CTRL register indicating engine readiness for reset. As part of the reset readiness HW will not allow any context switch to take place and also ensure any ongoing context switch is paused on a clean context boundary (context save in progress is completed, Context Switch Status Buffer updates are allowed to complete).
SW polls for "Ready for Reset" bit to be set before it does soft reset for the corresponding engine. Reading EXECLIST_STATUS register at this point provides the active context in HW that will get reset. On engine reset "Request Reset" bit will get reset with rest of the engine logic.
Upon polling EXECLIST_STATUS register for active context SW might decide not to reset the engine and can reset the "Request Reset" in RESET_CTRL register. On "Request Reset" getting reset by SW, HW must continue with execution.
SW setting "Ready for Reset" bit in RESET_CTRL register of an engine need not be followed by the corresponding

RESET_CTRL - Reset Control Register

engine reset.
SW writing to “Request Reset” bit in RESET_CTRL register is preparing the engine for reset whereas SW writing to GDRST triggers the actual reset flow in HW.

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15:3	**Reserved** Format: MBZ
	2	**Reserved**
	1	**Ready for Reset** Format: U1 When set indicates render engine is ready for reset. This bit gets cleared on engine reset or when Soft Reset In progress is cleared.
	0	**Request Reset** Format: U1 "Request Reset" bit must be read as "Readyness for Reset". When set indicates SW wishes to reset the render engine. On seeing this bit set Command Streamer will take appropriate action and set Ready For Reset status bit. This bit gets cleared on engine reset. This bit can also be cleared by writing "0" to this bit.

Reset Flow Control Messages

RSTFCTLMSG - Reset Flow Control Messages

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	08108h

Soft-Reset and FLR Flow Control Message Registers

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:12	**Reserved** Access: RO Reserved
	11	**MEDIA 1 Reset flow acknowldgement message** Access: R/W PM Acknowledgement Messages for Media 1 reset: '1' : PREP_RST_MEDIA1_ACK - Acknowledgement that graphics media1 (or 2nd vbox) is prepared for reset assertion. '0' : DONE_MEDIA1_RST_ACK - Acknowledgement that graphics media1 (or 2nd vbox) reset is de-asserted
	10	**Reserved**
	9	**Reserved**
	8	**Vebox Reset flow Acknowledge Message** Access: R/W PM Acknowledgement Messages for Vebox reset: '1' : PREP_RST_VEBOX_ACK - Acknowledgement that graphics VE is prepared for reset assertion. '0' : DONE_VEBOX_RST_ACK - Acknowledgement that graphics VE reset is de-asserted

RSTFCTLMSG - Reset Flow Control Messages

	7	**Blitter Reset Flow Acknowledgement Messages** Access: R/W PM Acknowledgement Messages for Blitter reset: '1' : PREP_RST_BLIT_ACK - Acknowledgement that graphics blitter is prepared for reset assertion. '0' : DONE_BLIT_RST_ACK - Acknowledgement that graphics blitter reset is de-asserted
	6	**Media Reset Flow Acknowledgement Messages** Access: R/W PM Acknowledgement Messages for Media reset: '1' : PREP_RST_MEDIA_ACK - Acknowledgement that graphics media block is prepared for reset assertion. '0' : DONE_MEDIA_RST_ACK - Acknowledgement that the graphics media reset is de-asserted
	5	**Render Reset Flow Acknowledgement Messages** Access: R/W PM Acknowledgement Messages for Render reset: '1' : PREP_RST_RENDER_ACK - Acknowledgement that the graphics render block is prepared for reset assertion. '0' : DONE_RENDER_RST_ACK - Acknowledgement that the graphics render reset is de-asserted
	4	**GTI-Device Reset Flow Acknowledgement Messages** Access: R/W PM Acknowledgement Messages for GTI-Device reset: '1' : PREP_RST_GTIDEV_ACK - Acknowledgement that the GTI device is prepared for reset assertion. '0' : DONE_GTIDEV_RST_ACK - Acknowledgement that the GTI device reset is de-asserted
	3	**Reserved** Access: RO Reserved
	2	**FLR Done ack from Pmunit** Access: R/W Set FLR Done ack from Pmunit: 1: PM unit sets this bit to acknowledge the FLR done message has been forwarded to SA through GAM interface. 0: Default Value. If the bit was set by PM then Cpunit hardware clears it once FLR is completed.

RSTFCTLMSG - Reset Flow Control Messages

	1	**Global Resource Arbitration Acknowledgement Messages** Access: R/W Global Resource Arbitration Acknowledgement Message from PM: '1' : CP_ARB_REQ_ACK - Acknowledgement for CPunit's global resource arbitration request '0' : CP_ARB_RELEASE_ACK - Acknowledgement to CPunit's release of global resources
	0	**CP Busy / Idle Status Acknowledgement Messages** Access: R/W CP Busy / Idle Status Acknowledgement Message from PM: '0' : CP_NOT_BUSY_ACK - Acknowledgement that the CPunit is idle. '1' : CP_BUSY_ACK - Acknowledgement that the CPunit is busy.

Resource Streamer Context Offset

RS_CXT_OFFSET - Resource Streamer Context Offset

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00005A40
Access:	Read/32 bit Write Only
Size (in bits):	32
Address:	021B4h

DWord	Bit	Description
0	31:6	**RS Offset** Format: U26 This field indicates the offset (64bytes granular) in to the logical rendering context to which Resource Streamer context is save/restored when enabled. This field register must not be written directly (via MMIO) unless the Command Streamer is completely idle (i.e., the Ring Buffer is empty and the pipeline is idle) and RC6 is disabled. On way to program this register is via Load Register Immediate command in the ring buffer as part of initialization sequence. Value: 169h — **[Default]** — DefaultValueDesc
	5:0	**Reserved** Format: MBZ

Resource Streamer Preemption Status

RS_PREEMPT_STATUS - Resource Streamer Preemption Status

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0215Ch

Preemption from First Level Batch Buffer:
This register contains the offset in to the Batch Buffer on which Resource streamer got preempted. Note that it is offset from the Batch Start Address and not the graphics address corresponding to the preempted instruction on Batch Buffer. This register's contents will be looked at by Command Streamer on the next RS Start Trigger to provide the appropriate batch start address. Following preemption, context save happens on which this register is context saved, after context save the register gets auto reset by Command Streamer. This register gets context save/restored by Render Command Streamer as part of its render context.

Preemption from Second Level Batch Buffer:
This register contains the graphics address of the instruction in Second Level Batch Buffer on which Resource streamer got preempted. This register's contents will be looked at by Command Streamer on the next RS Start Trigger to provide the appropriate batch start address. Following preemption, context save happens on which this register is context saved, after context save the register gets auto reset by Command Streamer. This register gets context save/restored by Render Command Streamer as part of its render context.

Programming Notes

- This register is accessed by Render Command Streamer as part of render context save/restore; this register should be exercised by S/W only for resetting the register contents if required.
- Following preemption if there is no context save, SW should program this register with 0x0 so that it does not interfere with proceeding workloads.

DWord	Bit	Description
0	31:2	**Batch Buffer Offset** Format: Offset[31:2] This field specifies the DWord-aligned offset from the batch start address on which Resource Streamer got preempted.
	1	**RS_PREEMPT_STATUS** Format: MBZ This field when not set indicates RS got preempted on a natural sync point else it got preempted on a draw call.

RS_PREEMPT_STATUS - Resource Streamer Preemption Status		
	0	**RS_PREEMPTED** Default Value: 0 Format: Enable If this bit is set indicates Resource Streamer got preempted. Other fields of this register are valid only when this bit is set.

Revision Identification

RID2_0_2_0_PCI - Revision Identification		
Register Space:	PCI: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	8	
Address:	00008h	
This register contains the revision number for Device #2 Functions 0.		
DWord	**Bit**	**Description**
0	7:4	**Revision Identification Number MSB** Default Value: 0000b Access: R/W Firmware Only Four MSB of RID
	3:0	**Revision Identification Number** Default Value: 0000b Access: R/W Firmware Only Four LSB of RID

RING_BUFFER_HEAD_PREEMPT_REG

RING_BUFFER_HEAD_PREEMPT_REG - RING_BUFFER_HEAD_PREEMPT_REG	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0214Ch-0214Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_RCSUNIT
Address:	1214Ch-1214Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VCSUNIT0
Address:	1A14Ch-1A14Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VECSUNIT
Address:	1C14Ch-1C14Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VCSUNIT1
Address:	2214Ch-2214Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_BCSUNIT

Description

This register contains the Head pointer offset in the ring when the last PREEMPTABLE command was executed and caused the head pointer to move due to the UHPTR register being valid. If the PREEMPTABLE command is executed as part of the batch buffer then the value of the register will be the offset in the ring of the command past the batch buffer start that contained the preemptable command.
This is a global register and context save/restored as part of power context image.

Preemptable Commands	Source
• MI_ARB_CHECK • 3D_PRIMITIVE • GPGPU_WALKER • MEDIA_STATE_FLUSH • PIPE_CONTROL (Only in GPGPU mode of pipeline selection)	RenderCS

RING_BUFFER_HEAD_PREEMPT_REG - RING_BUFFER_HEAD_PREEMPT_REG

- MI_ATOMIC (Post Sync Operation set in GPGPU mode of pipeline selection)
- MI_SEMAPHORE_SIGNAL (Post Sync Operation set in GPGPU mode of pipeline selection)

Preemptable Commands	Source
MI_ARB_CHECK	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS

Programming Notes

Programming Restriction:
This register should NEVER be programmed by driver. This is for HW internal use only.

DWord	Bit	Description
0	31:21	**Last Wrap Count**
	20:2	**Preempted Head Offset** Format: U19 This field contains the Head pointer offset in the ring when the last MI_ARB_CHECK command was executed and caused the head pointer to move due to the UHPTR register being valid.
	1:0	**Ring/Batch Indicator** Format: Enabled 0h Ring — Preemptable command was executed in ring and caused head pointer to be updated. 1h Batch — Preemptable command was executed in batch and caused head pointer to be updated. 2h 2nd level batch — Preemptable command was executed in second level batch and caused head pointer to be updated.

Ring Buffer Control

RING_BUFFER_CTL - Ring Buffer Control	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0203Ch-0203Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_RCSUNIT
Address:	1203Ch-1203Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_VCSUNIT0
Address:	1A03Ch-1A03Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_VECSUNIT
Address:	1C03Ch-1C03Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_VCSUNIT1
Address:	2203Ch-2203Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_BCSUNIT

Description	Source
These registers are used to define and operate the ring buffer mechanism which can be used to pass instructions to the command interface. The buffer itself is located in a physical memory region. The ring buffer is defined by a 4 Dword register set that includes starting address, length, head offset, tail offset, and control information. Refer to the Programming Interface chapter for a detailed description of the parameters specified in this ring buffer register set, restrictions on the placement of ring buffer memory, arbitration rules, and in how the ring buffer can be used to pass instructions.	RenderCS
Ring Buffer Head and Tail Offsets must be properly programmed before it is enabled. A Ring Buffer can be enabled when empty.	BlitterCS, VideoCS, VideoEnhancementCS
Graphics Engine doesn't go IDLE when head offset is not equal to tail offset when ring buffer is disabled.	

DWord	Bit	Description

RING_BUFFER_CTL - Ring Buffer Control

0 | 31:21 | Reserved

Format:	MBZ

20:12 | Buffer Length

Format:	U9-1 in 4 KB pages - 1

This field is written by SW to specify the length of the ring buffer in 4 KB Pages.Range = [0 = 1 page = 4 KB, 1FFh = 512 pages = 2 MB]

Value	Name	Description
0		1 page = 4 KB
1FFh		512 pages = 2 MB

11 | RBWait

Indicates that this ring has executed a WAIT_FOR_EVENT instruction and is currently waiting. Software can write a "1" to clear this bit, write of "0" has no effect. When the RB is waiting for an event and this bit is cleared, the wait will be terminated and the RB will be returned to arbitration.

10 | Semaphore Wait

Description
Indicates that this ring has executed a MI_SEMAPHORE_WAIT instruction and is currently waiting for wait condition to satisfy. Software can write a "1" to clear this bit, write of "0" has no effect.

Programming Notes
Writing a value of '1' will unconditionally cancel the semaphore wait on the next memory comparison. Memory comparison is triggered in signal mode on receiving a semaphore signal and in poll mode on wait timer getting expired.

9 | Reserved

Format:	MBZ

8 | Reserved

Format:	MBZ

7:3 | Reserved

Format:	MBZ

2:1 | Automatic Report Head Pointer

Source:	BSpec

Description
This field is written by software to control the automatic reporting (write) of this ring buffer's Head Pointer register (register DWord 1) to the corresponding location within the Hardware Status Page. Automatic reporting can either be disabled or enabled at 4KB, 64KB or 128KB boundaries within the ring buffer.
When **Execlist Enable** bit is set the head pointer will be reported to the head pointer location

RING_BUFFER_CTL - Ring Buffer Control

in the Per-Process Hardware Status Page.

Value	Name	Description
0	MI_AUTOREPORT_OFF	Automatic reporting disabled
1	MI_AUTOREPORT_64KB	Report every 16 pages (64KB)
2	MI_AUTOREPORT_4KB	Report every page (4KB) This mode must not be enabled in Ring Buffer mode of scheduling to minimize the auto reports.
3	MI_AUTO_REPORT_128KB	Report every 32 pages (128KB).

0 **Ring Buffer Enable**

Format:	Enable

This field is used to enable or disable this ring buffer. It can be enabled or disabled regardless of whether there are valid instructions pending. If disabled and the ring head equals ring tail, all state currently loaded in hardware is considered invalid.

Programming Notes	Source
Ring Buffer Mode of Scheduling: SW must follow the below programming notes during SW initialization phase or while enabling render engine's ring buffer for the first time, this would be coming out of boot, standby, hibernate or reset. This flow must be also followed during ring replay when ring buffer is disabled. • SW must set the Force Wakeup bit to prevent GT from entering C6. • SW must dispatch workload (dummy context) to initialize render engine with default state such that any context switches that occur subsequently (Power Save) will save and restore coherent device state. Indirect pointers used in 3D states must point to valid graphics surface existing in memory. PP_DCLV followed by PP_DIR_BASE register should be programmed as part of initialization workload if PPGTT is enabled in GFX_MODE register. • SW must ensure all the register (MMIO) initialization/programming through CPU happens in this block or latter, this ensures the MMIO state is save/restored on subsequent context switches (Power Sequences). • Once the render engine is programmed with valid state and the configuration, Force Wakeup bit should be reset to enable C6 entry.	RenderCS

Ring Buffer Head

RING_BUFFER_HEAD - Ring Buffer Head

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02034h-02037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_RCSUNIT
Address:	12034h-12037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_VCSUNIT0
Address:	1A034h-1A037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_VECSUNIT
Address:	1C034h-1C037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_VCSUNIT1
Address:	22034h-22037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_BCSUNIT

Description

This register is used to define and operate the ring buffer mechanism which can be used to pass instructions to the command interface. The buffer itself is located in a physical memory region. The ring buffer is defined by a 4 Dword register set that includes starting address, length, head offset, tail offset, and control information. Refer to the Programming Interface chapter for a detailed description of the parameters specified in this ring buffer register set, restrictions on the placement of ring buffer memory, arbitration rules, and in how the ring buffer can be used to pass instructions.
Ring Buffer Head Offsets must be properly programmed before ring is enabled. A Ring Buffer can be enabled when empty.

DWord	Bit	Description
0	31:21	**Wrap Count** Format: U11 count of ring buffer wraps This field is incremented by 1 whenever the **Head Offset** wraps from the end of the buffer back to the start (i.e., whenever it wraps back to 0). Appending this field to the **Head Offset** field effectively creates a virtual 4GB Head "Pointer" which can be used as a tag associated with

RING_BUFFER_HEAD - Ring Buffer Head

instructions placed in a ring buffer. The Wrap Count itself will wrap to 0 upon overflow.

20:2 Head Offset

Format:	GraphicsAddress[20:2] DWord Offset

This field indicates the offset of the *next* instruction DWord to be parsed. Software will initialize this field to select the first DWord to be parsed once the RB is enabled. (Writing the Head Offset while the RB is enabled is UNDEFINED). Subsequently, the device will increment this offset as it executes instructions - until it reaches the QWord specified by the **Tail Offset**. At this point the ring buffer is considered "empty".

Programming Notes
A RB can be enabled empty or containing some number of valid instructions.

1 Reserved

Format:	MBZ

0 Reserved

Format:	MBZ

Ring Buffer Start

RING_BUFFER_START - Ring Buffer Start	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02038h-0203Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_RCSUNIT
Address:	12038h-1203Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_VCSUNIT0
Address:	1A038h-1A03Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_VECSUNIT
Address:	1C038h-1C03Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_VCSUNIT1
Address:	22038h-2203Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_BCSUNIT

Description

These registers are used to define and operate the "ring buffer" mechanism which can be used to pass instructions to the command interface. The buffer itself is located in a physical memory region. The ring buffer is defined by a 4 Dword register set that includes starting address, length, head offset, tail offset, and control information. Refer to the Programming Interface chapter for a detailed description of the parameters specified in this ring buffer register set, restrictions on the placement of ring buffer memory, arbitration rules, and in how the ring buffer can be used to pass instructions.

DWord	Bit	Description
0	31:12	**Starting Address** Format: GraphicsAddress[31:12]RingBuffer This field specifies Bits 31:12 of the 4KB-aligned starting Graphics Address of the ring buffer. Address bits 31 down to 29 must be zero. All ring buffer pages must map to Main Memory (uncached) pages. Ring Buffer addresses are always translated through the global GTT.

RING_BUFFER_START - Ring Buffer Start			
	11:0	**Reserved**	
		Format:	MBZ

Ring Buffer Tail

RING_BUFFER_TAIL - Ring Buffer Tail

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02030h-02033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_RCSUNIT
Address:	12030h-12033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_VCSUNIT0
Address:	1A030h-1A033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_VECSUNIT
Address:	1C030h-1C033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_VCSUNIT1
Address:	22030h-22033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_BCSUNIT

Description

These registers are used to define and operate the "ring buffer" mechanism which can be used to pass instructions to the command interface. The buffer itself is located in a linear memory region. The ring buffer is defined by a 4 Dword register set that includes starting address, length, head offset, tail offset, and control information. Refer to the Programming Interface chapter for a detailed description of the parameters specified in this ring buffer register set, restrictions on the placement of ring buffer memory, arbitration rules, and in how the ring buffer can be used to pass instructions. Ring Buffer Tail Offsets must be properly programmed before ring is enabled. A Ring Buffer can be enabled when empty.

DWord	Bit	Description
0	31	**Reserved** Source: RenderCS
	30:21	**Reserved** Format: MBZ

RING_BUFFER_TAIL - Ring Buffer Tail

	20:3	**Tail Offset** Format: GraphicsAddress[20:3] This field is written by software to specify where the valid instructions placed in the ring buffer end. The value written points to the QWord past the last valid QWord of instructions. In other words, it can be defined as the next QWord that software will write instructions into. Software must write subsequent instructions to QWords following the Tail Offset, possibly wrapping around to the top of the buffer (i.e., software can't skip around within the buffer). Note that all DWords prior to the location indicated by the **Tail Offset** must contain valid instruction data - which may require instruction padding by software. See **Head Offset** for more information.
	2:0	**Reserved** Format: MBZ

Root Table Address Pointer Value First 31_0

RTAPV_1_310 - Root Table Address Pointer Value First 31_0		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F500h	
This register is used to store local copy of the Root Table address pointer value.		
DWord	**Bit**	**Description**
0	31:0	**First Address 31 to 0** Default Value: 00000000h Access: R/W Bits 31:11 = Root Table Address Pointer Value 31:11. Bits 10:1 = Reserved. Bit 0 = Enabled for Root Table Address Pointer Value 31:11.

Root Table Address Pointer Value Second 31_0

RTAPV_2_310 - Root Table Address Pointer Value Second 31_0		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F504h	
This register is used to store local copy of the Root Table address pointer value.		
DWord	**Bit**	**Description**
0	31:0	**Second Address 31 to 0** Default Value: 00000000h Access: R/W Bits 31:8 = Reserved. Bits 7:1 = Root Table Address Pointer Value 38:32. Bit 0 = Enabled for Root Table Address Pointer Value 38:32.

RPM Context Image Interface

MSG_RPM_CTXBASE - RPM Context Image Interface

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	08518h

This register is written by RPMunit, the content is provided to msqcunit in rc6 context address decode

DWord	Bit	Description
0	31:30	**Reserved** Access: RO
	29:22	**RC6 Context Base High** Access: R/W This field corresponds to bits [39:32] of RC6MEMBASE Use above 4GB is not currently supported, and these bits must be set to 0
	21:2	**RC6 Context Base Low** Access: R/W This field is used to set the base of memory where the RC6 power context will be saved This value MUST be above the base and below the top of stolen memory
	1	**RC6 DRAM Only** Access: R/W 1'b0 : Allow C6 context to go to either DRAM or C6SRAM, as specified by RC6LOCATION(default) 1'b1 : C6 context always goes to DRAM; RC6LOCATION is ignored
	0	**RC6 Location** Access: R/W 1'b0 : Send context data to C6SRAM (default) 1'b1 : Send context data to DRAM location specified in RC6CTXBASE

RS_PREEMPT_STATUS_UDW

RS_PREEMPT_STATUS_UDW - RS_PREEMPT_STATUS_UDW

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02174h

Preemption from First Level Batch Buffer:
This register contains the offset in to the Batch Buffer on which Resource streamer got preempted. Note that it is offset from the Batch Start Address and not the graphics address corresponding to the preempted instruction on Batch Buffer. This register's contents will be looked at by Command Streamer on the next RS Start Trigger to provide the appropriate batch start address. Following preemption, context save happens on which this register is context saved, after context save the register gets auto reset by Command Streamer. This register gets context save/restored by Render Command Streamer as part of its render context.

Preemption from Second Level Batch Buffer:
This register contains the graphics address of the instruction in Second Level Batch Buffer on which Resource streamer got preempted. This register's contents will be looked at by Command Streamer on the next RS Start Trigger to provide the appropriate batch start address. Following preemption, context save happens on which this register is context saved, after context save the register gets auto reset by Command Streamer. This register gets context save/restored by Render Command Streamer as part of its render context.

Programming Notes

- This register is accessed by Render Command Streamer as part of render context save/restore; this register should be exercised by S/W only for resetting the register contents if required.
- Following preemption if there is no context save, SW should program this register with 0x0 so that it does not interfere with proceeding workloads.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:0	**Batch Buffer Offset Upper DWord** Format: GraphicsAddress[47:32] This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the last preempted second level batch buffer in resource streamer. GraphicsAddress is 64-bit value [63:0], but only a portion of it is used by the hardware. Upper bits [63:48] are ignored and MBZ.

RS_PREEMPT_STATUS_UDW

RS_PREEMPT_STATUS_UDW - RS_PREEMPT_STATUS_UDW

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02174h

Preemption from First Level Batch Buffer:
This register contains the offset in to the Batch Buffer on which Resource streamer got preempted. Note that it is offset from the Batch Start Address and not the graphics address corresponding to the preempted instruction on Batch Buffer. This register's contents will be looked at by Command Streamer on the next RS Start Trigger to provide the appropriate batch start address. Following preemption, context save happens on which this register is context saved, after context save the register gets auto reset by Command Streamer. This register gets context save/restored by Render Command Streamer as part of its render context.

Preemption from Second Level Batch Buffer:
This register contains the graphics address of the instruction in Second Level Batch Buffer on which Resource streamer got preempted. This register's contents will be looked at by Command Streamer on the next RS Start Trigger to provide the appropriate batch start address. Following preemption, context save happens on which this register is context saved, after context save the register gets auto reset by Command Streamer. This register gets context save/restored by Render Command Streamer as part of its render context.

Programming Notes

- This register is accessed by Render Command Streamer as part of render context save/restore; this register should be exercised by S/W only for resetting the register contents if required.
- Following preemption if there is no context save, SW should program this register with 0x0 so that it does not interfere with proceeding workloads.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:0	**Batch Buffer Offset Upper DWord** Format: GraphicsAddress[47:32] This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the last preempted second level batch buffer in resource streamer. GraphicsAddress is 64-bit value [63:0], but only a portion of it is used by the hardware. Upper bits [63:48] are ignored and MBZ. Some GraphicsAddress fields only specify the upper address bits. For example GraphicsAddress[47:12] would be a 4KB page address

RS Preemption Hint

RS_PRE_HINT - RS Preemption Hint

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	024C0h

This register contains the Dword aligned Graphics address in to the Batch Buffer corresponding to either 3D_PRIMITIVE or RCS-RS sync command called Preemption Hint Address. When Preemption Hint Address is enabled, RS will honor preemption request from RCS only on parsing 3D_PRIMITIVE/RCS-RS sync command at Preemption Hint Address.

Programming Notes

Programming Restriction:
This register should NEVER be programmed in functional mode, this should be used only in validation mode to achieve deterministic behavior of preempting Resource Streamer in command stream. Programmer has to ensure that RS Preemption Hint register gets programmed well before RS gets preempted by RCS. Note that this register should be programmed with caution as it can lead to indefinite stalls in RS.

a. RS will preempt on receiving preemption request from RCS only on reaching the instruction in the batch buffer corresponding to the address mentioned in RS_PREEMPT_HINT. RS could hit an RCS-RS sync command before reaching the address mentioned in the RS_PREEMPT_HINT, in this case RS should preempt on the sync command.

b. RS could hit the address mentioned in 3D_PREEMPT_HINT before receiving preempt request from RCS. In this case RS will stall at this command until it receives preemption request from RCS and then preempts.

If RS is programmed to the same DRAW command as the Command Streamer, then a dummy DRAW command is required prior to the DRAW command with the HINT. Otherwise the RS will not initiate the sync with the DRAW command and will deadlock the hardware.

DWord	Bit	Description
0	31:2	**Preemption Hint Address** Format: U30 This field contains the Dword aligned Graphics Address in to the batch buffer as Preemption Hint.
	1	**Reserved** Format: Enabled

RS_PRE_HINT - RS Preemption Hint

	0	**Preemption Hint** Format: Enabled **Value** / **Name** / **Description** 0h / Disabled / Preemption hint is disabled for Resource Streamer. 1h / Enabled / Preemption hint is enabled for Resource streamer.

RS Preemption Hint UDW

RS_PREEMPTION_HINT_UDW - RS Preemption Hint UDW

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	024C4h

This register contains the upper DWord of the 4GB aligned base addres of the Batch Buffer for the Preemption Hint Addressfor either the 3D_PRIMITIVE or RCS-RS sync command. When Preemption Hint Address is enabled, RS will honor preemption requests from RCS only on parsing 3D_PRIMITIVE/RCS-RS sync command at the Preemption Hint Address.
GraphicsAddress is a 64-bit value [63:0], but only a portion of it is used by hardware. The uppermost reserved bits are ignored and MBZ.

Restriction

Restriction : This register should NEVER be programmed in functional mode, this should be used only in validation mode to achieve deterministic behavior of preempting Resource Streamer in command stream. See RS_PRE_HINT definition for further restrictions.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:0	**Preemption Hint Address Upper DWORD** Format: GraphicsAddress[47:32]

Sampler Busy per Subslice

EUMETRICS_EVENT5 - Sampler Busy per Subslice	
Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	00DA0h

This register mirrors an accumulating count for EU Metric Event5.
It is enabled by configuration bits in GPMunit and SPMunits.
Note that count is never cleared and delta should be calculated by sampling the initial register value at the start and subtracting that value off from the final sample value.

DWord	Bit	Description
0	31:0	**EU Metric Event Count** Access: RO

Sampler control register

SAMPLER_CTL - Sampler control register	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0E140h

DWord	Bit	Description
0	31:16	**ECO Reserved 1** Reserved: MBZ
	15:8	**Reserved**
	7:3	**Sampler unit select** 00000 ? SIUnit 00001 ? PLUnit 00010 ? DGUnit 00011 ? QCUnit 00100 ? FTUnit 00101 ? DMUnit 00110 ? SCUnit 00111 ? FLUnit 01000 ? SOUnit 01001 - AVSunit
	2	**ECO Reserved 2** Reserved MBZ (These bits are moved to CS unit MMIO register section at 0x208c, bit 2)
	1:0	**ECO Reserved 3** Reserved MBZ

SAMPLER EU STALL

EUMETRICS_EVENT3 - SAMPLER EU STALL	
Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	00D98h

This register mirrors an accumulating count for EU Metric Event3.
It is enabled by configuration bits in GPMunit and SPMunits.
Note that count is never cleared and delta should be calculated by sampling the initial register value at the start and subtracting that value off from the final sample value.

DWord	Bit	Description
0	31:0	**EU Metric Event Count** Access: RO

SAMPLER Mode Register

SAMPLER_MODE - SAMPLER Mode Register

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Size (in bits):	32
Trusted Type:	1
Address:	07028h

This register has bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].
To set bit0, for example, the data would be 0x0001_0001.
To clear bit0, for example, the data would be 0x0001_0000.
Note that mask bit is the data bit offset + 16.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO
	15	**ECO Reserved 1** Format: MBZ
	14	**ECO Reserved 1B** Format: MBZ
	13:12	**ECO Reserved 2** Format: MBZ
	11:10	**ECO Reserved 2b** Format: MBZ
	9:8	**ECO Reserved 2c** Format: MBZ
	7	**ECO Reserved 3** Format: MBZ
	6	**ECO_SCRATCH3C**
	5	**ECO_SCRATCH3B** Format: MBZ
	4	**ECO Reserved 4** Format: MBZ
	3	**ECO Reserved 5** Format: MBZ

SAMPLER_MODE - SAMPLER Mode Register		
	2	**ECO Reserved 4-2**
	1	**ECO Reserved4-1**

Save Timer

SVTIMER - Save Timer

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x60001000
Size (in bits):	32
Address:	0B434h

DWord	Bit	Description
0	31	**Reserved** Access: RO Reserved.
	30:29	**Counter Enabling Selection** Default Value: 11b Access: R/W LPFC provides rudimentary compression by allowing software to select from several predefined levels of event reporting. Based on the value of this bitfield, only a certain number of the programmed events in the "Event Selection and Base Counters" registers (CNT0CL, CNT1CL, ..., CNT7CL) will be tracked and reported: Value / Selected Counters: 00 – Counter 0; 01 – Counters 0 & 1; 10 – Counters 0, 1, 2, & 3; 11 – Counters 0 - 7 Signal - lpconf_lpfc_cnt_enabled [1:0].
	28:24	**Reserved** Access: RO Reserved.
	23:0	**Save Timer Intervel** Default Value: 000000000001000000000000b Access: R/W Save Timer Interval (SVTMRINT). Save Timer Interval: This is the interval for sampling the performance counters and writing to memory. Each time it expires, the counters are sampled and packetized to be sent to DMA controller. The minimum granularity of sampling period if 256clocks. The value in this register is used as 256

SVTIMER - Save Timer		
		x value to find the sampling window. For a 1Ghz core clock it provides up to 4ns of sampling period while matching the maximum capability of the event counters. 1h - 256clks. 2h - 512clks. ... 8h - 2048clks. Signal - lpconf_lpfc_savetimer_int [23:0].

SBLC_PWM_CTL1

SBLC_PWM_CTL1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	C8250h-C8253h
Name:	South BLM Control 1
ShortName:	SBLC_PWM_CTL1
Power:	Always on
Reset:	soft

DWord	Bit	Description
0	31	**PWM PCH Enable** This bit enables the PWM counter logic in the PCH. Disabled PWM will drive 0, which can be inverted to 1 with the polarity bit. Value / Name: 0b Disable; 1b Enable Restriction: Restriction : Program the frequency and duty cycle before enabling PWM.
	30	**Reserved** Format: MBZ
	29	**Backlight Polarity** This field controls the polarity of the PWM signal. Value / Name: 0b Active High; 1b Active Low
	28:0	**Reserved** Format: MBZ

SBLC_PWM_CTL2

SBLC_PWM_CTL2		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	C8254h-C8257h	
Name:	South BLM Control 2	
ShortName:	SBLC_PWM_CTL2	
Power:	Always on	
Reset:	soft	
DWord	**Bit**	**Description**
0	31:16	**Backlight Modulation Frequency** This field determines the number of time base events in total for a complete cycle of modulated backlight control. This field is normally set once during initialization based on the frequency of the clock that is being used and the desired PWM frequency. This value represents the period of the PWM stream in clock periods multiplied by 16 (default increment) or 128 (alternate increment selected in SCHICKEN_1 bit 0). PWM clock is 24 MHz, non-spread, <100ppm
	15:0	**Backlight Duty Cycle** This field determines the number of time base events for the active portion of the PWM backlight control. This should never be larger than the frequency field. A value of zero will turn the backlight off. A value equal to the backlight modulation frequency field will be full on. When written, the new value will take affect at the end of the current PWM cycle. This value represents the active time of the PWM stream in clock periods multiplied by 16 (default increment) or 128 (alternate increment selected in SCHICKEN_1 bit 0).

SCRATCH1

SCRATCH1 - SCRATCH1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000001 [KBL]	
Size (in bits):	32	
Address:	0B11Ch	
DWord	**Bit**	**Description**
0	31:13	**SCRATCH** Access: R/W
	12	**SLM Save ECC hang Fix Disable** Access: R/W 0 - Hang indication sent to ltiseqslunit when uncorrectable error detected in any of the SLM lanes 1 - Hang indication sent to ltiseqslunit when uncorrectable error detected only in SLM lane0 lbcf_slmsave_ecc_hang_fix_disable
	11	**Snoop SLM Save Restore Fix Disable** Access: R/W 0 (default): Snoop fix during SLM Save Restore is enabled 1 : Snoop fix in LTCD during SLM Save Restore is disabled lbcf_ltcd_snpfix_dis
	10	**LTCD LAST TX IROW FIX** Access: R/W 0 (default): last transaction hitting irow before self-init/ebb-init bug fix enabled 1 : last transaction hitting irow before self-init/ebb-init bug fix disabled lbcf_lasttx_hitirow_fix_dis
	9	**LSQC RORW Performance Fix Disable** Access: R/W 0 (default) : Order cam match should not be qualified with destination for read serialization fix. 1 : Order cam match will be qualified with destination for read serialization fix. lbcf_csr_lsqc_rorwperf_dis
	8	**Eviction Performance Fix Enable** Access: R/W Disable Eviction Performance fix 0 (default) - Enable Eviction Performance Fix in LSQC

SCRATCH1 - SCRATCH1

		1 - Disable Eviction Performance Fix in LSQC Value of this bit should be same as LBCF register bit 0xb118[22]. Value of this bit should be same as LNCF register bit 0xb008[0]. lbcf_csr_evict_perf_fix_en
	7	**Reserved** Access: R/W Reserved
	6	**Coherent SQCAM Disable** Access: R/W 0 (default) - Enable sqcam look up for coh cycles 1 - Disable sqcam look up for coh cycles lbcf_csr_coh_sqcam_en
	5	**SLM/Non-SLM Fair Arbitration Fix Disable** Access: R/W 0 (default) - SLM/non-SLM Fair arbitration fix is enabled 1 - SLM/non-SLM Fair arbitration fix is disabled This bit is not applicable for DevBXT:A0 lbcf_csr_fairarb_perf_fix_dis
	4	**LSQC Non Coherent Flush on PM Flush Disable** Access: R/W 0 :(default) When PM flush is sent to L3, LSQC will generate Query to flush coherent and Non coherent Lines (DC/L3 ways) from L3. 1: When PM flush is sent to L3, LSQC will generate Query to flush only the Coherent Lines (DC/L3 ways) from L3. lbcf_csr_lsqc_flush_nc_on_pm_flush_dis
	3	**roinv stall deassert** Default Value: 0 Access: R/W 0-When any of the text,const,state,text flag ro invalidation is in progress the stall is not deasserted 1-When any of the text,const,state,text flag ro invalidation is in progress the stall is deasserted lbcf_ltcd_roinv_stall_deassert
	2	**LBS SLA Retry Timer Decrement** Default Value: 0b Access: R/W

SCRATCH1 - SCRATCH1		
		1: LBS SLA Retry Timer Decrement is enabled 0: LBS SLA Retry Timer Decrement is disabled This bit needs to be programmed to 1 to avoid SNOOP response livelock lbcf_lbs_sla_retry_timer_dec_en
	1	**LSQC COH SNOOP COAMA STREAM FIX EN** Default Value: 0b Access: R/W 1: Coherent Snoop Coama Stream related fix is enabled. 0: Fix is disabled lbcf_lsqc_coh_snp_coama_stream_fix_en
	0	**Reserved**

SCRATCH1L3

SCRATCH1L3 - SCRATCH1L3

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000001
Size (in bits):	32
Address:	0B11Ch

DWord	Bit	Description
0	31:13	**SCRATCH** Access: R/W
	12	**SLM Save ECC hang Fix Disable** Access: R/W 0 - Hang indication sent to ltiseqslunit when uncorrectable error detected in any of the SLM lanes 1 - Hang indication sent to ltiseqslunit when uncorrectable error detected only in SLM lane0 lbcf_slmsave_ecc_hang_fix_disable
	11	**Snoop SLM Save Restore Fix Disable** Access: R/W 0 (default): Snoop fix during SLM Save Restore is enabled 1 : Snoop fix in LTCD during SLM Save Restore is disabled lbcf_ltcd_snpfix_dis
	31:10	**SCRATCH** Access: R/W
	10	**LTCD LAST TX IROW FIX** Access: R/W 0 (default): last transaction hitting irow before self-init/ebb-init bug fix enabled 1 : last transaction hitting irow before self-init/ebb-init bug fix disabled lbcf_lasttx_hitirow_fix_dis
	9	**LSQC RORW Performance Fix Disable** Access: R/W 0 (default) : Order cam match should not be qualified with destination for read serialization fix. 1 : Order cam match will be qualified with destination for read serialization fix. lbcf_csr_lsqc_rorwperf_dis

SCRATCH1L3 - SCRATCH1L3

	8	**Eviction Performance Fix Enable** Access: R/W Disable Eviction Performance fix 0 (default) - Enable Eviction Performance Fix in LSQC 1 - Disable Eviction Performance Fix in LSQC Value of this bit should be same as LBCF register bit 0xb118[22]. Value of this bit should be same as LNCF register bit 0xb008[0]. lbcf_csr_evict_perf_fix_en
	31:7	**SCRATCH** Access: R/W
	7	**Reserved** Access: R/W Reserved
	6	**Coherent SQCAM Disable** Access: R/W 0 (default) - Enable sqcam look up for coh cycles 1 - Disable sqcam look up for coh cycles lbcf_csr_coh_sqcam_en
	5	**SLM/Non-SLM Fair Arbitration Fix Disable** Access: R/W 0 (default) - SLM/non-SLM Fair arbitration fix is enabled 1 - SLM/non-SLM Fair arbitration fix is disabled This bit is not applicable for DevBXT:A0 lbcf_csr_fairarb_perf_fix_dis
	31:4	**SCRATCH** Access: R/W
	4	**LSQC Non Coherent Flush on PM Flush Disable** Access: R/W 0 :(default) When PM flush is sent to L3, LSQC will generate Query to flush coherent and Non coherent Lines (DC/L3 ways) from L3. 1: When PM flush is sent to L3, LSQC will generate Query to flush only the Coherent Lines (DC/L3 ways) from L3. lbcf_csr_lsqc_flush_nc_on_pm_flush_dis

SCRATCH1L3 - SCRATCH1L3

	3	**ROINV Stall Deassert** Default Value: 0 Access: R/W 0-When any of the text, const, state, text flag ro invalidation is in progress the stall is not deasserted 1-When any of the text, const, state, text flag ro invalidation is in progress the stall is deasserted lbcf_ltcd_roinv_stall_deassert
	2	**LBS SLA Retry Timer Decrement** Default Value: 0b Access: R/W 1: LBS SLA Retry Timer Decrement is enabled 0: LBS SLA Retry Timer Decrement is disabled This bit needs to be programmed to 1 to avoid SNOOP response livelock lbcf_lbs_sla_retry_timer_dec_en
	1	**LSQC COH SNOOP COAMA STREAM FIX EN** Default Value: 0b Access: R/W 1: Coherent Snoop Coama Stream related fix is enabled. 0: Fix is disabled lbcf_lsqc_coh_snp_coama_stream_fix_en
	0	**Reserved**

SCRATCH 2 for LNCFunit

SCRATCH_LNCF2 - SCRATCH 2 for LNCFunit		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000 [KBL]	
Size (in bits):	32	
Address:	0B0A0h	
DWord	**Bit**	**Description**
0	31	**Reserved** Access: R/W
	30	**Reserved2** Access: R/W
	29	**Reserved3** Access: R/W
	28	**Reserved4** Access: R/W
	27	**Reserved5** Access: R/W
	26	**Reserved6** Access: R/W
	25	**Reserved7** Access: R/W
	24	**Reserved8** Access: R/W
	23	**Reserved9** Access: R/W
	22:0	**SCRATCH 2 field for LNCFunit** Access: R/W

SCRATCH 2 for LNCFunit

SCRATCH_LNCF2 - SCRATCH 2 for LNCFunit		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B0A0h	
DWord	**Bit**	**Description**
0	31	**Reserved** Access: R/W
	30	**Reserved** Access: R/W
	29	**Reserved** Access: R/W
	28	**Reserved** Access: R/W
	27	**Reserved** Access: R/W
	26	**Reserved** Access: R/W
	25	**Reserved** Access: R/W
	24	**Reserved** Access: R/W
	23	**Reserved** Access: R/W
	22:0	**SCRATCH 2 field for LNCFunit** Access: R/W

SCRATCH2 Register

SCRATCH2 - SCRATCH2 Register		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B140h	
DWord	**Bit**	**Description**
0	31:0	**SCRATCH2** Access: R/W

SCRATCH for LNCFunit

SCRATCH_LNCF1 - SCRATCH for LNCFunit

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000001 [KBL]
Size (in bits):	32
Address:	0B008h

DWord	Bit	Description
0	31:8	**SCRATCH register for LNCFunit** Access: R/W
	7	**Enable LNI SNDARB Fairness Fix** Access: R/W 0: (Default) Disable LNIUNIT SNDARB Fairness Fix. 1: Enable LNIUNIT SNDARB Fairness Fix. The following bit needs to be programmed to 1 in GT3 and GT4 modes. lncf_csr_sndarb_fairness_fix_en
	6	**Disable LNI Page Fault Fix** Access: R/W 0: (Default) Enable LNIUNIT Page Fault Fix. 1: Disable LNIUNIT Page Fault Fix lncf_csr_lni_pgflt_fix_dis
	5	**Reserved** Access: R/W Reserved
	4	**Reserved** Access: R/W Reserved
	3	**LNE Arbitration Performance Fix** Access: R/W 0: (Default) Enable the performance fix for the case where LNE was inserting bubbles in SS read returns 1: Disable the performance fix. lncf_csr_lne_perf_fix_dis

SCRATCH_LNCF1 - SCRATCH for LNCFunit

	2	**Memory fill delay** Access: R/W lncf_csr_lni_gt2_memfill_dis. 0:mem fills gt2 latency will be 1 . 1:mem fill gt2 latency will be same as gt3.
	1	**flush start delay** Access: R/W lncf_csr_lni_disable_flush_start_delay. 0:Flush processing in LNIunit starts one clock after receiving the flush command default. 1:Flush processing in LNIunit starts in the same clock in which flush command is received.
	0	**Non-IA coherent atomics enable** Default Value: 1b Access: R/W 0: atomics in GTI (). 1: atomics in L3 (non-IA atomic) (Default). Output signal from LNCF unit lncf_csr_lni_glblatmcs_l3. Value for this bit should be same as lbcf_csr_lsqc_glblatmcs_l3 b118[22]. Value of this bit should be same as LBCF register bit 0xb11c[8]. Adding Xbuf 8 MCP.

Second Buffer Size

SBS - Second Buffer Size		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B424h	
DWord	**Bit**	**Description**
0	31:16	**Second Virtual Buffer Base** Access: R/W Second Virtual Buffer Base (SVBB0). Second Virtual Buffer Base: Programmed by driver to allocate a memory space for performance data storage. The buffer size should be aligned to the size of the memory allocated so it naturally aligns to the base (i.e. for 128KB bit[16]=0, 256KB bit[17:16]=0, 512KB bit[18:16]=0). Signal - lpconf_lpfc_virtual_base1 [31:16].
	15:12	**Second Buffer Size 0** Access: R/W Second Buffer Size: Determines the allowed buffer size for performance data storage. 0000b: 64KB. 0001b: 128KB. 0010b: 256KB. 0011b: 512KB. ... 1111b: 2GB. Signal - lpconf_lpfc_buffer_size1 [3:0].
	11:0	**Reserved** Access: RO Reserved.

Second Level Batch Buffer Head Pointer Preemption Register

SBB_PREEMPT_ADDR - Second Level Batch Buffer Head Pointer Preemption Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1

Address:	0213Ch-0213Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_RCSUNIT

Address:	1213Ch-1213Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VCSUNIT0

Address:	1A13Ch-1A13Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VECSUNIT

Address:	1C13Ch-1C13Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VCSUNIT1

Address:	2213Ch-2213Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_BCSUNIT

Description
This register gets updated with the DWord-aligned graphics memory address of the PREEMPTABLE command in the second level batch buffer on which preemption has occurred. This register value should be looked at only when the preemption has occurred in the second level batch buffer. This is indicated by "Ring/Batch Indicator" in "RING_BUFFER_HEAD_PREEMPT_REG". This register value retains its previous value and doesn't change when the preemption occurs on a preemptable command in ring buffer or in batch buffer. Preemption is triggered by valid UHPTR in ring buffer mode of scheduling and by a pending execlist in Exec-List mode of scheduling. This is a global register and context save/restored as part of power context image.

Preemptable Commands	Source

SBB_PREEMPT_ADDR - Second Level Batch Buffer Head Pointer Preemption Register

MI_ARB_CHECK 3D_PRIMITIVE GPGPU_WALKER MEDIA_STATE_FLUSH PIPE_CONTROL (Only in GPGPU mode of pipeline selection) MI_ATOMIC (Post Sync Operation set in GPGPU mode of pipeline selection) MI_SEMAPHORE_SIGNAL (Post Sync Operation set in GPGPU mode of pipeline selection)	RenderCS

Preemptable Commands	Source
MI_ARB_CHECK	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS

Programming Notes

Programming Restriction:
This register should NEVER be programmed by driver, this is for HW internal use only.

DWord	Bit	Description
0	31:2	**Second Level Batch Buffer Head Pointer** Format: GraphicsAddress[31:2] This field specifies the DWord-aligned Graphics Memory Address of the PREEMPTABLE command in a batch buffer where the Preemption has occurred.
	1:0	**Reserved** Format: MBZ

Second Level Batch Buffer Head Pointer Register

SBB_ADDR - Second Level Batch Buffer Head Pointer Register

Register Space:	MMIO: 0/2/0
Source:	CommandStreamer
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	02114h-02117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_RCSUNIT
Address:	12114h-12117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VCSUNIT0
Address:	1A114h-1A117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VECSUNIT
Address:	1C114h-1C117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VCSUNIT1
Address:	22114h-22117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_BCSUNIT

This register contains the current DWord Graphics Memory Address of the last-initiated batch buffer.

Programming Notes

This register should NEVER be programmed by driver, this is for HW internal use only. This register should not be written by software. These fields should only get written by a context restore. Software should always set these fields via the MI_BATCH_BUFFER_START command when initiating a batch buffer.
This register is saved and restored with context.

DWord	Bit	Description
0	31:2	**Second Level Batch Buffer Head Pointer** Format: GraphicsAddress[31:2] This field specifies the DWord-aligned Graphics Memory Address where the last initiated Second Level Batch Buffer is currently fetching commands. This field is meaningful only when Valid field is set to "1".

SBB_ADDR - Second Level Batch Buffer Head Pointer Register

	1	**Reserved** Format: MBZ
	0	**Valid** Format: U1

Value	Name	Description
0h	Invalid **[Default]**	Second Level Batch buffer Invalid
1h	Valid	Second Batch buffer Valid.

Second Level Batch Buffer State Register

SBB_STATE - Second Level Batch Buffer State Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32

Address:	02118h-0211Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_RCSUNIT

Address:	12118h-1211Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VCSUNIT0

Address:	1A118h-1A11Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VECSUNIT

Address:	1C118h-1C11Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VCSUNIT1

Address:	22118h-2211Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_BCSUNIT

This register contains the attributes of the second level batch buffer initiated from the batch Buffer.

This register should not be written by software. These fields should only get written by a context restore. Software should always set these fields via the MI_BATCH_BUFFER_START command when initiating a batch buffer.
This register is saved and restored with context.

DWord	Bit	Description
0	31:10	**Reserved** Format: MBZ
	9:8	**Reserved**
	7	**Resource Streamer Enable** Source: RenderCS Format: U1 When this bit is set, the Resource Streamer will execute the batch buffer. When this bit is clear the Resource Streamer will not execute the batch buffer.

SBB_STATE - Second Level Batch Buffer State Register

	7	**Reserved** Source: BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS Format: MBZ
	6	**Reserved** Format: MBZ
	5	**Address Space Indicator** Note: This field reflects the effective address space indicator security level and may not be the same as the Address Space Indicator written using MI_BATCH_BUFFER_START. Value / Name / Description 0h / GGTT **[Default]** / This second level batch buffer is located in GGTT memory and is privileged 1h / PPGTT / This second level batch buffer is located in PPGTT memory and is non-privileged.
	4	**Reserved** Source: RenderCS, BlitterCS Format: MBZ
	4	**Reserved**
	3:0	**Reserved** Format: MBZ

Second Level Batch Buffer Upper Head Pointer Preemption Register

SBB_PREEMPT_ADDR_UDW - Second Level Batch Buffer Upper Head Pointer Preemption Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02138h-0213Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_RCSUNIT
Address:	12138h-1213Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VCSUNIT0
Address:	1A138h-1A13Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VECSUNIT
Address:	1C138h-1C13Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VCSUNIT1
Address:	22138h-2213Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_BCSUNIT

Upper 32 bits of the 4GB aligned base address within the host's 64-bit virtual address space of the last preempted second level batch buffer. This register follows the same rules as the SBB_PREEMPT_ADDR register.

Programming Notes

Programming Restriction:
This register should NEVER be programmed by driver, this is for HW internal use only.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:0	**Second Level Batch Buffer Head Pointer Upper DWORD** Format: GraphicsAddress[47:32]

Second Level Batch Buffer Upper Head Pointer Register

SBB_ADDR_UDW - Second Level Batch Buffer Upper Head Pointer Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	RO
Size (in bits):	32

Address:	0211Ch-0211Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_RCSUNIT

Address:	1211Ch-1211Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_VCSUNIT0

Address:	1A11Ch-1A11Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_VECSUNIT

Address:	1C11Ch-1C11Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_VCSUNIT1

Address:	2211Ch-2211Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_BCSUNIT

Upper 32 bits of the 4GB aligned base address within the host's 64-bit virtual address space, where the last initiated Batch Buffer is currently fetching commands. If no batch buffer is currently active, the Valid bit in BB_ADDR will be 0 and this field is meaningless.

Programming Notes

This register should NEVER be programmed by driver. This is for HW internal use only.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:0	**Batch Buffer Head Pointer Upper DWORD** Format: GraphicsAddress[47:32]

Semaphore Polling Interval on Wait

SEMA_WAIT_POLL - Semaphore Polling Interval on Wait	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0224Ch-0224Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_RCSUNIT
Address:	1224Ch-1224Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VCSUNIT0
Address:	1A24Ch-1A24Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VECSUNIT
Address:	1C24Ch-1C24Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VCSUNIT1
Address:	2224Ch-2224Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_BCSUNIT

The SEMA_WAIT_POLL register contains Poll Interval field which specifies the minimum number of microseconds allowed for command streamer to wait before re-fetching the data from the address mentioned in the MI_SEMAPHORE_WAIT command on WAIT Mode set to POLL until the condition is satisfied while the context is not switched out.
When a value of 0 is written the poll interval will be equal to the memory latency of the read completion.

DWord	Bit	Description
0	31:21	**Reserved** Format: MBZ
	20:0	**Poll Interval** Minimum number of micro-seconds allowed

SF ACTIVE STALL Event

SF_ACTIVE_STALL - SF ACTIVE STALL Event			
Register Space:	MMIO: 0/2/0		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	00DB8h		
This register mirrors an accumulating count for EU Metric Event7. It is enabled by configuration bits in GPMunit and SPMunits. Note that count is never cleared and delta should be calculated by sampling the initial register value at the start and subtracting that value off from the final sample value.			
DWord	**Bit**	**Description**	
0	31:0	**SF Active Stall Count**	
		Access:	RO

SFUSE_STRAP

SFUSE_STRAP	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	C2014h-C2017h
Name:	South Fuses and Straps
ShortName:	SFUSE_STRAP
Power:	Always on
Reset:	soft

DWord	Bit	Description
0	31:9	**Reserved**
	8	**Reserved**
	7:5	**Reserved**
	4	**Reserved**
	3	**Reserved**
	2	**Digital Port B Present Strap** This bit indicates the state of the digital port B present strap. The strap is set if DDPB_CTRLDATA pin is 1b at rising edge of PCH_PWROK. Value: 0b — Name: Not Present Value: 1b — Name: Present
	1	**Digital Port C Present Strap** This bit indicates the state of the digital port C present strap. The strap is set if DDPC_CTRLDATA pin is 1b at rising edge of PCH_PWROK. Value: 0b — Name: Not Present Value: 1b — Name: Present
	0	**Digital Port D Present Strap** This bit indicates the state of the digital port D present strap. The strap is set if DDPD_CTRLDATA pin is 1b at rising edge of PCH_PWROK. Value: 0b — Name: Not Present Value: 1b — Name: Present

SHOTPLUG_CTL

SHOTPLUG_CTL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	C4030h-C4033h
Name:	South Hot Plug Control
ShortName:	SHOTPLUG_CTL
Power:	Always on
Reset:	soft

The short pulse duration is programmed in SHPD_PULSE_CNT.

DWord	Bit	Description
0	31:29	**Reserved** Format: MBZ
	28	**DDI A HPD Input Enable** This field controls the state of the HPD pin for the digital port A. Value: 0b — Name: Disable Value: 1b — Name: Enable
	27	**Reserved** Format: MBZ
	26	**Reserved** Format: MBZ
	25:24	**DDI A HPD Status** Access: R/WC This field reflects the hot plug detect status on port A. This bit is used for either monitor hotplug/unplug or for notification of a sink event. When HPD input is enabled and either a long or short pulse is detected, one of these bits will set and the hotplug IIR will be set (if unmasked in the IMR). The hotplug ISR gives the live state of the HPD pin. These are sticky bits, cleared by writing 1s to both of them. Value: 00b — Name: Hot plug event not detected Value: X1b — Name: Short pulse hot plug event detected

SHOTPLUG_CTL

	1Xb	Long pulse hot plug event detected

23:21	**Reserved** Format: MBZ
20	**DDI D HPD Input Enable** This field controls the state of the HPD pin for the digital port D. Value: 0b — Name: Disable Value: 1b — Name: Enable
19	**Reserved** Format: MBZ
18	**Reserved** Format: MBZ
17:16	**DDI D HPD Status** Access: R/WC This field reflects the hot plug detect status on port D. This bit is used for either monitor hotplug/unplug or for notification of a sink event. When HPD input is enabled and either a long or short pulse is detected, one of these bits will set and the hotplug IIR will be set (if unmasked in the IMR). The hotplug ISR gives the live state of the HPD pin. These are sticky bits, cleared by writing 1s to both of them. Value: 00b — Name: Hot plug event not detected Value: X1b — Name: Short pulse hot plug event detected Value: 1Xb — Name: Long pulse hot plug event detected
15:13	**Reserved** Format: MBZ
12	**DDI C HPD Input Enable** This field controls the state of the HPD pin for the digital port C. Value: 0b — Name: Disable Value: 1b — Name: Enable
11	**Reserved** Format: MBZ
10	**Reserved** Format: MBZ

SHOTPLUG_CTL

9:8 DDI C HPD Status

Access:	R/WC

This field reflects the hot plug detect status on port C. This bit is used for either monitor hotplug/unplug or for notification of a sink event.
When HPD input is enabled and either a long or short pulse is detected, one of these bits will set and the hotplug IIR will be set (if unmasked in the IMR).
The hotplug ISR gives the live state of the HPD pin.
These are sticky bits, cleared by writing 1s to both of them.

Value	Name
00b	Hot plug event not detected
X1b	Short pulse hot plug event detected
1Xb	Long pulse hot plug event detected

7:5 Reserved

Format:	MBZ

4 DDI B HPD Input Enable

This field controls the state of the HPD pin for the digital port B.

Value	Name
0b	Disable
1b	Enable

3 Reserved

Format:	MBZ

2 Reserved

Format:	MBZ

1:0 DDI B HPD Status

Access:	R/WC

This field reflects the hot plug detect status on port B. This bit is used for either monitor hotplug/unplug or for notification of a sink event.
When HPD input is enabled and either a long or short pulse is detected, one of these bits will set and the hotplug IIR will be set (if unmasked in the IMR).
The hotplug ISR gives the live state of the HPD pin.
These are sticky bits, cleared by writing 1s to both of them.

Value	Name
00b	Hot plug event not detected
X1b	Short pulse hot plug event detected
1Xb	Long pulse hot plug event detected

SHOTPLUG_CTL2

SHOTPLUG_CTL2

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	C403Ch-C403Fh
Name:	South Hot Plug Control 2
ShortName:	SHOTPLUG_CTL2
Power:	Always on
Reset:	soft

The short pulse duration is programmed in SHPD_PULSE_CNT.

DWord	Bit	Description
0	31:9	**Reserved** Format: MBZ
	8:5	**Reserved**
	4	**DDI E HPD Input Enable** This field controls the state of the HPD buffer for the digital port E. 0b – Disable 1b – Enable
	3	**Reserved** Format: MBZ
	2	**Reserved** Format: MBZ
	1:0	**DDI E HPD Status** Access: R/WC This field reflects the hot plug detect status on port E. This bit is used for either monitor hotplug/unplug or for notification of a sink event. When HPD input is enabled and either a long or short pulse is detected, one of these bits will set and the hotplug IIR will be set (if unmasked in the IMR). The hotplug ISR gives the live state of the HPD pin. These are sticky bits, cleared by writing 1s to both of them. 00b – Hot plug event not detected

SHOTPLUG_CTL2			
		X1b	Short pulse hot plug event detected
		1Xb	Long pulse hot plug event detected

SHPD_FILTER_CNT

SHPD_FILTER_CNT	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x000001F2
Access:	R/W
Size (in bits):	32
Address:	C4038h-C403Bh
Name:	South HPD Filter count
ShortName:	SHPD_FILTER_CNT
Power:	Always on
Reset:	global

This register must be programmed properly before enabling DDI HPD detection.

DWord	Bit	Description
0	31:17	**Reserved** Format: MBZ
	16:0	**HPD Filter Count** Default Value: 001F2h 500 microseconds These bits define the duration of the filter for DDI HPD. The value is the number of microseconds minus 2.

SHPD_PULSE_CNT

SHPD_PULSE_CNT	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x000007CE
Access:	R/W
Size (in bits):	32
Address:	C4034h-C4037h
Name:	South HPD Pulse count DDI B
ShortName:	SHPD_PULSE_CNT_B
Power:	Always on
Reset:	global
Address:	C4044h-C4047h
Name:	South HPD Pulse count DDI C
ShortName:	SHPD_PULSE_CNT_C
Power:	Always on
Reset:	global
Address:	C4048h-C404Bh
Name:	South HPD Pulse count DDI D
ShortName:	SHPD_PULSE_CNT_D
Power:	Always on
Reset:	global
Address:	C404Ch-C404Fh
Name:	South HPD Pulse count DDI A
ShortName:	SHPD_PULSE_CNT_A
Power:	Always on
Reset:	global
Address:	C4050h-C4053h
Name:	South HPD Pulse count DDI E
ShortName:	SHPD_PULSE_CNT_E
Power:	Always on
Reset:	global
This register must be programmed properly before enabling hotplug detection.	

DWord	Bit	Description
0	31:17	**Reserved**

SHPD_PULSE_CNT

		Format: MBZ
	16:0	**ShortPulse Count** These bits define the duration of the pulse defined as a short pulse for hotplug detection. The value is the number of microseconds minus 2.

Value	Name
007CEh	2,000 microseconds for DisplayPort **[Default]**
1869Eh	100,000 microseconds for HDMI or DVI

SINTERRUPT

SINTERRUPT

Register Space: MMIO: 0/2/0
Source: BSpec
Default Value: 0x00000000, 0x00000000, 0x00000000, 0x00000000
Access: RO, R/W, R/WC, R/W
Size (in bits): 128

See the South Display Engine Interrupt Bit Definition Table to find the source event for each interrupt bit.

DWord	Bit	Description
0	31:0	**ISR** Access: RO These are the Interrupt Status Register Bits. This field contains the non-persistent values of all interrupt status bits. The IMR selects which of these interrupt conditions are reported in the persistent IIR Value / Name: 0b – Condition Doesn't Exist 1b – Condition Exists **Programming Notes** Some inputs to this register are short pulses; therefore software should not expect to use this register to sample these conditions.
1	31:0	**IMR** Access: R/W These are the Interrupt Mask Register Bits. This field contains a bit mask which selects which interrupt bits from the ISR are reported in the IIR. Value / Name: 0b – Not Masked 1b – Masked
2	31:0	**IIR** Access: R/WC These are the Interrupt Identity Register Bits. This field holds the persistent values of the interrupt bits from the ISR which are unmasked by the IMR. If enabled by the IER, bits set in this register will generate a PCH display interrupt. Bits set in this register will remain set (persist) until the interrupt condition is cleared by writing a '1' to the appropriate bits. For each bit, the IIR can store a second pending interrupt if two or more of the same interrupt conditions occur before the first condition is cleared. Upon clearing the interrupt, the IIR bit and PCH display interrupt will momentarily go low, then return high to indicate there is another interrupt pending.

SINTERRUPT

		Value / **Name** 0b — Condition Not Detected 1b — Condition Detected
3	31:0	**IER** Access: R/W These are the Interrupt Enable Register Bits. The field enables a PCH display interrupt to be generated whenever the corresponding bit in the IIR becomes set. A disabled interrupt will still appear in the IIR. **Value** / **Name** 0b — Disabled 1b — Enabled

Slice 0 PFET control register with lock

PFETCTL - Slice 0 PFET control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0004005A [KBL]
Size (in bits):	32
Address:	24188h

DWord	Bit	Description
0	31	**PFET Control Lock** Access: R/W Lock 0 = Bits of this register are R/W 1 = All bits of this register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:21	**Reserved** Access: RO Reserved
	20	**Power Well Status** Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	19	**Powergood timer error** Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	18:16	**Delay from enabling secondary PFETs to power good.** Access: R/W Lock Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns 3'b010: 160ns 3'b011: 320ns

PFETCTL - Slice 0 PFET control register with lock

3'b100: 640ns
3'b101: 1280ns
3'b110: 2560ns
3'b111: 5120ns

Value	Name
100b	**[Default]**

15:13 **Time period last primay pfet strobe to secondary pfet strobe**

Access:	R/W Lock

Time period last primay pfet strobe to secondary pfet strobe
3'b000: 10ns (or 1 bclk)
3'b001: 20ns (or 2 bclk)
3'b010: 30ns (or 3 bclk)
3'b111: 80ns (or 8 bclk)

12:10 **Time period b/w two adjacent strobes**

Access:	R/W Lock

Time period b/w two adjacent strobes to the primary FETs
3'b000: 10ns (or 1 bclk)
3'b001: 20ns (or 2 bclk)
3'b010: 30ns (or 3 bclk)
3'b111: 80ns (or 8 bclk)

9:7 **FET setup margin from enable to strobe**

Access:	R/W Lock

Setup margin in design before sampling enable event at the first pre-charge sequencer/shift register flop
3'b000: 10ns (or 1 bclk)
3'b001: 20ns (or 2 bclk)
3'b010: 30ns (or 3 bclk)
3'b111: 80ns (or 8 bclk)

6:0 **Number of flops to enable primary FETs**

Default Value:	1011010b
Access:	R/W Lock

Number of flops to enable primary FETs. For a setting of N there will be N+1 total strobes generated
7'b0000000: 10 Flops to be strobed
7'b0000001: 11 Flops to be strobed
7'b0000010: 12 Flops to be strobed
7'b0001111: 26 Flops to be strobed

Slice 0 Power Context Save request

PGCTXREQ - Slice 0 Power Context Save request

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	24184h

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO Message Mask bots for lower 16 bits
	15:10	**Reserved** Access: RO Reserved
	9	**Power context save request** Access: R/W Set Power Context Save Request 1'b0 : Power context save is not being requested <default> 1'b1 : Power context save is being requested CPUnit self-clears this bit upon sampling.
	8:0	**Power Context Save request crdit count** Access: R/W QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

Slice 0 Power Down FSM control register with lock

POWERDNFSMCTL - Slice 0 Power Down FSM control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000088
Size (in bits):	32
Address:	24190h

DWord	Bit	Description
0	31	**power down control Lock** Access: R/W Lock 0 = Bits of Slice 0 POWERDNFSMCTL register are R/W 1 = All bits of Slice 0 POWERDNFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:13	**Reserved** Access: RO Reserved
	12	**Leave firewall disabled** Access: R/W Lock When This bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, i.e dont firewall the gated domain, but complete logical flow
	11	**Leave reset de-asserted** Access: R/W Lock When This bit is set SPC will not assert reset for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e assert resets during power down flows 1 = Leave reset de-asserted mode, i.e dont assert reset, but complete logical flow

POWERDNFSMCTL - Slice 0 Power Down FSM control register with lock

	10	**Leave CLKs ON** Access: R/W Lock When This bit is set SPC will not gate clks for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e gate clocks during power down flows 1 = Leave CLKS ON mode, i.e dont clock gate, but complete logical flow
	9	**Leave FET On** Access: R/W Lock When This bit is set SPC will not turn off the PFET eventhough it will complete the flow with PM Encodings: 0 = Default mode, i.e power off fets during power down flows 1 = Leave ON mode, i.e dont power off pfet, but complete logical flow **Programming Notes** This bit should be programmed before the powerup sequence is initiated for Slice 0.
	8:6	**Power Down state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Gate Clocks
	5:3	**Power Down state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default :Firewall ON

POWERDNFSMCTL - Slice 0 Power Down FSM control register with lock

	2:0	**Power Down state 1** Default Value: 000b Access: R/W Lock This will be the 1st state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Assert Reset

Slice 0 Power Gate Control Request

PGCTLREQ - Slice 0 Power Gate Control Request		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	24180h	
Clock Gating Messages Register		
DWord	**Bit**	**Description**
0	31:16	**Message Mask** Access: RO Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:2	**Reserved** Access: RO Reserved
	1	**CLK RST FWE Request** Access: R/W SLICE 0 CLK RST FWE request: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**Power Gate Request** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

Slice 0 Power on FSM control register with lock

POWERUPFSMCTL - Slice 0 Power on FSM control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000088
Size (in bits):	32
Address:	2418Ch

DWord	Bit	Description
0	31	**power up control Lock** Access: R/W Lock 0 = Bits of Slice 0 POWERUPFSMCTL register are R/W 1 = All bits of Slice 0 POWERUPFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:9	**Reserved** Access: RO Reserved
	8:6	**Power UP state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - De-assert resets 3'b000: 10ns (or 1 bclk)
	5:3	**Power UP state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Firewall OFF

POWERUPFSMCTL - Slice 0 Power on FSM control register with lock

	2:0	**Power UP state 1** Default Value: 000b Access: R/W Lock This will be the 1st state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Clock Ungate

Slice 0 SubSlice 0 PFET control register with lock

PFETCTL - Slice 0 SubSlice 0 PFET control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00070000
Size (in bits):	32
Address:	24408h

DWord	Bit	Description
0	31	**PFET Control Lock** Access: R/W Lock 0 = Bits of PFETCTL register are R/W 1 = All bits of PFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:21	**Reserved** Access: RO Reserved
	20	**Power Well Status** Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	19	**Powergood timer error** Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	18:16	**Delay from enabling secondary PFETs to power good.** Default Value: 111b Access: R/W Lock Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns

PFETCTL - Slice 0 SubSlice 0 PFET control register with lock

		3'b010: 160ns 3'b011: 320ns 3'b100: 640ns 3'b101: 1280ns 3'b110: 2560ns 3'b111: 5120ns
	15:13	**Time period last primay pfet strobe to secondary pfet strobe** Access: R/W Lock Time period last primay pfet strobe to secondary pfet strobe 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	12:10	**Time period b/w two adjacent strobes** Access: R/W Lock Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	9:7	**FET setup margin from enable to strobe** Access: R/W Lock Setup margin in design before sampling enable event at the first pre-charge sequencer/shift register flop 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	6:0	**Number of flops to enable primary FETs** Access: R/W Lock Number of flops to enable primary FETs. For a setting of N there will be N+1 total strobes generated 7'b0000000: 10 Flops to be strobed 7'b0000001: 11 Flops to be strobed 7'b0000010: 12 Flops to be strobed 7'b0001111: 26 Flops to be strobed

Slice 0 SubSlice 1 PFET control register with lock

PFETCTL - Slice 0 SubSlice 1 PFET control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00070000
Size (in bits):	32
Address:	24488h

DWord	Bit	Description
0	31	**PFET Control Lock** Access: R/W Lock 0 = Bits of Slice 0 PFETCTL register are R/W 1 = All bits of Slice 0 PFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:21	**Reserved** Access: RO Reserved
	20	**Power Well Status** Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	19	**Powergood timer error** Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	18:16	**Delay from enabling secondary PFETs to power good.** Default Value: 111b Access: R/W Lock Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns

PFETCTL - Slice 0 SubSlice 1 PFET control register with lock

		3'b010: 160ns 3'b011: 320ns 3'b100: 640ns 3'b101: 1280ns 3'b110: 2560ns 3'b111: 5120ns
	15:13	**Time period last primay pfet strobe to secondary pfet strobe** Access: R/W Lock Time period last primay pfet strobe to secondary pfet strobe 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	12:10	**Time period b/w two adjacent strobes** Access: R/W Lock Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	9:7	**FET setup margin from enable to strobe** Access: R/W Lock Setup margin in design before sampling enable event at the first pre-charge sequencer/shift register flop 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	6:0	**Number of flops to enable primary FETs** Access: R/W Lock Number of flops to enable primary FETs. For a setting of N there will be N+1 total strobes generated 7'b0000000: 10 Flops to be strobed 7'b0000001: 11 Flops to be strobed 7'b0000010: 12 Flops to be strobed 7'b0001111: 26 Flops to be strobed

Slice 0 SubSlice 1 Power Context Save request

PGCTXREQ - Slice 0 SubSlice 1 Power Context Save request

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	24484h

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO Message Mask bots for lower 16 bits
	15:10	**Reserved** Access: RO Reserved
	9	**Power context save request** Access: R/W Set Power Context Save Request 1'b0 : Power context save is not being requested <default> 1'b1 : Power context save is being requested CPUnit self-clears this bit upon sampling.
	8:0	**Power Context Save request crdit count** Access: R/W QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

Slice 0 SubSlice 1 Power Down FSM control register with lock

POWERDNFSMCTL - Slice 0 SubSlice 1 Power Down FSM control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000088
Size (in bits):	32
Address:	24490h

DWord	Bit	Description
0	31	**power down control Lock** Access: R/W Lock 0 = Bits of Slice 0 POWERDNFSMCTL register are R/W 1 = All bits of Slice 0 POWERDNFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:13	**Reserved** Access: RO Reserved
	12	**Leave firewall disabled** Access: R/W Lock When This bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, i.e dont firewall the gated domain, but complete logical flow
	11	**Leave reset de-asserted** Access: R/W Lock When This bit is set SPC will not assert reset for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e assert resets during power down flows 1 = Leave reset de-asserted mode, i.e dont assert reset, but complete logical flow

POWERDNFSMCTL - Slice 0 SubSlice 1 Power Down FSM control register with lock

	10	**Leave CLKs ON** Access: R/W Lock When This bit is set SPC will not gate clks for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e gate clocks during power down flows 1 = Leave CLKS ON mode, i.e dont clock gate, but complete logical flow
	9	**Leave FET On** Access: R/W Lock When This bit is set SPC will not turn off the PFET eventhough it will complete the flow with PM Encodings: 0 = Default mode, i.e power off fets during power down flows 1 = Leave ON mode, i.e dont power off pfet, but complete logical flow Programming note : This bit should be programmed before the powerup sequence is initiated for Slice 0 SSM1
	8:6	**Power Down state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Gate Clocks
	5:3	**Power Down state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default :Firewall ON

POWERDNFSMCTL - Slice 0 SubSlice 1 Power Down FSM control register with lock

	2:0	**Power Down state 1** Default Value: 000b Access: R/W Lock This will be the 1st state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Assert Reset

Slice 0 SubSlice 1 Power Gate Control Request

PGCTLREQ - Slice 0 SubSlice 1 Power Gate Control Request

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	24480h

Clock Gating Messages Register

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:2	**Reserved** Access: RO Reserved
	1	**CLK RST FWE Request** Access: R/W SLICE 0 CLK RST FWE request: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**Power Gate Request** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

Slice 0 SubSlice 1 Power on FSM control register with lock

POWERUPFSMCTL - Slice 0 SubSlice 1 Power on FSM control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000088
Size (in bits):	32
Address:	2448Ch

DWord	Bit	Description
0	31	**power up control Lock** Access: R/W Lock 0 = Bits of Slice 0 POWERUPFSMCTL register are R/W 1 = All bits of Slice 0 POWERUPFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:9	**Reserved** Access: RO Reserved
	8:6	**Power UP state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - De-assert resets 3'b000: 10ns (or 1 bclk)
	5:3	**Power UP state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF

POWERUPFSMCTL - Slice 0 SubSlice 1 Power on FSM control register with lock

		010 = De-assert resets 1xx = Rsvd for future Default - Firewall OFF
	2:0	**Power UP state 1** Default Value: 000b Access: R/W Lock This will be the 1st state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Clock Ungate

Slice 0 SubSlice 2 PFET control register with lock

PFETCTL - Slice 0 SubSlice 2 PFET control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00070000
Size (in bits):	32
Address:	24508h

DWord	Bit	Description
0	31	**PFET Control Lock** Access: R/W Lock 0 = Bits of Slice 0 PFETCTL register are R/W 1 = All bits of Slice 0 PFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:21	**Reserved** Access: RO Reserved
	20	**Power Well Status** Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	19	**Powergood timer error** Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	18:16	**Delay from enabling secondary PFETs to power good.** Default Value: 111b Access: R/W Lock Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns

PFETCTL - Slice 0 SubSlice 2 PFET control register with lock

		3'b010: 160ns 3'b011: 320ns 3'b100: 640ns 3'b101: 1280ns 3'b110: 2560ns 3'b111: 5120ns
	15:13	**Time period last primay pfet strobe to secondary pfet strobe** Access: R/W Lock Time period last primay pfet strobe to secondary pfet strobe 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	12:10	**Time period b/w two adjacent strobes** Access: R/W Lock Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	9:7	**FET setup margin from enable to strobe** Access: R/W Lock Setup margin in design before sampling enable event at the first pre-charge sequencer/shift register flop 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	6:0	**Number of flops to enable primary FETs** Access: R/W Lock Number of flops to enable primary FETs. For a setting of N there will be N+1 total strobes generated 7'b0000000: 10 Flops to be strobed 7'b0000001: 11 Flops to be strobed 7'b0000010: 12 Flops to be strobed 7'b0001111: 26 Flops to be strobed

Slice 0 SubSlice 2 Power Context Save request

PGCTXREQ - Slice 0 SubSlice 2 Power Context Save request

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	24504h

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO Message Mask bots for lower 16 bits
	15:10	**Reserved** Access: RO Reserved
	9	**Power context save request** Access: R/W Set Power Context Save Request 1'b0 : Power context save is not being requested <default> 1'b1 : Power context save is being requested CPUnit self-clears this bit upon sampling.
	8:0	**Power Context Save request crdit count** Access: R/W QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

Slice 0 SubSlice 2 Power Down FSM control register with lock

POWERDNFSMCTL - Slice 0 SubSlice 2 Power Down FSM control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000088
Size (in bits):	32
Address:	24510h

DWord	Bit	Description
0	31	**power down control Lock** Access: R/W Lock 0 = Bits of Slice 0 POWERDNFSMCTL register are R/W 1 = All bits of Slice 0 POWERDNFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:13	**Reserved** Access: RO Reserved
	12	**Leave firewall disabled** Access: R/W Lock When This bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, i.e dont firewall the gated domain, but complete logical flow
	11	**Leave reset de-asserted** Access: R/W Lock When This bit is set SPC will not assert reset for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e assert resets during power down flows 1 = Leave reset de-asserted mode, i.e dont assert reset, but complete logical flow

POWERDNFSMCTL - Slice 0 SubSlice 2 Power Down FSM control register with lock

	10	**Leave CLKs ON** Access: R/W Lock When This bit is set SPC will not gate clks for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e gate clocks during power down flows 1 = Leave CLKS ON mode, i.e dont clock gate, but complete logical flow
	9	**Leave FET On** Access: R/W Lock When This bit is set SPC will not turn off the PFET eventhough it will complete the flow with PM Encodings: 0 = Default mode, i.e power off fets during power down flows 1 = Leave ON mode, i.e dont power off pfet, but complete logical flow Programming note : This bit should be programmed before the powerup sequence is initiated for Slice 0 SSM2
	8:6	**Power Down state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Gate Clocks
	5:3	**Power Down state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default :Firewall ON

POWERDNFSMCTL - Slice 0 SubSlice 2 Power Down FSM control register with lock

	2:0	**Power Down state 1** Default Value: 000b Access: R/W Lock This will be the 1st state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Assert Reset

Slice 0 SubSlice 2 Power Gate Control Request

PGCTLREQ - Slice 0 SubSlice 2 Power Gate Control Request

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	24500h

Clock Gating Messages Register

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:2	**Reserved** Access: RO Reserved
	1	**CLK RST FWE Request** Access: R/W SLICE 0 CLK RST FWE request: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**Power Gate Request** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

Slice 0 SubSlice 2 Power on FSM control register with lock

POWERUPFSMCTL - Slice 0 SubSlice 2 Power on FSM control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000088
Size (in bits):	32
Address:	2450Ch

DWord	Bit	Description
0	31	**power up control Lock** Access: R/W Lock 0 = Bits of Slice 0 POWERUPFSMCTL register are R/W 1 = All bits of Slice 0 POWERUPFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:9	**Reserved** Access: RO Reserved
	8:6	**Power UP state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - De-assert resets 3'b000: 10ns (or 1 bclk)
	5:3	**Power UP state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF

POWERUPFSMCTL - Slice 0 SubSlice 2 Power on FSM control register with lock

		010 = De-assert resets 1xx = Rsvd for future Default - Firewall OFF
	2:0	**Power UP state 1** Default Value: 000b Access: R/W Lock This will be the 1st state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Clock Ungate

slice 1 PFET control register with lock

PFETCTL - slice 1 PFET control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0004005A
Size (in bits):	32
Address:	24208h

DWord	Bit	Description
0	31	**PFET Control Lock** Access: R/W Lock 0 = Bits of slice 1 PFETCTL register are R/W 1 = All bits of slice 1 PFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:21	**Reserved** Access: RO Reserved
	20	**Power Well Status** Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	19	**Powergood timer error** Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	18:16	**Delay from enabling secondary PFETs to power good.** Default Value: 100b Access: R/W Lock Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns

PFETCTL - slice 1 PFET control register with lock

		3'b010: 160ns 3'b011: 320ns 3'b100: 640ns 3'b101: 1280ns 3'b110: 2560ns 3'b111: 5120ns
	15:13	**Time period last primay pfet strobe to secondary pfet strobe** Access: R/W Lock Time period last primay pfet strobe to secondary pfet strobe 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	12:10	**Time period b/w two adjacent strobes** Access: R/W Lock Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	9:7	**FET setup margin from enable to strobe** Access: R/W Lock Setup margin in design before sampling enable event at the first pre-charge sequencer/shift register flop 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	6:0	**Number of flops to enable primary FETs** Default Value: 1011010b Access: R/W Lock Number of flops to enable primary FETs. For a setting of N there will be N+1 total strobes generated 7'b0000000: 10 Flops to be strobed 7'b0000001: 11 Flops to be strobed 7'b0000010: 12 Flops to be strobed 7'b0001111: 26 Flops to be strobed

slice 1 Power Context Save request

PGCTXREQ - slice 1 Power Context Save request		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	24204h	
DWord	**Bit**	**Description**
0	31:16	**Message Mask** Access: RO Message Mask bots for lower 16 bits
	15:10	**Reserved** Access: RO Reserved
	9	**Power context save request** Access: R/W Set Power Context Save Request 1'b0 : Power context save is not being requested <default> 1'b1 : Power context save is being requested CPUnit self-clears this bit upon sampling.
	8:0	**Power Context Save request crdit count** Access: R/W QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

slice 1 Power Down FSM control register with lock

POWERDNFSMCTL - slice 1 Power Down FSM control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000088
Size (in bits):	32
Address:	24210h

DWord	Bit	Description
0	31	**power down control Lock** Access: R/W Lock 0 = Bits of slice 1 POWERDNFSMCTL register are R/W 1 = All bits of slice 1 POWERDNFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:13	**Reserved** Access: RO Reserved
	12	**Leave firewall disabled** Access: R/W Lock When This bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, i.e dont firewall the gated domain, but complete logical flow
	11	**Leave reset de-asserted** Access: R/W Lock When This bit is set SPC will not assert reset for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e assert resets during power down flows 1 = Leave reset de-asserted mode, i.e dont assert reset, but complete logical flow

POWERDNFSMCTL - slice 1 Power Down FSM control register with lock

	10	**Leave CLKs ON** Access: R/W Lock When This bit is set SPC will not gate clks for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e gate clocks during power down flows 1 = Leave CLKS ON mode, i.e dont clock gate, but complete logical flow
	9	**Leave FET On** Access: R/W Lock When This bit is set SPC will not turn off the PFET eventhough it will complete the flow with PM Encodings: 0 = Default mode, i.e power off fets during power down flows 1 = Leave ON mode, i.e dont power off pfet, but complete logical flow Programming note : This bit should be programmed before the powerup sequence is initiated for Slice 1
	8:6	**Power Down state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Gate Clocks
	5:3	**Power Down state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default :Firewall ON

POWERDNFSMCTL - slice 1 Power Down FSM control register with lock

	2:0	**Power Down state 1** Default Value: 000b Access: R/W Lock This will be the 1st state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Assert Reset

slice 1 Power Gate Control Request

PGCTLREQ - slice 1 Power Gate Control Request

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	24200h

Clock Gating Messages Register

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:2	**Reserved** Access: RO Reserved
	1	**CLK RST FWE Request** Access: R/W SLICE 1 CLK RST FWE request: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**Power Gate Request** Access: R/W slice 1 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

slice 1 Power on FSM control register with lock

POWERUPFSMCTL - slice 1 Power on FSM control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000088
Size (in bits):	32
Address:	2420Ch

DWord	Bit	Description
0	31	**power up control Lock** Access: R/W Lock 0 = Bits of slice 1 POWERUPFSMCTL register are R/W 1 = All bits of slice 1 POWERUPFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:9	**Reserved** Access: RO Reserved
	8:6	**Power UP state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - De-assert resets 3'b000: 10ns (or 1 bclk)
	5:3	**Power UP state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF

POWERUPFSMCTL - slice 1 Power on FSM control register with lock

		010 = De-assert resets 1xx = Rsvd for future Default - Firewall OFF
	2:0	**Power UP state 1** Default Value: 000b Access: R/W Lock This will be the 1st state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Clock Ungate

slice 2 PFET control register with lock

PFETCTL - slice 2 PFET control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0004005A
Size (in bits):	32
Address:	24288h

DWord	Bit	Description
0	31	**PFET Control Lock** Access: R/W Lock 0 = Bits of slice 2 PFETCTL register are R/W 1 = All bits of slice 2 PFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:21	**Reserved** Access: RO Reserved
	20	**Power Well Status** Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	19	**Powergood timer error** Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	18:16	**Delay from enabling secondary PFETs to power good.** Default Value: 100b Access: R/W Lock Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns

PFETCTL - slice 2 PFET control register with lock

		3'b010: 160ns 3'b011: 320ns 3'b100: 640ns 3'b101: 1280ns 3'b110: 2560ns 3'b111: 5120ns
	15:13	**Time period last primay pfet strobe to secondary pfet strobe** Access: R/W Lock Time period last primay pfet strobe to secondary pfet strobe 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	12:10	**Time period b/w two adjacent strobes** Access: R/W Lock Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	9:7	**FET setup margin from enable to strobe** Access: R/W Lock Setup margin in design before sampling enable event at the first pre-charge sequencer/shift register flop 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	6:0	**Number of flops to enable primary FETs** Default Value: 1011010b Access: R/W Lock Number of flops to enable primary FETs. For a setting of N there will be N+1 total strobes generated 7'b0000000: 10 Flops to be strobed 7'b0000001: 11 Flops to be strobed 7'b0000010: 12 Flops to be strobed 7'b0001111: 26 Flops to be strobed

slice 2 Power Context Save request

PGCTXREQ - slice 2 Power Context Save request		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	24284h	
DWord	**Bit**	**Description**
0	31:16	**Message Mask** Access: RO Message Mask bots for lower 16 bits
	15:10	**Reserved** Access: RO Reserved
	9	**Power context save request** Access: R/W Set Power Context Save Request 1'b0 : Power context save is not being requested <default> 1'b1 : Power context save is being requested CPUnit self-clears this bit upon sampling.
	8:0	**Power Context Save request crdit count** Access: R/W QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

slice 2 Power Down FSM control register with lock

POWERDNFSMCTL - slice 2 Power Down FSM control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000088
Size (in bits):	32
Address:	24290h

DWord	Bit	Description
0	31	**power down control Lock** Access: R/W Lock 0 = Bits of slice 2 POWERDNFSMCTL register are R/W 1 = All bits of slice 2 POWERDNFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:13	**Reserved** Access: RO Reserved
	12	**Leave firewall disabled** Access: R/W Lock When This bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, i.e dont firewall the gated domain, but complete logical flow
	11	**Leave reset de-asserted** Access: R/W Lock When This bit is set SPC will not assert reset for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e assert resets during power down flows 1 = Leave reset de-asserted mode, i.e dont assert reset, but complete logical flow

POWERDNFSMCTL - slice 2 Power Down FSM control register with lock

	10	**Leave CLKs ON** Access: R/W Lock When This bit is set SPC will not gate clks for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e gate clocks during power down flows 1 = Leave CLKS ON mode, i.e dont clock gate, but complete logical flow
	9	**Leave FET On** Access: R/W Lock When This bit is set SPC will not turn off the PFET eventhough it will complete the flow with PM Encodings: 0 = Default mode, i.e power off fets during power down flows 1 = Leave ON mode, i.e dont power off pfet, but complete logical flow Programming note : This bit should be programmed before the powerup sequence is initiated for Slice 2
	8:6	**Power Down state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Gate Clocks
	5:3	**Power Down state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default :Firewall ON

POWERDNFSMCTL - slice 2 Power Down FSM control register with lock

	2:0	**Power Down state 1** Default Value: 000b Access: R/W Lock This will be the 1st state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Assert Reset

slice 2 Power Gate Control Request

PGCTLREQ - slice 2 Power Gate Control Request

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	24280h

Clock Gating Messages Register

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:2	**Reserved** Access: RO Reserved
	1	**CLK RST FWE Request** Access: R/W slice 2 CLK RST FWE request: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**Power Gate Request** Access: R/W slice 2 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

slice 2 Power on FSM control register with lock

POWERUPFSMCTL - slice 2 Power on FSM control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000088
Size (in bits):	32
Address:	2428Ch

DWord	Bit	Description
0	31	**power up control Lock** Access: R/W Lock 0 = Bits of slice 2 POWERUPFSMCTL register are R/W 1 = All bits of slice 2 POWERUPFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:9	**Reserved** Access: RO Reserved
	8:6	**Power UP state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - De-assert resets 3'b000: 10ns (or 1 bclk)
	5:3	**Power UP state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF

POWERUPFSMCTL - slice 2 Power on FSM control register with lock

		010 = De-assert resets 1xx = Rsvd for future Default - Firewall OFF
	2:0	**Power UP state 1** Default Value: 000b Access: R/W Lock This will be the 1st state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Clock Ungate

Snoop control register

SNPCR - Snoop control register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00001B40
Size (in bits):	32
Address:	0900Ch

Snoop control register

DWord	Bit	Description
0	31:23	**Reserved** Access: RO
	22:21	**IDICOS** Access: R/W 00b: default value. Resources for each setting is determined by uncore registers.
	20	**Non Temporal** Access: R/W Indication to uncore that - Request is of the type that should get minimal cache resources in the uncore.
	19:17	**RSVD** Access: RO
	16	**Restrict Snoops to MSQC, no forwarding to L3** Access: R/W 1'b0 - Snoops are not restricted. 1'b1 - Restrict snoops to MSQC and do not forward to Node snoop unit (L3).
	15	**Thread ID** Access: R/W 1 bit Thread ID for GT.
	14	**Force Invalidate** Access: R/W Force Invalidate - Forces the invalidate flag to be set with snoop lookups all the time. 0: Normal invalidation (based on req) - Default. 1: Forced invalidation.

SNPCR - Snoop control register

13:11 IDI Pend Timer

Default Value:	011b
Access:	R/W

IDIpend timer - Time to wait before monitoring the sq_snpc_idipend signal.
000b => 0 clocks.
001b => 1 clock.
010b => 2 clocks.
011b => 4 clocks (default.)
100b => 8.
101b => 16.
110b => 32.
111b => 64.

10:8 Retry Limit

Default Value:	011b
Access:	R/W

Retry Limit - Number of times to retry before switching to the freeze mechanism.
000b => Always freeze (first shot).
001b => 1 retry.
010b => 2 retry.
011b => 4 retry (default).
100b => 8 retry.
101b => 16 retry.
110b => 32 retry.
111b => infinite (no freeze).

7:3 Retry Timer

Default Value:	01000b
Access:	R/W

Retry Timer - Time between receiving a reject from SQ and repeating the monitor sequence.
00000b => 0 clocks.
00001b => 1 clock.
00010b => 2 clocks.
00011b => 3 clocks.
00111b => 7 clocks.
01000b => 8 clocks (Default).
...
11111b => 32 clocks.

SNPCR - Snoop control register

	2:0	**MLCSQ Timer** Access: R/W MLC-SQ Timer - Time between doing an MLC lookup and SQ lookup. 000b => 0 clocks (default). 001b => 1 clock. 010b => 2 clocks. 011b => 4 clocks. 100b => 8. 101b => 16. 110b => 32. 111b => 64.

Software SCI

SWSCI_0_2_0_PCI - Software SCI

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	16
Address:	000E8h

This register serves two purposes:

1. Support selection of SMI or SCI event source (SMISCISEL - bit15).
2. As an SCI Event trigger (GSSCIE - bit 0).

To generate a SW SCI event, software should program bit 15 (SMISCISEL) to 1. This is typically programmed once (assuming SMIs are never triggered). On a "0" to "1" subsequent transition in bit 0 of this register (caused by a software write operation), a SCI message will be sent to cause the TCOSCI_STS bit in GPE0 register to be set to 1. The corresponding SCI event handler in BIOS is to be defined as a _Lxx method, indicating level trigger to the operating system. Once written as 1, software must write a "0" to this bit to clear it, and all other write transitions (1-0, 0-0, 1-1) will not cause a SCI message to be sent. To generate a SW SMI event, software should program bit 15 to 0 and trigger SMI via writes to SWSMI register (See SWSMI register for programming details).

DWord	Bit	Description

0	15	**SMI or SCI event select**
		Default Value: 0b
		Access: R/W Once
		`0 = SMI (default)`
		`1 = SCI`
		If selected event source is SMI, SMI trigger and associated scratch bits accesses are performed via SWSMI register.
		If SCI event source is selected, the rest of the bits in this register provide SCI trigger capability and associated SW scratch pad area.

	14:1	**Software scratch bits** Default Value: 00000000000000b Access: R/W Read/write bits not used by hardware.
	0	**Software SCI Event** Default Value: 0b Access: R/W If SCI event is selected (SMISCISEL = 1), on a 0 to 1 transition of GSSCIE bit, a SCI message will be sent to cause the TCOSCI_STS bit in GPE0 register to be set to 1. Software must write a 0 to clear this bit.

Software SMI

SWSMI_0_2_0_PCI - Software SMI

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	16
Address:	000E0h

DWord	Bit	Description
0	15:8	**Software Scratch Bits** Default Value: 00000000b Access: R/W
	7:1	**Software Flag** Default Value: 0000000b Access: R/W Used to indicate caller and SMI function desired, as well as return result.
	0	**GMCH Software SMI Event** Default Value: 0b Access: R/W This bit will trigger an SMI even when set. Software must write a "0" to clear this bit. SMI will be triggered only if SWSCI[SMISCISEL] is set to select SMI.

South Display Engine Interrupt Bit Definition

South Display Engine Interrupt Bit Definition

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	C4000h-C400Fh
Name:	South Display Engine Interrupts
ShortName:	SDE_INTERRUPT
Power:	Always on
Reset:	soft

South Display Engine (SDE) interrupt bits come from events within the south display engine.
The SDE_IIR bits are ORed together to generate the South/PCH Display Interrupt Event which will appear in the North Display Engine Interrupt Control Registers.
The South Display Engine Interrupt Control Registers all share the same bit definitions from this table.

Programming Notes

Due to the possibility of back to back Hotplug events it is recommended that software filters the value read from the Hotplug ISRs.

DWord	Bit	Description
0	31:27	**Reserved** Format: MBZ
	26	**Reserved**
	25	**DDI E Hotplug** The ISR is an active high level representing the Digital Port E hotplug line when the Digital Port E hotplug detect input is enabled. The IIR is set on either a short or long pulse detection status in the Digital Port Hot Plug Control Register.
	24	**DDI A Hotplug** The ISR is an active high level representing the Digital Port A hotplug line when the Digital Port A hotplug detect input is enabled. The IIR is set on either a short or long pulse detection status in the Digital Port Hot Plug Control Register.
	23	**DDI D Hotplug** The ISR is an active high level representing the Digital Port D hotplug line when the Digital Port D hotplug detect input is enabled. The IIR is set on either a short or long pulse detection status in the Digital Port Hot Plug Control Register.
	22	**DDI C Hotplug** The ISR is an active high level representing the Digital Port C hotplug line when the Digital Port C hotplug detect input is enabled.

South Display Engine Interrupt Bit Definition		
		The IIR is set on either a short or long pulse detection status in the Digital Port Hot Plug Control Register.
	21	**DDI B Hotplug** The ISR is an active high level representing the Digital Port B hotplug line when the Digital Port B hotplug detect input is enabled. The IIR is set on either a short or long pulse detection status in the Digital Port Hot Plug Control Register.
	20:18	**Reserved** Format: MBZ
	17	**Gmbus** This is an active high pulse when any of the events unmasked events in GMBUS4 Interrupt Mask register occur.
	16:12	**Reserved** Format: MBZ
	11:8	**Reserved**
	7	**Reserved**
	6:0	**Reserved**

SQ Error Status

SQERR - SQ Error Status		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	09034h	
SQ Error Status register		

DWord	Bit	Description
0	31:9	**RSVD** Access: RO
	8	**SQ RW Port Address Decode Error** Access: RO SQ RW Address Decode Error. This bit is cleared when SW writes to this bit.
	7:1	**RSVD** Access: RO
	0	**SQ RO Port Address Decode Error** Access: RO SQ RO Address Decode Error. This bit is cleared when SW writes to this bit.

SQ RO Port Decode Error Address LSB

SQROERRADDR_LSB - SQ RO Port Decode Error Address LSB		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	09210h	
SQ RO Port Decode Error Address		
DWord	**Bit**	**Description**
0	31:0	**SQ RO Port Error Address LSB** Access: RO SQ RO Port Decode Error Address.

SQ RO Port Decode Error Address MSB

SQROERRADDR_MSB - SQ RO Port Decode Error Address MSB		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	09214h	
SQ RO Port Decode Error Address		
DWord	**Bit**	**Description**
0	31:8	**RSVD** Access: RO
	7:0	**SQ RO Port Error Address MSB** Access: RO SQ RO Port Decode Error Address.

SQ RW Port Decode Error Address LSB

SQRWERRADDR_LSB - SQ RW Port Decode Error Address LSB		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	09218h	
SQ RW Port Deocde Error Address		
DWord	**Bit**	**Description**
0	31:0	**SQ RW Port Error Address LSB** Access: RO SQ RW Port Error Address.

SQ RW Port Decode Error Address MSB

SQRWERRADDR_MSB - SQ RW Port Decode Error Address MSB		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0921Ch	
SQ RW Port Deocde Error Address		
DWord	**Bit**	**Description**
0	31:8	**RSVD** Access: RO
	7:0	**SQ RW Port Error Address MSB** Access: RO SQ RW Port Error Address.

SRD_CTL

SRD_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00100001
Access:	R/W
Size (in bits):	32
Address:	60800h-60803h
Name:	Transcoder A SRD Control
ShortName:	SRD_CTL_A
Power:	PG2
Reset:	soft
Address:	61800h-61803h
Name:	Transcoder B SRD Control
ShortName:	SRD_CTL_B
Power:	PG2
Reset:	soft
Address:	62800h-62803h
Name:	Transcoder C SRD Control
ShortName:	SRD_CTL_C
Power:	PG2
Reset:	soft
Address:	6F800h-6F803h
Name:	Transcoder EDP SRD Control
ShortName:	SRD_CTL_EDP
Power:	PG1
Reset:	soft
There is one instance of this register format per each transcoder A/B/C/EDP.	

Programming Notes

To use FBC modification tracking for idleness calculations when FBC is disabled, program FBC_CTL CPU Fence Enable, FBC_CONTROL_SA_REGISTER, FBC_CPU_FENCE_OFFSET_REGISTER, FBC_RT_BASE_ADDR_REGISTER, and BLITTER_TRACKING_REGISTER as they are programmed when FBC is enabled.

Cursor front buffer modifications are not tracked in hardware. If the cursor front buffer is modified, touch (write without changing) any cursor register to trigger the PSR idleness tracking.

Restriction

SRD_CTL

Restriction : Only the SRD Enable and Single Frame Update Enable fields can be changed while SRD is enabled. The other fields must not be changed while SRD is enabled.

DWord	Bit	Description
0	31	**SRD Enable** This bit enables the Self Refreshing Display function. Updates will take place at the start of the next vertical blank. The port will send SRD VDMs while enabled. When idleness conditions have been met for the programmed number of idle frames, hardware will enter SRD (sleep) and can disable the link and stop fetching data from memory. When activity occurs, hardware will exit SRD (wake) and re-enable the link and resume fetching data from memory.

Value	Name
0b	Disable
1b	Enable

Restriction
Restriction : SRD must not be enabled when the PSR Setup time from DPCD 00071h is greater than the time for vertical blank minus one line.
Restriction : SRD must not be enabled together with Interlacing, Black Frame Insertion (BFI), or audio on the same transcoder.

	30	**Single Frame Update Enable** Access: Double Buffered This field enables the single frame update mode where a plane flip will cause a single frame to be sent to the receiver. Updates to this field will take effect at the next vertical blank.

Value	Name
0b	Disable
1b	Enable

Programming Notes
Set register PIPE_MISC field Change Mask for Vblank Vsync Int to 1b (Masked) if vblank or vsync interrupts will be used together with single frame update.

Workaround
Workaround : When Single Frame Update is enabled, the CRC must be disabled for panel compatibility.

Restriction
Restriction : This mode should only be enabled with link standby.

SRD_CTL

29 Context restore to PSR Active

This field restores eDP context to PSR Active on a context restore.

Value	Name
0b	Disable
1b	Enable

Restriction
Restriction : This field is used for hardware communication. Software must not change this field.

28 Reserved

Format:	MBZ

27 Link Ctrl

This field controls the behavior of the link when in SRD (sleeping). The timing generator and pixel data fetches are disabled when the link is disabled. Only pixel data fetches are disabled when the link is in standby.
This field is ignored by transcoder A/B/C since they only operate in standby.

Value	Name	Description
0b	Disable	Link is disabled when in SRD (sleeping)
1b	Standby	Link is in standby when in SRD (sleeping)

26:25 Reserved

Format:	MBZ

24:20 Max Sleep Time

Default Value:	00001b 1/8 second

This field is the maximum time to spend in SRD (sleeping).
It is programmed in increments of approximately 1/8 a second.
Programming all 1s gives ~3.875 seconds.

Restriction
Restriction : Programming all 0s is invalid.

19:14 Reserved

Format:	MBZ

13 Reserved

12 Reserved

11 TP2 TP3 Select

This field controls whether TP1 is followed by TP2 or TP3 for training the link on exiting SRD (waking).

Value	Name	Description
0b	TP2	Use TP1 followed by TP2
1b	TP3	Use TP1 followed by TP3

SRD_CTL

10 CRC Enable

This field controls whether the PSR CRC value will be placed in the VSC packet.

Value	Name	Description
0b	Disable	Disable CRC output in VSC. VSC packet CRC value will be populated by VIDEO_DIP_DATA.
1b	Enable	Enable CRC output in VSC. VSC packet CRC value will be populated by the calculated CRC value.

Programming Notes
When CRC is enabled, the Max Sleep Timer should be disabled to provide additional power savings. Disable the Max Sleep Timer by setting register 0x6F860 bit 28 to 1. Re-enable the Max Sleep Timer by clearing register 0x6F860 bit 28 to 0.

Workaround
Workaround : When Single Frame Update is enabled, the CRC must be disabled for panel compatibility.

9:8 TP2 TP3 Time

This field selects the TP2 or TP3 time when training the link on exiting SRD (waking).

Value	Name
00b	500us
01b	100us
10b	2.5ms
11b	0us Skip TP2/TP3

7:6 Reserved

Format:	MBZ

5:4 TP1 Time

This field selects the TP1 time when training the link on exiting SRD (waking).

Value	Name
00b	500us
01b	100us
10b	2.5ms
11b	0us Slip TP1

3:0 Idle Frames

Default Value:	0001b 1 idle frame

This field is the number of idle frames required before entering SRD (sleeping).

SRD_IIR

SRD_IIR		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/WC	
Size (in bits):	32	
Address:	64838h-6483Bh	
Name:	SRD Interrupt Identity	
ShortName:	SRD_IIR	
Power:	PG1	
Reset:	soft	

See the SRD interrupt bit definition to find the source event for each interrupt bit.

DWord	Bit	Description
0	31:0	**Interrupt Identity Bits** This field holds the persistent values of the SRD interrupt bits which are unmasked by the SRD_IMR. Bits set in this register will propagate to the SRD interrupt in the Display Engine Miscellaneous Interrupts. Bits set in this register will remain set (persist) until the interrupt condition is cleared by writing a '1' to the appropriate bits

Value	Name
0b	Condition Not Detected
1b	Condition Detected

SRD_IMR

SRD_IMR	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x03030307
Access:	R/W
Size (in bits):	32
Address:	64834h-64837h
Name:	SRD Interrupt Mask
ShortName:	SRD_IMR
Power:	PG1
Reset:	soft

See the SRD interrupt bit definition to find the source event for each interrupt bit.

DWord	Bit	Description
0	31:0	**Interrupt_Mask_Bits** This field contains a bit mask which selects which SRD events are reported int the SRD_IIR.

Value	Name
0b	Not Masked
1b	Masked
03030307h	All interrupts masked **[Default]**

SRD_PERF_CNT

SRD_PERF_CNT	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	Write/Read Status
Size (in bits):	32
Address:	60844h-60847h
Name:	Transcoder A SRD Performance Counter
ShortName:	SRD_PERF_CNT_A
Power:	PG2
Reset:	soft
Address:	61844h-61847h
Name:	Transcoder B SRD Performance Counter
ShortName:	SRD_PERF_CNT_B
Power:	PG2
Reset:	soft
Address:	62844h-62847h
Name:	Transcoder C SRD Performance Counter
ShortName:	SRD_PERF_CNT_C
Power:	PG2
Reset:	soft
Address:	6F844h-6F847h
Name:	Transcoder EDP SRD Performance Counter
ShortName:	SRD_PERF_CNT_EDP
Power:	PG1
Reset:	soft

Description
There is one instance of this register format per each transcoder A/B/C/EDP.

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:0	**SRD Perf Cnt** This field increments every millisecond while in SRD (sleeping) and the display CD clock is running. It will stop incrementing when out of SRD (awake), then resume when back in SRD (sleeping).

SRD_PERF_CNT		
		The value is maintained while SRD is disabled, and counting will resume from the previous value when SRD is re-enabled. Writes to this register will set the count to the written value, then it will increment from that value onwards.

SRD_STATUS

SRD_STATUS	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	60840h-60843h
Name:	Transcoder A SRD Status
ShortName:	SRD_STATUS_A
Power:	PG2
Reset:	soft
Address:	61840h-61843h
Name:	Transcoder B SRD Status
ShortName:	SRD_STATUS_B
Power:	PG2
Reset:	soft
Address:	62840h-62843h
Name:	Transcoder C SRD Status
ShortName:	SRD_STATUS_C
Power:	PG2
Reset:	soft
Address:	6F840h-6F843h
Name:	Transcoder EDP SRD Status
ShortName:	SRD_STATUS_EDP
Power:	PG1
Reset:	soft

Description
There is one instance of this register format per each transcoder A/B/C/EDP.

DWord	Bit	Description
0	31:29	**SRD State** Access: RO This field indicates the live state of SRD

Value	Name	Description
000b	IDLE	Reset state

SRD_STATUS

001b	SRDONACK	Wait for TG/Stream to send on frame of data after SRD conditions are met
010b	SRDENT	SRD entry with Link OFF
011b	BUFOFF	Wait for buffer turn off
100b	BUFON	Wait for buffer turn on
101b	AUXACK	Wait for AUX to acknowledge on SRD exit
110b	SRDOFFACK	Wait for TG/Stream to acknowledge the SRD VDM exit
111b	SRDENT_ON	SRD entry with Link ON
Others	Reserved	Reserved

28 **Reserved**

Format:	MBZ

27:26 **Link Status**

Access:	RO

This field indicates the live status of the link.

Value	Name	Description
00b	Full Off	Link is fully off
01b	Full On	Link is fully on
10b	Standby	Link is in standby
11b	Reserved	Reserved

25 **Reserved**

Format:	MBZ

24:20 **Max Sleep Time Counter**

Access:	RO

This field provides the live status of the sleep time counter.

19:16 **SRD Entry Count**

Access:	RO

The value in this register represents the number of times SRD has been entered (gone to sleep). The count will increment with each entry. After reaching the maximum count value the counter will rollover and continue from 0.

15 **Aux Error**

Access:	RO

Description
This field indicates an error on the last SRD AUX handshake.
The Aux Error status non-EDP transcoders follows the mapping from Aux channel to transcoder:

SRD_STATUS

Aux B to SRD_STATUS_A.
Aux C to SRD_STATUS_B.
Aux D to SRD_STATUS_C.

Value	Name	Description
0b	No Error	AUX had no error
1b	Error	AUX error (receive error or timeout) occured

14:13 **Reserved**

Format:	MBZ

12 **Sending Aux**

Access:	RO

Description
This field indicates if the SRD AUX handshake is currently being sent.
The Sending Aux status non-EDP transcoders follows the mapping from Aux channel to transcoder: Aux B to SRD_STATUS_A. Aux C to SRD_STATUS_B. Aux D to SRD_STATUS_C.

Value	Name	Description
0b	Not Sending	Not sending AUX handshake
1b	Sending	Sending AUX handshake

11:10 **Reserved**

Format:	MBZ

9 **Sending Idle**

Access:	RO

This field indicates if idles are currently being sent.

Value	Name	Description
0b	Not Sending	Not sending idle
1b	Sending	Sending idle

8 **Sending TP2 TP3**

Access:	RO

This field indicates if TP2 or TP3 is currently being sent.

Value	Name	Description
0b	Not Sending	Not sending TP2 or TP3
1b	Sending	Sending TP2 or TP3

7 **Reserved**

SRD_STATUS

	6:5	**Reserved** Format: MBZ
	4	**Sending TP1** Access: RO This field indicates if TP1 is currently being sent.

Value	Name	Description
0b	Not Sending	Not sending TP1
1b	Sending	Sending TP1

	3:0	**Idle Frame Counter** Access: RO This field provides the live status of the idle frame counter.

Stream Output 0 Num Primitives Written Counter

SO0_NUM_PRIMS_WRITTEN - Stream Output 0 Num Primitives Written Counter

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	05200h-05207h

There is one 64-bit register for each of the 4 supported streams:

- 5200h-5207h SO_NUM_PRIMS_WRITTEN0 (for Stream Out Stream #0)
- 5208h-520Fh SO_NUM_PRIMS_WRITTEN1 (for Stream Out Stream #1)
- 5210h-5217h SO_NUM_PRIMS_WRITTEN2 (for Stream Out Stream #2)
- 5218h-521Fh SO_NUM_PRIMS_WRITTEN3 (for Stream Out Stream #3)

These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has successfully written to a particular "stream's" Streamed Vertex Output buffers, subject to buffer overflow detection. (See the Stream Output section of the 3D pipeline volume).
These registers are part of the context save and restore.
More details about the precise event counted by this register are located **here**.

DWord	Bit	Description
0	31:0	**Num Prims Written Count** Format: U32 This count is incremented (by one) every time a GS thread outputs a DataPort Streamed Vertex Buffer Write message with the Increment Num Prims Written bit set in the message header (see the Geometry Shader and Data Port chapters in the 3D Volume.)
1	31:0	**Num Prims Written Count** Format: U32 This count is incremented (by one) every time a GS thread outputs a DataPort Streamed Vertex Buffer Write message with the Increment Num Prims Written bit set in the message header (see the Geometry Shader and Data Port chapters in the 3D Volume.)

Stream Output 0 Primitive Storage Needed Counter

SO0_PRIM_STORAGE_NEEDED - Stream Output 0 Primitive Storage Needed Counter

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	05240h-05247h

There is one 64-bit register for each of the 4 supported streams:

- 5240h-5247h SO_PRIM_STORAGE_NEEDED0 (for Stream Out Stream #0)
- 5248h-524Fh SO_PRIM_STORAGE_NEEDED1 (for Stream Out Stream #1)
- 5250h-5257h SO_PRIM_STORAGE_NEEDED2 (for Stream Out Stream #2)
- 5258h-525Fh SO_PRIM_STORAGE_NEEDED3 (for Stream Out Stream #3)

These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has or would have written to a particular "stream's" Streamed Vertex Output buffers if all buffers had been large enough to accommodate the writes. (See the Stream Output section of the 3D pipeline volume).
These registers are part of the context save and restore.
More details about the precise event counted by this register are located **here**.

DWord	Bit	Description
0	31:0	**Prim Storage Needed Count** Format: U32 This count is incremented (by one) by the SOL stage for each object (point, line, triangle) it writes or attempts to write to the corresponding stream's output buffers. The count is not affected by the actual number of buffers bound to the stream.
1	31:0	**Prim Storage Needed Count** Format: U32 This count is incremented (by one) by the SOL stage for each object (point, line, triangle) it writes or attempts to write to the corresponding stream's output buffers. The count is not affected by the actual number of buffers bound to the stream.

Stream Output 0 Write Offset

SO0_WRITE_OFFSET - Stream Output 0 Write Offset

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	05280h-05283h

There is one R/W 32-bit register for each of the 4 supported stream output buffer slots:
5280h-5283h SO_WRITE_OFFSET0 (for Stream Out Buffer #0)
5284h-5287h SO_WRITE_OFFSET1 (for Stream Out Buffer #1)
5288h-528Bh SO_WRITE_OFFSET2 (for Stream Out Buffer #2)
528Ch-528Fh SO_WRITE_OFFSET3 (for Stream Out Buffer #3)
These registers are used to set and track a DWord-granular Write Offset for each of the 4 Stream Output Buffer slots. Software can directly write them via MI_LOAD_REGxxx commands. The SOL stage will increment them as part of stream output processing. Software can cause them to be written to memory via MI_STORE_REGxxx commands. (See the Stream Output section of the 3D pipeline volume).
These registers are part of the context save and restore.

Programming Notes

- Software must ensure that no HW stream output operations can be in process or otherwise pending at the point that the MI_LOAD/STORE commands are processed. This will likely require a pipeline flush.
- The SOL stage will effectively advance the write offset by the buffer's Surface Pitch after each vertex is written (assuming no overflow is detected in any targetted SO buffer). Under "normal" conditions one would expect software to initialize the WriteOffset to some (possibly zero) multiple of Surface Pitch in order to align vertex writes to the buffer's Base Address, though it is not required to do so.

DWord	Bit	Description
0	31:2	**Write Offset** Format: U30 This field contains a DWord offset from the corresponding SO buffer's Base Address value. The SOL stage uses this value as a write offset when performing writes to the buffer. The SOL stage will increment this value as a part of performing stream output to the buffer. Note that the SOL stage uses the buffer's Surface Pitch to advance the Write Offset, without regard to the buffer's Base Address (see Programming Notes above).
	1:0	**Reserved** Format: MBZ

Stream Output 1 Num Primitives Written Counter

SO1_NUM_PRIMS_WRITTEN - Stream Output 1 Num Primitives Written Counter

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	05208h-0520Fh

There is one 64-bit register for each of the 4 supported streams:
5200h-5207h SO_NUM_PRIMS_WRITTEN0 (for Stream Out Stream #0)
5208h-520Fh SO_NUM_PRIMS_WRITTEN1 (for Stream Out Stream #1)
5210h-5217h SO_NUM_PRIMS_WRITTEN2 (for Stream Out Stream #2)
5218h-521Fh SO_NUM_PRIMS_WRITTEN3 (for Stream Out Stream #3)
These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has successfully written to a particular "stream's" Streamed Vertex Output buffers, subject to buffer overflow detection. (See the Stream Output section of the 3D pipeline volume).
These registers are part of the context save and restore.

DWord	Bit	Description
0	31:0	**Num Prims Written Count** Format: U32 This count is incremented (by one) every time a GS thread outputs a DataPort Streamed Vertex Buffer Write message with the Increment Num Prims Written bit set in the message header (see the Geometry Shader and Data Port chapters in the 3D Volume.)
1	31:0	**Num Prims Written Count** Format: U32 This count is incremented (by one) every time a GS thread outputs a DataPort Streamed Vertex Buffer Write message with the Increment Num Prims Written bit set in the message header (see the Geometry Shader and Data Port chapters in the 3D Volume.)

Stream Output 1 Primitive Storage Needed Counter

SO1_PRIM_STORAGE_NEEDED - Stream Output 1 Primitive Storage Needed Counter

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	05248h-0524Fh

There is one 64-bit register for each of the 4 supported streams:
5240h-5247h SO_PRIM_STORAGE_NEEDED0 (for Stream Out Stream #0)
5248h-524Fh SO_PRIM_STORAGE_NEEDED1 (for Stream Out Stream #1)
5250h-5257h SO_PRIM_STORAGE_NEEDED2 (for Stream Out Stream #2)
5258h-525Fh SO_PRIM_STORAGE_NEEDED3 (for Stream Out Stream #3)
These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has or would have written to a particular "stream's" Streamed Vertex Output buffers if all buffers had been large enough to accommodate the writes. (See the Stream Output section of the 3D pipeline volume).
These registers are part of the context save and restore.

DWord	Bit	Description
0	31:0	**Prim Storage Needed Count** Format: U32 This count is incremented (by one) by the SOL stage for each object (point, line, triangle) it writes or attempts to write to the corresponding stream's output buffers. The count is not affected by the actual number of buffers bound to the stream.
1	31:0	**Prim Storage Needed Count** Format: U32 This count is incremented (by one) by the SOL stage for each object (point, line, triangle) it writes or attempts to write to the corresponding stream's output buffers. The count is not affected by the actual number of buffers bound to the stream.

Stream Output 1 Write Offset

SO1_WRITE_OFFSET - Stream Output 1 Write Offset

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	05284h-05287h

There is one R/W 32-bit register for each of the 4 supported stream output buffer slots:
5280h-5283h SO_WRITE_OFFSET0 (for Stream Out Buffer #0)
5284h-5287h SO_WRITE_OFFSET1 (for Stream Out Buffer #1)
5288h-528Bh SO_WRITE_OFFSET2 (for Stream Out Buffer #2)
528Ch-528Fh SO_WRITE_OFFSET3 (for Stream Out Buffer #3)
These registers are used to set and track a DWord-granular Write Offset for each of the 4 Stream Output Buffer slots. Software can directly write them via MI_LOAD_REGxxx commands. The SOL stage will increment them as part of stream output processing. Software can cause them to be written to memory via MI_STORE_REGxxx commands. (See the Stream Output section of the 3D pipeline volume).
These registers are part of the context save and restore.

Programming Notes

- Software must ensure that no HW stream output operations can be in process or otherwise pending at the point that the MI_LOAD/STORE commands are processed. This will likely require a pipeline flush.
- The SOL stage will effectively advance the write offset by the buffer's Surface Pitch after each vertex is written (assuming no overflow is detected in any targetted SO buffer). Under "normal" conditions one would expect software to initialize the WriteOffset to some (possibly zero) multiple of Surface Pitch in order to align vertex writes to the buffer's Base Address, though it is not required to do so.

DWord	Bit	Description
0	31:2	**Write Offset** Format: U30 This field contains a DWord offset from the corresponding SO buffer's Base Address value. The SOL stage uses this value as a write offset when performing writes to the buffer. The SOL stage will increment this value as a part of performing stream output to the buffer. Note that the SOL stage uses the buffer's Surface Pitch to advance the Write Offset, without regard to the buffer's Base Address (see Programming Notes above).
	1:0	**Reserved** Format: MBZ

Stream Output 2 Num Primitives Written Counter

SO2_NUM_PRIMS_WRITTEN - Stream Output 2 Num Primitives Written Counter

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	05210h-05217h

There is one 64-bit register for each of the 4 supported streams:
5200h-5207h SO_NUM_PRIMS_WRITTEN0 (for Stream Out Stream #0)
5208h-520Fh SO_NUM_PRIMS_WRITTEN1 (for Stream Out Stream #1)
5210h-5217h SO_NUM_PRIMS_WRITTEN2 (for Stream Out Stream #2)
5218h-521Fh SO_NUM_PRIMS_WRITTEN3 (for Stream Out Stream #3)
These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has successfully written to a particular "stream's" Streamed Vertex Output buffers, subject to buffer overflow detection. (See the Stream Output section of the 3D pipeline volume).
These registers are part of the context save and restore.

DWord	Bit	Description
0	31:0	**Num Prims Written Count** Format: U32 This count is incremented (by one) every time a GS thread outputs a DataPort Streamed Vertex Buffer Write message with the Increment Num Prims Written bit set in the message header (see the Geometry Shader and Data Port chapters in the 3D Volume.)
1	31:0	**Num Prims Written Count** Format: U32 This count is incremented (by one) every time a GS thread outputs a DataPort Streamed Vertex Buffer Write message with the Increment Num Prims Written bit set in the message header (see the Geometry Shader and Data Port chapters in the 3D Volume.)

Stream Output 2 Primitive Storage Needed Counter

SO2_PRIM_STORAGE_NEEDED - Stream Output 2 Primitive Storage Needed Counter

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	05250h-05257h

There is one 64-bit register for each of the 4 supported streams:
5240h-5247h SO_PRIM_STORAGE_NEEDED0 (for Stream Out Stream #0)
5248h-524Fh SO_PRIM_STORAGE_NEEDED1 (for Stream Out Stream #1)
5250h-5257h SO_PRIM_STORAGE_NEEDED2 (for Stream Out Stream #2)
5258h-525Fh SO_PRIM_STORAGE_NEEDED3 (for Stream Out Stream #3)
These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has or would have written to a particular "stream's" Streamed Vertex Output buffers if all buffers had been large enough to accommodate the writes. (See the Stream Output section of the 3D pipeline volume).
These registers are part of the context save and restore.

DWord	Bit	Description
0	31:0	**Prim Storage Needed Count** Format: U32 This count is incremented (by one) by the SOL stage for each object (point, line, triangle) it writes or attempts to write to the corresponding stream's output buffers. The count is not affected by the actual number of buffers bound to the stream.
1	31:0	**Prim Storage Needed Count** Format: U32 This count is incremented (by one) by the SOL stage for each object (point, line, triangle) it writes or attempts to write to the corresponding stream's output buffers. The count is not affected by the actual number of buffers bound to the stream.

Stream Output 2 Write Offset

SO2_WRITE_OFFSET - Stream Output 2 Write Offset

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	05288h-0528Bh

There is one R/W 32-bit register for each of the 4 supported stream output buffer slots:
5280h-5283h SO_WRITE_OFFSET0 (for Stream Out Buffer #0)
5284h-5287h SO_WRITE_OFFSET1 (for Stream Out Buffer #1)
5288h-528Bh SO_WRITE_OFFSET2 (for Stream Out Buffer #2)
528Ch-528Fh SO_WRITE_OFFSET3 (for Stream Out Buffer #3)
These registers are used to set and track a DWord-granular Write Offset for each of the 4 Stream Output Buffer slots. Software can directly write them via MI_LOAD_REGxxx commands. The SOL stage will increment them as part of stream output processing. Software can cause them to be written to memory via MI_STORE_REGxxx commands. (See the Stream Output section of the 3D pipeline volume).
These registers are part of the context save and restore.

Programming Notes

- Software must ensure that no HW stream output operations can be in process or otherwise pending at the point that the MI_LOAD/STORE commands are processed. This will likely require a pipeline flush.
- The SOL stage will effectively advance the write offset by the buffer's Surface Pitch after each vertex is written (assuming no overflow is detected in any targetted SO buffer). Under "normal" conditions one would expect software to initialize the WriteOffset to some (possibly zero) multiple of Surface Pitch in order to align vertex writes to the buffer's Base Address, though it is not required to do so.

DWord	Bit	Description
0	31:2	**Write Offset** Format: U30 This field contains a DWord offset from the corresponding SO buffer's Base Address value. The SOL stage uses this value as a write offset when performing writes to the buffer. The SOL stage will increment this value as a part of performing stream output to the buffer. Note that the SOL stage uses the buffer's Surface Pitch to advance the Write Offset, without regard to the buffer's Base Address (see Programming Notes above).
	1:0	**Reserved** Format: MBZ

Stream Output 3 Num Primitives Written Counter

SO3_NUM_PRIMS_WRITTEN - Stream Output 3 Num Primitives Written Counter

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	05218h-0521Fh

There is one 64-bit register for each of the 4 supported streams:
5200h-5207h SO_NUM_PRIMS_WRITTEN0 (for Stream Out Stream #0)
5208h-520Fh SO_NUM_PRIMS_WRITTEN1 (for Stream Out Stream #1)
5210h-5217h SO_NUM_PRIMS_WRITTEN2 (for Stream Out Stream #2)
5218h-521Fh SO_NUM_PRIMS_WRITTEN3 (for Stream Out Stream #3)
These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has successfully written to a particular "stream's" Streamed Vertex Output buffers, subject to buffer overflow detection. (See the Stream Output section of the 3D pipeline volume).
These registers are part of the context save and restore.

DWord	Bit	Description
0	31:0	**Num Prims Written Count** Format: U32 This count is incremented (by one) every time a GS thread outputs a DataPort Streamed Vertex Buffer Write message with the Increment Num Prims Written bit set in the message header (see the Geometry Shader and Data Port chapters in the 3D Volume.)
1	31:0	**Num Prims Written Count** Format: U32 This count is incremented (by one) every time a GS thread outputs a DataPort Streamed Vertex Buffer Write message with the Increment Num Prims Written bit set in the message header (see the Geometry Shader and Data Port chapters in the 3D Volume.)

Stream Output 3 Primitive Storage Needed Counter

SO3_PRIM_STORAGE_NEEDED - Stream Output 3 Primitive Storage Needed Counter

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	05258h-0525Fh

There is one 64-bit register for each of the 4 supported streams:
5240h-5247h SO_PRIM_STORAGE_NEEDED0 (for Stream Out Stream #0)
5248h-524Fh SO_PRIM_STORAGE_NEEDED1 (for Stream Out Stream #1)
5250h-5257h SO_PRIM_STORAGE_NEEDED2 (for Stream Out Stream #2)
5258h-525Fh SO_PRIM_STORAGE_NEEDED3 (for Stream Out Stream #3)
These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has or would have written to a particular "stream's" Streamed Vertex Output buffers if all buffers had been large enough to accommodate the writes. (See the Stream Output section of the 3D pipeline volume).
These registers are part of the context save and restore.

DWord	Bit	Description
0	31:0	**Prim Storage Needed Count** Format: U32 This count is incremented (by one) by the SOL stage for each object (point, line, triangle) it writes or attempts to write to the corresponding stream's output buffers. The count is not affected by the actual number of buffers bound to the stream.
1	31:0	**Prim Storage Needed Count** Format: U32 This count is incremented (by one) by the SOL stage for each object (point, line, triangle) it writes or attempts to write to the corresponding stream's output buffers. The count is not affected by the actual number of buffers bound to the stream.

Stream Output 3 Write Offset

SO3_WRITE_OFFSET - Stream Output 3 Write Offset

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0528Ch-0528Fh

There is one R/W 32-bit register for each of the 4 supported stream output buffer slots:
5280h-5283h SO_WRITE_OFFSET0 (for Stream Out Buffer #0)
5284h-5287h SO_WRITE_OFFSET1 (for Stream Out Buffer #1)
5288h-528Bh SO_WRITE_OFFSET2 (for Stream Out Buffer #2)
528Ch-528Fh SO_WRITE_OFFSET3 (for Stream Out Buffer #3)
These registers are used to set and track a DWord-granular Write Offset for each of the 4 Stream Output Buffer slots. Software can directly write them via MI_LOAD_REGxxx commands. The SOL stage will increment them as part of stream output processing. Software can cause them to be written to memory via MI_STORE_REGxxx commands. (See the Stream Output section of the 3D pipeline volume).
These registers are part of the context save and restore.

Programming Notes

- Software must ensure that no HW stream output operations can be in process or otherwise pending at the point that the MI_LOAD/STORE commands are processed. This will likely require a pipeline flush.
- The SOL stage will effectively advance the write offset by the buffer's Surface Pitch after each vertex is written (assuming no overflow is detected in any targetted SO buffer). Under "normal" conditions one would expect software to initialize the WriteOffset to some (possibly zero) multiple of Surface Pitch in order to align vertex writes to the buffer's Base Address, though it is not required to do so.

DWord	Bit	Description
0	31:2	**Write Offset** Format: U30 This field contains a DWord offset from the corresponding SO buffer's Base Address value. The SOL stage uses this value as a write offset when performing writes to the buffer. The SOL stage will increment this value as a part of performing stream output to the buffer. Note that the SOL stage uses the buffer's Surface Pitch to advance the Write Offset, without regard to the buffer's Base Address (see Programming Notes above).
	1:0	**Reserved** Format: MBZ

SubSlice 0 Power Context Save request

PGCTXREQ - SubSlice 0 Power Context Save request

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	24404h

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO Message Mask bots for lower 16 bits
	15:10	**Reserved** Access: RO Reserved
	9	**Power context save request** Access: R/W Set Power Context Save Request 1'b0 : Power context save is not being requested <default> 1'b1 : Power context save is being requested CPUnit self-clears this bit upon sampling.
	8:0	**Power Context Save request crdit count** Access: R/W QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

SubSlice0 Power Down FSM control register with lock

POWERDNFSMCTL - SubSlice0 Power Down FSM control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000088
Size (in bits):	32
Address:	24410h

DWord	Bit	Description
0	31	**power down control Lock** Access: R/W Lock 0 = Bits of POWERDNFSMCTL register are R/W 1 = All bits of POWERDNFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:13	**Reserved** Access: RO Reserved
	12	**Leave firewall disabled** Access: R/W Lock When This bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, i.e dont firewall the gated domain, but complete logical flow
	11	**Leave reset de-asserted** Access: R/W Lock When This bit is set SPC will not assert reset for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e assert resets during power down flows 1 = Leave reset de-asserted mode, i.e dont assert reset, but complete logical flow

POWERDNFSMCTL - SubSlice0 Power Down FSM control register with lock

	10	**Leave CLKs ON** Access: R/W Lock When This bit is set SPC will not gate clks for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e gate clocks during power down flows 1 = Leave CLKS ON mode, i.e dont clock gate, but complete logical flow
	9	**Leave FET On** Access: R/W Lock When This bit is set SPC will not turn off the PFET eventhough it will complete the flow with PM Encodings: 0 = Default mode, i.e power off fets during power down flows 1 = Leave ON mode, i.e dont power off pfet, but complete logical flow Programming note : This bit should be programmed before the powerup sequence is initiated for Slice 0 SSM 0
	8:6	**Power Down state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Gate Clocks
	5:3	**Power Down state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default :Firewall ON

POWERDNFSMCTL - SubSlice0 Power Down FSM control register with lock

	2:0	**Power Down state 1** Default Value: 000b Access: R/W Lock This will be the 1st state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Assert Reset

SubSlice 0 Power Gate Control Request

PGCTLREQ - SubSlice 0 Power Gate Control Request		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	24400h	
Clock Gating Messages Register		
DWord	**Bit**	**Description**
0	31:16	**Message Mask** Access: RO Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:2	**Reserved** Access: RO Reserved
	1	**CLK RST FWE Request** Access: R/W SLICE 0 CLK RST FWE request: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**Power Gate Request** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

SubSlice 0 Power on FSM control register with lock

POWERUPFSMCTL - SubSlice 0 Power on FSM control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000088
Size (in bits):	32
Address:	2440Ch

DWord	Bit	Description
0	31	**power up control Lock** Access: R/W Lock 0 = Bits of POWERUPFSMCTL register are R/W 1 = All bits of POWERUPFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:9	**Reserved** Access: RO Reserved
	8:6	**Power UP state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - De-assert resets 3'b000: 10ns (or 1 bclk)
	5:3	**Power UP state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF

POWERUPFSMCTL - SubSlice 0 Power on FSM control register with lock

		010 = De-assert resets 1xx = Rsvd for future Default - Firewall OFF
	2:0	**Power UP state 1** Default Value: 000b Access: R/W Lock This will be the 1st state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Clock Ungate

Subsystem Identification

SID2_0_2_0_PCI - Subsystem Identification

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	16
Address:	0002Eh

This register is used to uniquely identify the subsystem where the PCI device resides.

DWord	Bit	Description
0	15:0	**Subsystem Identification** Default Value: 0000000000000000b Access: R/W Once This value is used to identify a particular subsystem. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.

Subsystem Vendor Identification

SVID2_0_2_0_PCI - Subsystem Vendor Identification

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	16
Address:	0002Ch

This register is used to uniquely identify the subsystem where the PCI device resides.

DWord	Bit	Description
0	15:0	**Subsystem Vendor ID** Default Value: 0000000000000000b Access: R/W Once This value is used to identify the vendor of the subsystem. This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.

Super Queue GFX cycle Options register

SQCFG - Super Queue GFX cycle Options register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000180
Size (in bits):	32
Address:	0902Ch

Super Queue GFX Cycle Options register

DWord	Bit	Description
0	31:10	**Reserved** Access: RO
	9:3	**SQ Full Limit for Performance Monitor** Default Value: 0110000b Access: R/W Watermark for SQ Full Metrics This field sets a watermark where any SQ level above is considered as SQ FULL condition. This is added to compensate for the credit loop between the page walker and GTI which would make the number of active entries oscillate even the pipeline is backed up towards page walker. Range of allowed progamming is 0-64. Default is 48.
	2	**SQ Read-Only Port Reject Disable** Access: R/W This indicates whether rejections can be issued from the Super Queue to GFX for read cycles on the Read Only port. Rejected cycles are retried at a later time by GFX. By default, read cycles that have a matching address elsewhere in the Super Queue are rejected, and GFX is notified of the rejection. If this bit is set, no rejections ever occur on the SQ-GFX interface. SQ accepts all requests, but in the case of a matching address, the SQ stalls the Read-Only port until the address match disappears (matching entry is retired by SQ). 1 = Rejections are disabled, SQ stalls if needed. 0 = Rejections are enabled.
	1	**SQ Read Port GFX Read Ownership** Access: R/W SQ Read Port GFX Read Ownership (SQRWO): SQ Read-Only Port GFX Read Ownership Indication. This indicates the type of request that is issued to uncore for each read cycle from the GFX Read-Only port which produces a miss in the MLC. By default, read cycles that have no matching MLC entry produce a regular read request from uncore through the IDI. If this bit is set, the request is changed from a regular read to a

SQCFG - Super Queue GFX cycle Options register

		request for ownership (RFO) of the cacheline. This applies for all read requests from the GFX Read-Only port ONLY. 1 = All GFX reads from RO port require ownership of the cacheline. 0 = GFX reads from RO port do.
	0	**MSQD Poisoned Writes Propagation Enable** Access: R/W 0: POISON propagation disabled i.e. MSQD always drives 0 to BGF (default mode). 1: POISON propagation enabled. Poison bit from writes are passed out to BGF.

Super Queue Internal Cnt Register I

SQCNT1 - Super Queue Internal Cnt Register I

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	09024h

SQ Internal Counter Register

DWord	Bit	Description
0	31:24	**RSVD** Access: RO
	23:20	**SQRWCQD** Access: R/W Read-Write Request Queue Command Get Delay: This indicates the number of clocks that are inserted between each GFX cycle being accepted on the GFX Read or GFX Write ports. By default, this is disabled, which means that the RWRQ is able to accept one cycle per clock. By any other value, the RWRQ inserts the number of idle clocks listed in this register before accepting another cycle from GFX, essentially throttling the bandwidth. During each idle clock, RWRQ is guaranteed not to assert its command get to either read or write port. 0000b = Disabled (no additional clocks added). 0001b = One idle clock inserted between command gets. 0010b = Two idle clocks inserted between command gets. ... 1111b = Fifteen idle clocks inserted between command gets.
	19:16	**SQCQD** Access: R/W Read-Only Request Queue Command Get Delay: This indicates the number of clocks that are inserted between each GFX cycle being accepted on the GFX Read-Only port. By default, this is disabled, which means that the RORQ will be able to accept one cycle per clock. By any other value, the RORQ inserts the number of idle clocks listed in this register before accepting another cycle from GFX, essentially throttling the bandwidth. During each idle clock, RORQ is guaranteed not to assert its command get. 0000b = Disabled (no additional clocks added). 0001b = One idle clock inserted between command gets. 0010b = Two idle clocks inserted between command gets. ... 1111b = Fifteen idle clocks inserted between command gets.

SQCNT1 - Super Queue Internal Cnt Register I

	15:10	**SQDPTH** Access: R/W Super Queue Depth: This indicates the maximum number of cycles supported at any given time by Super Queue. By default, this is 64, which is the maximum size of the Super Queue, but can be throttled back to support fewer GFX cycles. Note: By limiting the depth of the super queue, effectively the recycle queue limits the SQIDs that are allowed to be used. 3Fh = SQ Depth of 63. 3Eh = SQ Depth of 62. ... 07h = SQ Depth of 7. 06h = SQ Depth of 6. 05h = SQ Depth of 5. 04h = SQ Depth of 4. 03h = SQ Depth of 3. 02h = SQ Depth of 2. 01h = Reserved. 00h = Disabled (SQ Depth of 64) (default).
	9	**RSVD** Access: RO
	8:6	**Reserved**
	5:0	**SQIDICNT** Access: R/W Outstanding SQ IDI Cycle Counter: This indicates the maximum number of outstanding cycles that are presented to IDI/uncore at any given time by Super Queue. By default, this is 64, but can be throttled back to support fewer IDI cycles. 0 = Disabled (64). 1-63 = Max number of outstanding IDI cycles.

Super Queue Internal Counters Register II

SQCNT2 - Super Queue Internal Counters Register II

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	09028h

Super Queue Internal Counter register

DWord	Bit	Description
0	31:30	**Reserved** Access: RO
	29	**Enable Promotion on Read** Access: R/W Enable Promotion on Read Match: Enable the promotion of write request if matched with a Read request.
	28	**Priority 3 Pool Count Disable** Access: R/W Priority3 Pool Count Disable: When set, priority3 pool becomes unlimited. And priority3 pool count value should not be used in reset of the remaining counters.
	27:25	**Priority3 Pool Count:** Access: R/W Priority3 Pool Count: The count of cycles is selected from priority3 pool before switching to lower priority pools. Count is used as the power of 2. 000b: 1 request 001b: 2 requests 010b: 4 requests 011b: 8 requests ... 111b: 128 requests
	24	**Priority2 Pool Count Disable** Access: R/W Priority2 Pool Count Disable: When set, priority2 pool becomes unlimited. And priority2 pool count value should not be used in reset of the remaining counters.

SQCNT2 - Super Queue Internal Counters Register II

23:21	**Priority2 Pool count** Access: R/W Priority2 Pool Count: The count of cycles is selected from priority2 pool before switching to lower priority pools. Count is used as the power of 2. 000: 1 request 001: 2 requests 010: 4 requests 011: 8 requests ... 111: 128 requests
20	**Priority1 Pool Count Disable** Access: R/W Priority1 Pool Count Disable: When set, priority1 pool becomes unlimited. And priority1 pool count value should not be used in reset of the remaining counters.
19:17	**Priority1 Pool Count** Access: R/W Priority1 Pool Count: The count of cycles is selected from priority1 pool before switching to lower priority pools. Count is used as the power of 2. 000: 1 request 001: 2 requests 010: 4 requests 011: 8 requests ... 111: 128 requests
16	**Priority0 Pool Count Disable** Access: R/W Priority0 Pool Count Disable: When set, priority0 pool becomes unlimited. And priority0 pool count value should not be used in reset of the remaining counters.
15:13	**Priority0 Pool Count** Access: R/W Priority0 Pool Count: The count of cycles is selected from priority0 pool before switching to lower priority pools. Count is used as the power of 2. 000: 1 request 001: 2 requests 010: 4 requests 011: 8 requests

SQCNT2 - Super Queue Internal Counters Register II

		... 111: 128 requests
	12	**Enable Priority Selection** Access: R/W Enable Priority Selection: Enables the use of priority bits coming from GFX core. If disabled, all slots in SQ are treated as same peiority 0b: Disabled (default). 1b: Enabled.
	11:8	**Reserved**
	7:0	**LRU Hint counter** Access: RO Reserved

SWF

SWF	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	4F000h-4F08Fh
Name:	Software Flags
ShortName:	SWF_*
Power:	PG0
Reset:	soft

These registers are used as scratch pad data storage space and have no direct effect on hardware operation. There are 36 instances of this register format.

DWord	Bit	Description
0	31:0	**Software Flags** Software flags

Thread Dispatched Count Register

TDL_THR_DISP_COUNT - Thread Dispatched Count Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	0E4BCh

This register provides the count of threads dispatched/valid in the subslice.

DWord	Bit	Description
0	31:6	**Reserved** Format: MBZ
	5:0	**Thread Count** Value: 0-56 — Name: Valid Range

Thread Faulted Count Register

TDL_THR_PF_COUNT - Thread Faulted Count Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	0E5BCh

This register provides the count of threads faulted in each subslice.

DWord	Bit	Description
0	31	**Canonical fault indication bit to CS** The bit is set when a canonical fault on data fetch is reported by EU.
	30:6	**Reserved** Format: MBZ
	5:0	**Thread Count** Value: 0-56 — Name: Valid Range

Thread Fault Status Register 0

TDL_THR_PF_STATUS0 - Thread Fault Status Register 0	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	0E6B8h

This register provides the status of each thread in the SubSlice. A bit set indicates the thread in the specific thread slot is faulted.

DWord	Bit	Description
0	31:24	**Row0, EU3, [Reserved, T6-T0]**
	23:16	**Row0, EU2, [Reserved, T6-T0]**
	15:8	**Row0, EU1, [Reserved, T6-T0]**
	7:0	**Row0, EU0, [Reserved, T6-T0]**

Thread Fault Status Register 1

TDL_THR_PF_STATUS1 - Thread Fault Status Register 1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	0E7B8h

This register provides the status of each thread in the SubSlice. A bit set indicates the thread in the specific thread slot is faulted.

DWord	Bit	Description
0	31:24	**Row1, EU3, [Reserved, T6-T0]**
	23:16	**Row1, EU2, [Reserved, T6-T0]**
	15:8	**Row1, EU1, [Reserved, T6-T0]**
	7:0	**Row1, EU0, [Reserved, T6-T0]**

Thread Load Status Register 0

TDL_THR_STATUS0 - Thread Load Status Register 0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Address:	0E4B8h	
This register provides the status of each thread in the SubSlice.		
DWord	**Bit**	**Description**
0	31:24	**Row0, EU3, [Reserved, T6-T0]**
	23:16	**Row0, EU2, [Reserved, T6-T0]**
	15:8	**Row0, EU1, [Reserved, T6-T0]**
	7:0	**Row0, EU0, [Reserved, T6-T0]**

Thread Load Status Register 1

TDL_THR_STATUS1 - Thread Load Status Register 1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	0E5B8h

This register provides the status of each thread in the SubSlice. A bit set indicates a valid thread is loaded in the thread slot.

DWord	Bit	Description
0	31:24	**Row1, EU3, [Reserved, T6-T0]**
	23:16	**Row1, EU2, [Reserved, T6-T0]**
	15:8	**Row1, EU1, [Reserved, T6-T0]**
	7:0	**Row1, EU0, [Reserved, T6-T0]**

Thread Mode Register

FF_MODE - Thread Mode Register

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x24A00000
Access:	R/W
Size (in bits):	32
Address:	020A0h

This register is used to program the FF shader Mode.

DWord	Bit	Description
0	31	**TE Autostrip Disable** Format: U1 Value / Name / Description: 0h / Enable **[Default]** / TE will generate "autostrip" primitives (if/where possible) during tessellation. 1h / Disable / TE will not generate "autostrip" primitives.
	30	**TDS external Cache Disable** Value / Name / Description: 0b / Enable **[Default]** / The external TDS Cache is enabled if there is enough handles to enable the cache. 1b / Disable / The external TDS Cache is disabled even if there is enough handles to enable the cache. Only the internal TDS Cache will be used.
	29:26	**DS Hit Max Value** Format: U4 Description: If the number of hits reaches the DS Hit Max Value and there is a pending miss to be dispatched, the DS will dispatch the pending miss vertex as a single dispatch. Since DS Reference Count Full Force miss enable was removed, the value can be [1,15]. Value / Name: 9 / **[Default]** [1,15] /
	25:20	**VS Hit Max Value** Format: U6

FF_MODE - Thread Mode Register

Description
If the number of hits reaches the VS Hit Max Value and there is a pending miss to be dispatched, the VS will dispatch the pending miss vertex as a single dispatch.
Since VS Reference Count Full Force miss enable was removed, the value can be [1,63].

Value	Name
10	**[Default]**
[1,63]	

19 Tessellation DOP gating Disable

Format:	Disable

Value	Name	Description
0h	Enable **[Default]**	HS, TE, TETG, DS, GS and SOL units are DOP gated if all units are disabled
1h	Disable	DOP gating is disabled for HS, TE, TETG, DS, GS and SOL units

Programming Notes
Once this bit is set to a 1, it must not be cleared to a 0 until after a reset.

18 Reserved

Format:	MBZ

17:16 Reserved

Format:	PBC

15 TDS Bypass Disable

Format:	Disable

Value	Name	Description
0h	Enable **[Default]**	Domain Shader logic is bypassed while TDS is disabled
1h	Disable	Domain Shader bypass logic is disabled

14:13 Reserved

Format:	PBC

12 Reserved

Default Value:	0h
Format:	PBC

11:7 Reserved

Format:	PBC

6:5 Reserved

Format:	PBC

FF_MODE - Thread Mode Register

	4	**Reserved** Default Value: 0h Format: PBC
	3	**Reserved** Format: PBC
	2	**Reserved** Format: PBC
	2	**TDS Tracking fifo wrap fix disable** Format: Disable **Value** / **Name** / **Description** 1h / / Disable the tds tracking fifo wrap fix. 0h / **[Default]** / Enable the tds tracking fifo wrap fix.
	1	**Reserved** Format: PBC
	0	**Reserved** Format: PBC

Thread Restart Control Register

TDL_THR_RESTART - Thread Restart Control Register		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	WO	
Size (in bits):	32	
Address:	0E450h	
This register provides control to restart page faulted and halted threads in each subslice.		
DWord	**Bit**	**Description**
0	31:1	**Reserved** Format: MBZ
	0	**Restart All Faulted Threads** A write of 1 to this register restarts all threads that have halted due to page fault.

THREADS ALLOCATED PER SUBSLICE

EUMETRICS_EVENT2 - THREADS ALLOCATED PER SUBSLICE	
Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	00D94h

This register mirrors an accumulating count for EU Metric Event2.
It is enabled by configuration bits in GPMunit and SPMunits.
Note that count is never cleared and delta should be calculated by sampling the initial register value at the start and subtracting that value off from the final sample value.

DWord	Bit	Description
0	31:0	**EU Metric Event Count** Access: RO

TiledResources Invalid Tile Detection Register

TRINVTILEDETCT - TiledResources Invalid Tile Detection Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04DECh

DWord	Bit	Description
0	31:0	**Invalid Tile Detection Value** Default Value: 00000000h Access: R/W A 32bit value programmed to enable h/w to perform a match of TR-VA TT entries to detect Invalid Tiles. Hardware will flag each entry and space behind it as Invalid Tile for matched entries.

TiledResources Null Tile Detection Register

TRNULLDETCT - TiledResources Null Tile Detection Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04DE8h

DWord	Bit	Description
0	31:0	**Null Tile Detection Value** Default Value: 00000000h Access: R/W A 32bit value programmed to enable h/w to perform a match of TR-VA TT entries to detect Null Tiles. Hardware will flag each entry and space behind it as Null Tile for matched entries.

Tiled Resources Translation Table Control Register

TRTTE - Tiled Resources Translation Table Control Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04DF4h

DWord	Bit	Description
0	31:2	**Reserved** Default Value: 00000000000000000000000000000000b Access: RO Reserved
	1	**TR-VA Translation Table Memory Location** Default Value: 0b Access: R/W This fields specifies whether the translation tables for TR-VA to VA are in virtual address space vs physical (GPA) address space. 0: Tables are in Physical (GPA) Space 1: Tables are in Virtual Address Space
	0	**TR - TT Enable** Default Value: 0b Access: R/W TR translation tables are disabled as default. This field needs to be enabled via s/w to get TR translation active.

Tiled Resources Translation Table Control Registers

TRTTCR - Tiled Resources Translation Table Control Registers

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	8
Address:	04DF4h
Name:	Tiled Resources Translation Table Control Register
ShortName:	TRTTE

DWord	Bit	Description
0	1	**TR-VA Translation Table Memory Location** Default Value: 0b Access: R/W This field specifies whether the translation tables for TR to VA are in virtual address space v/s physical (GPA) address space. 0: Tables are in Physical (GPA) space 1: Tables are in Virtual address space **Tiled Resource Translation Tables in GPA space is not supported in any GEN generations. For Gen9, this mode should never be set as GPA mode (always set to '1).**
	0	**TR - TT Enable** Default Value: 0b Access: R/W TR translation tables are disabled as default. This field needs to be enabled via s/w to get TR translation active.

TiledResources VA Detection Registers

TRVADR - TiledResources VA Detection Registers

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04DF0h

DWord	Bit	Description
0	31:8	**Reserved** Default Value: 000000h Access: RO Reserved
	7:4	**TR - VA Mask Value** Default Value: 0000b Access: R/W 4bit MASK value that is mapped to incoming address bits[47:44]. MASK bits are used to identify which address bits need to be considered for compare. If particular mask bit is "1", mapping address bit needs to be compared to DATA value provided. If "0", corresponding address bit is masked which makes it don't care for compare (this field defaults to "0000" to disable detection) Note: The only usage model for GFX driver to set this field to "1111". Behavior of h/w for any other setting is not defined Note: GFX driver shall use same TRVA MASK value for all contexts
	3:0	**TR - VA Data Value** Default Value: 0000b Access: R/W 4bit Data value that is mapped to incoming address bits[47:44]. Data bits are used to compare address values that are not filtered by the TRVAMV for match Note: GFX driver shall use same TRVA Data value for all contexts

TiledResources VA Transln Table L3 ptr - DW0

TRVATTL3PTRDW0 - TiledResources VA Transln Table L3 ptr - DW0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04DE0h

DWord	Bit	Description
0	31:12	**TR - VA transln Table L3 Pointer (Lower Address)** Default Value: 00000h Access: R/W Lower address bits for tiled resource VA to virtual address translation L3 table
	11:0	**Reserved** Default Value: 000h Access: RO Reserved

TiledResources VA Transln Table L3 ptr- DW1

TRVATTL3PTRDW1 - TiledResources VA Transln Table L3 ptr- DW1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04DE4h

DWord	Bit	Description
0	31:16	**Reserved** Default Value: 0000h Access: RO Reserved
	15:0	**TR - VA transln Table L3 Pointer (Upper Address)** Default Value: 0000h Access: R/W Upper address bits for tiled resource VA to virtual address translation L3 table

Tiled Resources Wrapper Write Data Port arbitration

TRWRPARB - Tiled Resources Wrapper Write Data Port arbitration

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00001089
Size (in bits):	32
Address:	04DF8h

DWord	Bit	Description
0	31:13	**Reserved** Default Value: 0000000000000000000b Access: R/W Reserved
	12:10	**L3 Max Write Request Limit Count** Default Value: 100b Access: R/W This is the MAX number of Allowed writes from L3 before switching the priority to Z Requests Count - Minimum count value must be = 1
	9	**Reserved** Default Value: 0b Access: R/W Reserved
	8:6	**Z Max Write Request Limit Count** Default Value: 010b Access: R/W This is the MAX number of Allowed writes from Z before switching the priority to C Requests Count - Minimum count value must be = 1
	5	**Reserved** Default Value: 0b Access: R/W Reserved

TRWRPARB - Tiled Resources Wrapper Write Data Port arbitration

	4:2	**C Max Write Request Limit Count** Default Value: 010b Access: R/W This is the MAX number of Allowed writes from C before switching the priority to L3 Requests Count - Minimum count value must be = 1
	1	**Reserved** Default Value: 0b Access: R/W Reserved
	0	**Fixed Arbitration enable** Default Value: 1b Access: R/W Fixed Arbitration enable when 1'b1 Programmable Arbitration when 1'b0

TIMESTAMP_CTR

TIMESTAMP_CTR	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/WC
Size (in bits):	32
Address:	44070h-44073h
Name:	Time Stamp Counter
ShortName:	TIMESTAMP_CTR
Power:	PG0
Reset:	global

The register is not reset by a FLR.

DWord	Bit	Description
0	31:0	**TIMESTAMP Counter** This field increments every microsecond. The value in this field is latched in the Pipe Flip TIMESTAMP registers when flips occur, and in the Pipe Frame TIMESTAMP registers at start of vertical blank. The register value will reset if any value is written to it. The register is not reset by a FLR.

TLB_RD_ADDRESS Register

TLB_RD_ADDR - TLB_RD_ADDRESS Register		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B00h	
DWord	**Bit**	**Description**
0	31:12	**Reserved** Default Value: 00000000000000000000b Access: RO
	11:0	**Reserved**

TLB_RD_DATA0 Register

TLB_RD_DATA0 - TLB_RD_DATA0 Register		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B04h	
DWord	**Bit**	**Description**
0	31:0	**TLB_READ_DATA0 Register** Default Value: 00000000h Access: RO address [43:12]

TLB_RD_DATA1 Register

TLB_RD_DATA1 - TLB_RD_DATA1 Register		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B08h	
DWord	**Bit**	**Description**
0	31:0	**TLB_READ_DATA1 Register** Default Value: 00000000h Access: RO Bit[31:5] Reserved Bit[4] Cycle GTT SEL (1-GGTT Cycle, 0-PPGTT Cycle) Bit[3:0] address [47:44]

TOUCH_MSG_ADDR

TOUCH_MSG_ADDR	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	45020h-45027h
Name:	Touch Message Address
ShortName:	TOUCH_MSG_ADDR_*
Power:	PG0
Reset:	soft

DWord	Bit	Description
0 0x45020	31:0	**Touch MSG Address** This field specifies the address bits 31:0 for the Display to PCH touch controller messages. **Restriction** Restriction : The address must be DWord aligned.
1 0x45024	31:8	**Reserved** Format: MBZ
	7:0	**Touch MSG Address Upper** This field specifies the address bits 39:32 for the Display to PCH touch controller messages.

TRANS_CLK_SEL

TRANS_CLK_SEL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	46140h-46143h
Name:	Transcoder A Clock Select
ShortName:	TRANS_CLK_SEL_A
Power:	PG0
Reset:	soft
Address:	46144h-46147h
Name:	Transcoder B Clock Select
ShortName:	TRANS_CLK_SEL_B
Power:	PG0
Reset:	soft
Address:	46148h-4614Bh
Name:	Transcoder C Clock Select
ShortName:	TRANS_CLK_SEL_C
Power:	PG0
Reset:	soft

Description
This register maps the port clock to the transcoder. There is one instance of this register format per transcoder A/B/C.

DWord	Bit	Description
0	31:29	**Trans Clock Select** Select which PLL to use for this transcoder. Trancoder EDP always uses DDIA clock.

Value	Name	Description
000b	None	No PLL selected. Clock is disabled for this transcoder.
010b	DDIB	Select DDIB clock
011b	DDIC	Select DDIC clock
100b	DDID	Select DDID clock.
101b	DDIE	Select DDIE clock
Others	Reserved	Reserved

TRANS_CLK_SEL		
		Restriction Restriction : This must not be changed while the transcoder is enabled.
	28:0	**Reserved**

TRANS_CONF

TRANS_CONF		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	Double Buffered	
Size (in bits):	32	
Double Buffer Update Point:	Start of vertical blank (WD cap sync) OR transcoder disabled	
Address:	70008h-7000Bh	
Name:	Transcoder A Configuration	
ShortName:	TRANS_CONF_A	
Power:	PG2	
Reset:	soft	
Address:	71008h-7100Bh	
Name:	Transcoder B Configuration	
ShortName:	TRANS_CONF_B	
Power:	PG2	
Reset:	soft	
Address:	72008h-7200Bh	
Name:	Transcoder C Configuration	
ShortName:	TRANS_CONF_C	
Power:	PG2	
Reset:	soft	
Address:	7E008h-7E00Bh	
Name:	Transcoder WD0 Configuration	
ShortName:	TRANS_CONF_WD0	
Power:	PG2	
Reset:	soft	
Address:	7F008h-7F00Bh	
Name:	Transcoder EDP Configuration	
ShortName:	TRANS_CONF_EDP	
Power:	PG1	
Reset:	soft	
DWord	**Bit**	**Description**

TRANS_CONF

0	31	**Transcoder Enable** Setting this bit to the value of one, turns on this transcoder. Turning the transcoder off disables the timing generator and synchronization pulses to the display will not be maintained. Enabling the transcoder may be internally delayed for one frame while the display data buffers are re-configured. **Value** / **Name** 0b – Disable 1b – Enable **Restriction** Restriction : Timing registers must contain valid values before this bit is enabled.
	30	**Transcoder State** Access: RO This read only bit indicates the actual state of the transcoder. **Value** / **Name** 0b – Disabled 1b – Enabled
	29:23	**Reserved**
	22:21	**Interlaced Mode** These bits control the transcoder interlaced mode. This field is ignored by WD. **Value** / **Name** / **Description** 00b – PF-PD – Progressive Fetch with Progressive Display 01b – PF-ID – Progressive Fetch with Interlaced Display 11b – IF-ID – Interlaced Fetch with Interlaced Display Others – Reserved – Reserved **Restriction** Restriction : VGA display modes do not work while in interlaced fetch mode. Progressive Fetch with Interlaced Display effectively down scales the vertical by 2X, which reduces the maximum supported pixel rate by half. Restriction : Progressive Fetch with Interlaced Display requires the pipe scaler to be functioning with the 7x5 filter. Restriction : Interlaced fetch mode is not supported with Y Tiling. Interlaced fetch mode is not supported with 90/270 rotation. Interlaced fetch mode is not supported with scaling. Interlaced fetch mode is not supported with YUV 420 hybrid planar source pixel formats.

TRANS_CONF		
	20:7	**Reserved** Format: MBZ
	6:0	**Reserved** Format: MBZ

TRANS_DDI_FUNC_CTL

TRANS_DDI_FUNC_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00030000
Access:	R/W
Size (in bits):	32
Address:	60400h-60403h
Name:	Transcoder A DDI Function Control
ShortName:	TRANS_DDI_FUNC_CTL_A
Power:	PG2
Reset:	soft
Address:	61400h-61403h
Name:	Transcoder B DDI Function Control
ShortName:	TRANS_DDI_FUNC_CTL_B
Power:	PG2
Reset:	soft
Address:	62400h-62403h
Name:	Transcoder C DDI Function Control
ShortName:	TRANS_DDI_FUNC_CTL_C
Power:	PG2
Reset:	soft
Address:	6F400h-6F403h
Name:	Transcoder EDP DDI Function Control
ShortName:	TRANS_DDI_FUNC_CTL_EDP
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31	**TRANS DDI Function Enable** This bit enables the transcoder DDI function. Value / Name: 0b – Disable 1b – Enable
	30:28	**DDI Select** These bits determine which DDI port this transcoder will connect to. It is not valid to enable and direct more than one transcoder to one DDI, except when using

TRANS_DDI_FUNC_CTL

DisplayPort multistreaming.
These bits are ignored by transcoder EDP since it can only connect to DDI A (EDP DDI).

Value	Name	Description
000b	None	No port connected
001b	DDI B	DDI B
010b	DDI C	DDI C
011b	DDI D	DDI D
100b	DDI E	DDI E
Others	Reserved	Reserved

Restriction
Restriction : This field must not be changed while the function is enabled.

27 **Reserved**

Format:	MBZ

26:24 **TRANS DDI Mode Select**
This field determines the mode of operation.
HDMI mode enables a null packet (32 bytes of a value of 0) to be sent when Vsync=1, and also enables preambles and guardbands prior to the null packets, in accordance with the HDMI specification.
DVI mode will function as HDMI if DIP packets or audio are enabled.

Value	Name	Description
000b	HDMI	Function in HDMI mode
001b	DVI	Function in DVI mode
010b	DP SST	Function in DisplayPort SST mode
011b	DP MST	Function in DisplayPort MST mode
Others	Reserved	Reserved

Restriction
Restriction : This field must not be changed while the function is enabled. The DisplayPort mode (SST or MST) selected here must match the mode selected in the DisplayPort Transport Control register for the transport attached to this transcoder. Transcoder EDP and DDI A can only function in DP SST mode.

23 **Reserved**

Format:	MBZ

22:20 **Bits Per Color**
This field selects the number of bits per color output on the DDI connected to this transcoder. Dithering should be enabled when selecting a pixel color depth higher or lower than the pixel color depth of the frame buffer.

Value	Name	Description

TRANS_DDI_FUNC_CTL

000b	8 bpc	
001b	10 bpc	
010b	6 bpc	
011b	12 bpc	
Others	Reserved	Reserved

Restriction
Restriction : This field must not be changed while the function is enabled.
Restriction : 10bpc not supported with HDMI.
Restriction : 6bpc not supported with HDMI.

19:18 **Port Sync Mode Master Select**

This field indicates which transcoder will be the master to this transcoder when in port sync mode. This bit is ignored by transcoder EDP since it cannot be slaved to another port.

Value	Name
00b	Transcoder EDP
01b	Transcoder A
10b	Transcoder B
11b	Transcoder C

Restriction
Restriction : A port cannot be slaved to itself.

17:16 **Sync Polarity**

This field indicates the polarity of Hsync and Vsync.

Value	Name	Description
00b	Low	VS and HS are active low (inverted)
01b	VS Low, HS High	VS is active low (inverted), HS is active high
10b	VS High, HS Low	VS is active high, HS is active low (inverted)
11b	High **[Default]**	VS and HS are active high

15 **Port Sync Mode Enable**

This field enables the DisplayPort SST port sync mode on this transcoder. This mode forces two or more transcoders to be in sync with one transcoder master and one or more transcoder slaves. The master is unaware that it is operating in this mode. Only the slave is aware that it is operating in this mode. Port sync mode is only enabled in the slave transcoder. This bit is ignored by transcoder EDP since it cannot be slaved to another port.

Value	Name
0b	Disable
1b	Enable

TRANS_DDI_FUNC_CTL

Restriction
Restriction : Follow the instructions for enabling and disabling Sync Mode in the Display Mode Set Sequence - Sequence for DisplayPort. Port Sync Mode must only be enabled with DisplayPort SST. Port Sync Mode Master Select must be programmed with a valid value when Port sync Mode is enabled. The slave and master transcoders and associated ports must have identical parameters and properties. They must be connected to the same PLL, have the same color format, link width (number of lanes enabled), resolution, refresh rate, dot clock, TU size, M and N programming, etc.

14:12 EDP Input Select

These bits determine the input to transcoder EDP. These bits are ignored by transcoders A/B/C.

Value	Name	Description
000b	A - Always On	Pipe A through the always on power well.
101b	B - On/Off	Pipe B through the on/off power well.
110b	C - On/Off	Pipe C through the on/off power well.
Others	Reserved	Reserved

Restriction
Restriction : This field must not be changed while the function is enabled. It is not valid to have the same pipes driving multiple enabled transcoders.

11:10 Reserved

Format:	MBZ

9 Reserved

8 DP VC Payload Allocate

This bit enables DisplayPort Virtual Channel payload allocation. This bit is ignored by transcoder EDP since it does not support multistreaming.

Value	Name
0b	Disable
1b	Enable

7:6 Reserved

Format:	MBZ

5 Reserved

4 Reserved

Format:	MBZ

3:1 DP Port Width Selection

Description
This bit selects the number of lanes to be enabled on the DDI link for DisplayPort.

TRANS_DDI_FUNC_CTL

This field is ignored for HDMI and DVI which always use all 4 lanes.

Value	Name	Description
000b	x1	x1 Mode
001b	x2	x2 Mode
011b	x4	x4 Mode Restriction : Not allowed with DDI-E, some restrictions with DDI-A
Others	Reserved	Reserved

Restriction
Restriction : When in DisplayPort mode the value selected here must match the value selected in the DDI Buffer Control register for the DDI attached to this pipe.
Restriction : This field must not be changed while the DDI is enabled.
Restriction : DDI E only supports x1 and x2 when DDI_BUF_CTL_A DDIA Lane Capability Control is set to DDIA x2, otherwise DDI E is not supported. DDI A (EDP) supports x1, x2, and x4 when DDI_BUF_CTL_A DDIA Lane Capability Control is set to DDIA x4, otherwise DDI A only supports x1 and x2.

0 **Reserved**

Format:	MBZ

TRANS_FRM_TIME

TRANS_FRM_TIME

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6E020h-6E023h
Name:	Transcoder WD0 Frame Time
ShortName:	TRANS_FRM_TIME_WD0
Power:	PG2
Reset:	soft

This register is only for WD transcoders.

Programming Notes

Examples: For 60Hz the frame time is 16,666.66us, program integer 16,665 and fraction 2/3. For 24Hz the frame time is 41,666.66us, program integer 41,665 and fraction 2/3. For 59.94Hz the frame time is 16,683.33us, program integer 16,682 and fraction 1/3.

Restriction

Restriction : This register should not be changed while the transcoder or port are enabled.

DWord	Bit	Description
0	31:16	**Frame Time Integer** This field specifies the integer portion of the time in microseconds for a display frame. This is used to determine the rate at which to generate frames when capturing display. This field is programmed to the integer number of microseconds desired minus one. **Restriction** Restriction : A value of 0 is invalid when the transcoder is enabled.
	15:14	**Frame Time Fraction** This field specifies the fractional portion of the time in microseconds for a display frame. This is used to determine the rate at which to generate frames when capturing display. Value / Name: 00b: 0 01b: 1/3 10b: 2/3 Others: Reserved
	13:0	**Reserved**

TRANS_HBLANK

TRANS_HBLANK	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	60004h-60007h
Name:	Transcoder A Horizontal Blank
ShortName:	TRANS_HBLANK_A
Power:	PG2
Reset:	soft
Address:	61004h-61007h
Name:	Transcoder B Horizontal Blank
ShortName:	TRANS_HBLANK_B
Power:	PG2
Reset:	soft
Address:	62004h-62007h
Name:	Transcoder C Horizontal Blank
ShortName:	TRANS_HBLANK_C
Power:	PG2
Reset:	soft
Address:	6F004h-6F007h
Name:	Transcoder EDP Horizontal Blank
ShortName:	TRANS_HBLANK_EDP
Power:	PG1
Reset:	soft

There is one instance of this register for each transcoder A/B/C/EDP.

Restriction
Restriction : This register should not be changed while the transcoder or port are enabled.

DWord	Bit	Description
0	31:29	**Reserved**
	28:16	**Horizontal Blank End** This field specifies Horizontal Blank End position relative to the horizontal active display start. **Restriction**

TRANS_HBLANK		
		Restriction : The minimum horizontal blank size is 32 pixels. For HDMI Audio transmission the minimum is 138 pixels. This register must always be programmed to the same value as the Horizontal Total.
	15:13	**Reserved**
	12:0	**Horizontal Blank Start** This field specifies the Horizontal Blank Start position relative to the horizontal active display start. **Restriction** Restriction : This register must always be programmed to the same value as the Horizontal Active.

TRANS_HSYNC

TRANS_HSYNC	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	60008h-6000Bh
Name:	Transcoder A Horizontal Sync
ShortName:	TRANS_HSYNC_A
Power:	PG2
Reset:	soft
Address:	61008h-6100Bh
Name:	Transcoder B Horizontal Sync
ShortName:	TRANS_HSYNC_B
Power:	PG2
Reset:	soft
Address:	62008h-6200Bh
Name:	Transcoder C Horizontal Sync
ShortName:	TRANS_HSYNC_C
Power:	PG2
Reset:	soft
Address:	6F008h-6F00Bh
Name:	Transcoder EDP Horizontal Sync
ShortName:	TRANS_HSYNC_EDP
Power:	PG1
Reset:	soft

Description
There is one instance of this register for each transcoder A/B/C/EDP.

Restriction
Restriction : This register should not be changed while the transcoder or port are enabled.

DWord	Bit	Description	
0	31:29	**Reserved**	
		Format:	MBZ

TRANS_HSYNC		
	28:16	**Horizontal Sync End** This field specifies the Horizontal Sync End position relative to the horizontal active display start. It is programmed with HorizontalActive+FrontPorch+Sync-1 **Restriction** Restriction : This value must be greater than the horizontal sync start and less than Horizontal Total.
	15:13	**Reserved** Format: MBZ
	12:0	**Horizontal Sync Start** This field specifies the Horizontal Sync Start position relative to the horizontal active display start. It is programmed with HorizontalActive + FrontPorch - 1 **Restriction** Restriction : This value must be greater than Horizontal Active. In HDMI modes the minimum gap between horizontal blank start and horizontal sync start is 16 pixels.

TRANS_HTOTAL

TRANS_HTOTAL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	60000h-60003h
Name:	Transcoder A Horizontal Total
ShortName:	TRANS_HTOTAL_A
Power:	PG2
Reset:	soft
Address:	61000h-61003h
Name:	Transcoder B Horizontal Total
ShortName:	TRANS_HTOTAL_B
Power:	PG2
Reset:	soft
Address:	62000h-62003h
Name:	Transcoder C Horizontal Total
ShortName:	TRANS_HTOTAL_C
Power:	PG2
Reset:	soft
Address:	6E000h-6E003h
Name:	Transcoder WD0 Horizontal Total
ShortName:	TRANS_HTOTAL_WD0
Power:	PG2
Reset:	soft
Address:	6F000h-6F003h
Name:	Transcoder EDP Horizontal Total
ShortName:	TRANS_HTOTAL_EDP
Power:	PG1
Reset:	soft

Restriction
Restriction : This register should not be changed while the transcoder or port are enabled.

DWord	Bit	Description

TRANS_HTOTAL

0	31:29	**Reserved** Format: MBZ
	28:16	**Horizontal Total** This field specifies Horizontal Total size. This should be equal to the sum of the horizontal active and the horizontal blank sizes. This field is programmed to the number of pixels desired minus one. This field is ignored by WD transcoders. **Restriction** Restriction : This register must always be programmed to the same value as the Horizontal Blank End.
	15:13	**Reserved** Format: MBZ
	12:0	**Horizontal Active** This field specifies Horizontal Active Display size. The first horizontal active display pixel is considered pixel number 0. This field is programmed to the number of pixels desired minus one. **Restriction** Restriction : The minimum horizontal active display size is 64 pixels. In HDMI modes the minimum is 256 pixels. This register must always be programmed to the same value as the Horizontal Blank Start.

TRANS_MSA_MISC

TRANS_MSA_MISC	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	60410h-60413h
Name:	Transcoder A MSA Misc
ShortName:	TRANS_MSA_MISC_A
Power:	PG2
Reset:	soft
Address:	61410h-61413h
Name:	Transcoder B MSA Misc
ShortName:	TRANS_MSA_MISC_B
Power:	PG2
Reset:	soft
Address:	62410h-62413h
Name:	Transcoder C MSA Misc
ShortName:	TRANS_MSA_MISC_C
Power:	PG2
Reset:	soft
Address:	6F410h-6F413h
Name:	Transcoder EDP MSA Misc
ShortName:	TRANS_MSA_MISC_EDP
Power:	PG1
Reset:	soft

Description

There is one instance of this register per each transcoder A/B/C/EDP. This register selects what value will be sent in the DisplayPort Main Stream Attribute (MSA) Miscellaneous (MISC) fields. The MSA MISC fields are mostly used to indicate the color encoding format and need to be programmed to indicate color space, bits per color, etc.

Programming Notes

See the DisplayPort specification for the details on what to program in these fields.

DWord	Bit	Description

TRANS_MSA_MISC		
0	31:16	**MSA Unused** This field selects the value that will be sent in the DisplayPort MSA unused fields. **Programming Notes** This should be usually programmed with all 0s.
	15:8	**MSA MISC1** This field selects the value that will be sent in the DisplayPort MSA MISC1 field. When TRANS_STEREO3D_CTL bit FS_MSA_MISC1_Drive_En is enabled, hardware will drive MISC1 bits 2:1 (bits 10:9 of this register) with the field sequential stereo 3D left or right eye indication, and any value written to those bits here will be ignored.
	7:0	**MSA MISC0** This field selects the value that will be sent in the DisplayPort MSA MISC0 field. **Restriction** Restriction : Before enabling DisplayPort, bit 0 should always be set to 1 to indicate link clock and stream clock are synchronous.

TRANS_MULT

TRANS_MULT

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32

Address:	6002Ch-6002Fh
Name:	Transcoder A Multiply
ShortName:	TRANS_MULT_A
Power:	PG2
Reset:	soft

Address:	6102Ch-6102Fh
Name:	Transcoder B Multiply
ShortName:	TRANS_MULT_B
Power:	PG2
Reset:	soft

Address:	6202Ch-6202Fh
Name:	Transcoder C Multiply
ShortName:	TRANS_MULT_C
Power:	PG2
Reset:	soft

Description
There is one instance of this register for each transcoder A/B/C.

Restriction
Restriction : This register should not be changed while the transcoder or port are enabled.

DWord	Bit	Description
0	31:3	**Reserved**
	2:0	**Multiplier** This field specifies the data multiplier value used by HDMI and DVI.

Value	Name	Description
000b	X1	Multiply by 1
001b	X2	Multiply by 2
011b	X4	Multiply by 4
Others	Reserved	Reserved

TRANS_SPACE

TRANS_SPACE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	60024h-60027h
Name:	Transcoder A Space
ShortName:	TRANS_SPACE_A
Power:	PG2
Reset:	soft
Address:	61024h-61027h
Name:	Transcoder B Space
ShortName:	TRANS_SPACE_B
Power:	PG2
Reset:	soft
Address:	62024h-62027h
Name:	Transcoder C Space
ShortName:	TRANS_SPACE_C
Power:	PG2
Reset:	soft
Address:	6F024h-6F027h
Name:	Transcoder EDP Space
ShortName:	TRANS_SPACE_EDP
Power:	PG1
Reset:	soft

Description
There is one instance of this register for each transcoder A/B/C/EDP.

Restriction
Restriction : This register should not be changed while the transcoder or port are enabled.

DWord	Bit	Description
0	31:12	**Reserved**
	11:0	**Vertical Active Space** This field specifies Stereo 3D Vertical Active space. This determines the number of constant pixel value lines inserted between the left and right eye

TRANS_SPACE		
		active video regions in the stereo 3D stacked frame mode. This field will only be used when the transcoder is in the stereo 3D stacked frame mode. This field should usually be programmed to be the same as the width of the vertical blank.

TRANS_STEREO3D_CTL

TRANS_STEREO3D_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x04000000
Access:	R/W
Size (in bits):	32
Address:	70020h-70023h
Name:	Transcoder A Stereo 3D Control
ShortName:	TRANS_STEREO3D_CTL_A
Power:	PG2
Reset:	soft
Address:	71020h-71023h
Name:	Transcoder B Stereo 3D Control
ShortName:	TRANS_STEREO3D_CTL_B
Power:	PG2
Reset:	soft
Address:	72020h-72023h
Name:	Transcoder C Stereo 3D Control
ShortName:	TRANS_STEREO3D_CTL_C
Power:	PG2
Reset:	soft
Address:	7F020h-7F023h
Name:	Transcoder EDP Stereo 3D Control
ShortName:	TRANS_STEREO3D_CTL_EDP
Power:	PG1
Reset:	soft

There is one instance of this register format per each transcoder A/B/C/EDP.
This register is sampled one line before vertical blank.

DWord	Bit	Description
0	31	**Transcoder S3D Enable** This bit enables the stereo 3D modes on this transcoder. Updates will take place at the start of the next vertical blank.

Value	Name
0b	Disable
1b	Enable

TRANS_STEREO3D_CTL

Restriction
Restriction : These modes are only for use with DisplayPort, HDMI, and DVI. HDMI/DVI: Stereo 3D can only be enabled with a mode set. It must be enabled before transcoder and port are enabled. It must be disabled after transcoder is disabled. DisplayPort: Stereo 3D can be enabled and disabled with a mode set, like HDMI and DVI, or it can be enabled after an enable mode set is complete and disabled prior to a disable mode set. VGA display modes, interlaced modes, SRD/PSR, WD, and frame buffer compression (FBC) do not work with stereo 3D. The left surface base address registers for the planes going to this transcoder must be programmed with valid addresses prior to enabling stereo 3D.

30:29 **Reserved**

28:27 **S3D Mode**

This field selects between the stereo 3D modes.

The stacked buffer mode combines both stereo 3D fields (left and right eye images) into a single tall frame with the left eye image on top, then a programmable space of black lines, then the right eye image on the bottom.

The field sequential mode sends one stereo 3D field (left or right eye image) out per frame. This mode is only for use with DisplayPort.

Field sequential hardware controlled mode automatically toggles between left and right eye at the start of each vertical blank. The starting field is selected using the FS_Field_Ctl register bit.

Field sequential software controlled mode will manually select left or right eye using the FS_Field_Ctl register bit.

Value	Name	Description
00b	FS HW Auto	Hardware controlled auto-toggle between left and right eye on each vertical blank.
01b	FS SW Manual	Software controlled selection between left and right eye
10b	Stacked	Stacked frame mode with both left and right eye images combined in a single tall frame
Others	Reserved	Reserved

Programming Notes
In the stacked frame mode, a vertical sync is not generated in the gap between left and right eye images, and the scan line count increments across the entire tall frame.

Restriction
Restriction : This field should only be changed when stereo 3D is disabled.

TRANS_STEREO3D_CTL

26 FS Field Ctl

The operation of this bit depends on the S3D Mode setting.
This field is ignored in the S3D stacked mode.
In the field sequential software controlled mode this bit selects the field sequential stereo 3D field (left or right eye).
In the field sequential hardware controlled mode this bit selects the field sequential stereo 3D starting field, the field used on the frame when field sequential stereo 3D is enabled.
Hardware does not wait for a specific eye when disabling.

Value	Name
0b	Right Eye
1b	Left Eye **[Default]**

Restriction
Restriction : The starting field must be set to the left eye for FS HW Auto usage.

25 Reserved

Format:	MBZ

24 S3D Current Field

Access:	RO

This read only bit indicates the current stereo 3D field (left or right eye).
This bit should be ignored when stereo 3D is not enabled.

Value	Name
0b	Right Eye
1b	Left Eye

23 FS MSA MISC1 Drive En

This bit enables hardware to drive the MSA MISC1 bits 2:1 with the internal field sequential stereo 3D left/right eye field indication.
Hardware will drive 00 when field sequential 3D stereo mode is not enabled, 01 when enabled and the upcoming video frame is the right eye, 11 when enabled and the upcoming video frame is the left eye.
This is based on the internal left/right indication which could be either generated by hardware in the HW auto mode or by software in the SW manual mode.
FS_MSA_Drive_Invert can be programmed to invert the left and right eye selection in the MSA.
When this bit is disabled, software may manually program TRANS_MSA_MISC to set MISC1 bits 2:1.

Value	Name	Description
0b	Disable	Disable hardware driving MSA MISC1 bits 2:1. Allow software to manually program MSA MISC1 bits 2:1 through TRANS_MSA_MISC.
1b	Enable	Enable hardware to drive MSA MISC1 bits 2:1 for stereo 3D.

Restriction

TRANS_STEREO3D_CTL		
		Restriction : This field should only be changed when stereo 3D is disabled and should not be enabled for the stacked frame mode.
	22	**Reserved**
	21:0	**Reserved** Format: MBZ

TRANS_VBLANK

TRANS_VBLANK	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	60010h-60013h
Name:	Transcoder A Vertical Blank
ShortName:	TRANS_VBLANK_A
Power:	PG2
Reset:	soft
Address:	61010h-61013h
Name:	Transcoder B Vertical Blank
ShortName:	TRANS_VBLANK_B
Power:	PG2
Reset:	soft
Address:	62010h-62013h
Name:	Transcoder C Vertical Blank
ShortName:	TRANS_VBLANK_C
Power:	PG2
Reset:	soft
Address:	6F010h-6F013h
Name:	Transcoder EDP Vertical Blank
ShortName:	TRANS_VBLANK_EDP
Power:	PG1
Reset:	soft

There is one instance of this register for each transcoder A/B/C/EDP.

Restriction
Restriction : This register should not be changed while the transcoder or port are enabled.

DWord	Bit	Description
0	31:29	**Reserved**
	28:16	**Vertical Blank End** This field specifies Vertical Blank End position relative to the vertical active display start. **Restriction**

TRANS_VBLANK		
		Restriction : This register must always be programmed to the same value as the Vertical Total. The minimum vertical blank size is 5 lines. With SRD/PSR and/or DisplayPort VDIP GMP the minimum is 8 lines.
	15:13	**Reserved**
	12:0	**Vertical Blank Start** This field specifies the Vertical Blank Start position relative to the vertical active display start. **Restriction** Restriction : This register must always be programmed to the same value as the Vertical Active.

TRANS_VSYNC

TRANS_VSYNC	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	60014h-60017h
Name:	Transcoder A Vertical Sync
ShortName:	TRANS_VSYNC_A
Power:	PG2
Reset:	soft
Address:	61014h-61017h
Name:	Transcoder B Vertical Sync
ShortName:	TRANS_VSYNC_B
Power:	PG2
Reset:	soft
Address:	62014h-62017h
Name:	Transcoder C Vertical Sync
ShortName:	TRANS_VSYNC_C
Power:	PG2
Reset:	soft
Address:	6F014h-6F017h
Name:	Transcoder EDP Vertical Sync
ShortName:	TRANS_VSYNC_EDP
Power:	PG1
Reset:	soft

Description
There is one instance of this register for each transcoder A/B/C/EDP.

Restriction
Restriction : This register should not be changed while the transcoder or port are enabled.

DWord	Bit	Description
0	31:29	**Reserved**

TRANS_VSYNC		
	28:16	**Vertical Sync End** This field specifies the Vertical Sync End position relative to the vertical active display start. It is programmed with VerticalActive+FrontPorch+Sync-1 **Restriction** Restriction : This value must be greater than the vertical sync start and less than Vertical Total.
	15:13	**Reserved**
	12:0	**Vertical Sync Start** This field specifies the Vertical Sync Start position relative to the vertical active display start. It is programmed with VerticalActive+FrontPorch-1 **Restriction** Restriction : This value must be greater than Vertical Active.

TRANS_VSYNCSHIFT

TRANS_VSYNCSHIFT	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	60028h-6002Bh
Name:	Transcoder A Vertical Sync Shift
ShortName:	TRANS_VSYNCSHIFT_A
Power:	PG2
Reset:	soft
Address:	61028h-6102Bh
Name:	Transcoder B Vertical Sync Shift
ShortName:	TRANS_VSYNCSHIFT_B
Power:	PG2
Reset:	soft
Address:	62028h-6202Bh
Name:	Transcoder C Vertical Sync Shift
ShortName:	TRANS_VSYNCSHIFT_C
Power:	PG2
Reset:	soft
Address:	6F028h-6F02Bh
Name:	Transcoder EDP Vertical Sync Shift
ShortName:	TRANS_VSYNCSHIFT_EDP
Power:	PG1
Reset:	soft

Description
There is one instance of this register for each transcoder A/B/C/EDP.

Restriction
Restriction : This register should not be changed while the transcoder or port are enabled.

DWord	Bit	Description
0	31:13	**Reserved**

TRANS_VSYNCSHIFT		
	12:0	**Second Field VSync Shift** This value specifies the vertical sync alignment for the start of the interlaced second field, expressed in terms of the absolute pixel number relative to the horizontal active display start. This value will only be used if the transcoder is programmed to an interlaced mode. Typically, the interlaced second field vertical sync should start one pixel after the point halfway between successive horizontal syncs, so the value of this register should be programmed = horizontal sync start - floor[horizontal total / 2] Calculate using the actual horizontal sync start and horizontal total values and not the minus one values programmed into the registers. This vertical sync shift only occurs during the interlaced second field. In all other cases the vertical sync start position is aligned with horizontal sync start.

TRANS_VTOTAL

TRANS_VTOTAL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6000Ch-6000Fh
Name:	Transcoder A Vertical Total
ShortName:	TRANS_VTOTAL_A
Power:	PG2
Reset:	soft
Address:	6100Ch-6100Fh
Name:	Transcoder B Vertical Total
ShortName:	TRANS_VTOTAL_B
Power:	PG2
Reset:	soft
Address:	6200Ch-6200Fh
Name:	Transcoder C Vertical Total
ShortName:	TRANS_VTOTAL_C
Power:	PG2
Reset:	soft
Address:	6E00Ch-6E00Fh
Name:	Transcoder WD0 Vertical Total
ShortName:	TRANS_VTOTAL_WD0
Power:	PG2
Reset:	soft
Address:	6F00Ch-6F00Fh
Name:	Transcoder EDP Vertical Total
ShortName:	TRANS_VTOTAL_EDP
Power:	PG1
Reset:	soft

Restriction
Restriction : This register should not be changed while the transcoder or port are enabled.

DWord	Bit	Description

TRANS_VTOTAL		
0	31:29	**Reserved**
	28:16	**Vertical Total** This field specifies Vertical Total size. This should be equal to the sum of the vertical active and the vertical blank sizes. For progressive display modes, this field is programmed to the number of lines desired minus one. For interlaced display modes, this field is programmed with the number of lines desired minus two. The vertical counter is incremented on the leading edge of the horizontal sync. Both even and odd vertical totals are supported. This field is ignored by WD transcoders. **Restriction** Restriction : This register must always be programmed to the same value as the Vertical Blank End.
	15:13	**Reserved**
	12	**Reserved**
	11:0	**Vertical Active** This field specifies Vertical Active Display size. The first vertical active display line is considered line number 0. This field is programmed to the number of lines desired minus one. **Restriction** Restriction : When using the internal panel fitting logic, the minimum vertical active area must be seven lines. This register must always be programmed to the same value as the Vertical Blank Start.

Unit Level Clock Gating Control 1

UCGCTL1 - Unit Level Clock Gating Control 1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x02F00000 [KBL]
Size (in bits):	32
Address:	09400h

Unit Level Clock Gating Control Registers.

DWord	Bit	Description
0	31	**Sarbunit Clock Gating Disable** Access: R/W SARB unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	30	**IEFunit Clock Gating Disable** Access: R/W IEFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	29	**IECPunit Clock Gating Disable** Access: R/W IECPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	28	**ICunit Clock Gating Disable** Access: R/W ICunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	27	**HIZunit Clock Gating Disable** Access: R/W

UCGCTL1 - Unit Level Clock Gating Control 1

		HIZunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	26	**GWunit Clock Gating Disable** Access: R/W GWunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	25	**GTIunit Clock Gating Disable** Default Value: 1b Access: R/W GTI Units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	24	**GSunit Clock Gating Disable** Access: R/W GSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	23	**GPMunit Clock Gating Disable** Default Value: 1b Access: R/W GPMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	22	**GAMunit Clock Gating Disable** Default Value: 1b Access: R/W GAMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL1 - Unit Level Clock Gating Control 1

	21	**GACunit Clock Gating Disable** Default Value: 1b Access: R/W GACunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	20	**GABunit Clock Gating Disable** Default Value: 1b Access: R/W GABunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	19	**FTunit Clock Gating Disable** Access: R/W FTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	18	**FLunit Clock Gating Disable** Access: R/W FLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	17	**EU_FPUunit Clock Gating Disable** Access: R/W EU_FPUunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	16	**EU_TCunit Clock Gating Disable** Access: R/W EU_TCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL1 - Unit Level Clock Gating Control 1

15	**EU_EMunit Clock Gating Disable** Access: R/W EU_EMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
14	**EU_GAunit Clock Gating Disable** Access: R/W EU_GAunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
13	**EUunit Clock Gating Disable** Access: R/W EUunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
12	**SVLunit Clock Gating Disable** Access: R/W SVLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
11	**DTunit Clock Gating Disable** Access: R/W DTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
10	**DMunit Clock Gating Disable** Access: R/W DMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL1 - Unit Level Clock Gating Control 1

	9	**DGunit Clock Gating Disable** Access: R/W DGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	8	**DAPunit Clock Gating Disable** Access: R/W DAPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	7	**CSunit Clock Gating Disable** Access: R/W CSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	6	**CLunit Clock Gating Disable** Access: R/W CLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	5	**BLBunit Clock Gating Disable** Access: R/W BLBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	4	**BFunit Clock Gating Disable** Access: R/W BFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL1 - Unit Level Clock Gating Control 1

	3	**BDunit Clock Gating Disable** Access: R/W BDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	2	**BCSunit Clock Gating Disable** Access: R/W BCSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	1	**AVSunit Clock Gating Disable** Access: R/W AVSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	0	**SPARE RAM Clock Gating Disable** Access: R/W SPARE RAM Clock Gating Disable Control: '0' : RAM Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : RAM Clock Gating Disabled. (that is, clocks are toggling, always)

Unit Level Clock Gating Control 2

UCGCTL2 - Unit Level Clock Gating Control 2		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000 [KBL]	
Size (in bits):	32	
Address:	09404h	
Unit Level Clock Gating Control Registers.		

DWord	Bit	Description
0	31	**VFunit Clock Gating Disable** Access: R/W VFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	30	**VDSunit Clock Gating Disable** Access: R/W VDSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	29	**VDIunit Clock Gating Disable** Access: R/W VDIunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	28	**VCSunit Clock Gating Disable** Access: R/W VCSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL2 - Unit Level Clock Gating Control 2

27	**DTOunit Clock Gating Disable** Access: R/W DTOunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
26	**VCPunit Clock Gating Disable** Access: R/W VCPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
25	**VCDunit Clock Gating Disable** Access: R/W VCDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
24	**URBMunit Clock Gating Disable** Access: R/W URBMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
23	**TSGunit Clock Gating Disable** Access: R/W TSGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
22	**TDLunit Clock Gating Disable** Access: R/W TDLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL2 - Unit Level Clock Gating Control 2

21	**TDSunit Clock Gating Disable** Access: R/W TDSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always) Programming note: To work around a clock gating issue for A0-D0, the clock gating disable must be set to a 1 unless the offset h229c bit 11, Replay Mode, is set to 0, mid-cmdbuffer preemption
20	**SVSMunit Clock Gating Disable** Access: R/W SVSMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
19	**SVGunit Clock Gating Disable** Access: R/W SVGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
18	**SOunit Clock Gating Disable** Access: R/W SOunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
17	**SIunit Clock Gating Disable** Access: R/W SIunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
16	**SFunit Clock Gating Disable** Access: R/W SFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL2 - Unit Level Clock Gating Control 2

15	**SECunit Clock Gating Disable** Access: R/W SECunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
14	**SCunit Clock Gating Disable** Access: R/W SCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
13	**RCZunit Clock Gating Disable** Access: R/W RCZunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
12	**RCPBunit Clock Gating Disable** Access: R/W RCPBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
11	**RCCunit Clock Gating Disable** Access: R/W RCCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
10	**QCunit Clock Gating Disable** Access: R/W QCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL2 - Unit Level Clock Gating Control 2

	9	**PSDunit Clock Gating Disable** Access: R/W PSDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	8	**PLunit Clock Gating Disable** Access: R/W PLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	7	**MTunit Clock Gating Disable** Access: R/W MTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	6	**MPCunit Clock Gating Disable** Access: R/W MPCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	5	**TDGunitClock Gating Disable** Access: R/W TDGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	4	**MSCunit Clock Gating Disable** Access: R/W MSCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL2 - Unit Level Clock Gating Control 2

	3	**TEunit Clock Gating Disable** Access: R/W TEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	2	**TETGunit Clock Gating Disable** Access: R/W TETGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	1	**MAunit Clock Gating Disable** Access: R/W MAunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	0	**IZunit Clock Gating Disable** Access: R/W IZunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

Unit Level Clock Gating Control 3

UCGCTL3 - Unit Level Clock Gating Control 3

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x04000000 [KBL]
Size (in bits):	32
Address:	09408h

Unit Level Clock Gating Control Registers.

DWord	Bit	Description
0	31	**Flunits 2nd Clock Gating Disable** Access: R/W Flunits 2nd Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	30	**SVRRunit Clock Gating Disable** Access: R/W SVRRunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	29	**VCRunit Clock Gating Disable** Access: R/W VCRunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	28	**EDTunit Clock Gating Disable** Access: R/W EDTunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL3 - Unit Level Clock Gating Control 3

27	**VCIunit Clock Gating Disable** Access: R/W VCIunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
26	**2x Assign fub XOR Clock Gating Disable** Default Value: 1b Access: R/W 2x Assign fub XOR Clock Gating Disable Control: '0' : 2x Assign fub XOR Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : 2x Assign fub XOR Clock Gating Disabled. (that is, clocks are toggling, always)
25	**HSunit Clock Gating Disable** Access: R/W HSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
24	**SOLunit Clock Gating Disable** Access: R/W SOLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
23	**QRCunit Clock Gating Disable** Access: R/W QRCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
22	**MSPBISTunit Clock Gating Disable** Access: R/W MSPBISTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL3 - Unit Level Clock Gating Control 3

21	**BSPunit Clock Gating Disable** Access: R/W BSPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
20	**OACSunit Clock Gating Disable** Access: R/W OACSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
19	**SBEunit Clock Gating Disable** Access: R/W SBEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
18	**BCunit Clock Gating Disable** Access: R/W BCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
17	**WMBE Clock Gating Disable** Access: R/W WMBEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
16	**WMFEunit Clock Gating Disable** Access: R/W WMFEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL3 - Unit Level Clock Gating Control 3

15	**VSCunit Clock Gating Disable** Access: R/W VSCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
14	**NOAunit Clock Gating Disable** Access: R/W NOAunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
13	**USBunit Clock Gating Disable** Access: R/W USBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
12	**STCunit Clock Gating Disable** Access: R/W STCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
11	**VSunit Clock Gating Disable** Access: R/W VSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
10	**VOPunit Clock Gating Disable** Access: R/W VOPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL3 - Unit Level Clock Gating Control 3

	9	**VMXunit Clock Gating Disable** Access: R/W VMXunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	8	**VMEunit Clock Gating Disable** Access: R/W VMEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	7	**VMDunit Clock Gating Disable** Access: R/W VMDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	6	**VMCunit Clock Gating Disable** Access: R/W VMCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	5	**VLFunit Clock Gating Disable** Access: R/W VLFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	4	**VITunit Clock Gating Disable** Access: R/W VITunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL3 - Unit Level Clock Gating Control 3

	3	**VIPunit Clock Gating Disable** Access: R/W VIPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	2	**VINunit Clock Gating Disable** Access: R/W VINunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	1	**VFTunit Clock Gating Disable** Access: R/W VFTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	0	**VFEunit Clock Gating Disable** Access: R/W VFEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

Unit Level Clock Gating Control 4

UCGCTL4 - Unit Level Clock Gating Control 4

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00F80003
Size (in bits):	32
Address:	0940Ch

Unit Level Clock Gating Control Registers.

DWord	Bit	Description
0	31:30	**Reserved** Access: RO rsvd
	29	**GAFSRRB unit Clock Gate Disable** Access: R/W GAFSRRB units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	28	**RAMDFT units Clock Gate Disable** Access: R/W RAMDFT units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	27	**L3 CBR 2x Clock Gate Disable** Access: R/W L3 CBR units 2x Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	26	**L3 CBR 1x Clock Gate Disable** Access: R/W L3 CBR units 1x Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL4 - Unit Level Clock Gating Control 4

	25	**L3 BANK 2x Clock Gate Disable** Access: R/W L3 BANK units 2x Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	24	**L3 BANK 1x Clock Gate Diable** Access: R/W L3 BANK units 1x Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	23	**MBGFunit Clock Gate Disable** Default Value: 1b Access: R/W MBGFunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	22	**MSQDunit 2x Clock Gate Disable** Default Value: 1b Access: R/W MSQD units cu2x Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	21	**MSQDunit Clock Gate Disable** Default Value: 1b Access: R/W MSQD units 1x Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL4 - Unit Level Clock Gating Control 4

	20	**MISDunits 2x Clock Gate Disable** Default Value: 1b Access: R/W MISDunits cu2x Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	19	**MISDunit Clock Gate Disable** Default Value: 1b Access: R/W MISDunits 1x Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	18	**GAFMunit Clock Gate Disable** Access: R/W GAFMunit' Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	17	**GAPCunit Clock Gate Disable** Access: R/W GAPCunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	16	**GAPZunit Clock Gate Disable** Access: R/W GAPZunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL4 - Unit Level Clock Gating Control 4

15	**GAPL3unit Clock Gate Disable** Access: R/W GAPL3 units' Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
14	**GAFSunit Clock Gate Disable** Access: R/W GAFSunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
13	**GAHSunit Clock Gate Disable** Access: R/W GAHSunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
12	**VISunit Clock Gate Disable** Access: R/W VISunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
11	**VACunit Clock Gate Disable** Access: R/W VACunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
10	**VAMunit Clock Gate Disable** Access: R/W VAMunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL4 - Unit Level Clock Gating Control 4

9	**VADuit Clock Gating Disable** Access: R/W VADunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
8	**JPGunit Clock Gating Disable** Access: R/W JPGunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
7	**VBPunits Clock Gating Disable** Access: R/W VBPunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
6	**VHRunit Clock Gating Disable** Access: R/W VHRunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
5	**VID4 VINunit Clock Gating Disable** Access: R/W VID4 VINunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
4	**VID3 VINunit Clock Gating Disable** Access: R/W VID3 VINunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL4 - Unit Level Clock Gating Control 4

	3	**VID2 VINunit Clock Gating Disable** Access: R/W VID2 VINunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	2	**VID1 VINunit Clock Gating Disable** Access: R/W VID1 VINunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	1:0	**MSQCunit Clock Gating Disable** Default Value: 11b Access: R/W MSQCunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

Unit Level Clock Gating Control 5

UCGCTL5 - Unit Level Clock Gating Control 5

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	09418h

Unit Clock Gating Control Register 5.

DWord	Bit	Description
0	31	**VCOPunit clock gating disable bit** Access: R/W WVCOP units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always).
	30	**VMBunit clock gate disable bit** Access: R/W VMB units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	29	**VDMunit clock gate disable bit** Access: R/W VDM units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	28	**L3BANK unit cuclkgating disable bit** Access: R/W L3bank units cuclk Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL5 - Unit Level Clock Gating Control 5

	27	**L3BANK cu2x clock gate disable bit** Access: R/W L3BANK units cu2x Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks
	26	**LNIunit clock gate disable bit** Access: R/W LNI units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	25	**LNEUNIT clock gate disable bit** Access: R/W LNE units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	24	**VVPunit clock gate disable bit** Access: R/W VVP units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	23	**WVFT unit clock gate disable bits** Access: R/W WVFT units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	22	**WBPS unit clock gate disable bit** Access: R/W WBPS units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL5 - Unit Level Clock Gating Control 5

	21	**WVMX unit clock gate disable bit** Access: R/W WVMX units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	20	**WVIP unit clock gate disable bit** Access: R/W WVIP unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	19	**WVIT unit clock gate disable bit** Access: R/W WVIT units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	18	**WVIS unit clock gate disable** Access: R/W WVIS units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	17	**RPM units clock gate disable** Access: R/W RPM units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	16	**OASC unit clock gating disable** Access: R/W OASC units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL5 - Unit Level Clock Gating Control 5

15	**VECS unit clock gate disable** Access: R/W VECS units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
14	**GAHSV unit clock gate disable** Access: R/W GAHSV units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
13	**GAHSD unit clock gate disable** Access: R/W GAHSD units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
12	**GAV unit's clock gate disable** Access: R/W GAV units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
11	**RSunit's clock gate disable** Access: R/W RW units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
10	**VFW units clock gate disable** Access: R/W VFW units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL5 - Unit Level Clock Gating Control 5

	9	**VCW unit's clock gate disable** Access: R/W VCW units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	8	**VEO unit's clock gate disable** Access: R/W VEO units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	7	**VDN unit's clock gate disable** Access: R/W VDN units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	6	**VTQunit's clock gate disable** Access: R/W VTQunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	5	**VPRunit's clock gate disable** Access: R/W VPR units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	4	**IMEunit's clock gate disable** Access: R/W IME units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL5 - Unit Level Clock Gating Control 5

	3	**CREunit clock gate disable** Access: R/W CRE units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	2	**GAPSL unit clock gate disable** Access: R/W GAPSL units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	1	**GAPSU Clock gate disable** Access: R/W GAPSU units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	0	**SPMunit Clock gate disable** Access: R/W SPM units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

Unit Level Clock Gating Control 6

UCGCTL6 - Unit Level Clock Gating Control 6

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000 [KBL]
Size (in bits):	32
Address:	09430h

Unit Level Clock Gating Disable bits.

DWord	Bit	Description
0	31	**SPARE 3 clock gate disable** Access: R/W SPARE 3 unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	30:28	**HDCunit clock gate disable** Access: R/W HDC units Clock Gating Disable Control: HDCREQ bit 28, HDCRET bit 29, HDCTLB bit 30. '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	27	**MUCunit clock gate disable** Access: R/W MUC units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	26	**GACVunit cuclk gate disable** Access: R/W GACV units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL6 - Unit Level Clock Gating Control 6

25	**GACBunit clock gate disable** Access: R/W GACB units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
24	**GAPSunit clock gate disable** Access: R/W GAPS units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
23	**GAMTunit clock gate disable** Access: R/W GAMT units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
22	**Reserved**
21	**OASCREP** Access: R/W OASCREP units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
20	**OAADDRunit clock gate disable bit** Access: R/W OAADDR units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
19	**GACVunit clock gate disable** Access: R/W GACV units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL6 - Unit Level Clock Gating Control 6

	18	**BDMunit clock gate disable** Access: R/W BDM units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	17	**GATSunit clock gate disable** Access: R/W GATS units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	16	**OATREPunit clock gate disable** Access: R/W OATREP units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	15	**STunit clock gate disable** Access: R/W ST units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	14	**SDEunit clock gate disable** Access: R/W SDE units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	13	**VIN(VID6) unit clock gate disable** Access: R/W VIN(VID6) units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL6 - Unit Level Clock Gating Control 6

	12	**VIN(VID5) unit clock gate disable** Access: R/W VIN(VID5) units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	11	**WVOPunit clock gate disable** Access: R/W WVOP units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	10	**WUSB unit clock gate disable** Access: R/W WUSB units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	9	**WSECunit clock gate disable** Access: R/W WSEC units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	8	**WRSunit clcok gate disable** Access: R/W WRS units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	7	**WQRCunit clock gate disable** Access: R/W WQRC units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL6 - Unit Level Clock Gating Control 6

	6	**WMPC unit level clock gate disable** Access: R/W WMPC units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	5	**WINunit Clock gate disable** Access: R/W WIN units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	4	**WIME unit clock gate disable** Access: R/W WIME units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	3	**WHME unit clock gate disable** Access: R/W WHME units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	2	**WAVMunit Clock Gate Disable** Access: R/W WAVM units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	1	**VSHMunit clock gate disable** Access: R/W VSHM units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL6 - Unit Level Clock Gating Control 6		
	0	**VSLunit Clock gating disable** Access: R/W VSL units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

Unit Level Clock Gating Control 7

UCGCTL7 - Unit Level Clock Gating Control 7

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	09434h

Unit Level Clock Gating Disable bits.

DWord	Bit	Description
0	31	**wrcunit Clock Gating Disable** Access: R/W wrcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	30	**mmcdunit Clock Gating Disable** Access: R/W mmcdunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	29	**bfceunit Clock Gating Disable** Access: R/W bfceunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	28	**ecpunit Clock Gating Disable** Access: R/W ecpunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL7 - Unit Level Clock Gating Control 7

27	**vdlunit1 Clock Gating Disable** Access: R/W vdlunit1 Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
26	**vhmeunit Clock Gating Disable** Access: R/W vhmeunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
25	**vimeunit Clock Gating Disable** Access: R/W vimeunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
24	**vcreunit Clock Gating Disable** Access: R/W vcreunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
23	**vdxunit Clock Gating Disable** Access: R/W vdxunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
22	**mdcunit Clock Gating Disable** Access: R/W mdcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL7 - Unit Level Clock Gating Control 7

	21	**hpounit Clock Gating Disable** Access: R/W hpounit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	20	**hrsunit Clock Gating Disable** Access: R/W hrsunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	19	**ftunit Clock Gating Disable** Access: R/W ftunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	18	**fqunit Clock Gating Disable** Access: R/W fqunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	17	**hleunit Clock Gating Disable** Access: R/W hleunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	16	**hlcunit Clock Gating Disable** Access: R/W hlcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL7 - Unit Level Clock Gating Control 7

15	**hhiunit Clock Gating Disable** Access: R/W hhiunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
14	**mlfunit Clock Gating Disable** Access: R/W mlfunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
13	**mmcunit Clock Gating Disable** Access: R/W mmcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
12	**mbdunit Clock Gating Disable** Access: R/W mbdunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
11	**mpdunit Clock Gating Disable** Access: R/W mpdunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
10	**mmxunit Clock Gating Disable** Access: R/W mmxunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL7 - Unit Level Clock Gating Control 7

	9	**hedunit Clock Gating Disable** Access: R/W hedunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	8	**hlfunit Clock Gating Disable** Access: R/W hlfunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	7	**hmcunit Clock Gating Disable** Access: R/W hmcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	6	**hmxunit Clock Gating Disable** Access: R/W hmxunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	5	**hppunit Clock Gating Disable** Access: R/W hppunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	4	**hprunit Clock Gating Disable** Access: R/W hprunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL7 - Unit Level Clock Gating Control 7

	3	**Reserved**
	2	**hwmunit Clock Gating Disable** Access: R/W hwmunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	1	**vmpcunit Clock Gating Disable** Access: R/W vmpcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	0	**vsecunit Clock Gating Disable** Access: R/W vsecunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

Unit Level Clock Gating Control 8

UCGCTL8 - Unit Level Clock Gating Control 8

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	09438h

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31	**jusbunit Clock Gating Disable** Access: R/W jusbunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	30	**sfiunit Clock Gating Disable** Access: R/W sfiunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	29	**sfeunit Clock Gating Disable** Access: R/W sfeunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	28	**sfaunit Clock Gating Disable** Access: R/W sfaunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL8 - Unit Level Clock Gating Control 8

	27	**sfounit Clock Gating Disable** Access: R/W sfounit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	26	**sfxunit Clock Gating Disable** Access: R/W sfxunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	25	**sfmunit Clock Gating Disable** Access: R/W sfmunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	24	**vmmunit Clock Gating Disable** Access: R/W vmmunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	23	**vrtunit Clock Gating Disable** Access: R/W vrtunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	22	**ccunit Clock Gating Disable** Access: R/W ccunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL8 - Unit Level Clock Gating Control 8

	21	**gassunit Clock Gating Disable** Access: R/W gassunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	20	**gamdunit Clock Gating Disable** Access: R/W gamdunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	19	**vdlunit1 Clock Gating Disable** Access: R/W vdlunit1 Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	18	**vhmeunit Clock Gating Disable** Access: R/W vhmeunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	17	**vcreunit Clock Gating Disable** Access: R/W vcreunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	16	**hleunit Clock Gating Disable** Access: R/W hleunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL8 - Unit Level Clock Gating Control 8

15	**mbdunit Clock Gating Disable** Access: R/W mbdunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
14	**mmxunit Clock Gating Disable** Access: R/W mmxunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
13	**mpdunit Clock Gating Disable** Access: R/W mpdunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
12	**hedunit Clock Gating Disable** Access: R/W hedunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
11	**hlfunit Clock Gating Disable** Access: R/W hlfunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
10	**hmcunit Clock Gating Disable** Access: R/W hmcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL8 - Unit Level Clock Gating Control 8

	9	**hmxunit Clock Gating Disable** Access: R/W hmxunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	8	**hppunit Clock Gating Disable** Access: R/W hppunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	7	**hprunit Clock Gating Disable** Access: R/W hprunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	6	**Reserved**
	5	**hwmunit Clock Gating Disable** Access: R/W hwmunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	4	**mdcunit Clock Gating Disable** Access: R/W mdcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	3	**vmpcunit Clock Gating Disable** Access: R/W vmpcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UCGCTL8 - Unit Level Clock Gating Control 8

	2	**sfmunit Clock Gating Disable EBB** Access: R/W sfmunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	1	**sfaunit Clock Gating Disable EBB** Access: R/W sfaunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	0	**sfeunit Clock Gating Disable EBB** Access: R/W sfeunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

Unit Level Clock Gating Control 9

UCGCTL9 - Unit Level Clock Gating Control 9

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	0943Ch

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31:4	**Reserved** Access: RO Reserved
	3	**vbspunit Clock Gating Disable** Access: R/W vbspunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	2	**vmmunit Clock Gating Disable** Access: R/W vmmunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	1	**AVSunit Clock Gating Disable** Access: R/W AVSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	0	**daprssunit Clock Gating Disable** Access: R/W daprssunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)

UNSLICE FF TDL Queues Full Event

UNSLICE_FF_EVENT2 - UNSLICE FF TDL Queues Full Event

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	00DACh

This register mirrors an accumulating count for Unslice Frequency COntrol Event 0.
It is enabled by configuration bits in GPMunit and SPMunits.
Note that count is never cleared and delta should be calculated by sampling the initial register value at the start and subtracting that value off from the final sample value.

DWord	Bit	Description
0	31:0	**Unslice FF TDL Queues Full Event BitField** Access: RO

UNSLICE FF THREADS MAX LOADED

UNSLICE_FF_EVENT3 - UNSLICE FF THREADS MAX LOADED	
Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	00DB0h

This register mirrors an accumulating count for Unslice Frequency COntrol Event 0.
It is enabled by configuration bits in GPMunit and SPMunits.
Note that count is never cleared and delta should be calculated by sampling the initial register value at the start and subtracting that value off from the final sample value.

DWord	Bit	Description
0	31:0	**Unslice FF Number of Threads Loaded at Max** Access: RO

Unslice Frequency Threshold Comparator 2 Count

UNSLICE_FF_EVENT1 - Unslice Frequency Threshold Comparator 2 Count	
Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	00DC0h

This register mirrors an accumulating count for Unslice Frequency COntrol Event 0.
It is enabled by configuration bits in GPMunit and SPMunits.
Note that count is never cleared and delta should be calculated by sampling the initial register value at the start and subtracting that value off from the final sample value.

DWord	Bit	Description
0	31:0	**Unslice Frequency Control Threshold Accumulator 2** Access: RO

Unslice Frequency Threshold Comparator 3 Count

UNSLICE_FF_EVENT0 - Unslice Frequency Threshold Comparator 3 Count

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	00DBCh

This register mirrors an accumulating count for Unslice Frequency COntrol Event 0.
It is enabled by configuration bits in GPMunit and SPMunits.
Note that count is never cleared and delta should be calculated by sampling the initial register value at the start and subtracting that value off from the final sample value.

DWord	Bit	Description
0	31:0	**Unslice Frequency Control Threshold Accumulator 3** Access: RO

URB Context Offset

URB_CXT_OFFSET - URB Context Offset		
Register Space:	MMIO: 0/2/0	
Source:	RenderCS	
Default Value:	0x0000C540	
Access:	Read/32 bit Write Only	
Size (in bits):	32	
Address:	021B8h	
DWord	**Bit**	**Description**
0	31:6	**URB Offset** Default Value: 315h This field indicates the offset (64bytes granular) in to the logical rendering context to which URB contents are save/restored when enabled. This field register must not be written directly (via MMIO) unless the Command Streamer is completely idle (i.e., the Ring Buffer is empty and the pipeline is idle) and RC6 is disabled. One way to program this register is via Load Register Immediate command in the ring buffer as part of initialization sequence.
	5:0	**Reserved** Format: MBZ

UTIL_PIN_CTL

UTIL_PIN_CTL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	48400h-48403h
Name:	Utility Pin Control
ShortName:	UTIL_PIN_CTL
Power:	PG0
Reset:	soft

This register controls the display utility pin. The nominal supply is 1 Volt and can be level shifted depending on usage. The maximum switching frequency is 100 KHz.

DWord	Bit	Description
0	31	**Util Pin Enable** This bit enables the utility pin. Value: 0b = Disable; 1b = Enable
	30:29	**Pipe Select** This bit selects which pipe will be used when the utility pin is outputting timing related signals. Value: 00b = Pipe A; 01b = Pipe B; 10b = Pipe C; 11b = Reserved Restriction : The field should only be changed when the utility pin is disabled or not configured to use any timing signals.
	28	**Reserved**
	27:24	**Util Pin Mode** This bit configures the utility pin mode of operation for output. Value: 0000b = Data (Output the Util_Pin_Output_Data value.)

UTIL_PIN_CTL

0001b	PWM	Output from the backlight PWM circuit.
0100b	Vblank	Output the vertical blank.
0101b	Vsync	Output the vertical sync.
1000b	Right/Left Eye Level	Output the stereo 3D right/left eye level signal. Asserted for the left eye and de-asserted for the right eye.
Others	Reserved	Reserved

Restriction
Restriction : The field should only be changed when the utility pin is disabled.

23	**Util Pin Output Data** This bit selects what the value to drive as an output when in the data mode. **Value** / **Name** 0b / 0 1b / 1
22	**Util Pin Output Polarity** This bit inverts the polarity of the pin output. **Value** / **Name** 0b / Not inverted 1b / Inverted
21:20	**Reserved**
19:16	**Reserved**
15:0	**Reserved**

Valid Bit Vector 0 for CVS

CVSTLB_VLD_0 - Valid Bit Vector 0 for CVS		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04C00h	
This register contains the valid bits for entries 0-31 of CVSTLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 0 for CVS** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 0 for L3

L3TLB_VLD_0 - Valid Bit Vector 0 for L3	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04D00h

This register contains the valid bits for entries 0-31 of L3TLB.

DWord	Bit	Description
0	31:0	**Valid Bit Vector 0 for L3** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 0 for MFX

MFXTLB_VLD_0 - Valid Bit Vector 0 for MFX		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04BA0h	
This register contains the valid bits for entries 0-31 of MFXTLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 0 for MFX** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 0 for MFX SL1

MFXTLB_VLD_SL1_0 - Valid Bit Vector 0 for MFX SL1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04BC0h
This register contains the valid bits for entries 0-31 of MFX SL1 TLB.	

DWord	Bit	Description
0	31:0	**Valid Bit Vector 0 for MFX SL1** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 0 for MTTLB

MTTLB_VLD0 - Valid Bit Vector 0 for MTTLB		
Register Space:	MMIO: 0/2/0	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	04780h-04783h	
This register contains the valid bits for entries 0-31 of MTTLB (Texture and constant cache TLB).		
DWord	**Bit**	**Description**
0	31:0	**Valid bits per entry**

Valid Bit Vector 0 for MTVICTLB

VICTLB_VLD0 - Valid Bit Vector 0 for MTVICTLB	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	04788h-0478Bh

This register contains the valid bits for entries 0-31 of VICTLB (Vertex Fetch, Instruction Cache, and Command Streamer TLB).

DWord	Bit	Description
0	31:0	**Valid bits per entry**

Valid Bit Vector 0 for RCC

RCCTLB_VLD_0 - Valid Bit Vector 0 for RCC		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04DA0h	
This register contains the valid bits for entries 0-31 of RCCTLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 0 for RCC** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 0 for RCCTLB

RCCTLB_VLD0 - Valid Bit Vector 0 for RCCTLB			
Register Space:	MMIO: 0/2/0		
Source:	RenderCS		
Default Value:	0x00000000		
Access:	RO		
Size (in bits):	32		
Trusted Type:	1		
Address:	04790h-04793h		
This register contains the valid bits for entries 0-31 of RCCTLB (Render Cache for Color TLB).			
DWord	**Bit**	**Description**	
0	31:0	**Valid bits per entry**	

Valid Bit Vector 0 for RCZTLB

RCZTLB_VLD0 - Valid Bit Vector 0 for RCZTLB	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	04798h-0479Bh

This register contains the valid bits for entries 0-31 of RCZTLB (Render Cache for Z (Depth), Hi Z, and Stencil TLB).

DWord	Bit	Description
0	31:0	**Valid bits per entry**

Valid Bit Vector 0 for RCZTLB

RCZTLB_VLD0 - Valid Bit Vector 0 for RCZTLB	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	04798h-0479Bh

This register contains the valid bits for entries 0-31 of RCZTLB (Render Cache for Z (Depth), Hi Z, and Stencil TLB).

DWord	Bit	Description
0	31:0	**Valid bits per entry**

Valid Bit Vector 0 for TLBPEND registers

TLBPEND_VLD0 - Valid Bit Vector 0 for TLBPEND registers			
Register Space:	MMIO: 0/2/0		
Source:	RenderCS		
Default Value:	0x00000000		
Access:	R/W		
Size (in bits):	32		
Trusted Type:	1		
Address:	04700h-04703h		
This register contains the valid bits for entries 0-31 of TLBPEND structure (Cycles pending TLB translation).			
DWord		**Bit**	**Description**
0		31:0	**Valid bits per entry**

Valid Bit Vector 0 for VEBX

VEBXTLB_VLD_0 - Valid Bit Vector 0 for VEBX	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04B20h

This register contains the valid bits for entries 0-31 of VEBXTLB.

DWord	Bit	Description
0	31:0	**Valid Bit Vector 0 for VEBX** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 0 for Z

ZTLB_VLD_0 - Valid Bit Vector 0 for Z			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	04B34h		
This register contains the valid bits for entries 0-31 of ZTLB.			
DWord	**Bit**	**Description**	
0	31:0	**Valid Bit Vector 0 for Z** Default Value: 00000000h Access: RO Valid Bits per Entry.	

Valid Bit Vector 1 for CVS

CVSTLB_VLD_1 - Valid Bit Vector 1 for CVS	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04C04h

This register contains the valid bits for entries 0-31 of CVSTLB.

DWord	Bit	Description
0	31:0	**Valid Bit Vector 1 for CVS** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 1 for L3

L3TLB_VLD_1 - Valid Bit Vector 1 for L3		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04D04h	
This register contains the valid bits for entries 0-31 of L3TLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 1 for L3** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 1 for MFX

MFXTLB_VLD_1 - Valid Bit Vector 1 for MFX		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04BA4h	
This register contains the valid bits for entries 0-31 of MFXTLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 1 for MFX** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 1 for MFX SL1

MFXTLB_VLD_SL1_1 - Valid Bit Vector 1 for MFX SL1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04BC4h
This register contains the valid bits for entries 0-31 of MFX SL1 TLB.	

DWord	Bit	Description
0	31:0	**Valid Bit Vector 1 for MFX SL1** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 1 for MTTLB

MTTLB_VLD1 - Valid Bit Vector 1 for MTTLB	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	04784h-04787h

This register contains the valid bits for entries 0-31 of MTTLB (Texture and constant cache TLBVertex Fetch, Instruction Cache, and Command Streamer TLB).

DWord	Bit	Description
0	31:0	**Valid bits per entry**

Valid Bit Vector 1 for MTVICTLB

MTVICTLB_VLD1 - Valid Bit Vector 1 for MTVICTLB	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	0478Ch-0478Fh

This register contains the valid bits for entries 0-31 of VICTLB (Vertex Fetch, Instruction Cache, and Command Streamer TLB).

DWord	Bit	Description
0	31:0	**Valid bits per entry**

Valid Bit Vector 1 for RCC

RCCTLB_VLD_1 - Valid Bit Vector 1 for RCC		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04DA4h	
This register contains the valid bits for entries 0-31 of RCCTLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 1 for RCC** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 1 for RCCTLB

RCCTLB_VLD1 - Valid Bit Vector 1 for RCCTLB			
Register Space:	MMIO: 0/2/0		
Source:	RenderCS		
Default Value:	0x00000000		
Access:	RO		
Size (in bits):	32		
Trusted Type:	1		
Address:	04794h-04797h		
This register is reserved for future RCC TLB extension.			
DWord	**Bit**	**Description**	
0	31:0	**Reserved**	
		Format:	MBZ

Valid Bit Vector 1 for RCZTLB

RCZTLB_VLD1 - Valid Bit Vector 1 for RCZTLB	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	0479Ch-0479Fh

This register contains the valid bits for entries 0-31 of RCZTLB (Render Cache for Z (Depth), Hi Z, and Stencil TLB).

DWord	Bit	Description
0	31:0	**Valid bits per entry**

Valid Bit Vector 1 for RCZTLB

RCZTLB_VLD1 - Valid Bit Vector 1 for RCZTLB		
Register Space:	MMIO: 0/2/0	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	0479Ch-0479Fh	
This register contains the valid bits for entries 0-31 of RCZTLB (Render Cache for Z (Depth), Hi Z, and Stencil TLB).		
DWord	**Bit**	**Description**
0	31:0	**Valid bits per entry**

Valid Bit Vector 1 for TLBPEND registers

TLBPEND_VLD1 - Valid Bit Vector 1 for TLBPEND registers			
Register Space:	MMIO: 0/2/0		
Source:	RenderCS		
Default Value:	0x00000000		
Access:	R/W		
Size (in bits):	32		
Trusted Type:	1		
Address:	04704h-04707h		
This register contains the valid bits for entries 32-63 of TLBPEND structure (Cycles pending TLB translation).			
DWord		**Bit**	**Description**
0		31:0	**Valid bits per entry**

Valid Bit Vector 1 for VEBX

VEBXTLB_VLD_1 - Valid Bit Vector 1 for VEBX	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04B24h

This register contains the valid bits for entries 0-31 of VEBXTLB.

DWord	Bit	Description
0	31:0	**Valid Bit Vector 1 for VEBX** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 1 for Z

ZTLB_VLD_1 - Valid Bit Vector 1 for Z	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04B38h

This register contains the valid bits for entries 0-31 of ZTLB.

DWord	Bit	Description
0	31:0	**Valid Bit Vector 1 for Z** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 2 for CVS

CVSTLB_VLD_2 - Valid Bit Vector 2 for CVS			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	04C08h		
This register contains the valid bits for entries 0-31 of CVSTLB.			
DWord	**Bit**	**Description**	
0	31:0	**Valid Bit Vector 2 for CVS** Default Value: 00000000h Access: RO Valid Bits per Entry.	

Valid Bit Vector 2 for GAB

BWDTLB_VLD_3 - Valid Bit Vector 2 for GAB	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04DCCh

This register contains the valid bits for entries 0-31 of BWDTLB.

DWord	Bit	Description
0	31:0	**Valid Bit Vector 3 for GAB** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 2 for L3

L3TLB_VLD_2 - Valid Bit Vector 2 for L3			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	04D08h		
This register contains the valid bits for entries 0-31 of L3TLB.			
DWord	**Bit**	**Description**	
0	31:0	**Valid Bit Vector 2 for L3** Default Value: 00000000h Access: RO Valid Bits per Entry.	

Valid Bit Vector 2 for MFX

MFXTLB_VLD_2 - Valid Bit Vector 2 for MFX	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04BA8h

This register contains the valid bits for entries 0-31 of MFXTLB.

DWord	Bit	Description
0	31:0	**Valid Bit Vector 2 for MFX** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 2 for MFX SL1

MFXTLB_VLD_SL1_2 - Valid Bit Vector 2 for MFX SL1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04BC8h

This register contains the valid bits for entries 0-31 of MFX SL1 TLB.

DWord	Bit	Description
0	31:0	**Valid Bit Vector 2 for MFX SL1** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 2 for RCC

RCCTLB_VLD_2 - Valid Bit Vector 2 for RCC		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04DA8h	
This register contains the valid bits for entries 0-31 of RCCTLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 2 for RCC** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 2 for VEBX

VEBXTLB_VLD_2 - Valid Bit Vector 2 for VEBX		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B28h	
This register contains the valid bits for entries 0-31 of VEBXTLB2.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 2 for VEBX** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 2 for Z

ZTLB_VLD_2 - Valid Bit Vector 2 for Z			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	04B3Ch		
This register contains the valid bits for entries 0-31 of ZTLB.			
DWord	**Bit**	**Description**	
0	31:0	**Valid Bit Vector 2 for Z** Default Value: 00000000h Access: RO Valid Bits per Entry.	

Valid Bit Vector 3 for CVS

CVSTLB_VLD_3 - Valid Bit Vector 3 for CVS		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04C0Ch	
This register contains the valid bits for entries 0-31 of CVSTLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 3 for CVS** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 3 for L3

L3TLB_VLD_3 - Valid Bit Vector 3 for L3	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04D0Ch

This register contains the valid bits for entries 0-31 of L3TLB.

DWord	Bit	Description
0	31:0	**Valid Bit Vector 3 for L3** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 3 for MFX

MFXTLB_VLD_3 - Valid Bit Vector 3 for MFX		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04BACh	
This register contains the valid bits for entries 0-31 of MFXTLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 3 for MFX** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 3 for MFX SL1

MFXTLB_VLD_SL1_3 - Valid Bit Vector 3 for MFX SL1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04BCCh
This register contains the valid bits for entries 0-31 of MFX SL1 TLB.	

DWord	Bit	Description
0	31:0	**Valid Bit Vector 3 for MFX SL1** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 3 for RCC

RCCTLB_VLD_3 - Valid Bit Vector 3 for RCC	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04DACh

This register contains the valid bits for entries 0-31 of RCCTLB.

DWord	Bit	Description
0	31:0	**Valid Bit Vector 3 for RCC** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 3 for VEBX

VEBXTLB_VLD_3 - Valid Bit Vector 3 for VEBX			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	04B74h		
This register contains the valid bits for entries 0-31 of VEBXTLB2.			
DWord	**Bit**	**Description**	
0	31:0	**Valid Bit Vector 3 for VEBX**	
		Default Value:	00000000h
		Access:	RO
		Valid Bits per Entry.	

Valid Bit Vector 3 for Z

ZTLB_VLD_3 - Valid Bit Vector 3 for Z			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	04B40h		
This register contains the valid bits for entries 0-31 of ZTLB.			
DWord	**Bit**	**Description**	
0	31:0	**Valid Bit Vector 3 for Z**	
		Default Value:	00000000h
		Access:	RO
		Valid Bits per Entry.	

Valid Bit Vector 4 for L3

L3TLB_VLD_4 - Valid Bit Vector 4 for L3	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04D10h

This register contains the valid bits for entries 0-31 of L3TLB.

DWord	Bit	Description
0	31:0	**Valid Bit Vector 4 for L3** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 4 for MFX

MFXTLB_VLD_4 - Valid Bit Vector 4 for MFX			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	04BB0h		
This register contains the valid bits for entries 0-31 of MFXTLB.			
DWord	**Bit**	**Description**	
0	31:0	**Valid Bit Vector 4 for MFX** Default Value: 00000000h Access: RO Valid Bits per Entry.	

Valid Bit Vector 4 for MFX SL1

MFXTLB_VLD_SL1_4 - Valid Bit Vector 4 for MFX SL1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04BD0h
This register contains the valid bits for entries 0-31 of MFX SL1 TLB.	

DWord	Bit	Description
0	31:0	**Valid Bit Vector 4 for MFX SL1** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 4 for RCC

RCCTLB_VLD_4 - Valid Bit Vector 4 for RCC		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04DB0h	
This register contains the valid bits for entries 0-31 of RCCTLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 4 for RCC** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 4 for VEBX

VEBXTLB_VLD_4 - Valid Bit Vector 4 for VEBX		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B78h	
This register contains the valid bits for entries 0-31 of VEBXTLB2.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 4 for VEBX** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 4 for Z

ZTLB_VLD_4 - Valid Bit Vector 4 for Z		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B44h	
This register contains the valid bits for entries 0-31 of ZTLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 4 for Z** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 5 for L3

L3TLB_VLD_5 - Valid Bit Vector 5 for L3	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04D14h

This register contains the valid bits for entries 0-31 of L3TLB.

DWord	Bit	Description
0	31:0	**Valid Bit Vector 5 for L3** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 5 for MFX

MFXTLB_VLD_5 - Valid Bit Vector 5 for MFX		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04BB4h	
This register contains the valid bits for entries 0-31 of MFXTLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 5 for MFX** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 5 for MFX SL1

MFXTLB_VLD_SL1_5 - Valid Bit Vector 5 for MFX SL1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04BD4h
This register contains the valid bits for entries 0-31 of MFX SL1 TLB.	

DWord	Bit	Description
0	31:0	**Valid Bit Vector 5 for MFX SL1** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 5 for RCC

RCCTLB_VLD_5 - Valid Bit Vector 5 for RCC		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04DB4h	
This register contains the valid bits for entries 0-31 of RCCTLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 5 for RCC** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 5 for VEBX

VEBXTLB_VLD_5 - Valid Bit Vector 5 for VEBX	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04B7Ch

This register contains the valid bits for entries 0-31 of VEBXTLB2.

DWord	Bit	Description
0	31:0	**Valid Bit Vector 5 for VEBX** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 5 for Z

ZTLB_VLD_5 - Valid Bit Vector 5 for Z		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B48h	
This register contains the valid bits for entries 0-31 of ZTLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 5 for Z** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 6 for L3

L3TLB_VLD_6 - Valid Bit Vector 6 for L3		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04D18h	
This register contains the valid bits for entries 0-31 of L3TLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 6 for L3** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 6 for MFX

MFXTLB_VLD_6 - Valid Bit Vector 6 for MFX		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04BB8h	
This register contains the valid bits for entries 0-31 of MFXTLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 6 for MFX** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 6 for MFX SL1

MFXTLB_VLD_SL1_6 - Valid Bit Vector 6 for MFX SL1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04BD8h
This register contains the valid bits for entries 0-31 of MFX SL1 TLB.	

DWord	Bit	Description
0	31:0	**Valid Bit Vector 6 for MFX SL1** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 6 for RCC

RCCTLB_VLD_6 - Valid Bit Vector 6 for RCC		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04DB8h	
This register contains the valid bits for entries 0-31 of RCCTLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 6 for RCC** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 6 for Z

ZTLB_VLD_6 - Valid Bit Vector 6 for Z			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	04B4Ch		
This register contains the valid bits for entries 0-31 of ZTLB.			
DWord	**Bit**	**Description**	
0	31:0	**Valid Bit Vector 6 for Z**	
		Default Value:	00000000h
		Access:	RO
		Valid Bits per Entry.	

Valid Bit Vector 7 for L3

L3TLB_VLD_7 - Valid Bit Vector 7 for L3		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04D1Ch	
This register contains the valid bits for entries 0-31 of L3TLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 7 for L3** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 7 for MFX

MFXTLB_VLD_7 - Valid Bit Vector 7 for MFX		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04BBCh	
This register contains the valid bits for entries 0-31 of MFXTLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 7 for MFX** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 7 for MFX SL1

MFXTLB_VLD_SL1_7 - Valid Bit Vector 7 for MFX SL1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04BDCh
This register contains the valid bits for entries 0-31 of MFX SL1 TLB.	

DWord	Bit	Description
0	31:0	**Valid Bit Vector 7 for MFX SL1** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 7 for RCC

RCCTLB_VLD_7 - Valid Bit Vector 7 for RCC	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04DBCh

This register contains the valid bits for entries 0-31 of RCCTLB.

DWord	Bit	Description
0	31:0	**Valid Bit Vector 7 for RCC** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 7 for Z

ZTLB_VLD_7 - Valid Bit Vector 7 for Z		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B50h	
This register contains the valid bits for entries 0-31 of ZTLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 7 for Z** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 8 for L3

L3TLB_VLD_8 - Valid Bit Vector 8 for L3		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04D20h	
This register contains the valid bits for entries 0-31 of L3TLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 8 for L3** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 8 for RCC

RCCTLB_VLD_8 - Valid Bit Vector 8 for RCC		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B80h	
This register contains the valid bits for entries 0-31 of RCCTLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 8 for RCC** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 8 for Z

ZTLB_VLD_8 - Valid Bit Vector 8 for Z			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	04B54h		
This register contains the valid bits for entries 0-31 of ZTLB.			
DWord	**Bit**	**Description**	
0	31:0	**Valid Bit Vector 8 for Z**	
		Default Value:	00000000h
		Access:	RO
		Valid Bits per Entry.	

Valid Bit Vector 9 for L3

L3TLB_VLD_9 - Valid Bit Vector 9 for L3		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04D24h	
This register contains the valid bits for entries 0-31 of L3TLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 9 for L3** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 9 for RCC

RCCTLB_VLD_9 - Valid Bit Vector 9 for RCC		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B84h	
This register contains the valid bits for entries 0-31 of RCCTLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 9 for RCC** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 9 for Z

ZTLB_VLD_9 - Valid Bit Vector 9 for Z		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B58h	
This register contains the valid bits for entries 0-31 of ZTLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 9 for Z** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 10 for L3

L3TLB_VLD_10 - Valid Bit Vector 10 for L3	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04D28h

This register contains the valid bits for entries 0-31 of L3TLB.

DWord	Bit	Description
0	31:0	**Valid Bit Vector 10 for L3** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 10 for RCC

RCCTLB_VLD_10 - Valid Bit Vector 10 for RCC		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B88h	
This register contains the valid bits for entries 0-31 of RCCTLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 10 for RCC** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 10 for Z

ZTLB_VLD_10 - Valid Bit Vector 10 for Z		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B5Ch	
This register contains the valid bits for entries 0-31 of ZTLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 10 for Z** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 11 for L3

L3TLB_VLD_11 - Valid Bit Vector 11 for L3		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04D2Ch	
This register contains the valid bits for entries 0-31 of L3TLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 11 for L3** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 11 for RCC

RCCTLB_VLD_11 - Valid Bit Vector 11 for RCC		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B8Ch	
This register contains the valid bits for entries 0-31 of RCCTLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 11 for RCC** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 11 for Z

ZTLB_VLD_11 - Valid Bit Vector 11 for Z		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B60h	
This register contains the valid bits for entries 0-31 of ZTLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 11 for Z** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 12 for L3

L3TLB_VLD_12 - Valid Bit Vector 12 for L3	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04D30h

This register contains the valid bits for entries 0-31 of L3TLB.

DWord	Bit	Description
0	31:0	**Valid Bit Vector 12 for L3** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 12 for RCC

RCCTLB_VLD_12 - Valid Bit Vector 12 for RCC		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B90h	
This register contains the valid bits for entries 0-31 of RCCTLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 12 for RCC** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 12 for Z

ZTLB_VLD_12 - Valid Bit Vector 12 for Z		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B64h	
This register contains the valid bits for entries 0-31 of ZTLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 12 for Z** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 13 for L3

L3TLB_VLD_13 - Valid Bit Vector 13 for L3	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04D34h

This register contains the valid bits for entries 0-31 of L3TLB.

DWord	Bit	Description
0	31:0	**Valid Bit Vector 13 for L3** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 13 for RCC

RCCTLB_VLD_13 - Valid Bit Vector 13 for RCC		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B94h	
This register contains the valid bits for entries 0-31 of RCCTLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 13 for RCC** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 13 for Z

ZTLB_VLD_13 - Valid Bit Vector 13 for Z			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	04B68h		
This register contains the valid bits for entries 0-31 of ZTLB.			
DWord	**Bit**	**Description**	
0	31:0	**Valid Bit Vector 13 for Z**	
		Default Value:	00000000h
		Access:	RO
		Valid Bits per Entry.	

Valid Bit Vector 14 for L3

L3TLB_VLD_14 - Valid Bit Vector 14 for L3	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04D38h

This register contains the valid bits for entries 0-31 of L3TLB.

DWord	Bit	Description
0	31:0	**Valid Bit Vector 14 for L3** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 14 for Z

ZTLB_VLD_14 - Valid Bit Vector 14 for Z		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B6Ch	
This register contains the valid bits for entries 0-31 of ZTLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 14 for Z** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 15 for L3

L3TLB_VLD_15 - Valid Bit Vector 15 for L3	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04D3Ch

This register contains the valid bits for entries 0-31 of L3TLB.

DWord	Bit	Description
0	31:0	**Valid Bit Vector 15 for L3** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 15 for Z

ZTLB_VLD_15 - Valid Bit Vector 15 for Z		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B70h	
This register contains the valid bits for entries 0-31 of ZTLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 15 for Z** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 16 for L3

L3TLB_VLD_16 - Valid Bit Vector 16 for L3	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04D40h

This register contains the valid bits for entries 0-31 of L3TLB.

DWord	Bit	Description
0	31:0	**Valid Bit Vector 16 for L3** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 17 for L3

L3TLB_VLD_17 - Valid Bit Vector 17 for L3		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04D44h	
This register contains the valid bits for entries 0-31 of L3TLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 17 for L3** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 18 for L3

L3TLB_VLD_18 - Valid Bit Vector 18 for L3	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04D48h

This register contains the valid bits for entries 0-31 of L3TLB.

DWord	Bit	Description
0	31:0	**Valid Bit Vector 18 for L3** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 19 for L3

L3TLB_VLD_19 - Valid Bit Vector 19 for L3		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04D4Ch	
This register contains the valid bits for entries 0-31 of L3TLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 19 for L3** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 20 for L3

L3TLB_VLD_20 - Valid Bit Vector 20 for L3	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04D50h

This register contains the valid bits for entries 0-31 of L3TLB.

DWord	Bit	Description
0	31:0	**Valid Bit Vector 20 for L3** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 21 for L3

L3TLB_VLD_21 - Valid Bit Vector 21 for L3	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04D54h

This register contains the valid bits for entries 0-31 of L3TLB.

DWord	Bit	Description
0	31:0	**Valid Bit Vector 21 for L3** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 22 for L3

L3TLB_VLD_22 - Valid Bit Vector 22 for L3	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04D58h

This register contains the valid bits for entries 0-31 of L3TLB.

DWord	Bit	Description
0	31:0	**Valid Bit Vector 22 for L3** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector 23 for L3

L3TLB_VLD_23 - Valid Bit Vector 23 for L3		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04D5Ch	
This register contains the valid bits for entries 0-31 of L3TLB.		

DWord	Bit	Description
0	31:0	**Valid Bit Vector 23 for L3** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector for VLF

VLFTLB_VLD - Valid Bit Vector for VLF	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	04B30h

This register contains the valid bits for entries 0-31 of VLFTLB.

DWord	Bit	Description
0	31:0	**Valid Bit Vector for VLF** Default Value: 00000000h Access: RO Valid Bits per Entry.

Valid Bit Vector for VLFSL1

VLFSL1TLB_VLD - Valid Bit Vector for VLFSL1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B2Ch	
This register contains the valid bits for entries 0-31 of VLFSL1TLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector for VLFSL1** Default Value: 00000000h Access: RO Valid Bits per Entry.

VCS2 CSB Fifo Status Register

VCS2_CSB_FSR - VCS2 CSB Fifo Status Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	0C5D0h
Name:	VCS2 CSB Fifo Status Register
ShortName:	VCS2_CSB_FSR

This RO register holds status of the CSB fifo.

DWord	Bit	Description
0	31	**Not Empty** Access: RO
	30:13	**Reserved**
	12:8	**FIFO Maximum Occupancy Count**
	7:5	**Reserved**
	4:0	**FIFO Occupancy Count** Access: RO

VCW Clock Count

VCW_CLOCK_CNT - VCW Clock Count		
Register Space:	MMIO: 0/2/0	
Source:	VideoEnhancementCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	08820h	
Address:	08920h	
DWord	**Bit**	**Description**
0	31:24	**Reserved** Format: MBZ
	23:0	**Max clock count** Default Value: 0h Maximum number of clocks taken by VCW to process a column

VCW Internal Latency

VCW_INTERNAL_LAT - VCW Internal Latency

Register Space:	MMIO: 0/2/0
Source:	VideoEnhancementCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	08824h
Address:	08924h

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:0	**VCW internal data latency count** Default Value: 0h

VCW Min Max Latency

VCW_MINMAX_LAT - VCW Min Max Latency		
Register Space:	MMIO: 0/2/0	
Source:	VideoEnhancementCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	08828h	
Address:	08928h	

DWord	Bit	Description
0	31:16	**Current request count** Default Value: 0h
	15:8	**Max latency** Default Value: 0h Maximum number of clocks taken for tag 200h
	7:0	**Min latency** Default Value: 0h Minimum number of clocks taken for tag 200h

VCW Total Latency

VCW_TOTAL_LAT - VCW Total Latency		
Register Space:	MMIO: 0/2/0	
Source:	VideoEnhancementCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	0882Ch	
Address:	0892Ch	

DWord	Bit	Description
0	31:0	**Total latency** Default Value: 0h Accumumation of latency per frame for tag 200h

VCW XY position

VCW_XY_POS - VCW XY position		
Register Space:	MMIO: 0/2/0	
Source:	VideoEnhancementCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	08830h	
Address:	08930h	
DWord	**Bit**	**Description**
0	31:16	**Current Y value** Default Value: 0h Current Y position of VCW walker
	15:0	**Current X value** Default Value: 0h Current X position of VCW walker

VEBOX MOCS Register0

VEBOX_MOCS_0 - VEBOX MOCS Register0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030 [KBL]
Size (in bits):	32
Address:	0CB00h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_0 - VEBOX MOCS Register0

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register1

VEBOX_MOCS_1 - VEBOX MOCS Register1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034 [KBL]
Size (in bits):	32
Address:	0CB04h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_1 - VEBOX MOCS Register1

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register2

VEBOX_MOCS_2 - VEBOX MOCS Register2

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038 [KBL]
Size (in bits):	32
Address:	0CB08h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_2 - VEBOX MOCS Register2

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register3

VEBOX_MOCS_3 - VEBOX MOCS Register3

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031 [KBL]
Size (in bits):	32
Address:	0CB0Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_3 - VEBOX MOCS Register3

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register4

VEBOX_MOCS_4 - VEBOX MOCS Register4

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032 [KBL]
Size (in bits):	32
Address:	0CB10h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_4 - VEBOX MOCS Register4

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register5

VEBOX_MOCS_5 - VEBOX MOCS Register5

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036 [KBL]
Size (in bits):	32
Address:	0CB14h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_5 - VEBOX MOCS Register5

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register6

VEBOX_MOCS_6 - VEBOX MOCS Register6

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A [KBL]
Size (in bits):	32
Address:	0CB18h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_6 - VEBOX MOCS Register6

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register7

VEBOX_MOCS_7 - VEBOX MOCS Register7

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033 [KBL]
Size (in bits):	32
Address:	0CB1Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_7 - VEBOX MOCS Register7

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register8

VEBOX_MOCS_8 - VEBOX MOCS Register8

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037 [KBL]
Size (in bits):	32
Address:	0CB20h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_8 - VEBOX MOCS Register8

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register9

VEBOX_MOCS_9 - VEBOX MOCS Register9

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B [KBL]
Size (in bits):	32
Address:	0CB24h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_9 - VEBOX MOCS Register9

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register10

VEBOX_MOCS_10 - VEBOX MOCS Register10

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032 [KBL]
Size (in bits):	32
Address:	0CB28h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_10 - VEBOX MOCS Register10

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register11

VEBOX_MOCS_11 - VEBOX MOCS Register11

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036 [KBL]
Size (in bits):	32
Address:	0CB2Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_11 - VEBOX MOCS Register11

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register12

VEBOX_MOCS_12 - VEBOX MOCS Register12

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A [KBL]
Size (in bits):	32
Address:	0CB30h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_12 - VEBOX MOCS Register12

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register13

VEBOX_MOCS_13 - VEBOX MOCS Register13

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033 [KBL]
Size (in bits):	32
Address:	0CB34h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_13 - VEBOX MOCS Register13

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register14

VEBOX_MOCS_14 - VEBOX MOCS Register14

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037 [KBL]
Size (in bits):	32
Address:	0CB38h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_14 - VEBOX MOCS Register14

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register15

VEBOX_MOCS_15 - VEBOX MOCS Register15

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B [KBL]
Size (in bits):	32
Address:	0CB3Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_15 - VEBOX MOCS Register15

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register16

VEBOX_MOCS_16 - VEBOX MOCS Register16

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030 [KBL]
Size (in bits):	32
Address:	0CB40h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_16 - VEBOX MOCS Register16

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register17

VEBOX_MOCS_17 - VEBOX MOCS Register17

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034 [KBL]
Size (in bits):	32
Address:	0CB44h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_17 - VEBOX MOCS Register17

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register18

VEBOX_MOCS_18 - VEBOX MOCS Register18

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038 [KBL]
Size (in bits):	32
Address:	0CB48h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_18 - VEBOX MOCS Register18

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register19

VEBOX_MOCS_19 - VEBOX MOCS Register19

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031 [KBL]
Size (in bits):	32
Address:	0CB4Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_19 - VEBOX MOCS Register19

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register20

VEBOX_MOCS_20 - VEBOX MOCS Register20

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032 [KBL]
Size (in bits):	32
Address:	0CB50h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_20 - VEBOX MOCS Register20

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register21

VEBOX_MOCS_21 - VEBOX MOCS Register21

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036 [KBL]
Size (in bits):	32
Address:	0CB54h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_21 - VEBOX MOCS Register21

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register22

VEBOX_MOCS_22 - VEBOX MOCS Register22

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A [KBL]
Size (in bits):	32
Address:	0CB58h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_22 - VEBOX MOCS Register22

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register23

VEBOX_MOCS_23 - VEBOX MOCS Register23

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033 [KBL]
Size (in bits):	32
Address:	0CB5Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_23 - VEBOX MOCS Register23

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register24

VEBOX_MOCS_24 - VEBOX MOCS Register24

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037 [KBL]
Size (in bits):	32
Address:	0CB60h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_24 - VEBOX MOCS Register24

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register25

VEBOX_MOCS_25 - VEBOX MOCS Register25

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B [KBL]
Size (in bits):	32
Address:	0CB64h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_25 - VEBOX MOCS Register25

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register26

VEBOX_MOCS_26 - VEBOX MOCS Register26

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032 [KBL]
Size (in bits):	32
Address:	0CB68h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_26 - VEBOX MOCS Register26

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register27

VEBOX_MOCS_27 - VEBOX MOCS Register27

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036 [KBL]
Size (in bits):	32
Address:	0CB6Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_27 - VEBOX MOCS Register27

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register28

VEBOX_MOCS_28 - VEBOX MOCS Register28

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A [KBL]
Size (in bits):	32
Address:	0CB70h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_28 - VEBOX MOCS Register28

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register29

VEBOX_MOCS_29 - VEBOX MOCS Register29

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033 [KBL]
Size (in bits):	32
Address:	0CB74h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_29 - VEBOX MOCS Register29

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register30

VEBOX_MOCS_30 - VEBOX MOCS Register30

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037 [KBL]
Size (in bits):	32
Address:	0CB78h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_30 - VEBOX MOCS Register30

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register31

VEBOX_MOCS_31 - VEBOX MOCS Register31

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B [KBL]
Size (in bits):	32
Address:	0CB7Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_31 - VEBOX MOCS Register31

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register32

VEBOX_MOCS_32 - VEBOX MOCS Register32

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030 [KBL]
Size (in bits):	32
Address:	0CB80h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_32 - VEBOX MOCS Register32

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register33

VEBOX_MOCS_33 - VEBOX MOCS Register33

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034 [KBL]
Size (in bits):	32
Address:	0CB84h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_33 - VEBOX MOCS Register33

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register34

VEBOX_MOCS_34 - VEBOX MOCS Register34

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038 [KBL]
Size (in bits):	32
Address:	0CB88h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_34 - VEBOX MOCS Register34

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register35

VEBOX_MOCS_35 - VEBOX MOCS Register35

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031 [KBL]
Size (in bits):	32
Address:	0CB8Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_35 - VEBOX MOCS Register35

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register36

VEBOX_MOCS_36 - VEBOX MOCS Register36

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032 [KBL]
Size (in bits):	32
Address:	0CB90h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_36 - VEBOX MOCS Register36

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register37

VEBOX_MOCS_37 - VEBOX MOCS Register37

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036 [KBL]
Size (in bits):	32
Address:	0CB94h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_37 - VEBOX MOCS Register37

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register38

VEBOX_MOCS_38 - VEBOX MOCS Register38

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A [KBL]
Size (in bits):	32
Address:	0CB98h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_38 - VEBOX MOCS Register38

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register39

VEBOX_MOCS_39 - VEBOX MOCS Register39

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033 [KBL]
Size (in bits):	32
Address:	0CB9Ch

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_39 - VEBOX MOCS Register39

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register40

VEBOX_MOCS_40 - VEBOX MOCS Register40

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037 [KBL]
Size (in bits):	32
Address:	0CBA0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_40 - VEBOX MOCS Register40

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register41

VEBOX_MOCS_41 - VEBOX MOCS Register41

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B [KBL]
Size (in bits):	32
Address:	0CBA4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_41 - VEBOX MOCS Register41

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register42

VEBOX_MOCS_42 - VEBOX MOCS Register42

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032 [KBL]
Size (in bits):	32
Address:	0CBA8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_42 - VEBOX MOCS Register42

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register43

VEBOX_MOCS_43 - VEBOX MOCS Register43

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036 [KBL]
Size (in bits):	32
Address:	0CBACh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_43 - VEBOX MOCS Register43

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register44

VEBOX_MOCS_44 - VEBOX MOCS Register44

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A [KBL]
Size (in bits):	32
Address:	0CBB0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_44 - VEBOX MOCS Register44

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register45

VEBOX_MOCS_45 - VEBOX MOCS Register45

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033 [KBL]
Size (in bits):	32
Address:	0CBB4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_45 - VEBOX MOCS Register45

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register46

VEBOX_MOCS_46 - VEBOX MOCS Register46

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037 [KBL]
Size (in bits):	32
Address:	0CBB8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 0000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_46 - VEBOX MOCS Register46

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register47

VEBOX_MOCS_47 - VEBOX MOCS Register47

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B [KBL]
Size (in bits):	32
Address:	0CBBCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_47 - VEBOX MOCS Register47

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register48

VEBOX_MOCS_48 - VEBOX MOCS Register48

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000030 [KBL]
Size (in bits):	32
Address:	0CBC0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_48 - VEBOX MOCS Register48

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register49

VEBOX_MOCS_49 - VEBOX MOCS Register49

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000034 [KBL]
Size (in bits):	32
Address:	0CBC4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_49 - VEBOX MOCS Register49

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register50

VEBOX_MOCS_50 - VEBOX MOCS Register50

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000038 [KBL]
Size (in bits):	32
Address:	0CBC8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_50 - VEBOX MOCS Register50

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register51

VEBOX_MOCS_51 - VEBOX MOCS Register51

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000031 [KBL]
Size (in bits):	32
Address:	0CBCCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_51 - VEBOX MOCS Register51

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register52

VEBOX_MOCS_52 - VEBOX MOCS Register52

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032 [KBL]
Size (in bits):	32
Address:	0CBD0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_52 - VEBOX MOCS Register52

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register53

VEBOX_MOCS_53 - VEBOX MOCS Register53

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036 [KBL]
Size (in bits):	32
Address:	0CBD4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_53 - VEBOX MOCS Register53

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register54

VEBOX_MOCS_54 - VEBOX MOCS Register54

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A [KBL]
Size (in bits):	32
Address:	0CBD8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_54 - VEBOX MOCS Register54

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register55

VEBOX_MOCS_55 - VEBOX MOCS Register55

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033 [KBL]
Size (in bits):	32
Address:	0CBDCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_55 - VEBOX MOCS Register55

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register56

VEBOX_MOCS_56 - VEBOX MOCS Register56

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037 [KBL]
Size (in bits):	32
Address:	0CBE0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_56 - VEBOX MOCS Register56

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register57

VEBOX_MOCS_57 - VEBOX MOCS Register57

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B [KBL]
Size (in bits):	32
Address:	0CBE4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_57 - VEBOX MOCS Register57

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register58

VEBOX_MOCS_58 - VEBOX MOCS Register58

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000032 [KBL]
Size (in bits):	32
Address:	0CBE8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_58 - VEBOX MOCS Register58

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register59

VEBOX_MOCS_59 - VEBOX MOCS Register59

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000036 [KBL]
Size (in bits):	32
Address:	0CBECh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 000000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_59 - VEBOX MOCS Register59

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register60

VEBOX_MOCS_60 - VEBOX MOCS Register60

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003A [KBL]
Size (in bits):	32
Address:	0CBF0h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_60 - VEBOX MOCS Register60

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register61

VEBOX_MOCS_61 - VEBOX MOCS Register61

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000033 [KBL]
Size (in bits):	32
Address:	0CBF4h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_61 - VEBOX MOCS Register61

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register62

VEBOX_MOCS_62 - VEBOX MOCS Register62

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000037 [KBL]
Size (in bits):	32
Address:	0CBF8h

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_62 - VEBOX MOCS Register62

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX MOCS Register63

VEBOX_MOCS_63 - VEBOX MOCS Register63

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0000003B [KBL]
Size (in bits):	32
Address:	0CBFCh

MOCS register

DWord	Bit	Description
0	31:15	**Reserved** Default Value: 00000000000000000b Access: RO
	14	**Reserved1** Default Value: 0b Access: RO
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC

VEBOX_MOCS_63 - VEBOX MOCS Register63

	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)

VEBOX TLB Control Register

VTCR - VEBOX TLB Control Register

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	04270h

DWord	Bit	Description
0	31:1	**Reserved** Default Value: 00000000000000000000000000000000b Access: RO
	0	**Invalidate TLBs on the corresponding Engine** Default Value: 0b Access: R/W SW writes 1 to invalidate the TLBs for the associated engine and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs. This bit is self clear.

VEBX Context Element Descriptor (High Part)

VEBX_CTX_EDR_H - VEBX Context Element Descriptor (High Part)		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	044C4h	
DWord	**Bit**	**Description**
0	31:0	**VEBX Context Element Descriptor (High Part)** Default Value: 00000000h Access: R/W

VEBX Context Element Descriptor (Low Part)

VEBX_CTX_EDR_L - VEBX Context Element Descriptor (Low Part)		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000009	
Size (in bits):	32	
Address:	044C0h	
DWord	**Bit**	**Description**
0	31:0	**VEBX Context Element Descriptor (Low Part)** Default Value: 00000009h Access: R/W

VEBX Fault Counter

VEBX_FAULT_CNTR - VEBX Fault Counter		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	045C0h	
DWord	**Bit**	**Description**
0	31:0	**VEBX Fault Counter** Default Value: 00000000h Access: RO This counter only applies to advance context when fault and stream mode is selected.

VEBX Fixed Counter

VEBX_FIXED_CNTR - VEBX Fixed Counter		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	045C4h	
DWord	**Bit**	**Description**
0	31:0	**VEBX Fixed Counter** Default Value: 00000000h Access: RO This counter only applies to advance context when fault and stream mode is selected.

VEBX LRA 0

VEBX_LRA_0 - VEBX LRA 0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x6F201F00	
Size (in bits):	32	
Address:	04A80h	
DWord	**Bit**	**Description**
0	31:24	**VEBX LRA1 Max** Default Value: 01101111b Access: R/W Maximum value of programmable LRA1.
	23:16	**VEBX LRA1 Min** Default Value: 00100000b Access: R/W Minimum value of programmable LRA1.
	15:8	**VEBX LRA0 Max** Default Value: 00011111b Access: R/W Maximum value of programmable LRA0.
	7:0	**VEBXLRA0 Min** Default Value: 00000000b Access: R/W Minimum value of programmable LRA0.

VEBX LRA 1

VEBX_LRA_1 - VEBX LRA 1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0600BF70
Size (in bits):	32
Address:	04A84h

DWord	Bit	Description
0	31:30	**Reserved** Default Value: 00b Access: RO
	29:28	**VECS** Default Value: 00b Access: R/W Which LRA should VECS use.
	27:26	**VFW** Default Value: 01b Access: R/W Which LRA should VFW use.
	25:24	**VEO** Default Value: 10b Access: R/W Which LRA should VEO use.
	15:8	**VEBXLRA2 Max** Default Value: 10111111b Access: R/W Minimum value of programmable LRA2.
	7:0	**VEBXLRA2 Min** Default Value: 01110000b Access: R/W Minimum value of programmable LRA2.

VEBX PDP0/PML4/PASID Descriptor (High Part)

VEBX_CTX_PDP0_H - VEBX PDP0/PML4/PASID Descriptor (High Part)

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	044CCh

DWord	Bit	Description
0	31:0	**VEBX PDP0/PML4/PASID Descriptor (High Part)** Default Value: 00000000h Access: R/W

VEBX PDP0/PML4/PASID Descriptor (Low Part)

VEBX_CTX_PDP0_L - VEBX PDP0/PML4/PASID Descriptor (Low Part)

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	044C8h

DWord	Bit	Description
0	31:0	**VEBX PDP0/PML4/PASID Descriptor (Low Part)** Default Value: 00000000h Access: R/W

VEBX PDP1 Descriptor Register (High Part)

VEBX_CTX_PDP1_H - VEBX PDP1 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	044D4h	
DWord	**Bit**	**Description**
0	31:0	**VEBX PDP1 Descriptor Register (High Part)** Default Value: 00000000h Access: R/W

VEBX PDP1 Descriptor Register (Low Part)

VEBX_CTX_PDP1_L - VEBX PDP1 Descriptor Register (Low Part)		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	044D0h	
DWord	**Bit**	**Description**
0	31:0	**VEBX PDP1 Descriptor Register (Low Part)** Default Value: 00000000h Access: R/W

VEBX PDP2 Descriptor Register (High Part)

VEBX_CTX_PDP2_H - VEBX PDP2 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	044DCh	
DWord	**Bit**	**Description**
0	31:0	**VEBX PDP2 Descriptor Register (High Part)** Default Value: 00000000h Access: R/W

VEBX PDP2 Descriptor Register (Low Part)

VEBX_CTX_PDP2_L - VEBX PDP2 Descriptor Register (Low Part)		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	044D8h	
DWord	**Bit**	**Description**
0	31:0	**VEBX PDP2 Descriptor Register (Low Part)** Default Value: 00000000h Access: R/W

VEBX PDP3 Descriptor Register (High Part)

VEBX_CTX_PDP3_H - VEBX PDP3 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	044E4h	
DWord	**Bit**	**Description**
0	31:0	**VEBX PDP3 Descriptor Register (High Part)** Default Value: 00000000h Access: R/W

VEBX PDP3 Descriptor Register (Low Part)

VEBX_CTX_PDP3_L - VEBX PDP3 Descriptor Register (Low Part)		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	044E0h	
DWord	**Bit**	**Description**
0	31:0	**VEBX PDP3 Descriptor Register (Low Part)** Default Value: 00000000h Access: R/W

VECS CSB Fifo Status Register

VECS_CSB_FSR - VECS CSB Fifo Status Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	0C5D4h
Name:	VECS CSB Fifo Status Register
ShortName:	VECS_CSB_FSR

This RO register holds status of the CSB fifo.

DWord	Bit	Description
0	31	**Not Empty** Access: RO
	30:13	**Reserved**
	12:8	**FIFO Maximum Occupancy Count**
	7:5	**Reserved**
	4:0	**FIFO Occupancy Count** Access: RO

Vendor Identification

VID2_0_2_0_PCI - Vendor Identification		
Register Space:	PCI: 0/2/0	
Source:	BSpec	
Default Value:	0x00008086	
Size (in bits):	16	
Address:	00000h	
This register combined with the Device Identification register uniquely identifies any PCI device.		
DWord	**Bit**	**Description**
0	15:0	**Vendor Identification Number** Default Value: 1000000010000110b Access: RO PCI standard identification for Intel.

VEO Current Pipe 0 XY Register

VEO_CURRENT0_XY - VEO Current Pipe 0 XY Register	
Register Space:	MMIO: 0/2/0
Source:	VideoEnhancementCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	08854h
Address:	08954h

DWord	Bit	Description
0	31:30	**Reserved**
	29:16	**Current Input Pipe 0 X** Default Value: 0h
	15	**Reserved**
	14:0	**Current Input Pipe 0 Y** Default Value: 0h

VEO DN Pipe 0 XY Register

VEO_DN0_XY - VEO DN Pipe 0 XY Register			
Register Space:	MMIO: 0/2/0		
Source:	VideoEnhancementCS		
Default Value:	0x00000000		
Access:	RO		
Size (in bits):	32		
Trusted Type:	1		
Address:	0884Ch		
Address:	0894Ch		
DWord	**Bit**	**Description**	
0	31:30	**Reserved**	
	29:16	**DN Pipe 0 X**	
		Default Value:	0h
		dn_input_x[13:0]	
	15	**Reserved**	
	14:0	**DN Pipe 0 Y**	
		Default Value:	0h
		dn_input_y[14:0]	

VEO DN Pipe 1 XY Register

VEO_DN1_XY - VEO DN Pipe 1 XY Register			
Register Space:	MMIO: 0/2/0		
Source:	VideoEnhancementCS		
Default Value:	0x00000000		
Access:	RO		
Size (in bits):	32		
Trusted Type:	1		
Address:	08850h		
Address:	08950h		
DWord	**Bit**	**Description**	
0	31:30	**Reserved**	
	29:16	**DN Pipe 1 X**	
		Default Value:	0h
	15	**Reserved**	
	14:0	**DN Pipe 1 Y**	
		Default Value:	0h

VEO DV Count Register

VEO_DV_COUNT - VEO DV Count Register		
Register Space:	MMIO: 0/2/0	
Source:	VideoEnhancementCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	08844h	
Address:	08944h	
DWord	**Bit**	**Description**
0	31:24	**Pipe1 Motion History DV/Hold Maxcount** Default Value: 0h
	23:16	**Pipe1 Pixel History DV/Hold Maxcount** Default Value: 0h
	15:8	**Pipe0 Motion History DV/Hold Maxcount** Default Value: 0h
	7:0	**Pipe0 Pixel History DV/Hold Maxcount** Default Value: 0h

VEO DV Hold Register

VEO_DVHOLD - VEO DV Hold Register		
Register Space:	MMIO: 0/2/0	
Source:	VideoEnhancementCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	0885Ch	
Address:	0895Ch	
Datavalid/Hold signals for VEO interface		
DWord	**Bit**	**Description**
0	31	**vdn_p0_veo_pixel_dv** Default Value: 0h
	30	**veo_vdn_p0_pixel_hold** Default Value: 0h
	29	**vdn_p0_veo_mh_dv** Default Value: 0h
	28	**veo_vdn_p0_mh_hold** Default Value: 0h
	27	**vdn_p0_veo_bne_luma_dv** Default Value: 0h
	26	**veo_vdn_p0_bne_luma_hold** Default Value: 0h
	25	**vdn_p0_veo_bne_chroma_dv** Default Value: 0h
	24	**veo_vdn_p0_bne_chroma_hold** Default Value: 0h
	23	**vdi_p0_veo_pixel_dv** Default Value: 0h
	22	**veo_vdi_p0_pixel_hold** Default Value: 0h
	21	**vdi_p0_veo_stmm_dv** Default Value: 0h

VEO_DVHOLD - VEO DV Hold Register

	20	**veo_vdi_p0_stmm_hold** Default Value: 0h
	19	**vdi_p0_veo_fmd_dv** Default Value: 0h
	18	**veo_vdi_p0_fmd_hold** Default Value: 0h
	17	**iecp_p0_veo_dv** Default Value: 0h
	16	**veo_iecp_p0_hold** Default Value: 0h
	15	**vdn_p1_veo_pixel_dv** Default Value: 0h
	14	**veo_vdn_p1_pixel_hold** Default Value: 0h
	13	**vdn_p1_veo_mh_dv** Default Value: 0h
	12	**veo_vdn_p1_mh_hold** Default Value: 0h
	11	**vdn_p1_veo_bne_luma_dv** Default Value: 0h
	10	**veo_vdn_p1_bne_luma_hold** Default Value: 0h
	9	**vdn_p1_veo_bne_chroma_dv** Default Value: 0h
	8	**veo_vdn_p1_bne_chroma_hold** Default Value: 0h
	7	**vdi_p1_veo_pixel_dv** Default Value: 0h
	6	**veo_vdi_p1_pixel_hold** Default Value: 0h
	5	**vdi_p1_veo_stmm_dv** Default Value: 0h
	4	**veo_vdi_p1_stmm_hold** Default Value: 0h

VEO_DVHOLD - VEO DV Hold Register		
	3	**vdi_p1_veo_fmd_dv** Default Value: 0h
	2	**veo_vdi_p1_fmd_hold** Default Value: 0h
	1	**iecp_p1_veo_dv** Default Value: 0h
	0	**veo_iecp_p1_hold** Default Value: 0h

VEO IECP DV Count Register

VEO_IECP_DV_COUNT - VEO IECP DV Count Register			
Register Space:	MMIO: 0/2/0		
Source:	VideoEnhancementCS		
Default Value:	0x00000000		
Access:	RO		
Size (in bits):	32		
Trusted Type:	1		
Address:	08848h		
Address:	08948h		
DWord	**Bit**	**Description**	
0	31:24	**IECP DV/Hold Maxcount**	
		Default Value:	0h
	23:16	**DI/FMD DV/Hold Maxcount**	
		Default Value:	0h
	15:8	**DI/STMM DV/Hold Maxcount**	
		Default Value:	0h
	7:0	**DI Pixel DV/Hold Maxcount**	
		Default Value:	0h

VEO Previous Pipe 0 XY Register

VEO_PREVIOUS0_XY - VEO Previous Pipe 0 XY Register			
Register Space:	MMIO: 0/2/0		
Source:	VideoEnhancementCS		
Default Value:	0x00000000		
Access:	RO		
Size (in bits):	32		
Trusted Type:	1		
Address:	08858h		
Address:	08958h		
DWord	**Bit**	**Description**	
0	31:30	**Reserved**	
	29:16	**Previous Input Pipe 0 X**	
		Default Value:	0h
	15	**Reserved**	
	14:0	**Previous Input Pipe 0 Y**	
		Default Value:	0h

VEO State Register

VEO_STATE - VEO State Register

Register Space:	MMIO: 0/2/0
Source:	VideoEnhancementCS
Default Value:	0x00048000 [KBL]
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	08840h
Address:	08940h

Data valids and holds for the statistics interface

DWord	Bit	Description
0	31	**iecp_p0_veo_his_dv** Default Value: 0h
	30	**iecp_p0_veo_skin_dv** Default Value: 0h
	29	**iecp_p0_veo_rgb_his_dv** Default Value: 0h
	28	**iecp_p0_veo_out_dist_dv** Default Value: 0h
	27	**iecp_p1_veo_his_dv** Default Value: 0h
	26	**iecp_p1_veo_skin_dv** Default Value: 0h
	25	**iecp_p1_veo_out_dist_dv** Default Value: 0h
	24	**veo_iecp_p0_rgb_his_hold** Default Value: 0h
	23	**Reserved**
	22:19	**VSC_FSM_State** Default Value: 0h State of the VEO_VSC_CNTRL state machine
	18:16	**GAV Command Credit Count** Value: 4h — Name: **[Default]**

VEO_STATE - VEO State Register

	15:12	**GAV Data Credit Count** **Value** / **Name** 8h / **[Default]**
	11:8	**Reserved** Format: MBZ
	7:0	**GAV Stall Clk Cnt Max** Default Value: 0h The longest stall from GAV since the beginning of the frame.

Vertex Fetch Context Offset

VF_CXT_OFFSET - Vertex Fetch Context Offset

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00001EC0
Access:	R/W
Size (in bits):	32
Address:	021BCh

DWord	Bit	Description
0	31:6	**VF Offset** Format: U26 This field indicates the offset (64bytes granular) in to the logical rendering context to which Vertex Fetch unit context is save/restored. This field register must not be written directly (via MMIO) unless the Command Streamer is completely idle (i.e., the Ring Buffer is empty and the pipeline is idle) and RC6 is disabled. One way to program this register is via Load Register Immediate command in the ring buffer as part of initialization sequence. Value: 7Bh — Name: **[Default]** — Description:
	5:0	**Reserved** Format: MBZ

VE SFC Forced Lock Acknowledgement Register

VE_SFC_FORCED_LOCK_ACK - VE SFC Forced Lock Acknowledgement Register		
Register Space:	MMIO: 0/2/0	
Source:	VideoEnhancementCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Address:	08818h	
DWord	**Bit**	**Description**
0	31:1	**Reserved** Format: MBZ
	0	**VE_SFC_FORCED_LOCK_ACK** Format: U1 This bit can only be set by hardware and it has to be clear by hardware as well. This bit is going to be polled by driver. This bit indicates that VE has received MFX_SFC_Forced_Lock from driver and it has sent that signal to SFC. Once this bit is set, it indicates SFC status (lock or unlock) will not be changed anymore. Driver will be safe to start the reset process after this bit is set. Hardware has to de-assert this bit after driver de-assert VE_SFC_Forced_Lock as well.

VE SFC Forced Lock Register

VE_SFC_FORCED_LOCK - VE SFC Forced Lock Register		
Register Space:	MMIO: 0/2/0	
Source:	VideoEnhancementCS	
Default Value:	0x00000000	
Access:	WO	
Size (in bits):	32	
Address:	0881Ch	
DWord	**Bit**	**Description**
0	31:1	**Reserved** Format: MBZ
	0	**VE_SFC_FORCED_LOCK** Format: U1 This bit can only be set by driver and it has to be clear by driver as well. Driver should set this bit before issuing the software (watchdog timer) reset. It tells VEBox that a software reset is going to happen. VE then issues a forced lock to SFC. If SFC is currently locked to VE, SFC should not unlock itself from VE. If SFC is NOT currently locked to VE, SFC should not accept the lock request from VE. Driver needs to clear this bit after the software reset sequence is complete.

VE VFW SFC Usage Register

VE_SFC_USAGE - VE VFW SFC Usage Register		
Register Space:	MMIO: 0/2/0	
Source:	VideoEnhancementCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Address:	08814h	
DWord	**Bit**	**Description**
0	31:1	**Reserved** Format: MBZ
	0	**VE_SFC_USAGE** Format: U1 This bit can only be set by hardware and it has to be clear by hardware as well. This bit indicates SFC is currently locked to VE. This bit should be set after SFC accepts the lock request from VE. This bit should be clear once SFC finishes the workload and unlocked from VEBox. In case a reset happens on MFX, this bit must be reset once a new workload is received

VF Scratch Pad

VFSKPD - VF Scratch Pad

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	083A8h-083ABh

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask[15:0] Must be set to modify corresponding bit in Bits 15:0. (All bits implemented)
	15	**Reserved** Access: r/w Format: PBC
	14:13	**Reserved** Access: r/w Format: PBC
	12	**Reserved** Access: r/w Format: PBC
	11	**Reserved** Access: r/w Format: PBC
	10	**Reserved** Access: r/w Format: PBC
	9	**Reserved** Access: r/w Format: PBC
	8	**Reserved** Access: r/w Format: PBC

VFSKPD - VF Scratch Pad

7	**Reserved**
	Access: r/w
	Format: PBC
6	**Autostrip Disable**
	Access: r/w
	Format: U1

Value	Name	Description
0h	Enable **[Default]**	The VF can generate "autostrip" primitives from TRILIST inputs (if/when possible).
1h	Disable	VF will not generate "autostrip" primitives.

5	**TLB Prefectch Enable**
	Access: r/w
	Format: U1

Value	Name	Description
0h	Disable **[Default]**	The VF will generate prefetch of TLB when it is fetching sequential vertex data and four or fewer vertex buffers are valid.
1h	Enable	VF will disable prefetch of TLB entries.

4	**Reserved**
	Access: r/w
	Format: PBC
3	**Nullprim early credit release disable**
	Access: r/w

Value	Name	Description
0h	**[Default]**	The nullprim credit release will be returned to csunit when the upper pipe of vfunit is emtpy.
1h		The nullprim credit release will be returned to csunit when the upper pipe and the lower pipe of vfunit are emtpy.

2	**Vertex Cache Implicit Disable Inhibit**
	Access: r/w
	Format: U1

Value	Name	Description
0h	**[Default]**	Allow VF to disable VS0 when Sequential index or Prim ID is a valid Element.
1h		VF never implicitly disables the vertex cache. Software must disable the VS0 Cache when required.

VFSKPD - VF Scratch Pad

1 Disable Over Fetch Cache

Access:	r/w

Value	Name	Description
0h	**[Default]**	Cache will check for data in cache before making a request to memory
1h		Always re-fetch new data from memory.

Programming Notes
Note that the Disable Multiple Miss Read squash bit must be cleared for Disable Over Fetch Cache to be set.

0 Disable Multiple Miss Read squash

Access:	r/w
Format:	Disable

Value	Name	Description
0h	**[Default]**	Allow VF to squash reads that are to the same cacheline for vertex buffer requests.
1h		Disallow VF from squashing reads that are to the same cacheline for vertex buffer requests.

VFW Credit Count Register

VFW_CREDIT_CNT - VFW Credit Count Register		
Register Space:	MMIO: 0/2/0	
Source:	VideoEnhancementCS	
Default Value:	0x00000004 [KBL]	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	08810h	
Address:	08910h	

DWord	Bit	Description
0	31:8	**Reserved**
	7:0	**Credit Count** The number of outstanding credits between VFW and GAV. If zero VEBOX cannot proceed due to GAV not releasing credits.

Value	Name
4h	**[Default]**

VGA_CONTROL

VGA_CONTROL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x80000000
Access:	R/W
Size (in bits):	32
Address:	41000h-41003h
Name:	VGA Control
ShortName:	VGA_CONTROL
Power:	PG0
Reset:	global

Restriction

Restriction : VGA requires panel fitting to be enabled.
VGA is always connected to pipe A.
VGA can not be enabled while the display power well is powered down.
VGA display should only be enabled if all display planes other than VGA are disabled.

DWord	Bit	Description
0	31	**VGA Display Disable** This bit will disable the VGA compatible display mode. It has no effect on VGA register or A0000-BFFFF memory aperture accesses which are controlled by the PCI configuration and VGA I/O register settings. **Value** / **Name** 0b – Enable 1b – Disable **[Default]** **Restriction** Restriction : The VGA SR01 screen off bit must be programmed when enabling and disabling VGA. See the VGA Registers document.
	30:27	**Reserved** Format: PBC
	26	**VGA Border Enable** This bit determines if the VGA border areas are included in the active display area. The border will be scaled along with the pixel data. **Value** / **Name** 0b – Disable 1b – Enable

VGA_CONTROL

	25	**Reserved** Format: PBC
	24	**Pipe CSC Enable** **Description** This bit enables pipe color space conversion for the VGA pixel data. **Value** / **Name** 0b Disable 1b Enable
	23:21	**Reserved** Format: PBC
	20	**Legacy 8Bit Palette En** This bit affects reads and writes to the palette through VGA I/O addresses. In the 6-bit mode, the 8-bits of data are shifted up two bits on the write (upper two bits are lost) and shifted two bits down on the read. This provides backward compatibility for original VGA programs as well as VESA VBE support for 8-bit palette. It does not affect palette accesses through the palette register MMIO path. **Value** / **Name** 0b 6 bit DAC 1b 8 bit DAC
	19	**Reserved**
	18	**Reserved**
	17:16	**Reserved** Format: PBC
	15:12	**Reserved**
	11:8	**Reserved**
	7:6	**Blink Duty Cycle** Controls the VGA text mode blink duty cycle relative to the VGA cursor blink duty cycle. **Value** / **Name** / **Description** 00b 100% 100% Duty Cycle, Full Cursor Rate 01b 25% 25% Duty Cycle, 1/2 Cursor Rate 10b 50% 50% Duty Cycle, 1/2 Cursor Rate 11b 75% 75% Duty Cycle, 1/2 Cursor Rate

VGA_CONTROL		
	5:0	**VSYNC Blink Rate** Controls the VGA blink rate in terms of the number of VSYNCs per on/off cycle. **Programming Notes** Program with (VSYNCs/cycle)/2-1

VIC Virtual page Address Registers

VICTLB_VA - VIC Virtual page Address Registers

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	04900h-04903h

These registers are directly mapped to the current Virtual Addresses in the VICTLB (Vertex Fetch, Instruction Cache, and Command Streamer TLB.)

DWord	Bit	Description
0	31:12	**Address** Format: GraphicsAddress[31:12] Page virtual address.
	11:0	**Reserved** Format: MBZ

VIDEO_DIP_CTL

VIDEO_DIP_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	60200h-60203h
Name:	Transcoder A Video Data Island Packet Control
ShortName:	VIDEO_DIP_CTL_A
Power:	PG2
Reset:	soft
Address:	61200h-61203h
Name:	Transcoder B Video Data Island Packet Control
ShortName:	VIDEO_DIP_CTL_B
Power:	PG2
Reset:	soft
Address:	62200h-62203h
Name:	Transcoder C Video Data Island Packet Control
ShortName:	VIDEO_DIP_CTL_C
Power:	PG2
Reset:	soft
Address:	6F200h-6F203h
Name:	Transcoder EDP Video Data Island Packet Control
ShortName:	VIDEO_DIP_CTL_EDP
Power:	PG1
Reset:	soft

Each type of Video DIP will be sent once each frame while it is enabled.

Restriction
Restriction : Transcoder EDP going to DDI A supports only VSC DIP.

DWord	Bit	Description
0	31:29	**Reserved**
	28	**Reserved**
	27	**Reserved**
	26:25	**Reserved**

VIDEO_DIP_CTL

	24	**Reserved**
	23:21	**Reserved**
	20	**VDIP Enable VSC** This bit enables the output of the Video Stream Configuration DIP. **Value** / **Name** 0b – Disable VSC DIP 1b – Enable VSC DIP **Restriction** Restriction : VSC can only be enabled with DisplayPort. VSC should be enabled prior to enabling PSR or stereo 3D if VSC will be used to transmit stereo 3D related information.
	19:17	**Reserved**
	16	**VDIP Enable GCP** This bit enables the output of the General Control Packet (GCP) DIP. GCP is different from other DIPs in that much of the payload is automatically reflected in the packet, and therefore there is a VIDEO_DIP_GCP register instead of DIP data buffers for GCP. **Value** / **Name** 0b – Disable GCP DIP 1b – Enable GCP DIP **Restriction** Restriction : GCP is only supported with HDMI when the bits per color is not equal to 8. GCP must be enabled prior to enabling TRANS_DDI_FUNC_CTL for HDMI with bits per color not equal to 8 and disabled after disabling TRANS_DDI_FUNC_CTL
	15:13	**Reserved**
	12	**VDIP Enable AVI** This bit enables the output of the Auxiliary Video Information DIP. **Value** / **Name** 0b – Disable AVI DIP 1b – Enable AVI DIP **Restriction** Restriction : Only enable with HDMI.
	11:9	**Reserved**

VIDEO_DIP_CTL

	8	**VDIP Enable VS** This bit enables the output of the Vendor Specific (VS) DIP. **Value** / **Name** 0b – Disable VS DIP 1b – Enable VS DIP **Restriction** Restriction : Only enable with HDMI.
	7:5	**Reserved**
	4	**VDIP Enable GMP** This bit enables the output of the Gamut Metadata Packet (GMP) DIP. GMP can be enabled with either DisplayPort or HDMI. **Value** / **Name** 0b – Disable GMP DIP 1b – Enable GMP DIP **Restriction** Restriction : GMP is not supported on transcoder EDP going to DDI A.
	3:1	**Reserved**
	0	**VDIP Enable SPD** This bit enables the output of the Source Product Description (SPD) DIP. **Value** / **Name** 0b – Disable SPD DIP 1b – Enable SPD DIP **Restriction** Restriction : Only enable with HDMI.

VIDEO_DIP_DATA

VIDEO_DIP_DATA	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	60220h-6023Fh
Name:	Transcoder A Video Data Island Packet AVI Data
ShortName:	VIDEO_DIP_AVI_DATA_A_*
Power:	PG2
Reset:	soft
Address:	60260h-6027Fh
Name:	Transcoder A Video Data Island Packet VS Data
ShortName:	VIDEO_DIP_VS_DATA_A_*
Power:	PG2
Reset:	soft
Address:	602A0h-602BFh
Name:	Transcoder A Video Data Island Packet SPD Data
ShortName:	VIDEO_DIP_SPD_DATA_A_*
Power:	PG2
Reset:	soft
Address:	602E0h-602FFh
Name:	Transcoder A Video Data Island Packet GMP Data
ShortName:	VIDEO_DIP_GMP_DATA_A_*
Power:	PG2
Reset:	soft
Address:	60320h-60343h
Name:	Transcoder A Video Data Island Packet VSC Data
ShortName:	VIDEO_DIP_VSC_DATA_A_*
Power:	PG2
Reset:	soft
Address:	61220h-6123Fh
Name:	Transcoder B Video Data Island Packet AVI Data
ShortName:	VIDEO_DIP_AVI_DATA_B_*

VIDEO_DIP_DATA

Power:	PG2
Reset:	soft
Address:	61260h-6127Fh
Name:	Transcoder B Video Data Island Packet VS Data
ShortName:	VIDEO_DIP_VS_DATA_B_*
Power:	PG2
Reset:	soft
Address:	612A0h-612BFh
Name:	Transcoder B Video Data Island Packet SPD Data
ShortName:	VIDEO_DIP_SPD_DATA_B_*
Power:	PG2
Reset:	soft
Address:	612E0h-612FFh
Name:	Transcoder B Video Data Island Packet GMP Data
ShortName:	VIDEO_DIP_GMP_DATA_B_*
Power:	PG2
Reset:	soft
Address:	61320h-61343h
Name:	Transcoder B Video Data Island Packet VSC Data
ShortName:	VIDEO_DIP_VSC_DATA_B_*
Power:	PG2
Reset:	soft
Address:	62220h-6223Fh
Name:	Transcoder C Video Data Island Packet AVI Data
ShortName:	VIDEO_DIP_AVI_DATA_C_*
Power:	PG2
Reset:	soft
Address:	62260h-6227Fh
Name:	Transcoder C Video Data Island Packet VS Data
ShortName:	VIDEO_DIP_VS_DATA_C_*
Power:	PG2
Reset:	soft
Address:	622A0h-622BFh
Name:	Transcoder C Video Data Island Packet SPD Data
ShortName:	VIDEO_DIP_SPD_DATA_C_*

VIDEO_DIP_DATA

Power:	PG2
Reset:	soft

Address:	622E0h-622FFh
Name:	Transcoder C Video Data Island Packet GMP Data
ShortName:	VIDEO_DIP_GMP_DATA_C_*
Power:	PG2
Reset:	soft

Address:	62320h-62343h
Name:	Transcoder C Video Data Island Packet VSC Data
ShortName:	VIDEO_DIP_VSC_DATA_C_*
Power:	PG2
Reset:	soft

Address:	6F320h-6F343h
Name:	Transcoder EDP Video Data Island Packet VSC Data
ShortName:	VIDEO_DIP_VSC_DATA_EDP_*
Power:	PG1
Reset:	soft

There are multiple instances of this register format per DIP type and per transcoder.

DWord	Bit	Description
0	31:0	**Video DIP DATA** This field contains the video DIP data to be transmitted. **Restriction** Restriction : Data should be loaded before enabling the transmission through the DIP type enable bit.

VIDEO_DIP_ECC

VIDEO_DIP_ECC	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	60240h-60247h
Name:	Transcoder A Video Data Island Packet AVI ECC
ShortName:	VIDEO_DIP_AVI_ECC_A_*
Power:	PG2
Reset:	soft
Address:	60280h-60287h
Name:	Transcoder A Video Data Island Packet VS ECC
ShortName:	VIDEO_DIP_VS_ECC_A_*
Power:	PG2
Reset:	soft
Address:	602C0h-602C7h
Name:	Transcoder A Video Data Island Packet SPD ECC
ShortName:	VIDEO_DIP_SPD_ECC_A_*
Power:	PG2
Reset:	soft
Address:	60300h-60313h
Name:	Transcoder A Video Data Island Packet GMP ECC
ShortName:	VIDEO_DIP_GMP_ECC_A_*
Power:	PG2
Reset:	soft
Address:	60344h-6034Fh
Name:	Transcoder A Video Data Island Packet VSC ECC
ShortName:	VIDEO_DIP_VSC_ECC_A_*
Power:	PG2
Reset:	soft
Address:	61240h-61247h
Name:	Transcoder B Video Data Island Packet AVI ECC
ShortName:	VIDEO_DIP_AVI_ECC_B_*

VIDEO_DIP_ECC	
Power:	PG2
Reset:	soft
Address:	61280h-61287h
Name:	Transcoder B Video Data Island Packet VS ECC
ShortName:	VIDEO_DIP_VS_ECC_B_*
Power:	PG2
Reset:	soft
Address:	612C0h-612C7h
Name:	Transcoder B Video Data Island Packet SPD ECC
ShortName:	VIDEO_DIP_SPD_ECC_B_*
Power:	PG2
Reset:	soft
Address:	61300h-61313h
Name:	Transcoder B Video Data Island Packet GMP ECC
ShortName:	VIDEO_DIP_GMP_ECC_B_*
Power:	PG2
Reset:	soft
Address:	61344h-6134Fh
Name:	Transcoder B Video Data Island Packet VSC ECC
ShortName:	VIDEO_DIP_VSC_ECC_B_*
Power:	PG2
Reset:	soft
Address:	62240h-62247h
Name:	Transcoder C Video Data Island Packet AVI ECC
ShortName:	VIDEO_DIP_AVI_ECC_C_*
Power:	PG2
Reset:	soft
Address:	62280h-62287h
Name:	Transcoder C Video Data Island Packet VS ECC
ShortName:	VIDEO_DIP_VS_ECC_C_*
Power:	PG2
Reset:	soft
Address:	622C0h-622C7h
Name:	Transcoder C Video Data Island Packet SPD ECC
ShortName:	VIDEO_DIP_SPD_ECC_C_*

VIDEO_DIP_ECC

Power:	PG2
Reset:	soft
Address:	62300h-62313h
Name:	Transcoder C Video Data Island Packet GMP ECC
ShortName:	VIDEO_DIP_GMP_ECC_C_*
Power:	PG2
Reset:	soft
Address:	62344h-6234Fh
Name:	Transcoder C Video Data Island Packet VSC ECC
ShortName:	VIDEO_DIP_VSC_ECC_C_*
Power:	PG2
Reset:	soft
Address:	6F344h-6F34Fh
Name:	Transcoder EDP Video Data Island Packet VSC ECC
ShortName:	VIDEO_DIP_VSC_ECC_EDP_*
Power:	PG1
Reset:	soft

There are multiple instances of this register format per DIP type and per transcoder.

DWord	Bit	Description
0	31:0	**Video DIP ECC** This field contains the video DIP ECC value for read back.

VIDEO_DIP_GCP

VIDEO_DIP_GCP

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32

Address:	60210h-60213h
Name:	Transcoder A Video Data Island Packet GCP
ShortName:	VIDEO_DIP_GCP_A
Power:	PG2
Reset:	soft

Address:	61210h-61213h
Name:	Transcoder B Video Data Island Packet GCP
ShortName:	VIDEO_DIP_GCP_B
Power:	PG2
Reset:	soft

Address:	62210h-62213h
Name:	Transcoder C Video Data Island Packet GCP
ShortName:	VIDEO_DIP_GCP_C
Power:	PG2
Reset:	soft

<table>
<tr><th>DWord</th><th>Bit</th><th>Description</th></tr>
<tr><td>0</td><td>31:3</td><td>Reserved
<table>
<tr><td>Format:</td><td>MBZ</td></tr>
</table></td></tr>
<tr><td></td><td>2</td><td>GCP color indication
<table>
<tr><th>Value</th><th>Name</th><th>Description</th></tr>
<tr><td>0b</td><td>Don't Indicate</td><td>Don't indicate color depth. CD and PP bits in GCP set to zero.</td></tr>
<tr><td>1b</td><td>Indicate</td><td>Indicate color depth using CD bits in GCP. The color depth value comes from the TRANS_DDI_FUNC_CTL register.</td></tr>
</table>
<table>
<tr><th>Restriction</th></tr>
<tr><td>Restriction : This bit must be set when in HDMI deep color (>8 BPC) mode.</td></tr>
</table></td></tr>
</table>

VIDEO_DIP_GCP

	1	**GCP default phase enable** GCP default phase indicates that video timings meet alignment requirements such that the following conditions are met: 1. Htotal is an even number 2. Hactive is an even number 3. Front and back porches for Hsync are even numbers 4. Vsync always starts on an even-numbered pixel within a line in interlaced modes (starting counting with 0)

Value	Name	Description
0b	Clear	Default phase bit in GCP is cleared.
1b	Set	Default phase bit in GCP is set.

Restriction
Restriction : Do not set this bit if these requirements are not met.

	0	**Reserved**

Video BIOS ROM Base Address

ROMADR_0_2_0_PCI - Video BIOS ROM Base Address

Register Space:	PCI: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	00030h

The IGD does not use a separate BIOS ROM, therefore this register is hardwired to 0s.

DWord	Bit	Description
0	31:18	**ROM Base Address** Default Value: 00000000000000b Access: RO Hardwired to 0's.
	17:11	**Address Mask** Default Value: 0000000b Access: RO Hardwired to 0s to indicate 256 KB address range.
	10:1	**Reserved** Format: MBZ
	0	**ROM BIOS Enable** Default Value: 0b Access: RO Hardwired to 0 to indicate ROM not accessible.

VS Invocation Counter

VS_INVOCATION_COUNT - VS Invocation Counter		
Register Space:	MMIO: 0/2/0	
Source:	RenderCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Trusted Type:	1	
Address:	02320h	
This register stores the value of the vertex count shaded by VS. This register is part of the context save and restore. More details about the precise event counted by this register are located **here**.		
DWord	**Bit**	**Description**
0	63:32	**VS Invocation Count Report UDW** Number of vertices that are dispatched as threads by the VS stage. Updated only when **Statistics Enable** is set in VS_STATE (see the Vertex Shader Chapter in the 3D Volume.)
	31:0	**VS Invocation Count Report LDW** Number of vertices that are dispatched as threads by the VS stage. Updated only when **Statistics Enable** is set in VS_STATE (see the Vertex Shader Chapter in the 3D Volume.)

VTd Status

VTD_STATUS_0_2_0_PCI - VTd Status		
Register Space:	PCI: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	8	
Address:	00063h	
This register contains indicator bits for Graphics VTd mode.		
DWord	**Bit**	**Description**
0	0	**GFX VTd Active** Default Value: 0b Access: RO Variant Firmware Only Reflects GFX VTd Mode is active. 1 - if active, 0 if inactive.

Wait For Event and Display Flip Flags Register

SYNC_FLIP_STATUS - Wait For Event and Display Flip Flags Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32

Address:	022D0h-022D3h
Name:	Wait For Event and Display Flip Flags Register
ShortName:	SYNC_FLIP_STATUS_RCSUNIT

Address:	122D0h-122D3h
Name:	Wait For Event and Display Flip Flags Register
ShortName:	SYNC_FLIP_STATUS_VCSUNIT0

Address:	1A2D0h-1A2D3h
Name:	Wait For Event and Display Flip Flags Register
ShortName:	SYNC_FLIP_STATUS_VECSUNIT

Address:	1C2D0h-1C2D3h
Name:	Wait For Event and Display Flip Flags Register
ShortName:	SYNC_FLIP_STATUS_VCSUNIT1

Address:	222D0h-222D3h
Name:	Wait For Event and Display Flip Flags Register
ShortName:	SYNC_FLIP_STATUS_BCSUNIT

This register is the saved value of what wait for events are still valid. This register is part of context save and restore for RC6 feature.

Programming Notes	Source
Programming Restriction: This register should NEVER be programmed by SW, this is for HW internal use only.	
VideoCS/VideoCS2/VideoEnhancementCS: This register functionality is not supported and must not be exercised for reads or writes.	VideoCS, VideoCS2, VideoEnhancementCS

DWord	Bit	Description
0	31	**Reserved** Format: MBZ

SYNC_FLIP_STATUS - Wait For Event and Display Flip Flags Register

	30	**Display Plane 1 Asyncronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 1 "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	29	**Display Plane 1 Syncronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 1 "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	28	**Display Plane 4 Syncronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 4 "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	27	**Reserved** Format: MBZ
	26	**Display Plane 2 Asyncronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 2 "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	25	**Display Plane 2 Syncronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS - Wait For Event and Display Flip Flags Register

	24	**Display Plane 5 Syncronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 5 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	23	**Reserved** Source: BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS Format: MBZ
	23	**Display Plane 1 Asyncronous Performance Flip Pending Wait Enable** Source: RenderCS Format: Enable This field enables a wait for the duration of a Display Plane 1 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	22	**Display Plane 1 Asyncronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 1 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	21	**Display Plane 1 Syncronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 1 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	20	**Display Plane 4 Syncronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 4 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS - Wait For Event and Display Flip Flags Register

	19	**Reserved** Format: MBZ
	18	**Display Pipe A Scan Line Wait Enable** Format: Enable This field enables a wait while a Display Pipe A Scan Line condition exists. This condition is defined as the the start of the scan line specified in the Pipe A Display Scan Line Count Range Compare Register. See Scan Line Event in the Device Programming Interface chapter of MI Functions.
	17	**Display Pipe A Vertical Blank Wait Enable** Format: Enable This field enables a wait until the next Display Pipe A Vertical Blank event occurs. This event is defined as the start of the next Display Pipe A vertical blank period. Note that this can cause a wait for up to an entire refresh period. See Vertical Blank Event (See Programming Interface).
	16	**Reserved** Format: MBZ
	15	**Reserved** Source: BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS Format: MBZ
	15	**Display Plane 2 Asyncronous Performance Flip Pending Wait Enable** Source: RenderCS Format: Enable This field enables a wait for the duration of a Display Plane 2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	14	**Display Plane 2 Asyncronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS - Wait For Event and Display Flip Flags Register

	13	**Display Plane 2 Syncronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	12	**Display Plane 5 Syncronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 5 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	11	**Reserved** Format: MBZ
	10	**Display Pipe B Scan Line Wait Enable** Format: Enable This field enables a wait while a Display Pipe B Scan Line condition exists. This condition is defined as the the start of the scan line specified in the Pipe B Display Scan Line Count Range Compare Register. See Scan Line Event in the Device Programming Interface chapter of MI Functions.
	9	**Display Pipe B Vertical Blank Wait Enable** Format: Enable This field enables a wait until the next Display Pipe B Vertical Blank event occurs. This event is defined as the start of the next Display Pipe B vertical blank period. Note that this can cause a wait for up to an entire refresh period. See Vertical Blank Event (See Programming Interface).
	8:0	**Reserved** Format: MBZ

Wait For Event and Display Flip Flags Register 1

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	022D4h-022D7h
Name:	Wait For Event and Display Flip Flags Register 1
ShortName:	SYNC_FLIP_STATUS_1_RCSUNIT
Address:	122D4h-122D7h
Name:	Wait For Event and Display Flip Flags Register 1
ShortName:	SYNC_FLIP_STATUS_1_VCSUNIT0
Address:	1A2D4h-1A2D7h
Name:	Wait For Event and Display Flip Flags Register 1
ShortName:	SYNC_FLIP_STATUS_1_VECSUNIT
Address:	1C2D4h-1C2D7h
Name:	Wait For Event and Display Flip Flags Register 1
ShortName:	SYNC_FLIP_STATUS_1_VCSUNIT1
Address:	222D4h-222D7h
Name:	Wait For Event and Display Flip Flags Register 1
ShortName:	SYNC_FLIP_STATUS_1_BCSUNIT

This register is the saved value of what wait for events are still valid. This register is part of context save and restore for RC6 feature.

Programming Notes	Source
Programming Restriction: This register should NEVER be programmed by SW, this is for HW internal use only.	
VideoCS/VideoCS2/VideoEnhancementCS: This register functionality is not supported and must not be exercised for reads or writes.	VideoCS, VideoCS2, VideoEnhancementCS

DWord	Bit	Description	
0	31:21	**Reserved**	
		Format:	MBZ

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

	20	**Display Plane 9 Synchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 9 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	19	**Display Plane 9 Synchronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 9 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	18	**Display Plane 8 Synchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 8 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	17	**Display Plane 8 Synchronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 8 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	16	**Display Plane 7 Synchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 7 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

	15	**Display Plane 7 Synchronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 7 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	14	**Display Pipe C Scan Line Event Pending** Format: Enable This field indicates scan line event operation is pending from Display Pipe C. This field gets set when MI_SCANLINE_INCL/EXCL command is parsed for Display Plane-C and gets reset on scan line event completion for Display Plane-C.
	13	**Display Pipe B Scan Line Event Pending** Format: Enable This field indicates scan line event operation is pending from Display Pipe B. This field gets set when MI_SCANLINE_INCL/EXCL command is parsed for Display Plane-B and gets reset on scan line event completion for Display Plane 3.
	12	**Display Pipe A Scan Line Event Pending** Format: Enable This field indicates scan line event operation is pending from Display Pipe A. This field gets set when MI_SCANLINE_INCL/EXCL command is parsed for Display Plane-A and gets reset on scan line event completion for Display Plane 1.
	11	**Reserved** Format: MBZ
	10	**Display Plane 3 Asyncronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	9	**Display Plane 3 Syncronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

	8	**Display Plane 6 Syncronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 6 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	7	**Reserved** Source: BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS Format: MBZ
	7	**Display Plane 3 Asyncronous Performance Flip Pending Wait Enable** Source: RenderCS Format: Enable This field enables a wait for the duration of a Display Plane 3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	6	**Display Plane 3 Asyncronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 3 "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	5	**Display Plane 3 Syncronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	4	**Display Plane 6 Syncronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 6 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

	3	**Reserved** Format: MBZ
	2	**Display Pipe C Scan Line Wait Enable** Format: Enable This field enables a wait while a Display Pipe C Scan Line condition exists. This condition is defined as the the start of the scan line specified in the Pipe C Display Scan Line Count Range Compare Register. See Scan Line Event in the Device Programming Interface chapter of MI Functions.
	1	**Display Pipe C Vertical Blank Wait Enable** Format: Enable This field enables a wait until the next Display Pipe C Vertical Blank event occurs. This event is defined as the start of the next Display Pipe C vertical blank period. Note that this can cause a wait for up to an entire refresh period. See Vertical Blank Event (See Programming Interface).
	0	**Reserved** Format: MBZ

Wait For Event and Display Flip Flags Register 2

SYNC_FLIP_STATUS_2 - Wait For Event and Display Flip Flags Register 2

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32

Address:	022ECh-022EFh
Name:	Wait For Event and Display Flip Flags Register 2
ShortName:	SYNC_FLIP_STATUS_2_RCSUNIT

Address:	122ECh-122EFh
Name:	Wait For Event and Display Flip Flags Register 2
ShortName:	SYNC_FLIP_STATUS_2_VCSUNIT0

Address:	1A2ECh-1A2EFh
Name:	Wait For Event and Display Flip Flags Register 2
ShortName:	SYNC_FLIP_STATUS_2_VECSUNIT

Address:	1C2ECh-1C2EFh
Name:	Wait For Event and Display Flip Flags Register 2
ShortName:	SYNC_FLIP_STATUS_2_VCSUNIT1

Address:	222ECh-222EFh
Name:	Wait For Event and Display Flip Flags Register 2
ShortName:	SYNC_FLIP_STATUS_2_BCSUNIT

This register is the saved value of what wait for events are still valid. This register is part of context save and restore for RC6 feature.

Programming Notes	Source
Programming Restriction: This register should NEVER be programmed by SW, this is for HW internal use only.	
VideoCS/VideoCS2/VideoEnhancementCS: This register functionality is not supported and must not be exercised for reads or writes.	VideoCS, VideoCS2, VideoEnhancementCS

DWord	Bit	Description
0	31:27	**Reserved** Format: MBZ

SYNC_FLIP_STATUS_2 - Wait For Event and Display Flip Flags Register 2

	26	**Display Plane 12 Asyncronous Performance Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 12 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	25	**Display Plane 12 Asyncronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 12 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	24	**Display Plane 12 Asyncronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 12 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	23	**Display Plane 11 Asyncronous Performance Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 11 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	22	**Display Plane 11 Asyncronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 11 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	21	**Display Plane 11 Asyncronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 11 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_2 - Wait For Event and Display Flip Flags Register 2

	20	**Display Plane 10 Asyncronous Performance Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 10 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	19	**Display Plane 10 Asyncronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 10 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	18	**Display Plane 10 Asyncronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 10 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	17	**Display Plane 9 Asyncronous Performance Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 9 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	16	**Display Plane 9 Asyncronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 9 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	15	**Display Plane 9 Asyncronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 9 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_2 - Wait For Event and Display Flip Flags Register 2

	14	**Display Plane 8 Asyncronous Performance Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 8 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	13	**Display Plane 8 Asyncronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 8 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	12	**Display Plane 8 Asyncronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 8 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	11	**Display Plane 7 Asyncronous Performance Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 7 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	10	**Display Plane 7 Asyncronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 7 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	9	**Display Plane 7 Asyncronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 7 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_2 - Wait For Event and Display Flip Flags Register 2

	8	**Display Plane 6 Asyncronous Performance Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 6 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	7	**Display Plane 6 Asyncronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 6 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	6	**Display Plane 6 Asyncronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 6 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	5	**Display Plane 5 Asyncronous Performance Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 5 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	4	**Display Plane 5 Asyncronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 5 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	3	**Display Plane 5 Asyncronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 5 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_2 - Wait For Event and Display Flip Flags Register 2

	2	**Display Plane 4 Asyncronous Performance Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 4 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	1	**Display Plane 4 Asyncronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 4 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	0	**Display Plane 4 Asyncronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 4 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

Walkers Fault Register

WF_REG - Walkers Fault Register

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32
Address:	04098h

DWord	Bit	Description
0	31:1	**Walkers Fault Register** Default Value: 00000000000000000000000000000000b Access: R/W All bits are only valid with bit[0]=1.
	0	**Valid Bit** Default Value: 0b Access: R/W This bit indicates that the first fault for this engine has been recorded. It can only be cleared by SW, which also clears the other fields.

Watchdog Counter

PR_CTR - Watchdog Counter

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	02190h-02193h
Name:	Watchdog Counter
ShortName:	PR_CTR_RCSUNIT
Address:	12190h-12193h
Name:	Watchdog Counter
ShortName:	PR_CTR_VCSUNIT0
Address:	1A190h-1A193h
Name:	Watchdog Counter
ShortName:	PR_CTR_VECSUNIT
Address:	1C190h-1C193h
Name:	Watchdog Counter
ShortName:	PR_CTR_VCSUNIT1
Address:	22190h-22193h
Name:	Watchdog Counter
ShortName:	PR_CTR_BCSUNIT

DWord	Bit	Description
0	31:0	**Counter Value** Format: U32 This register reflects the render watchdog counter value itself. It cannot be written to.

Watchdog Counter Control

PR_CTR_CTL - Watchdog Counter Control

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000001 [KBL]
Access:	R/W
Size (in bits):	32
Address:	02178h-0217Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_RCSUNIT
Address:	12178h-1217Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_VCSUNIT0
Address:	1A178h-1A17Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_VECSUNIT
Address:	1C178h-1C17Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_VCSUNIT1
Address:	22178h-2217Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_BCSUNIT

Programming Notes

Ring Buffer Mode of scheduling SW must enable and disable watch dog counter inline to a command sequence of any given workload within the same command buffer dispatch. Watch Dog counter once enabled doesn't stop unless it is explicitly disabled. SW must explicitly reset the watch dog counter by disabling it before enabling the watch dog counter for a new command sequence. Preemption could happen in a command sequence prior to watch dog counter getting disabled resulting in watch dog counter enabled following preemption. SW must explicitly take care of disabling the watch dog counter as part of the preemption sequence. Execution List Mode of Scheduling: SW must enable and disable watch dog counter inline to a command sequence of any given workload within the same command buffer dispatch. On a context switch "Watch Dog Counter Control" and "Watch dog Threshold" are context save restored, whereas watch dog counter gets reset to 0x0 and remains disabled until it gets enabled by another context during context restore or due to explicit programming. Watch dog counter value doesn't get accumulated across multiple submissions of a given context.

DWord	Bit	Description
0	31	**Count Select**

PR_CTR_CTL - Watchdog Counter Control

		Format: U1 **Value** / **Name** / **Description** 0h / **[Default]** / Use eight times the time stamp base unit to increment the watch dog count. The granularity of the time stamp base unit is defined in the "Time Stamp Bases" subsection in Power Management chapter. 1h / / Use the fixed function clock (csclk) to increment the watchdog count
	30:0	**Counter Logic Op** Default Value: 1h This field specifies the action to be taken by the clock counter to generate interrupts. Writing a Zero value to this register starts the counting. Writing a Value of 0000_0001 to this counter stops the counter.

Watchdog Counter Threshold

PR_CTR_THRSH - Watchdog Counter Threshold

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00145855
Access:	R/W
Size (in bits):	32
Address:	0217Ch-0217Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_RCSUNIT
Address:	1217Ch-1217Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_VCSUNIT0
Address:	1A17Ch-1A17Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_VECSUNIT
Address:	1C17Ch-1C17Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_VCSUNIT1
Address:	2217Ch-2217Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_BCSUNIT

DWord	Bit	Description
0	31:0	**Counter Logic Threshold** Default Value: 00145855h Format: U32 This field specifies the threshold that the hardware checks against for the value of the render clock counter before generating an interrupt. The counter in hardware generates an interrupt when the threshold is reached, rolls over and starts counting again. The interrupt generated is the "Media Hang Notify" interrupt since this watchdog timer is intended primarily to remedy VLD hangs on the main pipeline.

Window Hardware Generated Clear Value

WMHWCLRVAL - Window Hardware Generated Clear Value

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	05524h

This register reflects the count value of the OA Performance counter A30. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**WM HW Generated Clear Value** Format: MBZ This register stores HW generated Z clear value.

WM_LINETIME

WM_LINETIME	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	45270h-45273h
Name:	Pipe Watermark Line Time
ShortName:	WM_LINETIME_A
Power:	PG1
Reset:	soft
Address:	45274h-45277h
Name:	Pipe Watermark Line Time
ShortName:	WM_LINETIME_B
Power:	PG2
Reset:	soft
Address:	45278h-4527Bh
Name:	Pipe Watermark Line Time
ShortName:	WM_LINETIME_C
Power:	PG2
Reset:	soft

There is one instance of this register format per each pipe A, B, C.

DWord	Bit	Description
0	31:25	**Reserved**
	24:16	**Reserved**
	15:9	**Reserved**
	8:0	**Line Time** This field specifies the line time for the current screen resolution in units of 0.125us. **Programming Notes** Line time in microseconds = Pipe horizontal total number of pixels / pixel rate in MHz. Multiply by 8 to get units of 0.125us and round to nearest integer. Program the smallest line time when using multiple refresh rates. **Restriction** Restriction : The line time value must be programmed before enabling any display low power

WM_LINETIME		
		watermark. Maximum supported line time is 63.875us (111111111b).

WM_MISC

WM_MISC	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000 [KBL]
Access:	R/W
Size (in bits):	32
Address:	45260h-45263h
Name:	Watermark Miscellaneous
ShortName:	WM_MISC
Power:	PG0
Reset:	soft

DWord	Bit	Description
0	31	**Reserved** Format: PBC
	30:28	**Reserved**
	27	**Reserved** Format: PBC
	26:20	**Reserved** Format: PBC
	19:0	**Reserved**

WRID_VALID_REG0

WRID_VALID_REG0 - WRID_VALID_REG0		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04070h	
DWord	**Bit**	**Description**
0	31:0	**WRID_VALID_REG0** Default Value: 00000000h Access: RO This register is for WRID Comparison usage. RO register with IA Access Type on DEV reset. wrdp_wrid_valid_vector[31:0] There are 96 write buffer. Each bit indicate the buffer is valid if set. Divide into 3 registers to accommodate all 96 deep

WRID_VALID_REG1

WRID_VALID_REG1 - WRID_VALID_REG1		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04074h	
DWord	**Bit**	**Description**
0	31:0	**WRID_VALID_REG1** Default Value: 00000000h Access: RO This register is for WRID Comparison usage. RO register with IA Access Type on DEV reset. wrdp_wrid_valid_vector[63:32] There are 96 write buffer. Each bit indicate the buffer is valid if set. Divide into 3 registers to accommodate all 96 deep.

WRID_VALID_REG2

WRID_VALID_REG2 - WRID_VALID_REG2		
Register Space:	MMIO: 0/2/0	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04078h	
DWord	**Bit**	**Description**
0	31:0	**WRID_VALID_REG2** Default Value: 00000000h Access: RO This register is for WRID Comparison usage. RO register with IA Access Type on DEV reset. wrdp_wrid_valid_vector[95:64] There are 96 write buffer. Each bit indicate the buffer is valid if set. Divide into 3 registers to accommodate all 96 deep.

Write Watermark

WR_WATERMARK - Write Watermark

Register Space:	MMIO: 0/2/0
Default Value:	0x000FFEA4
Size (in bits):	32
Address:	04028h

DWord	Bit	Description
0	31:20	**Extra Bits** Default Value: 000000000000b Access: R/W
	19	**Watermark Timeout Enable** Default Value: 1b Access: R/W
	18:8	**Watermark Timeout** Default Value: 11111111110b Access: R/W Number of clocks that the write pipe queue is allowed to keep a ready write cycle, without reads or writes to the queue. Once this value is met, and if the feature is enabled, the watermark is considered reached, and all pending write requests are issued.
	7	**Watermark Enable** Default Value: 1b Access: R/W Enable Write Request Grouping
	6:0	**High Watermark** Default Value: 0100100b Access: R/W This is the number of write requests to be collected before initiating a write burst. Once a burst is initiated, it continues until all the available writes are requested.

WRPLL_CTL

WRPLL_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	46040h-46043h
Name:	WRPLL 1 Control
ShortName:	WRPLL_CTL1
Power:	PG0
Reset:	soft
Address:	46060h-46063h
Name:	WRPLL 2 Control
ShortName:	WRPLL_CTL2
Power:	PG0
Reset:	soft

Description

The register is used to enable DPLL2 (WRPLL 1) and DPLL3 (WRPLL 2).
DPLL frequency, SSC, and port mapping programming is done through the DPLL_CTRL* and DPLL*_CFGCR* registers.
There are two instances of this register format to support DPLL2 (WRPLL 1) and DPLL3 (WRPLL 2).

DWord	Bit	Description
0	31	**PLL Enable** This bit will enable or disable the PLL. Value / Name: 0b Disable; 1b Enable **Restriction** Restriction : This field must not be changed while any port is using this PLL. Restriction : Configure DPLL frequency and SSC prior to enabling.
	30	**Reserved** Format: MBZ
	29:28	**Reserved**

WRPLL_CTL		
	27:24	**Reserved** Format: MBZ
	23:16	**Reserved**
	15:14	**Reserved** Format: MBZ
	13:8	**Reserved**
	7:0	**Reserved**

ZTLB LRA 0

ZTLB_LRA_0 - ZTLB LRA 0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x0200FE00 [KBL]
Size (in bits):	32
Address:	04A30h

DWord	Bit	Description
0	31	**Reserved**
	30:29	**Reserved** Default Value: 00b Access: RO
	28:27	**STC LRA** Default Value: 00b Access: R/W Which LRA should STC use.
	26:18	**ZTLB LRA1 Min** Default Value: 010000000b Access: R/W Minimum value of programmable LRA1.
	17:9	**ZTLB LRA0 Max** Default Value: 001111111b Access: R/W Maximum value of programmable LRA0.
	8:0	**ZTLB LRA0 Min** Default Value: 000000000b Access: R/W Minimum value of programmable LRA0.

ZTLB LRA 1

ZTLB_LRA_1 - ZTLB LRA 1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x36BE813F [KBL]
Size (in bits):	32
Address:	04A34h

DWord	Bit	Description
0	31	**Reserved** Default Value: 0b Access: RO
	30:29	**HIZ LRA** Default Value: 01b Access: R/W Which LRA should HIZ use.
	28:27	**RCZ LRA** Default Value: 10b Access: R/W Which LRA should RCZ use.
	26:18	**ZTLB LRA2 Max** Default Value: 110101111b Access: R/W Maximum value of programmable LRA2. If ZTLBLRA3Min == ZTLBLRA3Max , GATR LRA is disabled, GATR cycles are mapped to ZTLBLRA0 If ZTLBLRA3Min == ZTLBLRA3Max , GATR LRA is disabled, ZTLBLRA2Max will default to ZTLBLRA3Max to reuse GATR entries
	17:9	**ZTLB LRA2 Min** Default Value: 101000000b Access: R/W Minimum value of programmable LRA2.
	8:0	**ZTLB LRA1 Max** Default Value: 100111111b Access: R/W Maximum value of programmable LRA1.

ZTLB LRA 2

ZTLB_LRA_2 - ZTLB LRA 2

Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x000F7FB0 [KBL]
Size (in bits):	32
Address:	04A38h

DWord	Bit	Description
0	31:20	**Reserved** Default Value: 000000000000b Access: RO
	19:18	**GATR LRA** Default Value: 11b Access: R/W Which LRA should GATR use.
	17:9	**ZTLB LRA3 Max** Access: R/W Maximum value of programmable LRA3. Value: 110111111b — Name: **[Default]**
	8:0	**ZTLB LRA3 Min** Access: R/W Minimum value of programmable LRA3. Value: 110110000b — Name: **[Default]**