1 Command FIS

A Command FIS is a Host to Device FIS Type (27h) with the C bit set to one. There are three Command Structure mappings into a Command FIS in the serial transport.

48-bit Command Transport mapping

28-bit Command and Non-Data Command Transport mapping

1.1 Command FIS - 48-bit Command Transport Mapping

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Features (7:0)								Command (7:0)								C 1	R	R	Reserved (0)					FIS Type (27h)							
1	Device (7:0)								LBA (23:0)																							
	R	L 1	R	D	R	R	R	R																								
2	Features (15:8)								LBA (24:47)																							
3	Control (7:0)								Reserved (0)								Sector Count (15:0)															
	H	R	R	R	R	S 0	N	Z 0																								
4	Reserved (0)								Reserved (0)								Reserved (0)								Reserved (0)							

Figure 1 - Command FIS - 48-bit Command Transport FIS layout

Field Definitions

FIS Type - Set to a value of 27h.

C - This bit shall be set to one to indicate that this FIS is a Command. (See x.x.x for a Control FIS description when C bit is cleared to zero).

Command - word 5 bits 7:0 of the Command Structure.

LBA - 48-bit value found in the Command Structure words 2, 3, and 4.

R - Reserved.

Control – Contains bits which are individually assigned to specific functions as defined below. In ATA-7, these bits were mapped to the Device Control Register of the Shadow Command Block for parallel ATA Emulation.

Z – Fixed, This bit shall be cleared to zero

N – Variable, this bit was mapped as the nIEN bit in ATA-7 parallel emulation. This bit is not used in the Serial Transport, and may be transmitted with a zero or a one value. It is recommended that it be cleared to zero.

S – Fixed, this bit shall be cleared to zero. This bit was mapped as the SRST bit in ATA-7 parallel emulation. (See x.x.x for SRST description of the Control FIS when C bit is cleared to zero).

H - Variable, this bit was mapped as the HOB bit in ATA-7 parallel emulation. This bit is not used in the Serial Transport, and may be transmitted with a zero or a one value. It is recommended that it be cleared to zero.

Device – Contains Word 5 bits 15:8 of the Command Structure. These bits are individually assigned to specific functions as defined below. In ATA-7, these bits were mapped to the Device Register of the Shadow Command Block for parallel ATA Emulation.

L – Fixed for all commands in the 48-bit feature set. This bit shall be set to one. This bit was mapped as the LBA bit in ATA-7.

D – Variable, this bit was mapped as the DEV bit in ATA-7 parallel emulation. This bit is not used in the Serial Transport, and may be transmitted with a zero or a one value. It is recommended that it be cleared to zero.

Features (7:0) - Contains word 0 bits 7:0 of the Command Structure (see x.x.x). In ATA-7 parallel emulation, this field was mapped to the Current Value in the Features Register.

Features (15:8) - Contains word 0 bits 15:8 of the Command Structure (see x.x.x). In ATA-7 parallel emulation, this field was mapped to the Previous Value in the Features Register.

Sector Count - word 1 bits 15:0 of the Command Structure.

Sector Count (7:0) - Contains word 1 bits 7:0 of the Command Structure (see x.x.x). In ATA-7 parallel emulation, this field was mapped to the Current Value in the sector count Register.

Sector Count (15:8) - Contains word 1 bits 15:8 of the Command Structure (see x.x.x). In ATA-7 parallel emulation, this field was mapped to the Previous Value in the Sector Count Register.

1.2 Command FIS - 28-bit Command and Non-data Command Transport Mapping

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Features (7:0)								Command (7:0)								C 1	R	R	Reserved (0)					FIS Type (27h)							
1	Device (7:0) R	L 1	R	D	LBA (27:24)				LBA (23:0)																							
2	Reserved (Note 4)								Reserved (Note 3)								Reserved (Note 2)								Reserved (Note 1)							
3	Control (7:0) H	R	R	R	R	S 0	N	Z 0	Reserved (0)								Reserved (Note 5)								Sector Count (7:0)							
4	Reserved (0)								Reserved (0)								Reserved (0)								Reserved (0)							

Figure 2 - Command FIS - 28-bit Command Transport FIS layout

Field Definitions

FIS Type - Set to a value of 27h.

C - This bit shall be set to one to indicate that this FIS is a Command. (See x.x.x for a Control FIS description when C bit is cleared to zero).

Command - word 5 bits 7:0 of the Command Structure.

LBA (23:0) - 16-bit value found in the Command Structure word 4 bits 15:0 and word 3 bits 7:0.

In ATA-7 parallel emulation, these bits were mapped to LBA Low, LBA Mid, and LBA High Registers of the Shadow Command block.

R - Reserved.

Control – Contains bits which are individually assigned to specific functions as defined below. In ATA-7, these bits were mapped to the Device Control Register of the Shadow Command Block for parallel ATA Emulation.

Z – Fixed, This bit shall be cleared to zero

N – Variable, this bit was mapped as the nIEN bit in ATA-7 parallel emulation. This bit is not used in the Serial Transport, and may be transmitted with a zero or a one value. It is recommended that it be cleared to zero.

S – Fixed, this bit shall be cleared to zero. This bit was mapped as the SRST bit in ATA-7 parallel emulation. (See x.x.x for SRST description of the Control FIS when C bit is cleared to zero).

H - Variable, this bit was mapped as the HOB bit in ATA-7 parallel emulation. This bit is not used in the Serial Transport, and may be transmitted with a zero or a one value. It is recommended that it be cleared to zero.

Device – Word 5 bits 15:8 of the Command Structure. These bits are individually assigned to specific functions as defined below. In ATA-7, these bits were mapped to the Device Register of the Shadow Command Block for parallel ATA Emulation.

LBA (27:24) – 4 bit value found in Command Structure word 3 bits 11:8.

In ATA-7 parallel emulation, these bits were mapped to the Device Register bits 0:3 of the Shadow Command block.

D – Variable, this bit was mapped as the DEV bit in ATA-7 parallel emulation. This bit is not used in the Serial Transport, and may be transmitted with a zero or a one value. It is recommended that it be cleared to zero.

L – Fixed for all commands in the 28-bit feature set. This bit shall be set to one. This bit was mapped as the LBA bit in ATA-7.

Features (7:0) - Contains word 0 bits 7:0 of the Command Structure (see x.x.x).

In ATA-7 parallel emulation, this field was mapped to the Current Value in the Features Register.

Sector Count - Contains word 1 bits 7:0 of the Command Structure (see x.x.x)

In ATA-7 parallel emulation, this field was mapped to the Current Value in the Sector Count Register.

Notes 1-5: This field is not used in the 28-bit command transport mapping in the Serial Transport. Due to prior implementations of ATA and parallel ATA emulation, this field may contain indeterminate values. It is recommended that it be cleared to zero.

Note 1: In ATA-7, this field was mapped to the LBA Low Previous Value of the Shadow Command Block.

Note 2: In ATA-7, this field was mapped to the LBA Mid Previous Value of the Shadow Command Block.

Note 3: In ATA-7, this field was mapped to the LBA High Previous Value of the Shadow Command Block.

Note 4: In ATA-7, this field was mapped to the Features Previous Value of the Shadow Command Block.

Note 5: In ATA-7, this field was mapped to the Sector Count Previous Value of the Shadow Command Block.

2 Control FIS

A Control FIS is a Host to Device FIS Type (27h) with the C bit set to zero. There is one Command Structure mapping into a Control FIS in the Serial Transport.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Reserved (Note 2)								Reserved (Note 1)								C 0	R	R	Reserved (0)					FIS Type (27h)							
1	Reserved (Note 4)								Reserved (Note 3)																							
2	Reserved (Note 6)								Reserved (Note 5)																							
3	Control (7:0)								Reserved (0)								Reserved (Note 8)								Reserved (Note 7)							
	H	R	R	R	R	S	N	Z 0																								
4	Reserved (0)								Reserved (0)								Reserved (0)								Reserved (0)							

Figure 3 - Control FIS - Serial Transport FIS layout

Field Definitions

FIS Type - Set to a value of 27h.

R - Reserved.

C - This bit shall be set to zero to indicate that this FIS is a Control FIS. (See x.x.x for a Command FIS description when the C bit is set to one).

Control – Contains bits which are individually assigned to specific functions as defined below. In ATA-7, these bits were mapped to the Device Control Register of the Shadow Command Block for parallel ATA Emulation.

Z – Fixed, This bit shall be cleared to zero

N – Variable, this bit was mapped as the nIEN bit in ATA-7 parallel emulation. This bit is not used in the Serial Transport, and may be transmitted with a zero or a one value. It is recommended that it be cleared to zero.

S – SRST, Soft Reset. When set to one, this bit indicates a Soft Reset operation is requested by the host. (see x.x.x for description of Soft Reset protocol).

H - Variable, this bit was mapped as the HOB bit in ATA-7 parallel emulation. This bit is not used in the Serial Transport, and may be transmitted with a zero or a one value. It is recommended that it be cleared to zero.

Notes 1-8: This field is not used in the Serial Transport Control FIS. Due to prior implementations of ATA and parallel ATA emulation, this field may contain indeterminate values. It is recommended that it be cleared to zero.

Note 1: In ATA-7 parallel emulation, these bits were mapped to the Command register.

Note 2: In ATA-7 parallel emulation, these bits were mapped to the Features register.

Note 3 - In ATA-7 parallel emulation, these bits were mapped to LBA Low, LBA Mid, and LBA High Registers.

Note 4: In ATA-7 parallel emulation, these bits were mapped to the Device register.

Note 5: In ATA-7 parallel emulation, these bits were mapped to the LBA Low (previous), LBA Mid (previous), and LBA High (previous) registers.

Note 6: In ATA-7 parallel emulation, these bits were mapped to the Features (previous) register.

Note 7: In ATA-7 parallel emulation, these bits were mapped to the Sector Count register.

Note 8: In ATA-7 parallel emulation, these bits were mapped to the Sector Count (previous) register.

3 Response FIS

A Response FIS is a Device to Host FIS Type (27h). There are two Command Structure Response mappings into a Response FIS in the serial transport.

48-bit Command Structure Response mapping

28-bit Command Structure Response mapping

3.1 Response FIS - 48-bit Command Structure Response Mapping

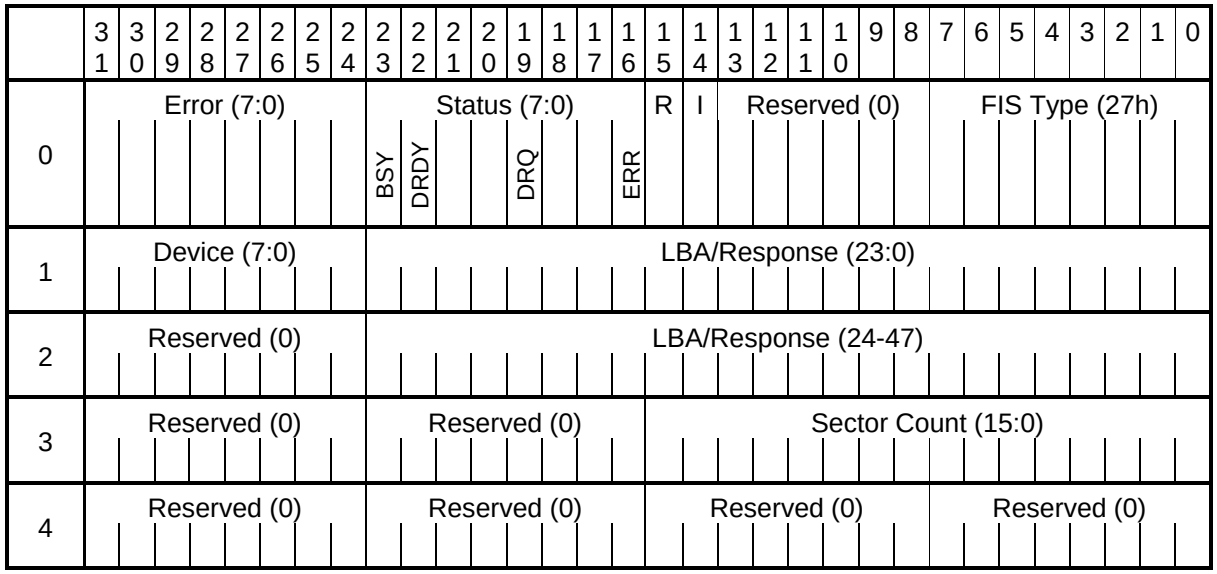

Figure 4 - Response FIS - 48-bit Command Structure Response FIS layout

Field Definitions

FIS Type - Set to a value of 27h.

I – Interrupt Pending. This bit reflects the Interrupt Pending state of the device. Behavior of this bit is command dependent.

Status - Word 5 bits 7:0 of the Command Structure response outputs.

Bit 0: ERR/CHK: (Error/Check) This bit indicates that an error or check condition occurred during the execution of a command. (See x.x.x for a complete description of ERR/CHK bit handling) In the Serial Transport Response FIS, its function is defined by the Device Transport state machines (see x.x.x)

Bit 1-2: Use of these bits is command dependent.

Bit 3: DRQ: (Data Request) This bit indicates that the device is ready to transfer data between the host and the device. Use of this bit is command and transfer protocol dependent. In the Serial Transport Response FIS, its function is defined by the Device Transport state machines (see x.x.x)

Bit 4-5: Use of these bits is command dependent.

Bit 6: DRDY (Device Ready) This bit is used to indicate device readiness to receive and attempt to execute all implemented commands. In the Serial Transport Response FIS, its function is defined by the Device Transport state machines (see x.x.x)

Bit 7: BSY (Busy) This bit is used to indicate that the device is busy. In some protocols, this bit is used in combination with DRQ (bit 3) to indicate readiness to transfer data. In the Serial Transport Response FIS, its function is defined by the Device Transport state machines (see x.x.x)

In ATA-7 parallel emulation, Status (7:0) were mapped to the Status register of the Command Block. In the Serial Transport, their function is defined by the Device Transport state machines (see x.x.x)

Device - Word 5 bits 15:8 of the Command Structure response outputs. Content of these bits is command dependent. In ATA-7 parallel emulation, these bits were mapped to the Device register.

Error - Word 0 bits 7:0 of the Command Structure response outputs. Content of these bits is command dependent and defined by the Command Structure response outputs. In ATA-7 parallel emulation, these bits were mapped to the Error register of the Command Block.

LBA/Response (23:0) – Lower 24 bits of the Command Structure response outputs words 2, 3, and 4.

In ATA-7 parallel emulation, these bits were mapped to LBA Low, LBA Mid, and LBA High Registers of the Command block.

LBA/Response (24:47) – Higher 24 bits of the Command Structure response words 2, 3, and 4.

In ATA-7 parallel emulation, these bits were mapped to the LBA Low (Previous), LBA Mid (Previous) and LBA High (Previous) registers of the Command block.

R - Reserved.

Sector Count – Contains word 1 bits 15:0 of the Command Structure response outputs.

Sector Count (7:0) - In ATA-7 parallel emulation, this field was mapped to the Current Value in the Sector Count Register.

Sector Count (15:8) - In ATA-7 parallel emulation, this field was mapped to the Previous Value in the Sector Count Register.

3.2 Response FIS - 28-bit Command and Non-Data Command Structure Response Mapping

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Error (7:0)								Status (7:0)								R	I	Reserved (0)						FIS Type (27h)							
									BSY	DRDY			DRQ			ERR																
1	Device (7:0)								LBA/Response (23:0)																							
2	Reserved (0))								Reserved (Note 3)								Reserved (Note 2)								Reserved (Note 1)							
3	Reserved (0)								Reserved (0)								Reserved (Note 4)								Sector Count (7:0)							
4	Reserved (0)								Reserved (0)								Reserved (0)								Reserved (0)							

Figure 5 - Response FIS - 28-bit Command Structure Response FIS layout

FIS Type - Set to a value of 27h.

I – Interrupt Pending. This bit reflects the Interrupt Pending state of the device. Behavior of this bit is command dependent.

Status - Word 5 bits 7:0 of the Command Structure response outputs.

Bit 0: ERR/CHK: (Error/Check) This bit indicates that an error or check condition occurred during the execution of a command. (See x.x.x for a complete description of ERR/CHK bit handling) In the Serial Transport Response FIS, its function is defined by the Device Transport state machines (see x.x.x)

Bit 1-2: Use of these bits is command dependent.

Bit 3: DRQ: (Data Request) This bit indicates that the device is ready to transfer data between the host and the device. Use of this bit is command and transfer protocol dependent. In the Serial Transport, the function is defined by the Device Transport state machines (see x.x.x)

Bit 4-5: Use of these bits is command dependent.

Bit 6: DRDY (Device Ready) This bit is used to indicate device readiness to receive and attempt to execute all implemented commands. In the Serial Transport Response FIS, its function is defined by the Device Transport state machines (see x.x.x)

Bit 7: BSY (Busy) This bit is used to indicate that the device is busy. In some protocols, this bit is used in combination with DRQ (bit 3) to indicate readiness to transfer data. In the Serial Transport Response FIS, its function is defined by the Device Transport state machines (see x.x.x)

In ATA-7 parallel emulation, Status (7:0) were mapped to the Status register of the Command Block.

Device - Word 5 bits 15:8 of the Command Structure response outputs. Content of these bits is command dependent.

Bits 0:3 are mapped to LBA 27:24 in 28-bit data commands error response outputs.

In ATA-7 parallel emulation, these bits were mapped to the Device register.

Error - Word 0 bits 7:0 of the Command Structure response outputs. Content of these bits is command dependent. In ATA-7 parallel emulation, these bits were mapped to the Error register of the Command Block.

LBA/Response (23:0) – Lower 24 bits of the Command Structure response outputs words 2, 3, and 4.

In ATA-7 parallel emulation, these bits were mapped to LBA Low, LBA Mid, and LBA High Registers of the Command block.

LBA/Response (47:24) – Higher 24 bits of the Command Structure response words 2, 3, and 4.

In ATA-7 parallel emulation, these bits were mapped to the LBA Low (Previous), LBA Mid (Previous) and LBA High (Previous) registers of the Command block.

R - Reserved.

Sector Count – Contains word 1 bits 7:0 of the Command Structure response outputs.

Sector Count (7:0) - In ATA-7 parallel emulation, this field was mapped to the Current Value in the Sector Count Register.

Notes 1-4: This field is not used in the 28-bit Command Structure Response mapping in the Serial Transport. Due to prior implementations of ATA and parallel ATA emulation, this field may contain indeterminate values. It is recommended that it be cleared to zero.

Note 1: In ATA-7, this field was mapped to the LBA Low (Previous) Value of the Command Block.

Note 2: In ATA-7, this field was mapped to the LBA Mid (Previous) Value of the Command Block.

Note 3: In ATA-7, this field was mapped to the LBA High (Previous) Value of the Command Block.

Note 4: In ATA-7, this field was mapped to the Sector Count (Previous) Value of the Command Block.

4 Update Bits FIS

An Update Bits FIS is a Device to Host FIS Type (A1h). This FIS is used for updating the host Adapter with changes to the device's condition or status, and provides a mechanism to cause an interrupt to the host if implemented by the Host Adapter.

4.1 Update Bits FIS – Device to Host

The Update Bits FIS is used to provide the Host Adapter with updated device information during times when all commands are released (BSY and DRQ have been cleared by a Response FIS).

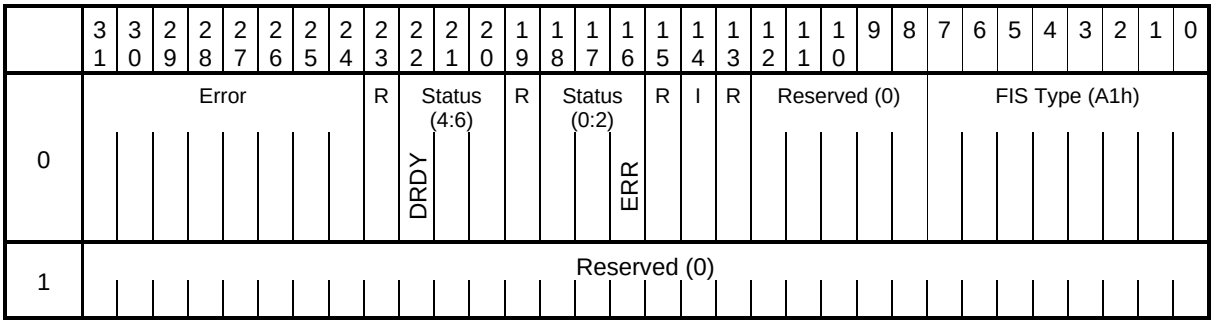

Figure 6 – Update Bits - Device to Host FIS layout

Field Definitions

FIS Type- Set to a value of A1h.

I - Interrupt Pending. This bit signals a Host Adapter that the device has performed an operation that requires the interrupt pending bit be set.

Prior implementations of ATA host adapters which use parallel ATA emulation use this bit to set interrupts to the host when both BSY and DRQ have been cleared to zero by a Response FIS.

Devices shall not modify the behavior of this bit based on the state of the nIEN bit received in Command or Control Host to Device FIS's.

Error - Word 0 bits 7:0 of the Command Structure response outputs. Content of these bits is command dependent. In ATA-7 parallel emulation, these bits were placed into the Error register of the Shadow Command Block.

Status (0:2) - Contains the contents to be placed into Word 0 bits 2,1, and 0 of the Command Structure Response outputs. IN ATA-7 parallel ATA emulation, these bits were placed into the Status register of the Shadow Command Block.

Bit 0: ERR/CHK: (Error/Check) This bit indicates that an error or check condition occurred during the execution of a command. (See x.x.x for a complete description of ERR/CHK bit handling) In the Serial Transport Update Bits FIS, its function is defined by the Device Transport state machines (see x.x.x)

Bit 1-2: Use of these bits is command dependent.

Status (4:6) - Contains the contents to be placed into Word 0, bits 6, 5, and 4 of the Command Structure Response outputs. In ATA-7 parallel emulation, these bits were placed into the Status register of the Shadow Command Block.

Bit 4-5: Use of these bits is command dependent.

Bit 6: DRDY (Device Ready) This bit is used to indicate device readiness to receive and attempt to execute all implemented commands. In the Serial Transport Update Bits FIS, its function is defined by the Device Transport state machines (see x.x.x)

In ATA-7 parallel emulation, Status (7:0) were mapped to the Status register of the Command Block. In the Serial Transport, their function is defined by the Device Transport state machines (see x.x.x)

5 PIO Setup - Device to Host

The PIO Setup - Device to Host FIS is used by the device to provide the host adapter with data transfer count and DRQ block status within the PIO data phase to allow the host adapter to control PIO data transfers. There are two Command Structure Response mappings into a Response FIS in the serial transport.

48-bit Command Structure PIO Setup mapping

28-bit Command Structure PIO Setup mapping

5.1 PIO Setup FIS - 48-bit Command PIO Setup Mapping

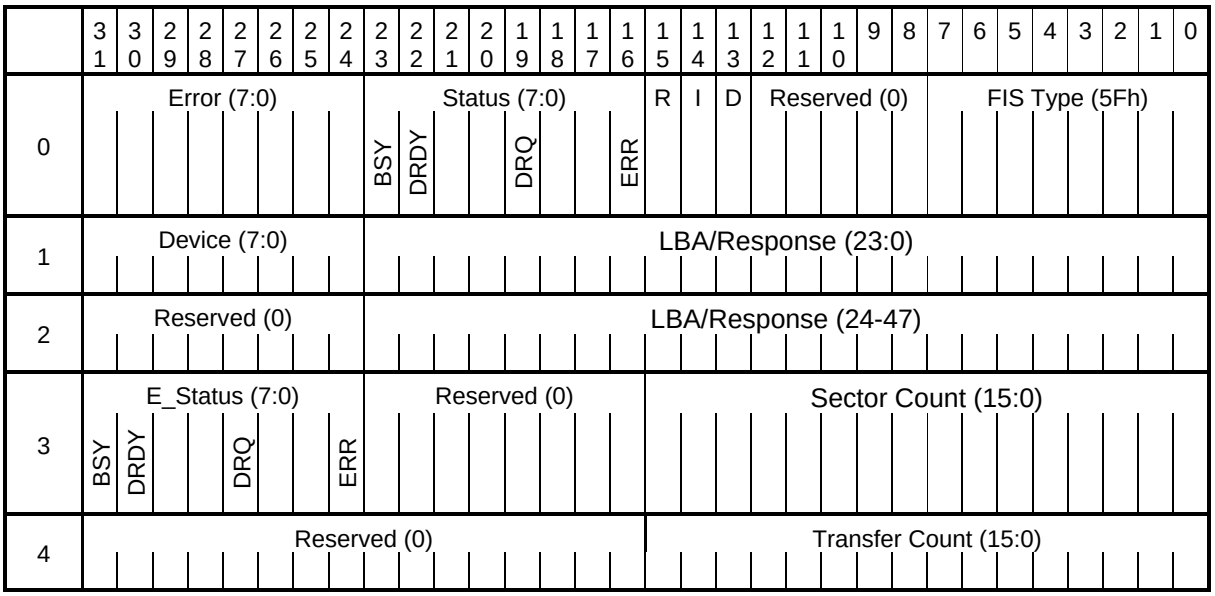

Figure 7 - PIO Setup – 48-bit Command Structure Device to Host FIS layout

Field Definitions

FIS Type - Set to a value of 5Fh.

I – Interrupt Pending. This bit reflects the Interrupt Pending state of the device. Behavior of this bit is defined by the Device Transport Protocol (see x.x.x).

D - Indicates whether host memory is being written or read by the device. 1 = write (device to host), 0 = read (host to device).

R - Reserved.

Status – This field contains Word 5 bits 7:0 of the Command Structure response outputs and is used by the Host Adapter Transport for ending status if (Status bits BSY=0 and DRQ=0), or to prepare for a subsequent data transfer if (Status bits BSY=1 or DRQ=1). If (Status bits BSY=1 or DRQ=1), then operation of these bits is defined by the Host and Device Transport State machines (see x.x.x). Definition of these bits is the same as for the Response FIS - 48-bit Command Structure Response Mapping (see 3.1). Note that the contents of the Status fields and the E_Status fields contain different information.

Device - Word 5 bits 15:8 of the Command Structure response outputs. Content of these bits is command dependent. In ATA-7 parallel emulation, these bits were mapped to the Device register. This value is only valid if both the BSY and DRQ bits in the E_Status field are cleared. If (E_Status bit BSY=1 or DRQ=1), the contents are indeterminate.

Error - Word 0 bits 7:0 of the Command Structure response outputs. Content of these bits is command dependent. This value is only valid if both the BSY and DRQ bits in the E_Status field are cleared. If (E_Status bit BSY=1 or DRQ=1), the contents are indeterminate. In ATA-7 parallel emulation, these bits were mapped to the Error register of the Command Block.

LBA/Response (23:0) – Lower 24 bits of the Command Structure response outputs words 2, 3, and 4. This value is only valid if both the BSY and DRQ bits in the E_Status field are cleared. If (E_Status bit BSY=1 or DRQ=1), the contents are indeterminate.

In ATA-7 parallel emulation, these bits were mapped to LBA Low, LBA Mid, and LBA High Registers of the Command block.

LBA/Response (47:24) – Higher 24 bits of the Command Structure response words 2, 3, and 4. This value is only valid if both the BSY and DRQ bits in the E_Status field are cleared. If (E_Status bit BSY=1 or DRQ=1), the contents are indeterminate.

In ATA-7 parallel emulation, these bits were mapped to the LBA Low (Previous), LBA Mid (Previous) and LBA High (Previous) registers of the Command block.

Sector Count – Contains word 1 bits 15:0 of the Command Structure response outputs. This value is only valid if both the BSY and DRQ bits in the E_Status field are cleared. If (E_Status bit BSY=1 or DRQ=1), the contents are indeterminate.

Sector Count (7:0) - In ATA-7 parallel emulation, this field was mapped to the Current Value in the Sector Count Register.

Sector Count (15:8) - In ATA-7 parallel emulation, this field was mapped to the Previous Value in the Sector Count Register.

E_Status – Value to be placed into Word 5 bits 7:0 of the Command Structure response outputs at the expiration of the Transfer Count for this PIO Setup if this is the final PIO Setup for this command. If (E_Status bits BSY=1 or DRQ=1), then this not the final PIO setup for this command, and the contents of this field are used by the Host Adapter for data transfer control as defined by the Host and Device Transport state machines (see x.x.x). Definition of these bits is the same as for the Response FIS - 48-bit Command Structure Response Mapping (see 3.1).

Transfer Count - Holds the number of bytes to be transferred in the subsequent Data FIS. The Transfer Count value shall be non-zero and the low order bit shall be zero (even number of bytes transferred).

5.2 PIO Setup FIS - 28-bit Command PIO Setup Mapping

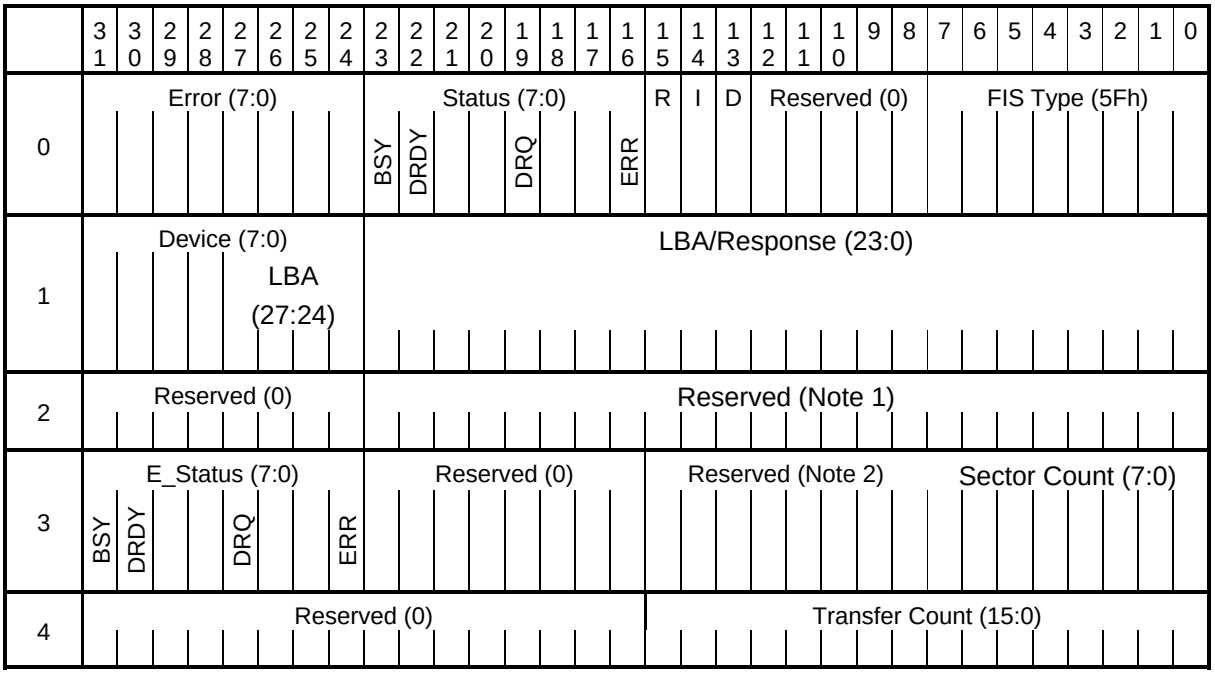

Figure 8 - PIO Setup – 28-bit Command Structure Device to Host FIS layout

Field Definitions

FIS Type - Set to a value of 5Fh.

I – Interrupt Pending. This bit reflects the Interrupt Pending state of the device. Behavior of this bit is defined by the Device Transport Protocol (see x.x.x).

D - Indicates whether host memory is being written or read by the device. 1 = write (device to host), 0 = read (host to device).

R - Reserved.

Status – This field contains Word 5 bits 7:0 of the Command Structure response outputs and is used by the Host Adapter Transport for ending status if (Status bits BSY=0 and DRQ=0), or to prepare for a subsequent data transfer if (Status bits BSY=1 or DRQ=1). If (Status bits BSY=1 or DRQ=1), then operation of these bits is defined by the Host and Device Transport State machines (see x.x.x). Definition of these bits is the same as for the Response FIS - 48-bit Command Structure Response Mapping (see 3.1). Note that the contents of the Status fields and the E_Status fields contain different information.

Device - Word 5 bits 15:8 of the Command Structure response outputs. Content of these bits is command dependent. In ATA-7 parallel emulation, these bits were mapped to the Device register. This value is only valid if both the BSY and DRQ bits in the E_Status field are cleared. If (E_Status bit BSY=1 or DRQ=1), the contents are indeterminate.

Error - Word 0 bits 7:0 of the Command Structure response outputs. Content of these bits is command dependent. This value is only valid if both the BSY and DRQ bits in the E_Status field are cleared. If (E_Status bit BSY=1 or DRQ=1), the contents are indeterminate. In ATA-7 parallel emulation, these bits were mapped to the Error register of the Command Block.

LBA/Response (23:0) – Lower 24 bits of the Command Structure response outputs words 2, 3, and 4. This value is only valid if both the BSY and DRQ bits in the E_Status field are cleared. If (E_Status bit BSY=1 or DRQ=1), the contents are indeterminate.

In ATA-7 parallel emulation, these bits were mapped to LBA Low, LBA Mid, and LBA High Registers of the Command block.

Sector Count – Contains word 1 bits 7:0 of the Command Structure response outputs. This value is only valid if both the BSY and DRQ bits in the E_Status field are cleared. If (E_Status bit BSY=1 or DRQ=1), the contents are indeterminate. In ATA-7 parallel emulation, this field was mapped to the Current Value in the Sector Count Register.

E_Status – Value to be placed into Word 5 bits 7:0 of the Command Structure response outputs at the expiration of the Transfer Count for this PIO Setup if this is the final PIO Setup for this command. If (E_Status bits BSY=1 or DRQ=1), then this not the final PIO setup for this command, and the contents of this field are used by the Host Adapter for data transfer control as defined by the Host and Device Transport state machines (see x.x.x). Definition of these bits is the same as for the Response FIS - 48-bit Command Structure Response Mapping (see 3.1).

Transfer Count - Holds the number of bytes to be transferred in the subsequent Data FIS. The Transfer Count value shall be non-zero and the low order bit shall be zero (even number of bytes transferred).

Note 1 – In the Serial Transport, the contents are indeterminate for 28-bit commands.

In ATA-7 parallel emulation, these bits were mapped to the LBA Low (Previous), LBA Mid (Previous) and LBA High (Previous) registers of the Command block.

Note 2 – In the Serial Transport, the contents are indeterminate for 28-bit commands.

In ATA-7 parallel emulation, these bits were mapped to the Sector Count (Previous) register of the Command block.