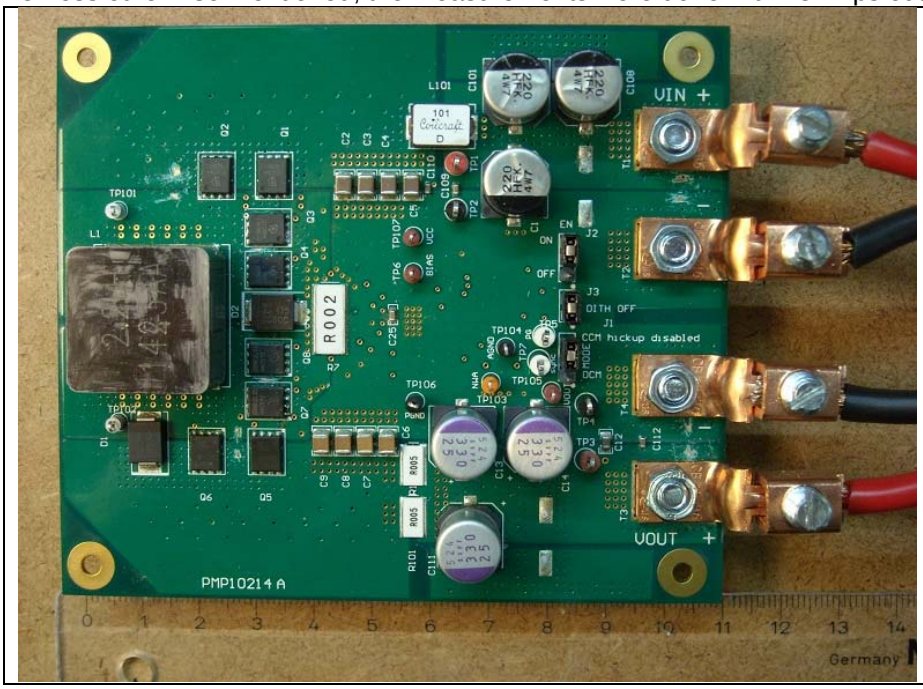
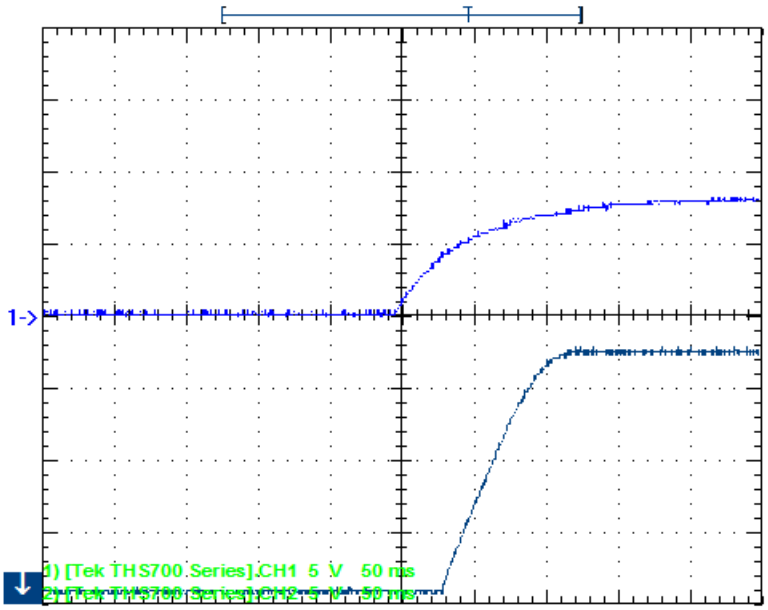
PMP10214RevB Test Results

Topology: 4 Switch BuckBoost >300W
Device: LM5175
Unless otherwise mentioned, the measurements were done with 18Amps output current



1 Startup

The startup waveform is shown in the Figure 1. The input voltage was set to 8V and load current was 15A. Power supply (6574A) was switched on.



Ch1=> input voltage 5V/div

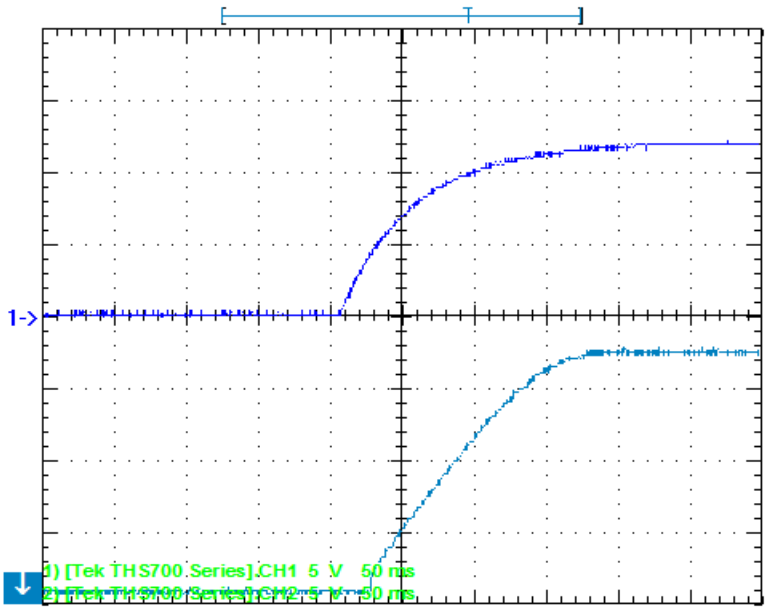
Ch2=> output voltage 5V/div

50ms/div

20MHz bw

Figure 1

The startup waveform is shown in the Figure 2. The input voltage was set at 12V. Power supply (6574A) was switched on.



Ch1=> input voltage 5V/div

Ch2=> output voltage 5V/div

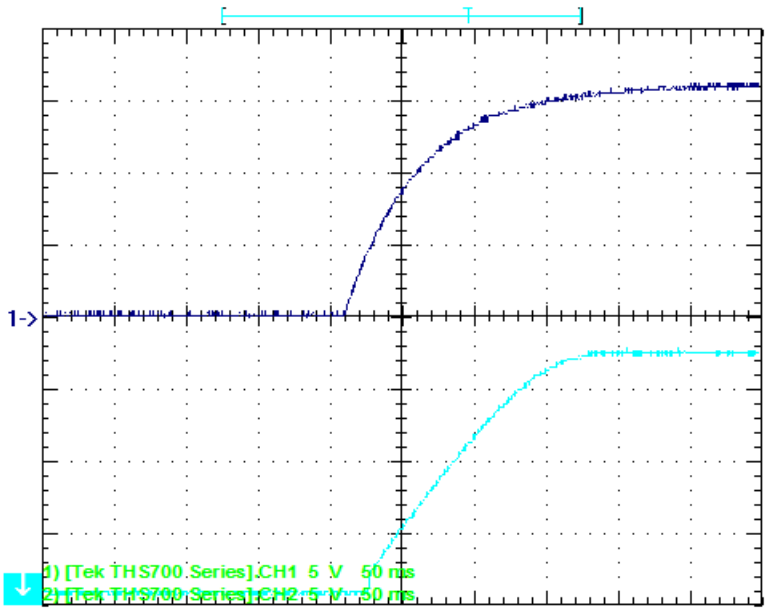
50ms/div

20MHz bw

Figure 2

PMP10214RevB Test Results

The startup waveform is shown in the Figure 3. The input voltage was set at 16V. Power supply (6574A) was switched on.



Ch1=> input voltage 5V/div

Ch2=> output voltage 5V/div

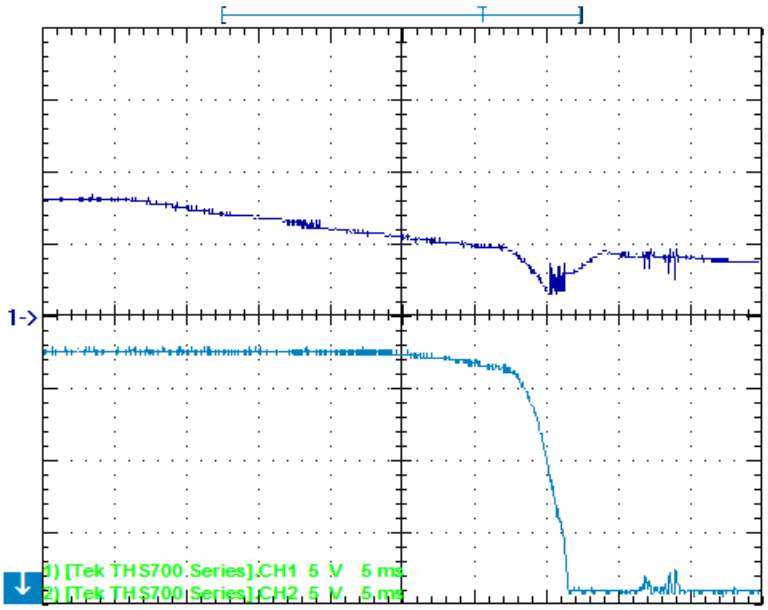
50ms/div

20MHz bw

Figure 3

2 Shutdown

The shutdown waveform is shown in the Figure 4. The input voltage was set to 8V with 15A load current. The power supply was switched off.



Ch1=> input voltage 5V/div

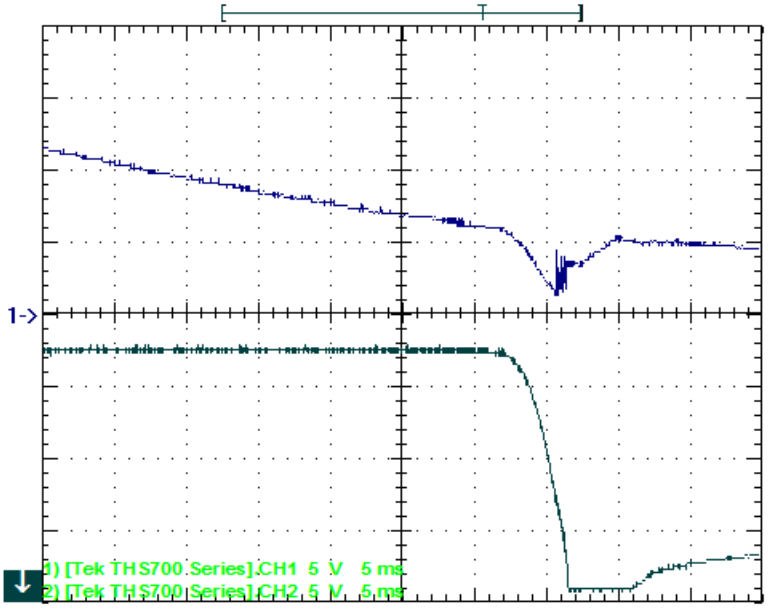
Ch2=> output voltage 5V/div

5ms/div

20MHz bw

Figure 4

The shutdown waveform is shown in the Figure 5. The input voltage was set at 12V. The power supply was switched off.



Ch1=> input voltage 5V/div

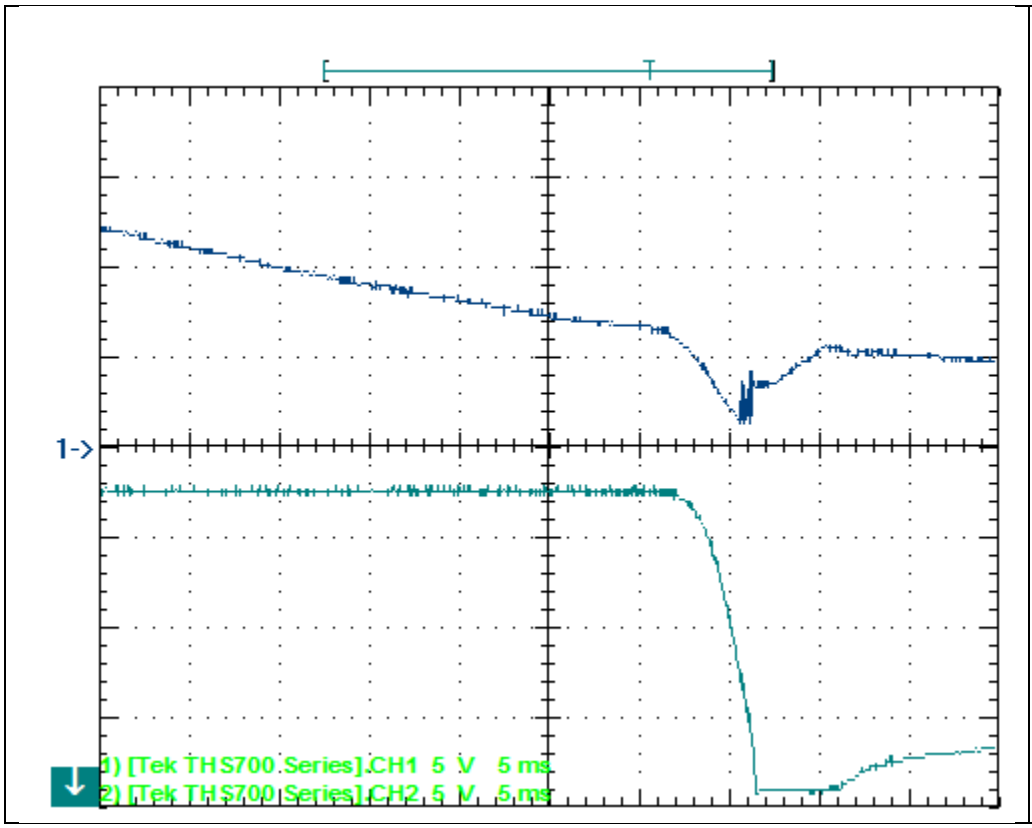
Ch2=> output voltage 5V/div

5ms/div

20MHz bw

Figure 5

The shutdown waveform is shown in the Figure 6. The input voltage was set at 16V. The power supply was switched off.



Ch1=> input voltage 5V/div

Ch2=> output voltage 5V/div

5ms/div

20MHz bw

Figure 6

3 Efficiency

The efficiency is shown in the Figure 7 below. The input voltage was set to 9V, 12V and 16V.

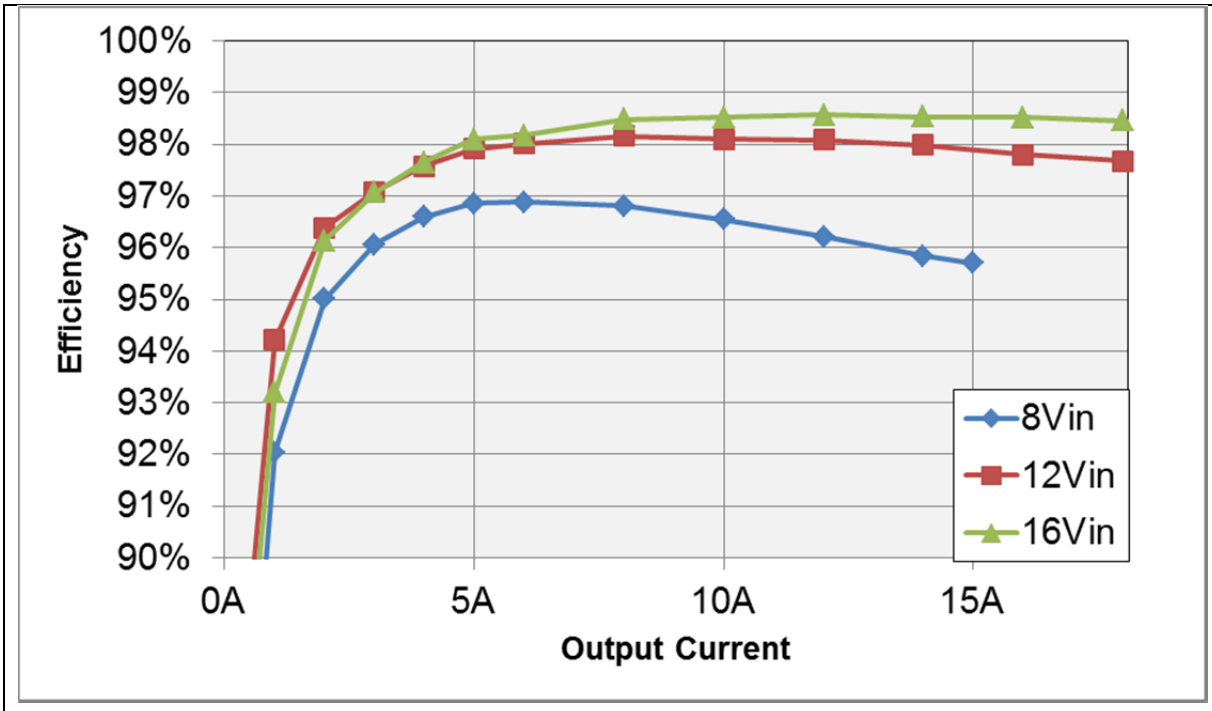


Figure 7

VIN	IIN	VOUT	IOUT	PIN	POUT	Eff
12.01	25.944	16.908	18	311.5874	304.344	0.976753
12.002	23.059	16.916	16	276.7541	270.656	0.977966
12.011	20.121	16.914	14	241.6733	236.796	0.979818
12.003	17.237	16.911	12	206.8957	202.932	**0.980842**
12.011	14.352	16.91	10	172.3819	169.1	**0.980962**
12.004	11.478	16.907	8	137.7819	135.256	**0.981667**
12.012	8.615	16.905	6	103.4834	101.43	**0.980157**
12.007	7.189	16.904	5	86.31832	84.52	0.979166
12.003	5.773	16.903	4	69.29332	67.612	0.975736
12.015	4.347	16.902	3	52.22921	50.706	0.970836
12.01	2.92	16.901	2	35.0692	33.802	0.963866
12.006	1.494	16.9	1	17.93696	16.9	0.942188
12.012	0.791	16.899	0.5	9.501492	8.4495	0.889281
12.014	0.504	16.899	0.3	6.055056	5.0697	0.837267
12.016	0.217	16.898	0.1	2.607472	1.6898	0.648061
12.017	0.153	16.898	0.05	1.838601	0.8449	0.459534

At typical input range 12V efficiency is >98% in a load range 6Amps to 12 Amps

4 Load Regulation

The load regulation of the output is shown in the Figure 8 below. The input voltage was set to 8V, 12V and 16V.

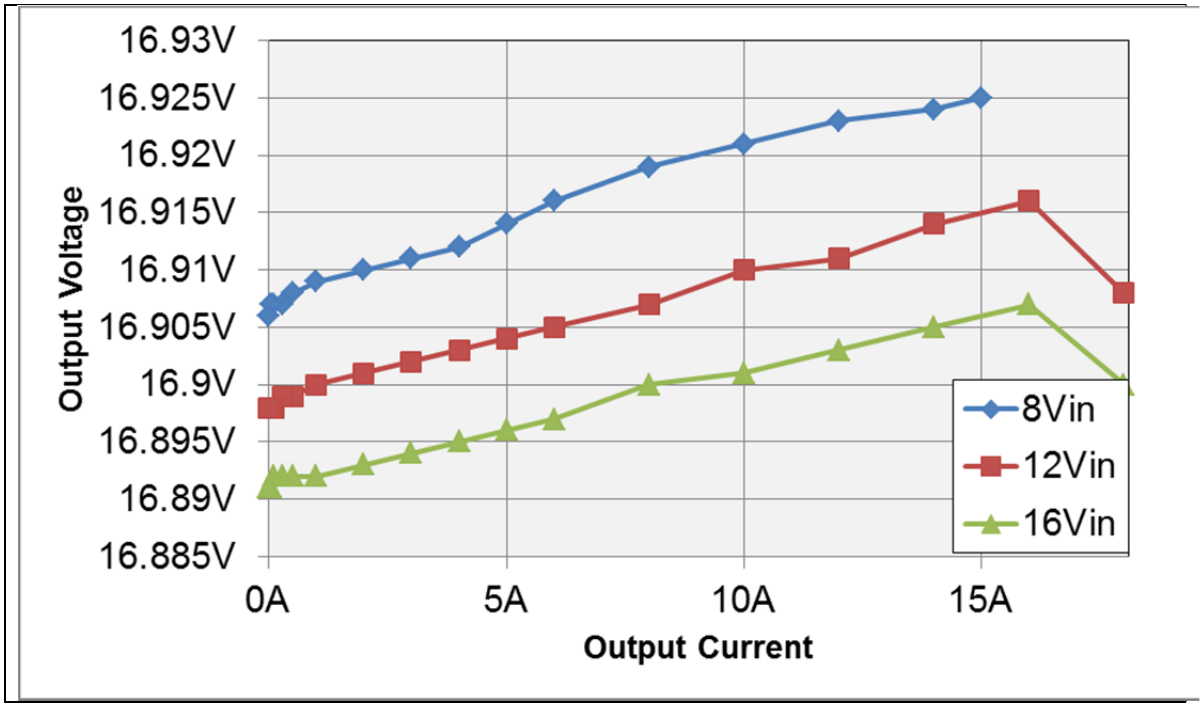


Figure 8

5 Line Regulation

The line regulation is shown in Figure 9. The output current was set to 15A.

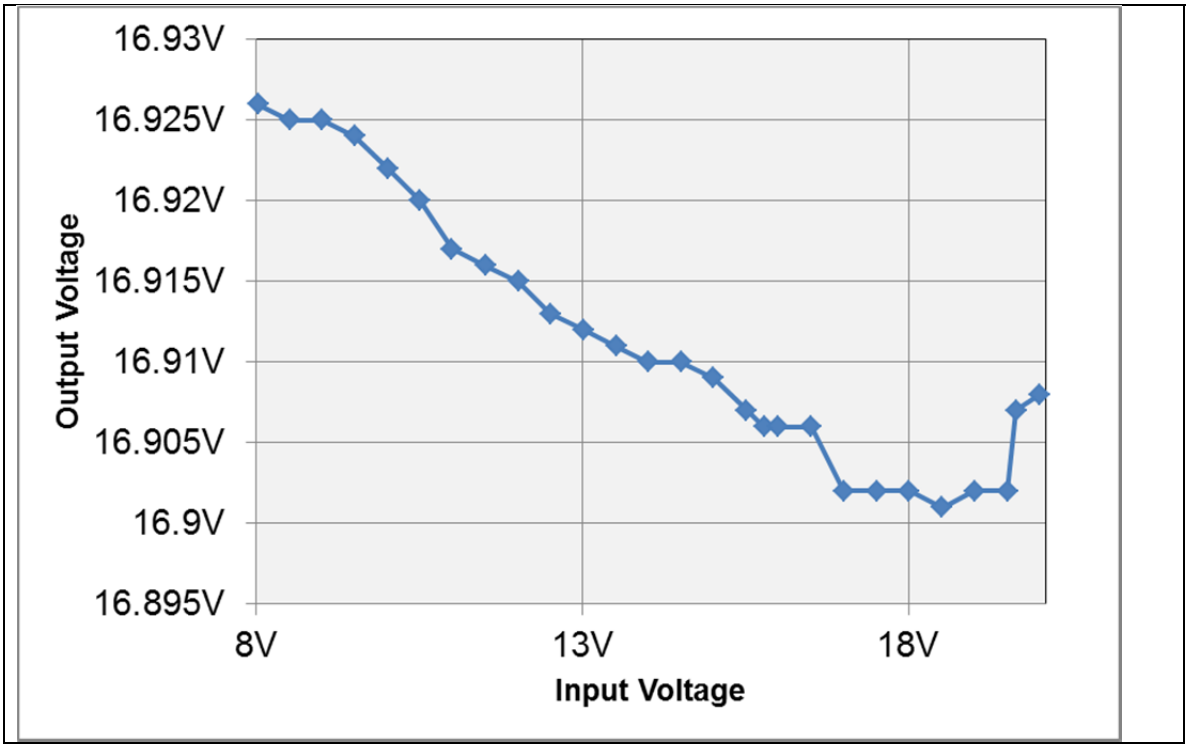


Figure 9

With the same setup the efficiencies are shown in Figure 10.

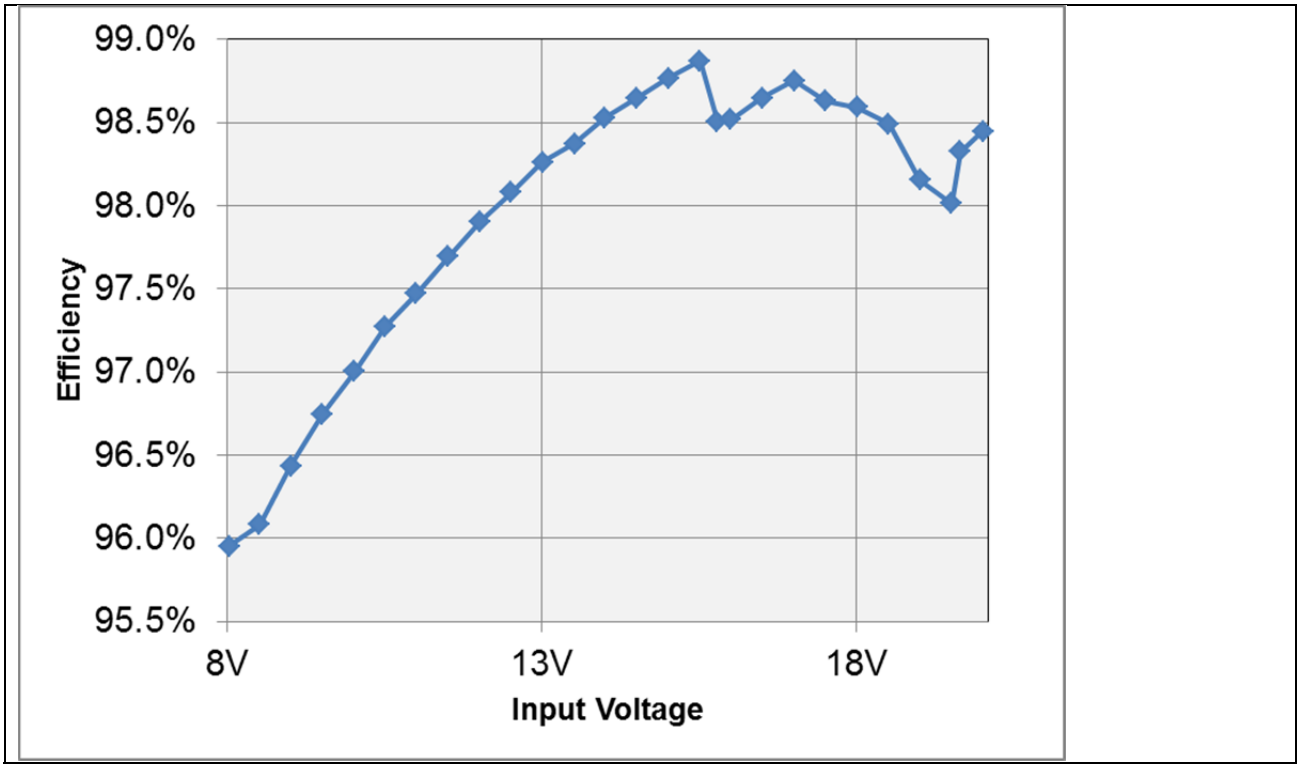
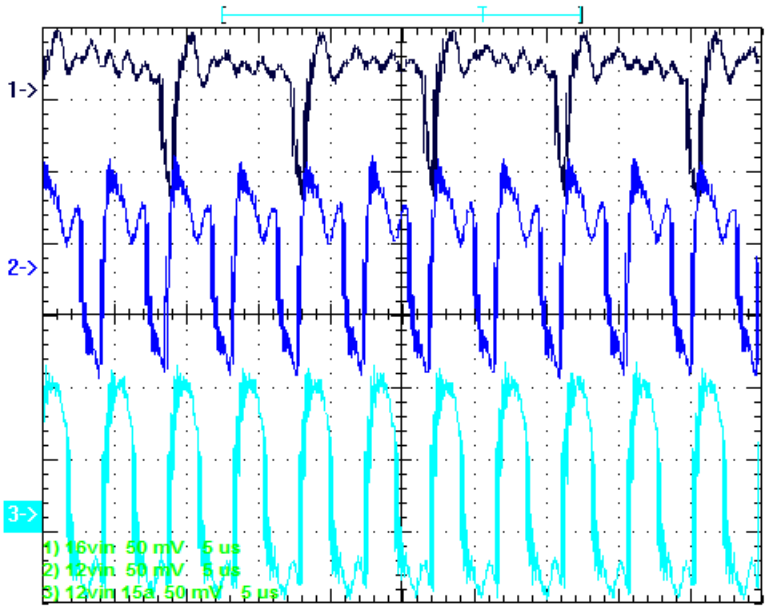


Figure 10

6 Output Ripple Voltage

The output ripple voltage is shown in Figure 11.



Ch1 => output voltage@16Vin

Ch2 => output voltage@12Vin

Ch3 => output voltage@8Vin/15Aout

Vin 50mV/div

AC coupled

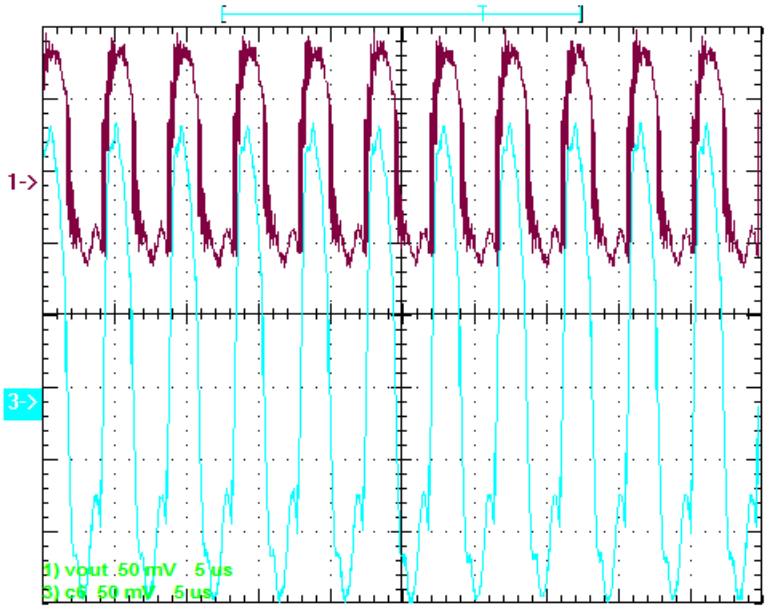
20MHz bw

5µs/div

Figure 11

Output voltage ripple is around 150mVpp, so 1% of Vout 16.8V

The output ripple voltage is shown in Figure 12. Input voltage was set to 8V with 15A load. The waveforms were captured separately.



Ch1 => voltage near output terminals

Ch3 => voltage at C6

Vin 50mV/div

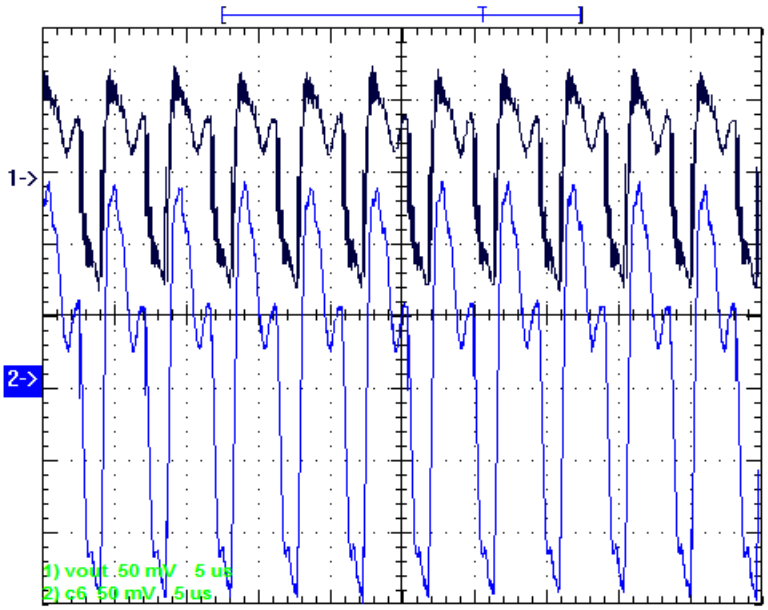
AC coupled

20MHz bw

5µs/div

Figure 12

The output ripple voltage is shown in Figure 13. Input voltage was set to 12V. The waveforms were captured separately.



Ch1 => voltage near output terminals

Ch3 => voltage at C6

Vin 50mV/div

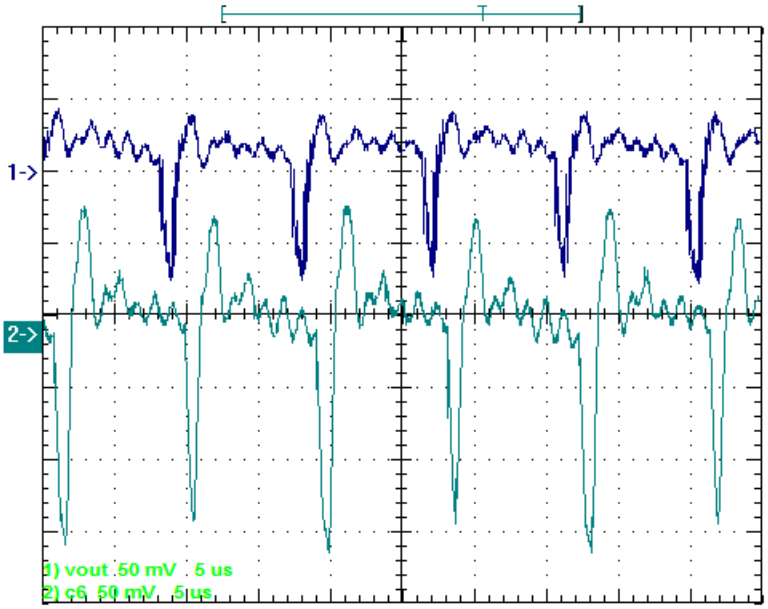
AC coupled

20MHz bw

5µs/div

Figure 13

The output ripple voltage is shown in Figure 14. Input voltage was set to 16V. The waveforms were captured separately.



Ch1 => voltage near output terminals

Ch2 => voltage at C6

Vin 50mV/div

AC coupled

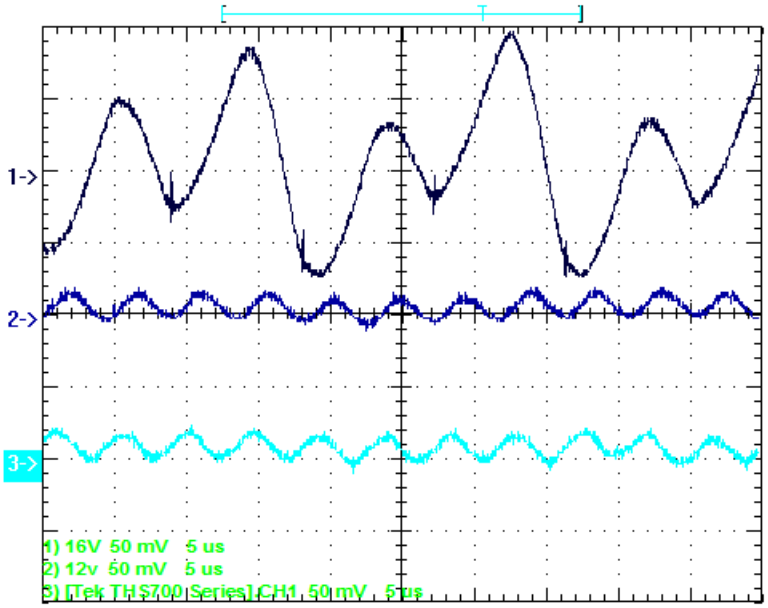
20MHz bw

5µs/div

Figure 14

7 Input Ripple Voltage

The input ripple voltage is shown in Figure 15.



Ch1 => input voltage@16Vin

Ch2 => input voltage@12Vin

Ch3 => input voltage@8Vin/15A

Vin 50mV/div

AC coupled

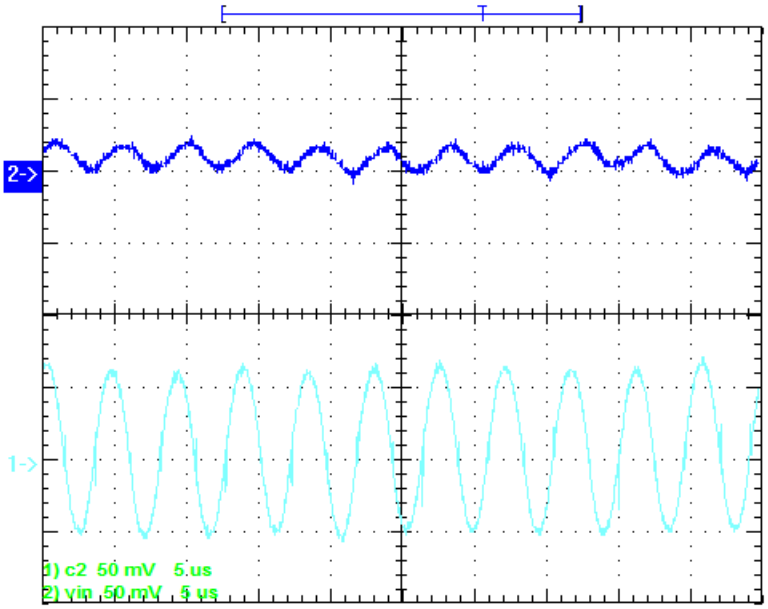
20MHz bw

5µs/div

Figure 15

At 16V input voltage the converter is in transfer mode (Vin = Vout); the typical operation for this automotive application could be expected in a range of 11V to 15V input voltage.

The input ripple voltage is shown in Figure 16. Input voltage was set to 8V with 15A load current. The waveforms were captured separately.



Ch2 => voltage near input terminals

Ch1 => voltage at C2

Vin 50mV/div

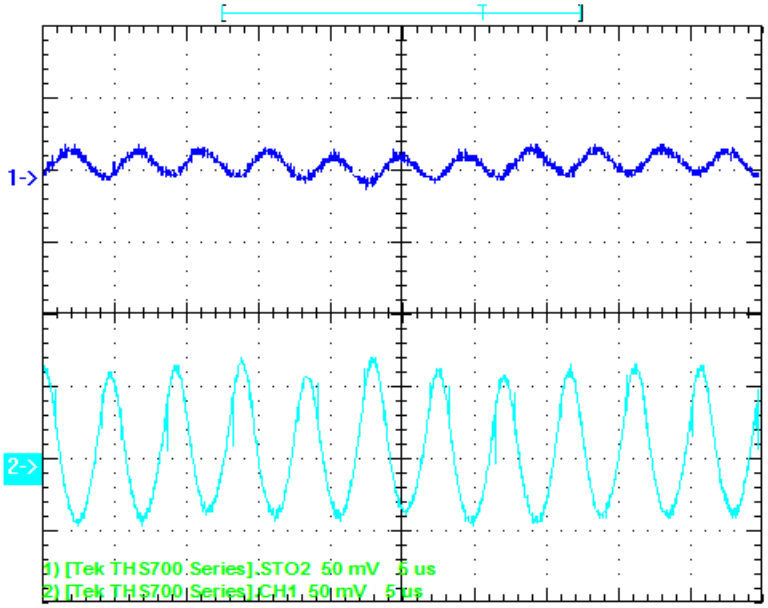
AC coupled

20MHz bw

5µs/div

Figure 16

The input ripple voltage is shown in Figure 17. Input voltage was set to 12V. The waveforms were captured separately.



Ch1 => voltage near input terminals

Ch2 => voltage at C2

Vin 50mV/div

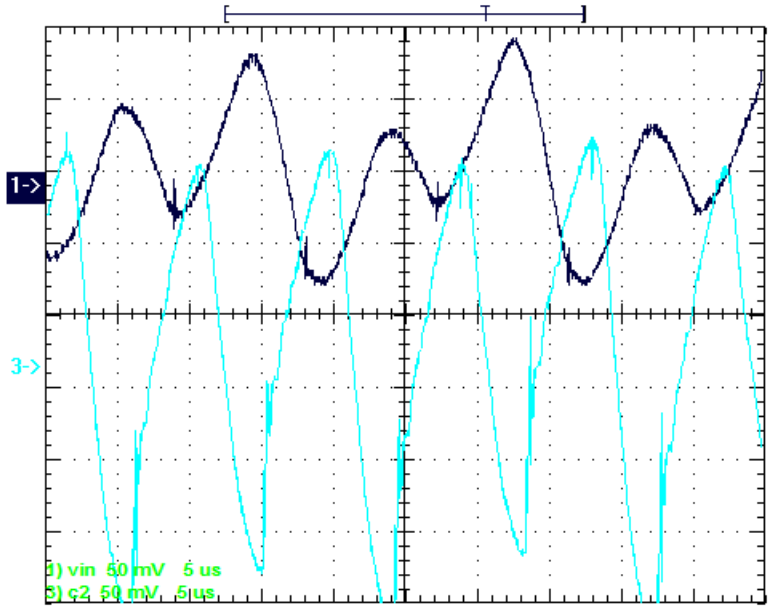
AC coupled

20MHz bw

5µs/div

Figure 17

The input ripple voltage is shown in Figure 18. Input voltage was set to 16V. The waveforms were captured separately.



Ch1 => voltage near input terminals

Ch3 => voltage at C2

Vin 50mV/div

AC coupled

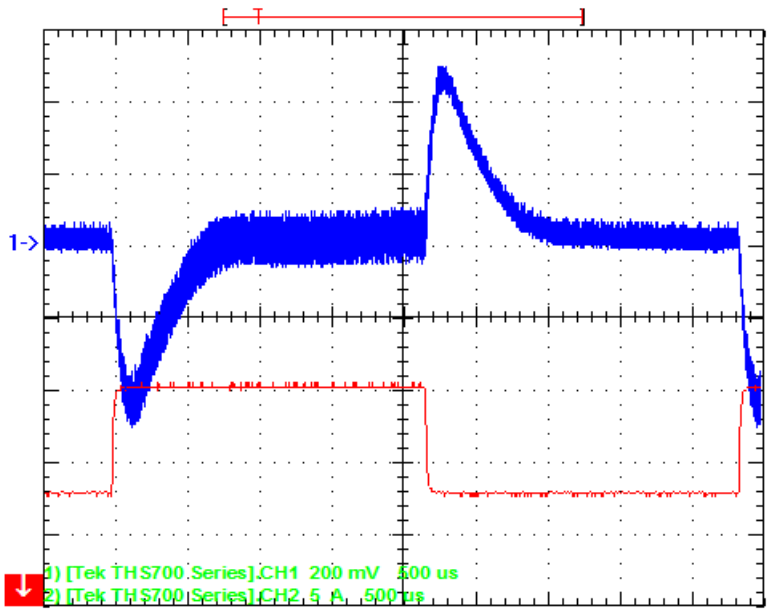
20MHz bw

5µs/div

Figure 18

8 Load Transients

The Figure 19 shows the response to load transients. The load is switching from 7.5A to 15A with a frequency of 230Hz. The input voltage was set to 8V



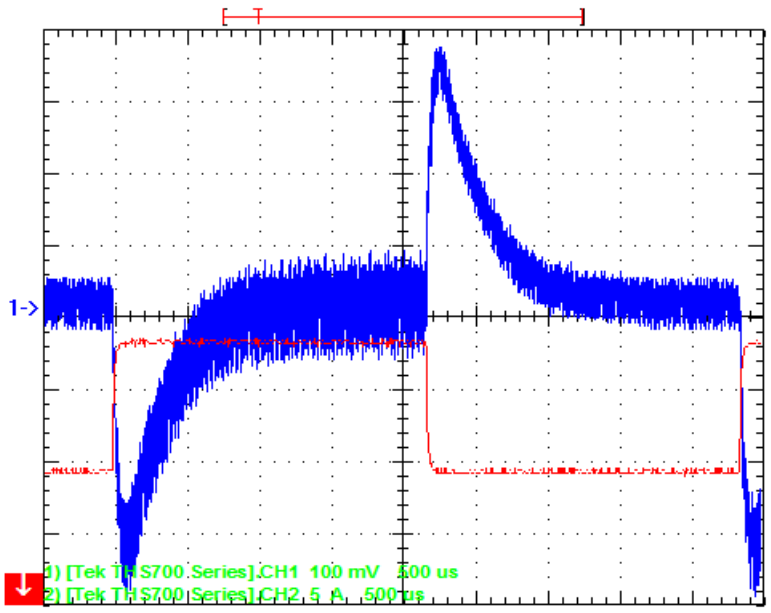
Ch1 => output voltage **200mV/div**

Ch2=> output current 5A/div

500µs/div

Figure 19

The Figure 20 shows the response to load transients. The load is switching from 9A to 18A with a frequency of 230Hz. The input voltage was set to 12V, deviation is <400mVpk, so less than 2.5%.



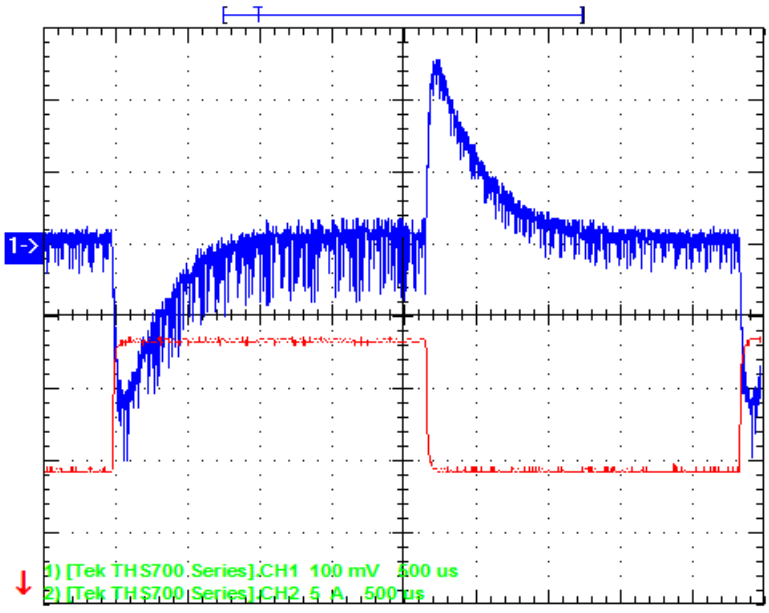
Ch1 => output voltage 100mV/div

Ch2=> output current 5A/div

500µs/div

Figure 20

The Figure 21 shows the response to load transients. The load is switching from 9A to 18A with a frequency of 230Hz. The input voltage was set to 16V



Ch1 => output voltage 100mV/div

Ch2=> output current 5A/div

20MHz bandwidth setting

500µs/div

Figure 21

9 Control Loop Frequency Response

Figure 22 shows the loop response. 15A-load applied (electronic load). The input voltage was set to 8V.

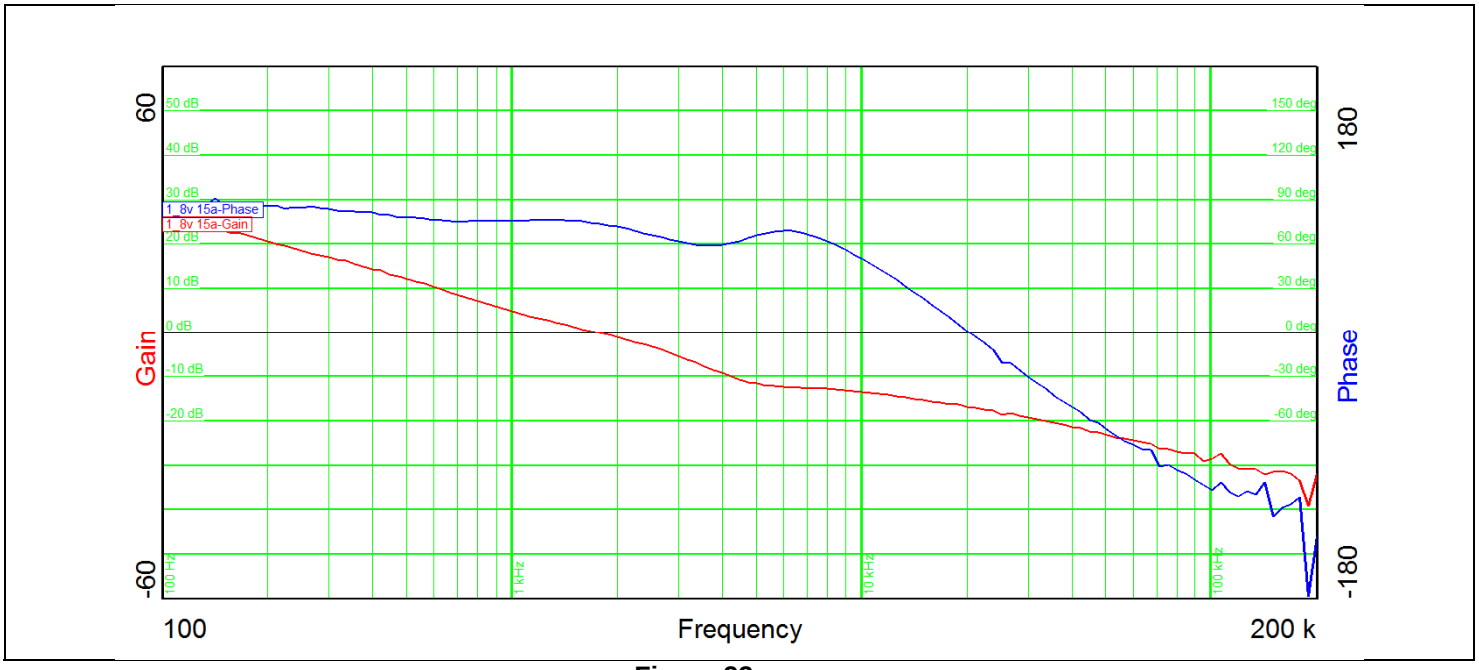


Figure 22

Figure 23 shows the loop response. 18A-load applied (Electronic load). The input voltage was set to 12V.

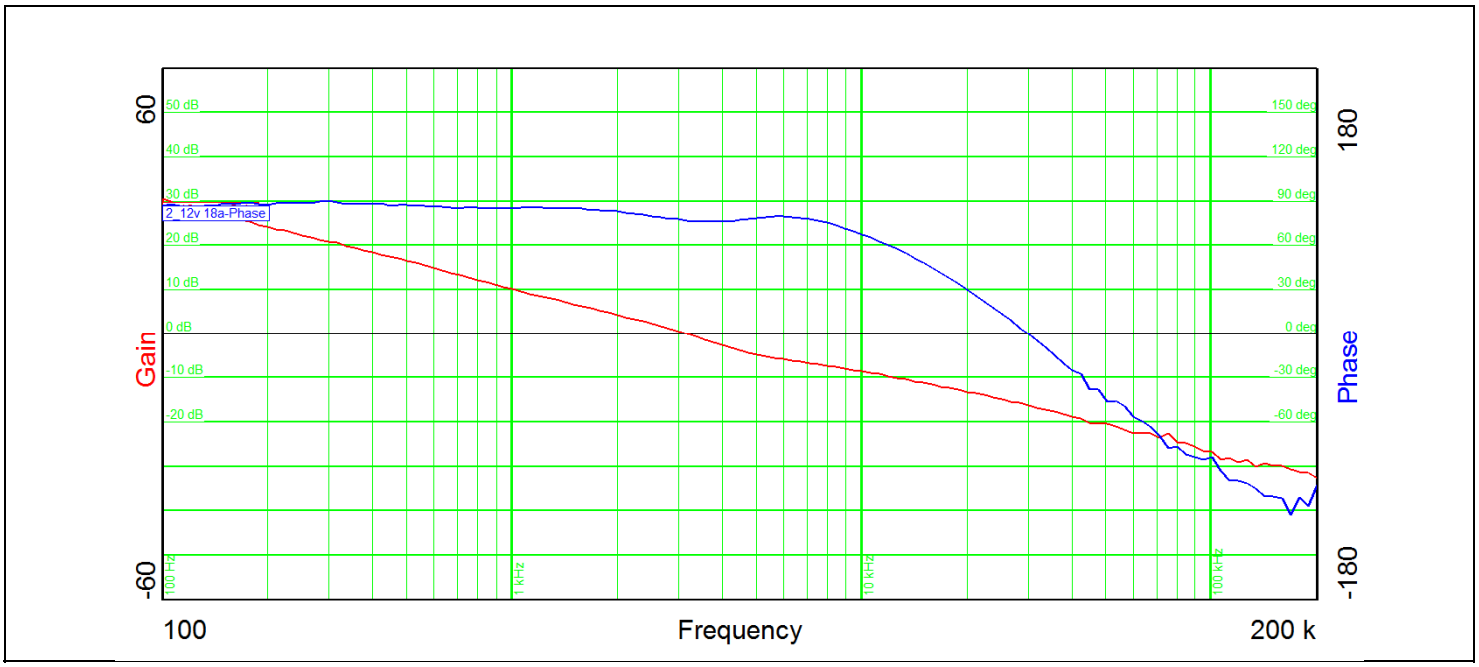


Figure 23

Figure 24 shows the loop response. 18A-load applied (electronic load). The input voltage was set to 16V.

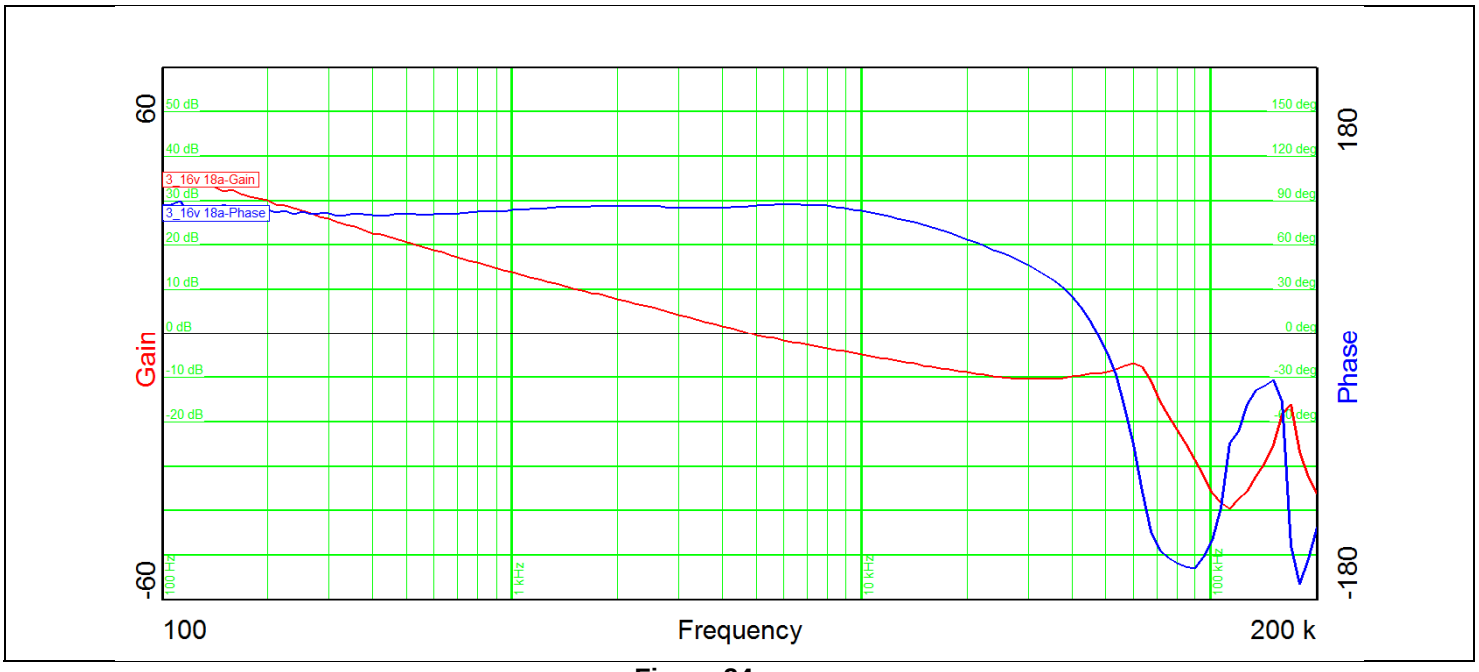


Figure 24

Table 1 summarizes the results from the frequency response.

Vin	8V	12V	16V
Bandwidth (kHz)	1.78	3.15	4.86
Phase margin	74°	77°	86°
slope (20dB/decade)	-0.97	-1.24	-0.93
gain margin (dB)	-16.8	-16.3	-9
slope (20dB/decade)	-0.56	-1.04	+0.49
freq (kHz)	20.4	29.9	47.2

Table 1

10 Miscellaneous Waveforms

10.1 8V Input Voltage (15A Load Current)

10.1.1 Boost High Side (SW2)

10.1.1.1 Source Drain

The waveform measured on source drain is shown Figure 25. (referenced to VOUT')

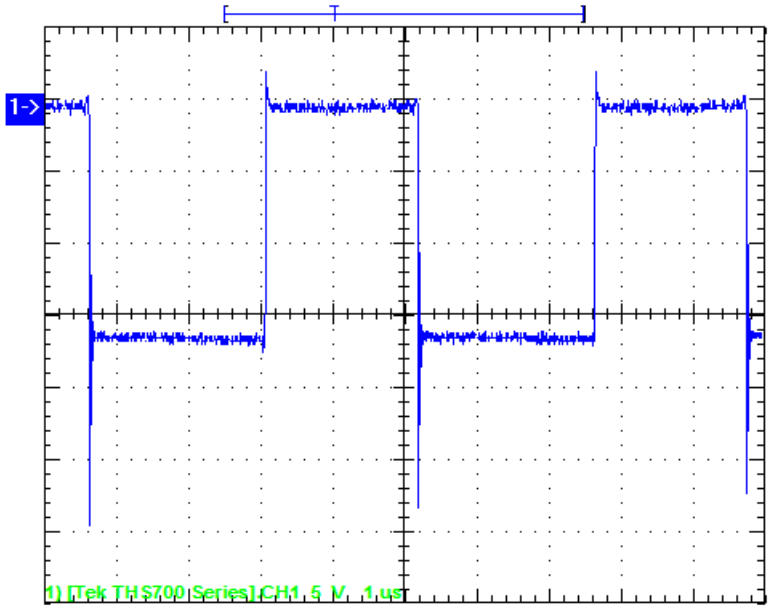
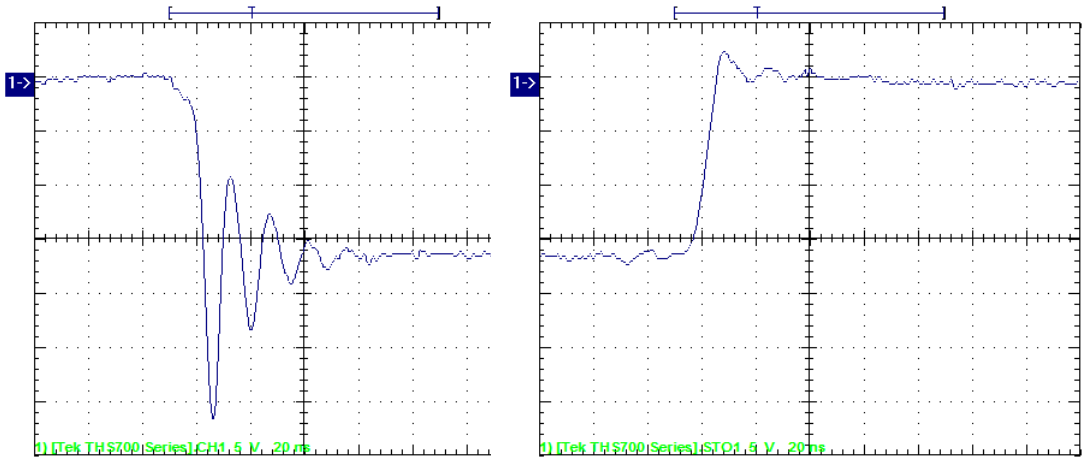
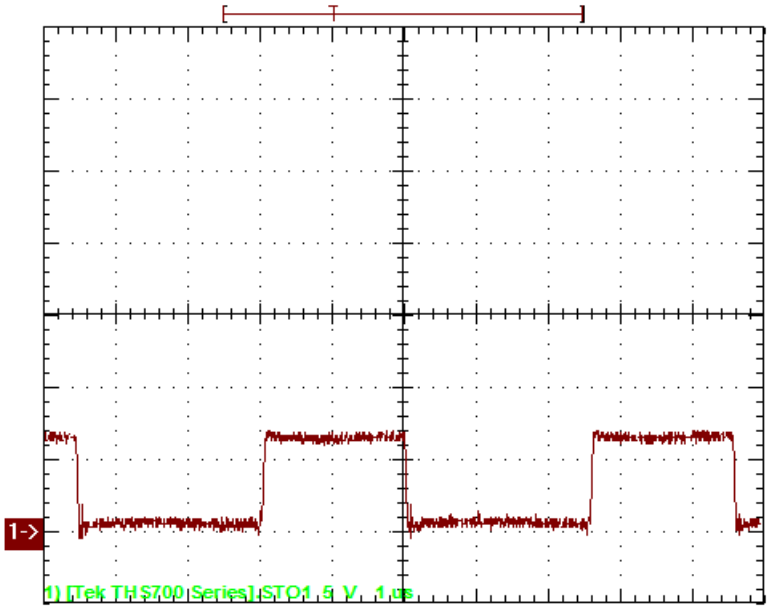
	Ch1 => 5V/div 1µs/div full bandwidth
	Ch1 => 5V/div 20ns/div

Figure 25

A 30V FET or a RC snubber is recommended for the synchronuous rectifier !

10.1.1.2 Gate-Source

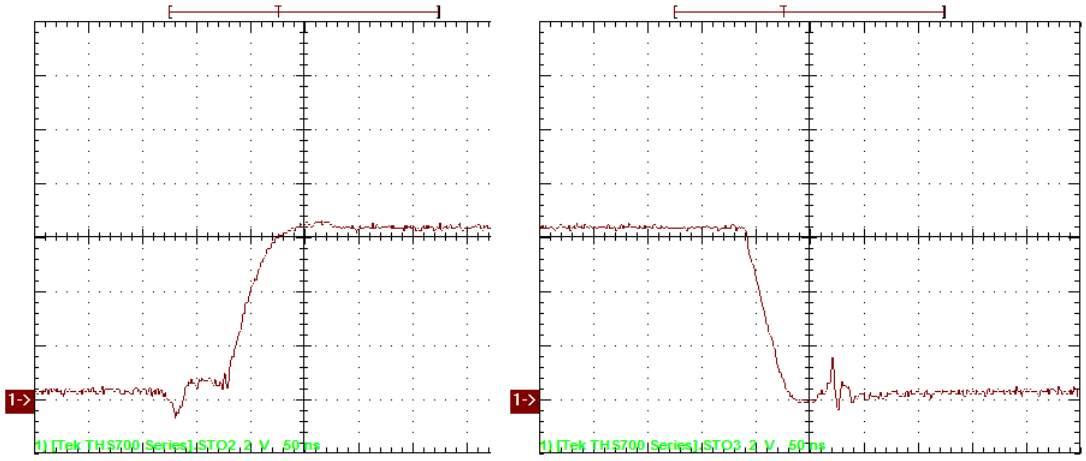
The waveform of the **gate-source** voltage is shown in Figure 26 (boost HS).



Ch1 =>
2V/div

1µs/div

full bandwidth



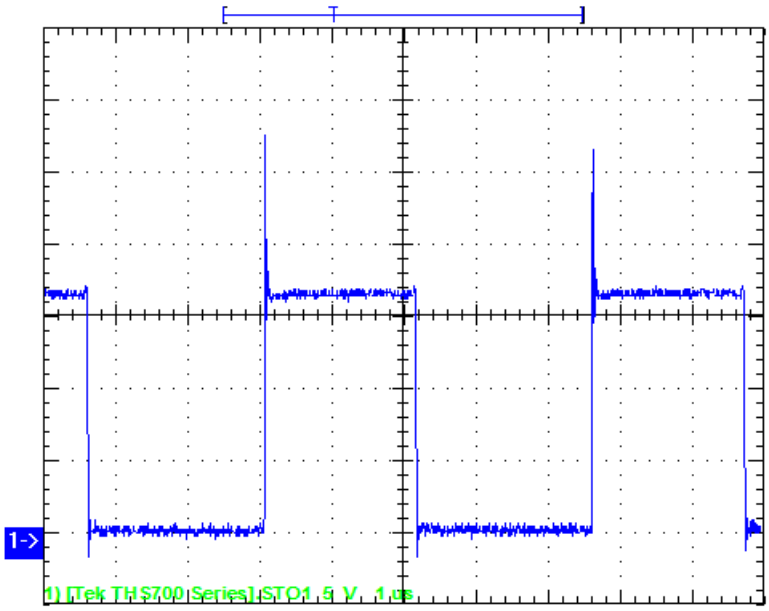
Ch1 =>
2V/div
20ns/div

Figure 26

10.1.2 Boost Low Side (SW2)

10.1.2.1 Drain-Source

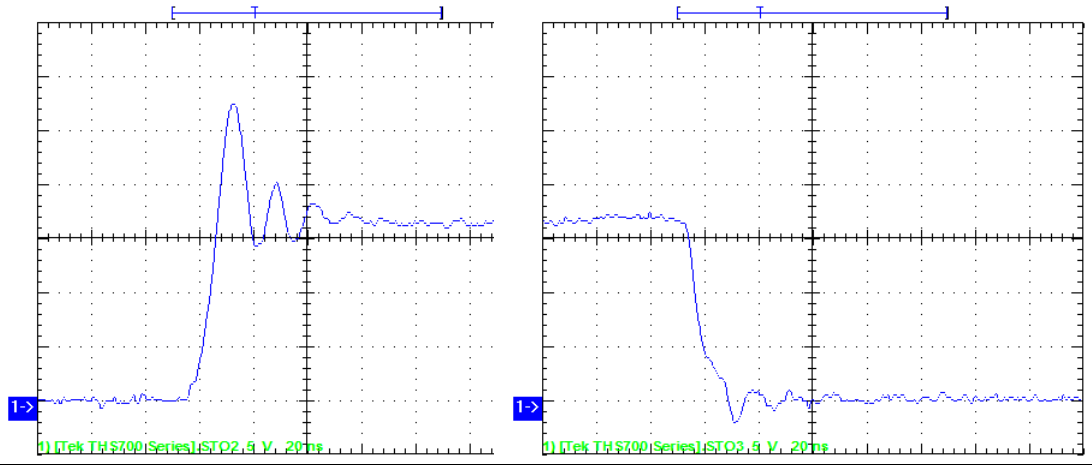
The waveform of the drain-source voltage on is shown in Figure 27.



Ch1 =>
5V/div

1µs/div

full bandwidth

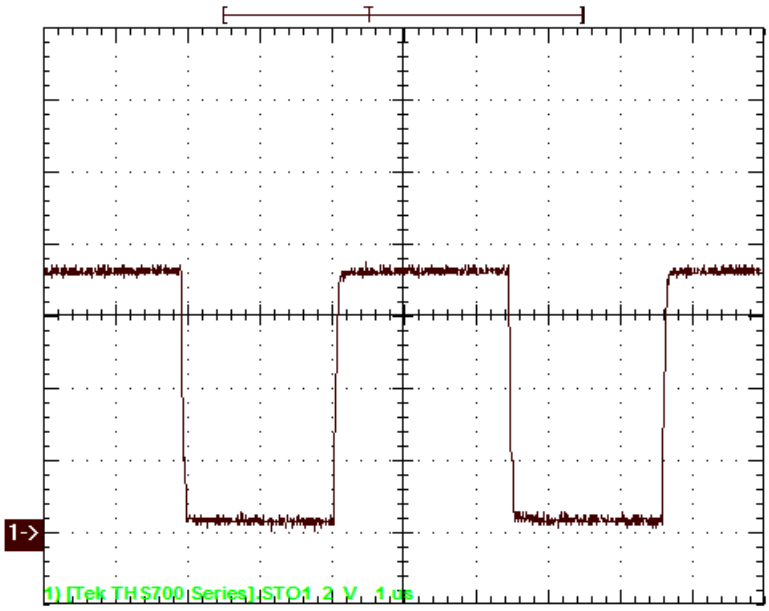


Ch1 =>
5V/div
20ns/div

Figure 27

10.1.2.2 Gate Source

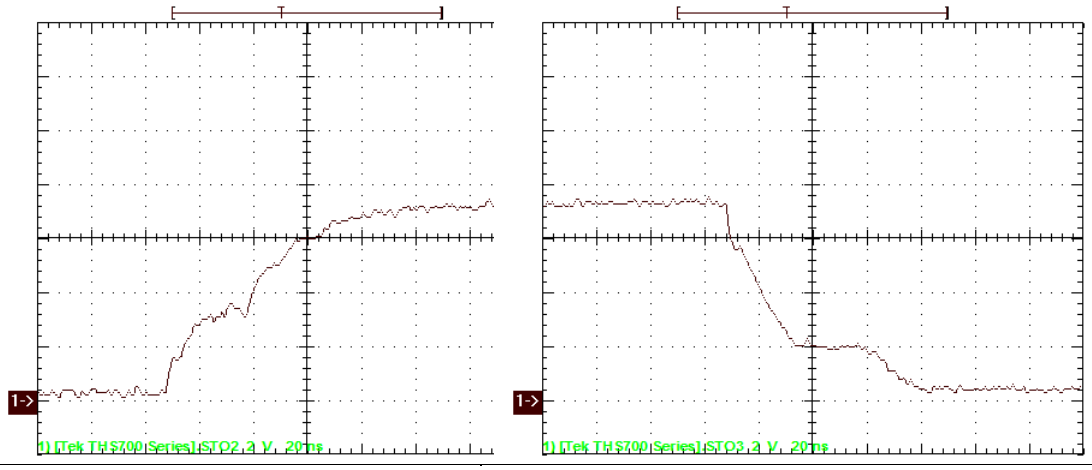
The waveform of the **gate-source** voltage is shown in Figure 28 (boost LS).



Ch1 =>
2V/div

1µs/div

full bandwidth



Ch1 =>
2V/div
20ns/div

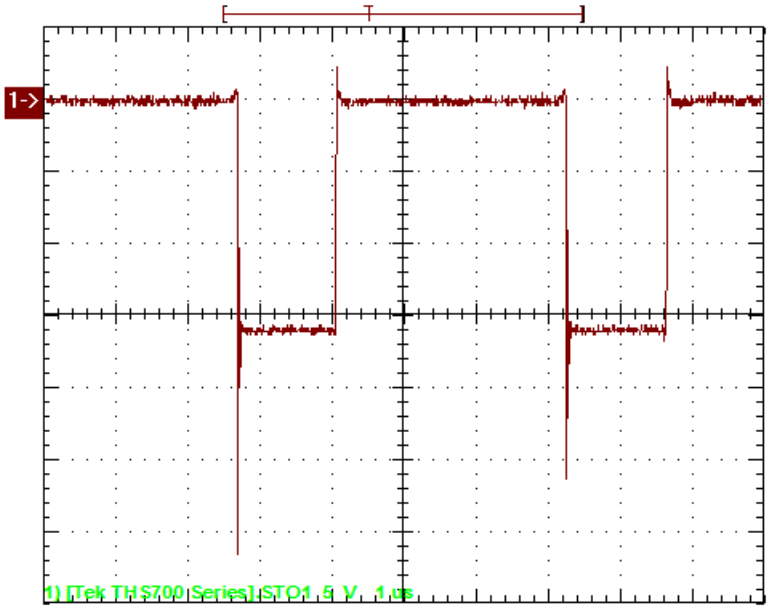
Figure 28

10.2 12V Input Voltage

10.2.1 Boost High Side (SW2)

10.2.1.1 Source Drain

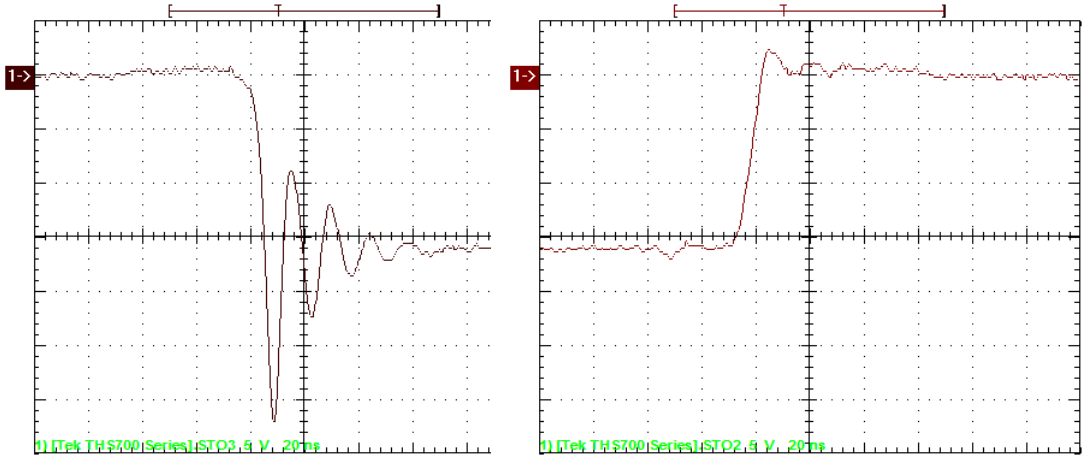
The waveform of the source-drain voltage is shown in Figure 29. (referenced to VOUT')



Ch1 =>
5V/div

1µs/div

full bandwidth



Ch1 =>
5V/div
20ns/div

Figure 29

10.2.1.2 Gate-Source

The waveform of the gate-source voltage is shown in Figure 30 (boost HS).

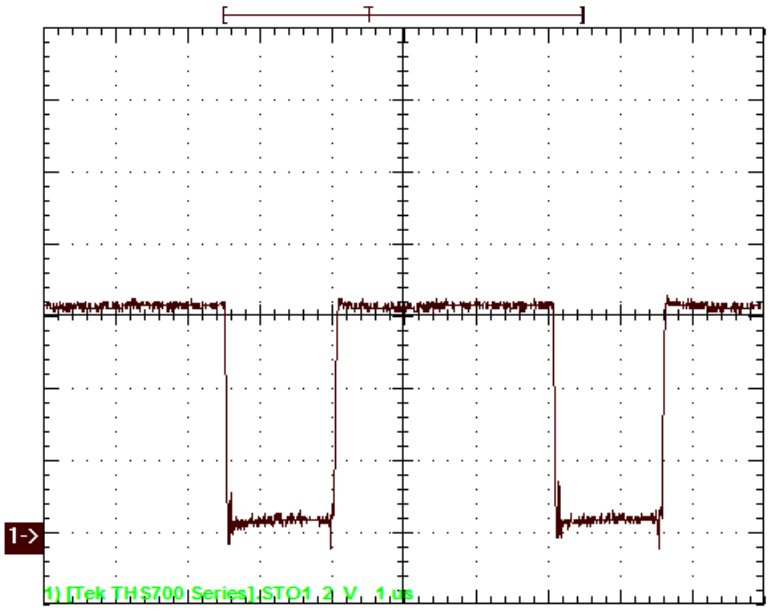
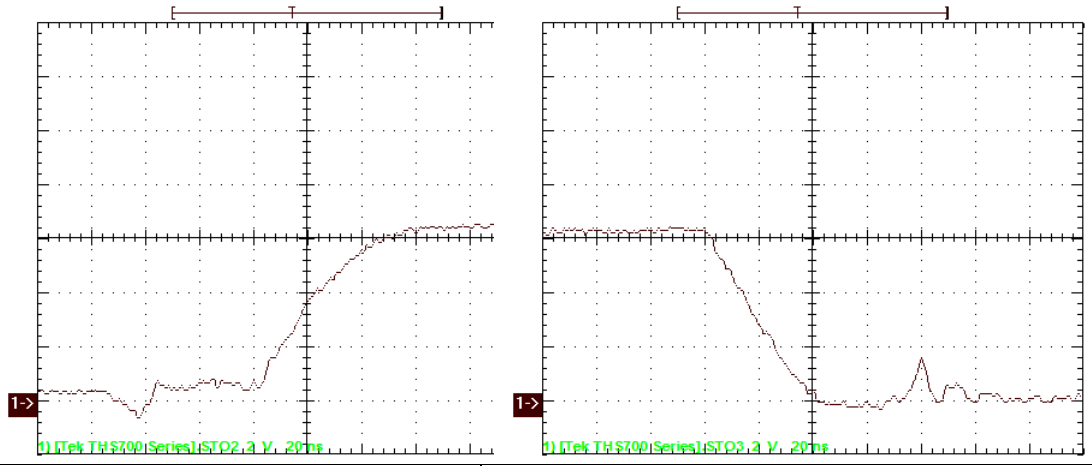
	Ch1 => 2V/div 1µs/div full bandwidth
	Ch1 => 2V/div 20ns/div

Figure 30

10.2.2 Boost Low Side (SW2)

10.2.2.1 Drain-Source

The waveform of the **drain-source** voltage is shown in Figure 31.

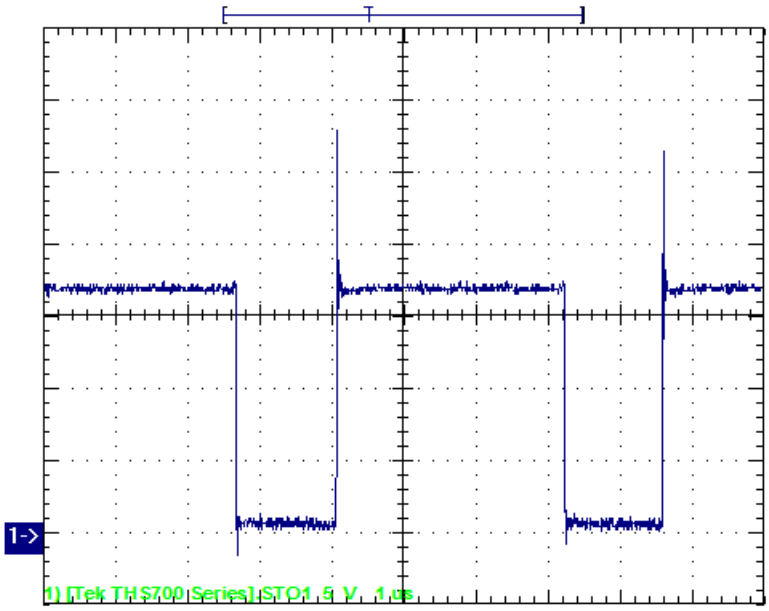
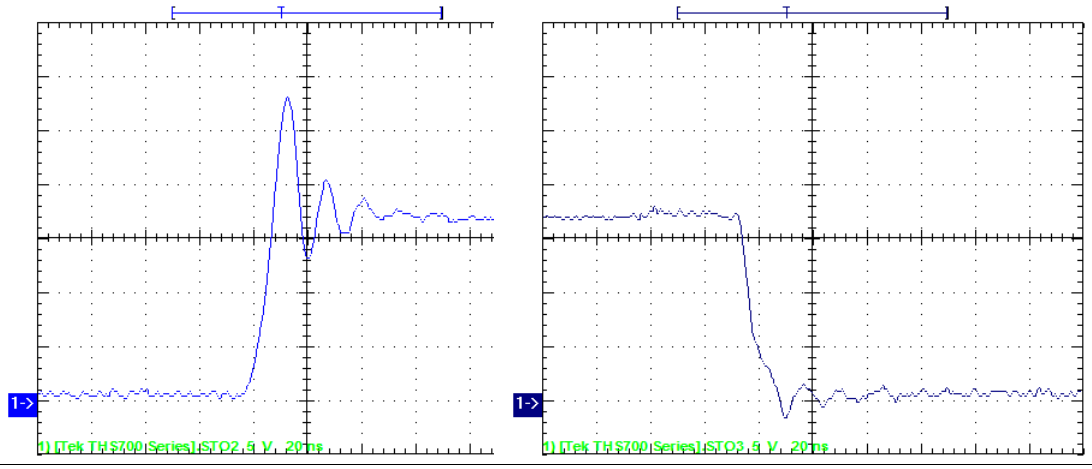
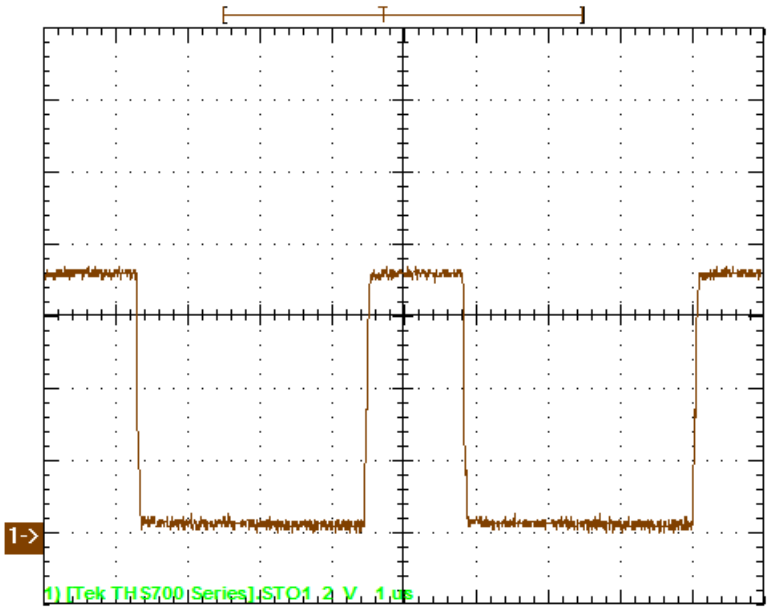
	Ch1 => 5V/div 1µs/div full bandwidth
	Ch1 => 5V/div 20ns/div

Figure 31

10.2.2.2 Gate Source

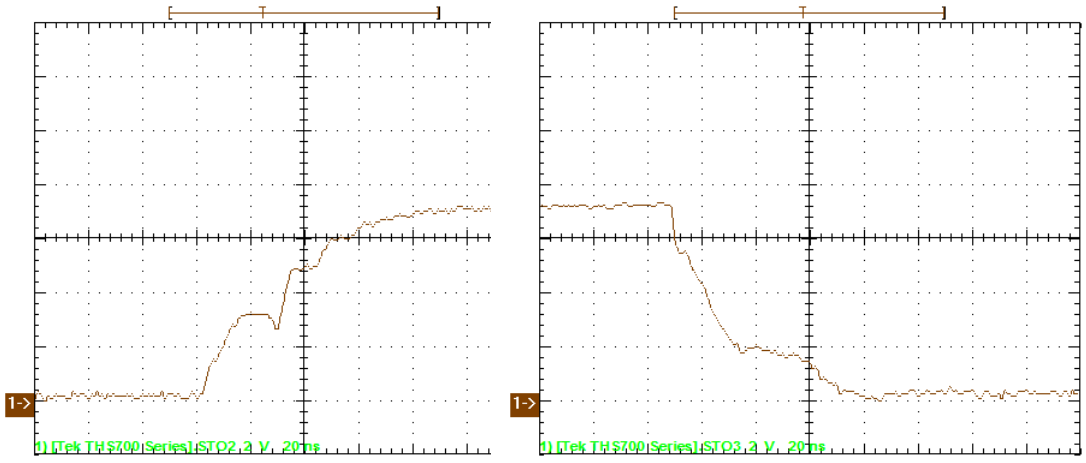
The waveform of the **gate-source** voltage on is shown in Figure 32 (boost LS).



Ch1 =>
2V/div

2µs/div

full bandwidth



Ch1 =>
2V/div
20ns/div

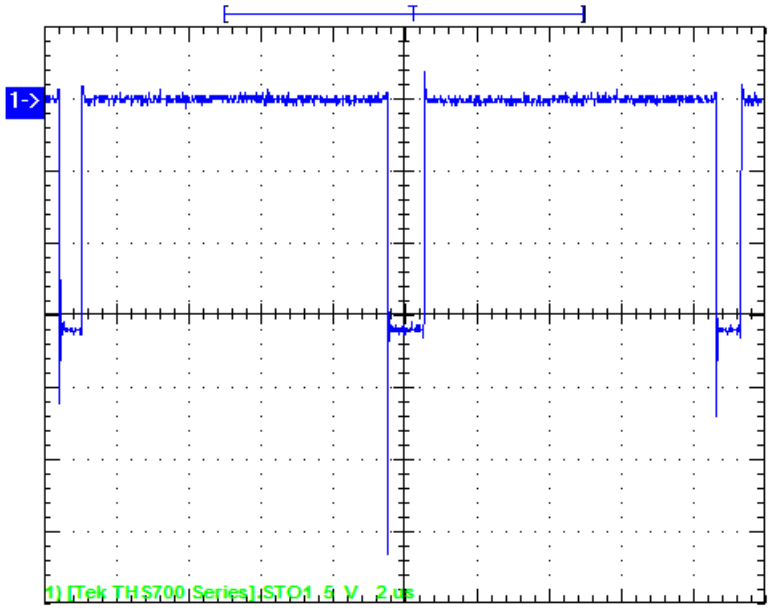
Figure 32

10.3 16V Input Voltage

10.3.1 Boost High Side

10.3.1.1 Source Drain

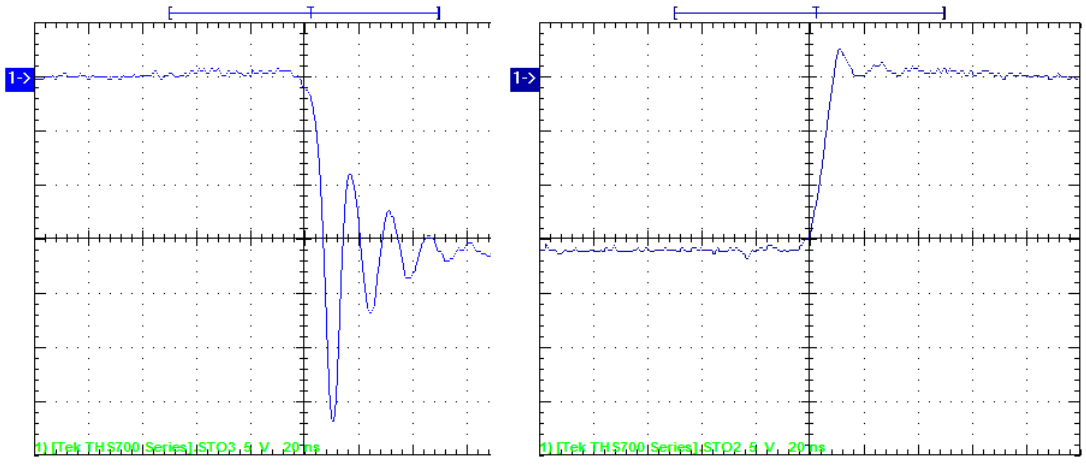
The waveform of the source-drain voltage is shown in Figure 33 (referenced to VOUT').



Ch1 =>
5V/div

2µs/div

full bandwidth



Ch1 =>
5V/div
20ns/div

Figure 33

10.3.1.2 Gate Source

The waveform of the **gate-source** voltage is shown in Figure 34 (boost HS).

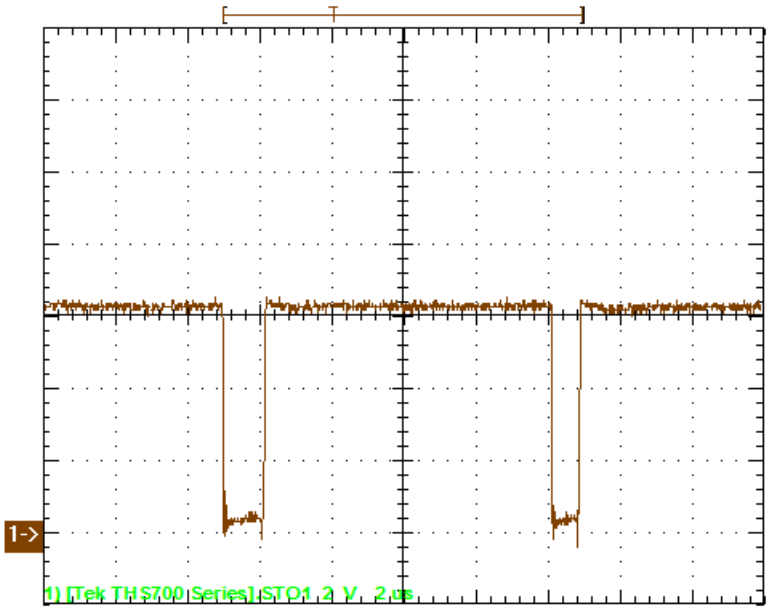
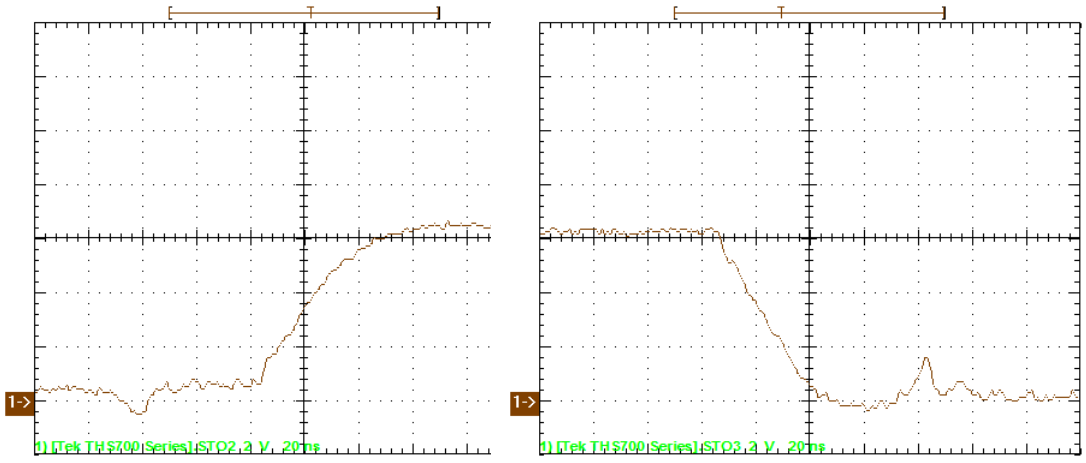
	Ch1 => 2V/div **2µs/div** full bandwidth
	Ch1 => 2V/div 20ns/div

Figure 34

10.3.2 Boost Low Side (SW1)

10.3.2.1 Drain Source

The waveform of the drain-source voltage is shown in Figure 35.

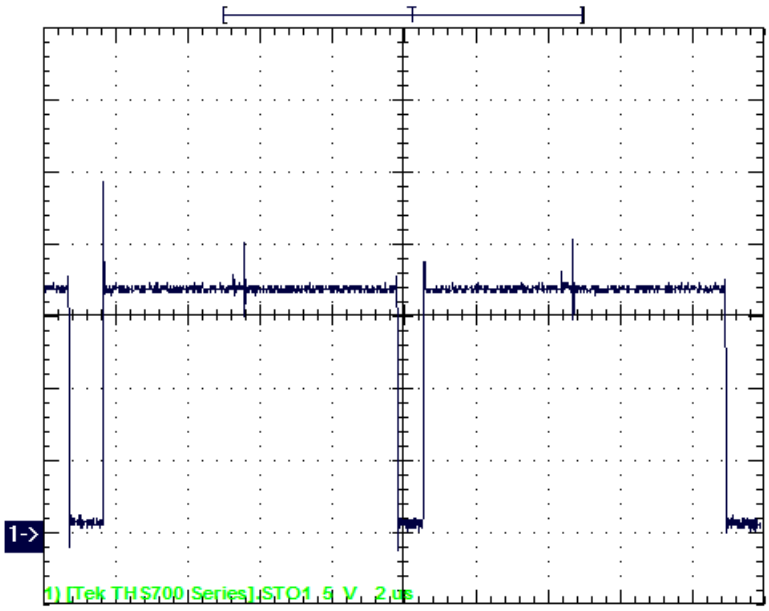
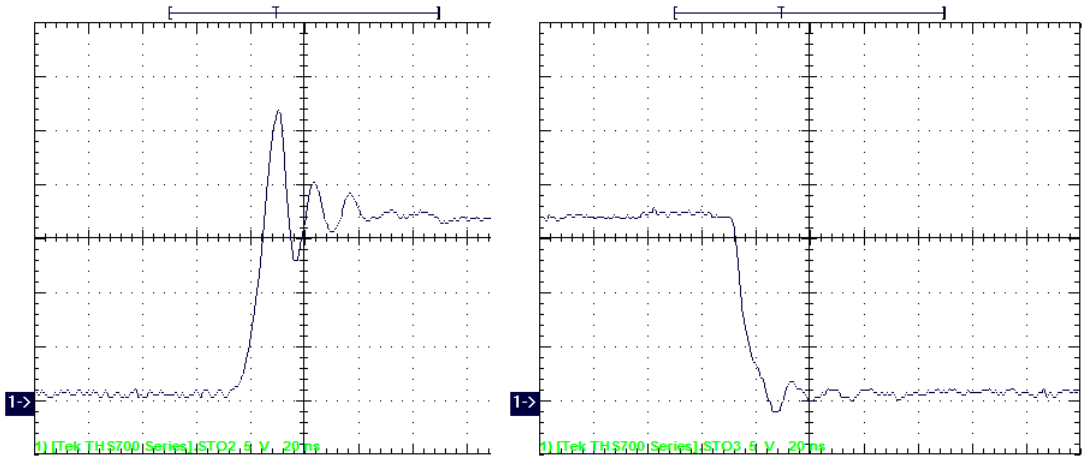
	Ch1 => 5V/div 2µs/div full bandwidth
	Ch1 => 5V/div 20ns/div

Figure 35

10.3.2.2 Gate Source

The waveform of the gate source voltage is shown in Figure 36 (boost LS).

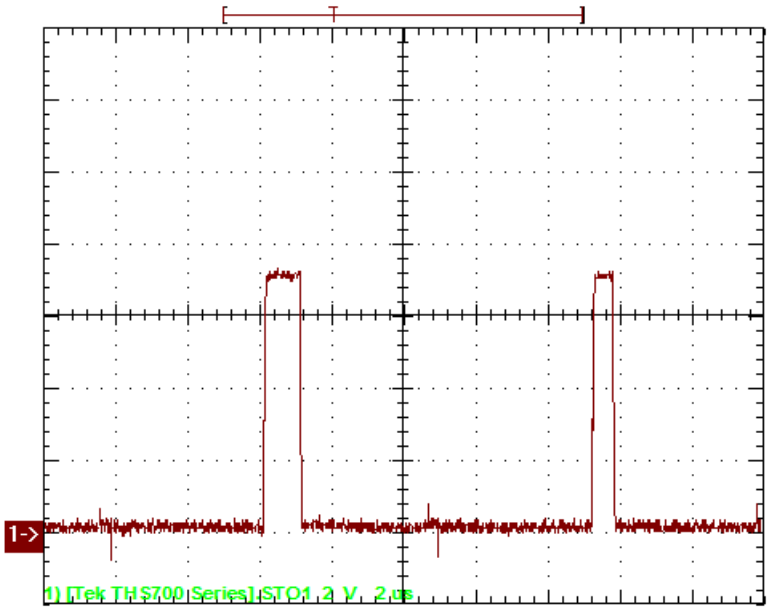
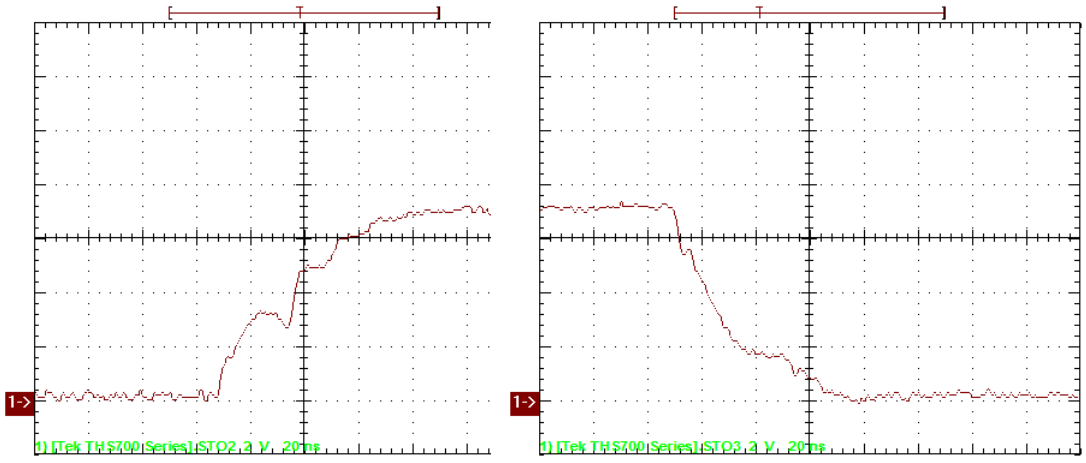
	Ch1 => 2V/div **2µs/div** full bandwidth
	Ch1 => 2V/div 20ns/div

Figure 36

10.3.3 **Buck** High Side (SW1) at 16V input = transfer region

10.3.3.1 Drain-Source

The waveform of the drain-source voltage is shown in Figure 37.

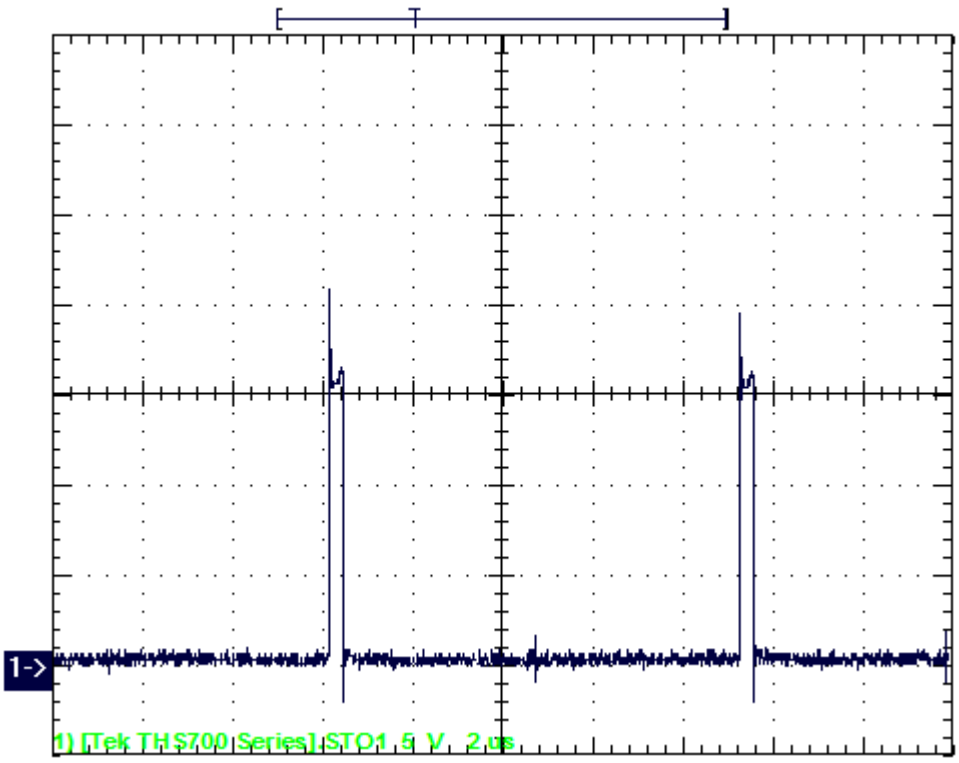
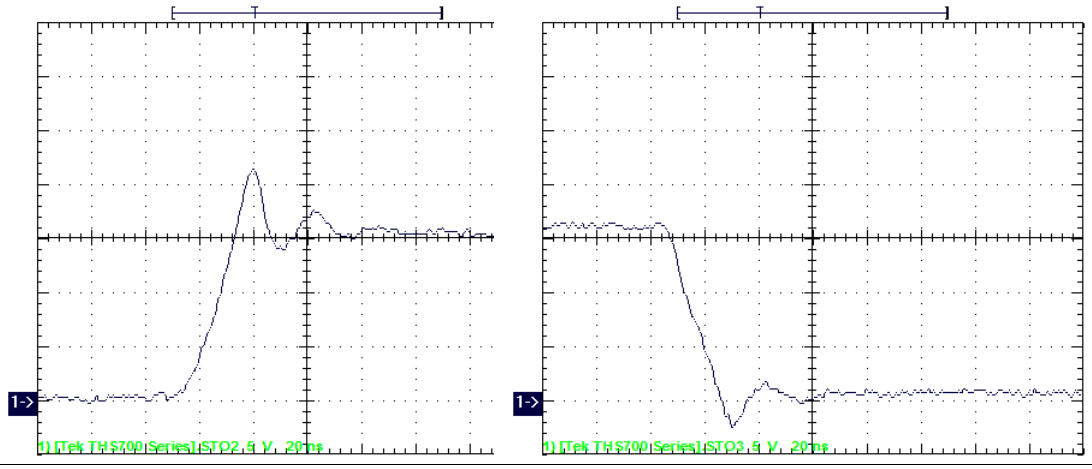
	Ch1 => 5V/div **2µs/div** full bandwidth
	Ch1 => 5V/div 20ns/div

Figure 37

10.3.3.2 Gate Source

The waveform of the **gate-source** voltage is shown in Figure 38 (buck HS)

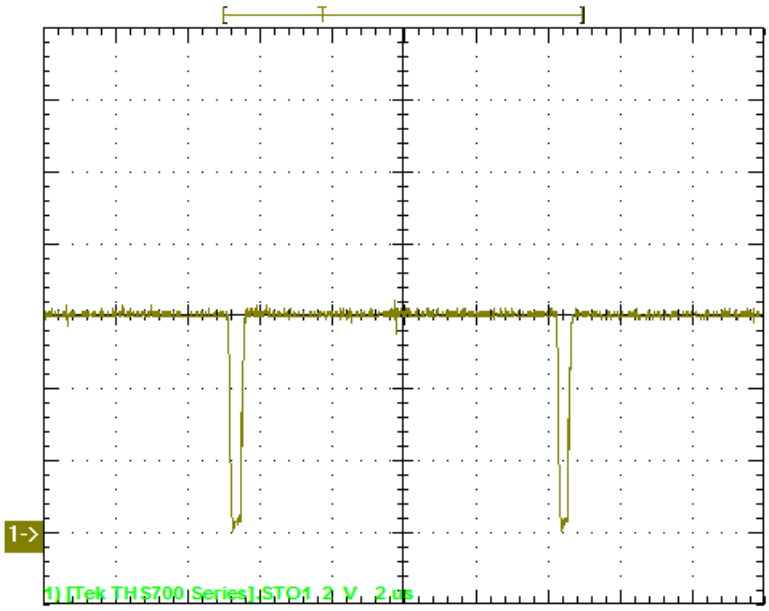
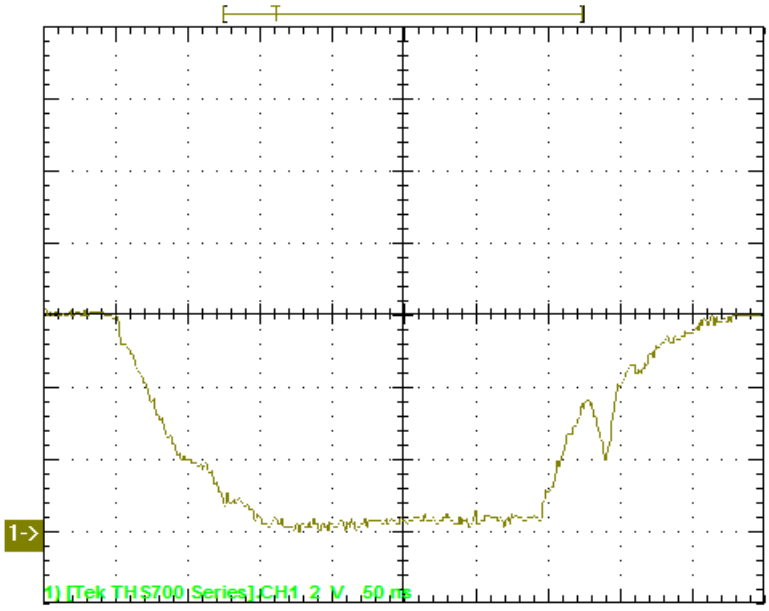
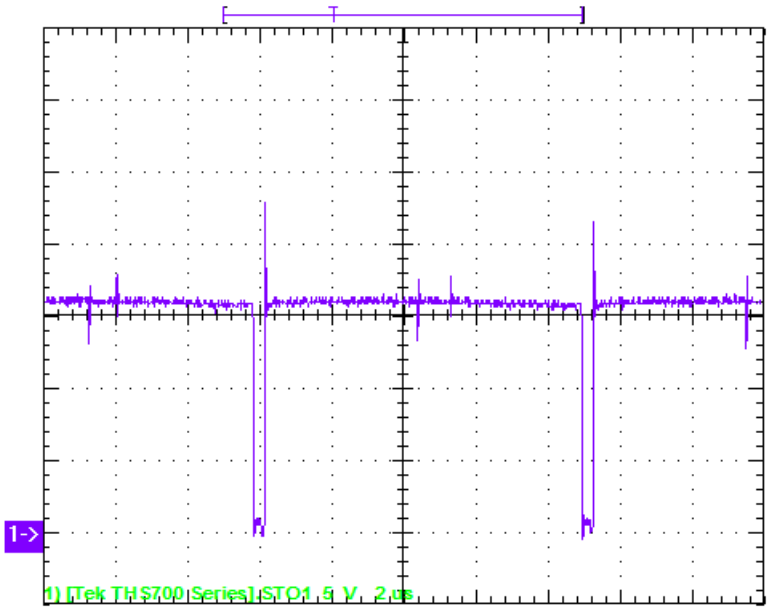
	Ch1 => 2V/div **2µs/div** full bandwidth
	Ch1 => 2V/div **50ns/div**

Figure 38

10.3.4 Buck Low Side (SW1)

10.3.4.1 Drain-Source

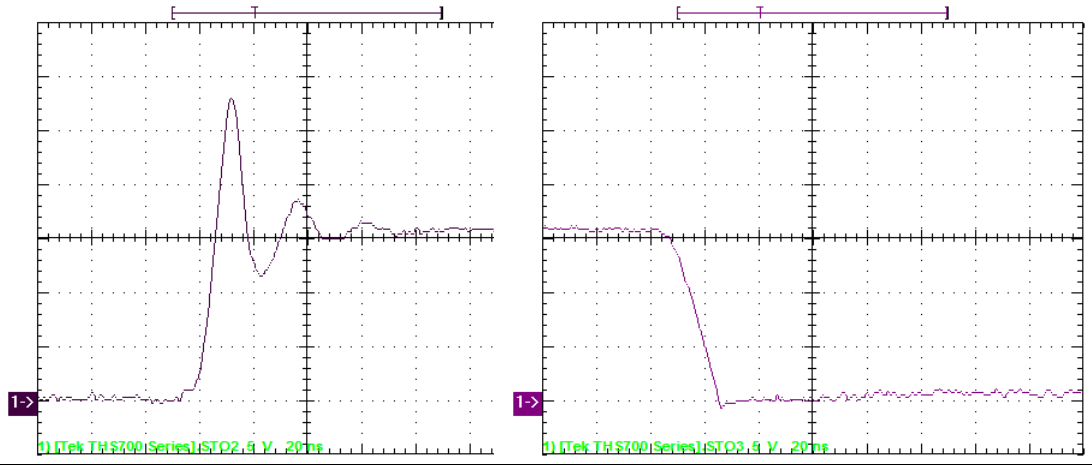
The waveform of the drain-source voltage is shown in Figure 39.



Ch1 =>
5V/div

2µs/div

full bandwidth



Ch1 =>
5V/div
20ns/div

Figure 39

10.3.4.2 Gate Source

The waveform of the **gate-source** voltage is shown in Figure 40 (buck LS)

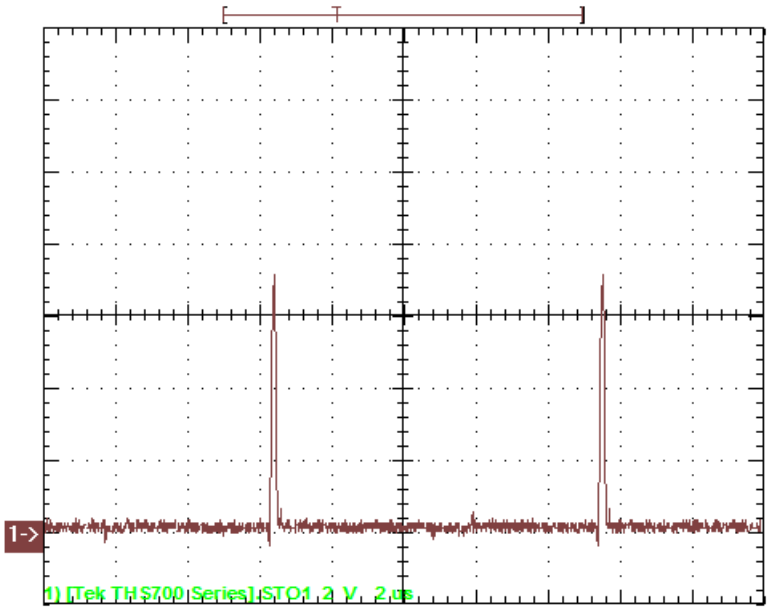
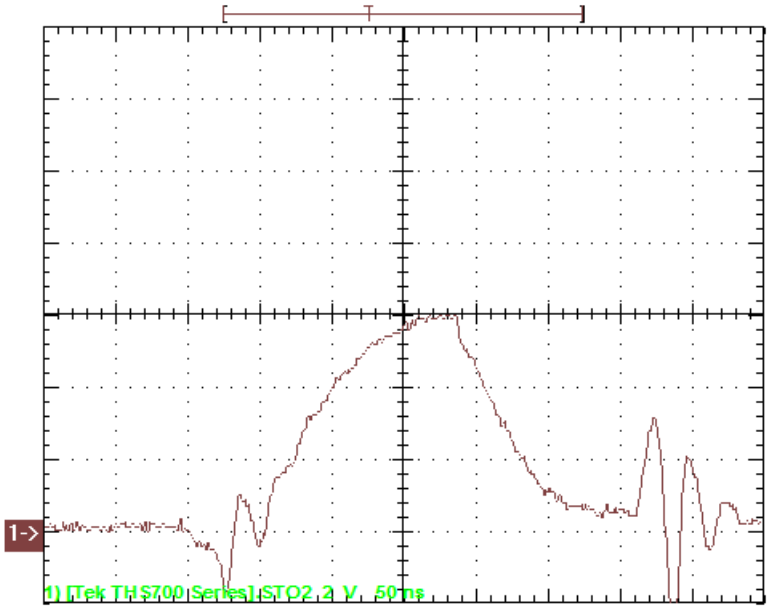
	Ch1 => 2V/div **2µs/div** full bandwidth
	Ch1 => 2V/div **50ns/div**

Figure 40

11 Thermal Image

Figure 41 shows the thermal image at 12V input voltage and 18A output current.

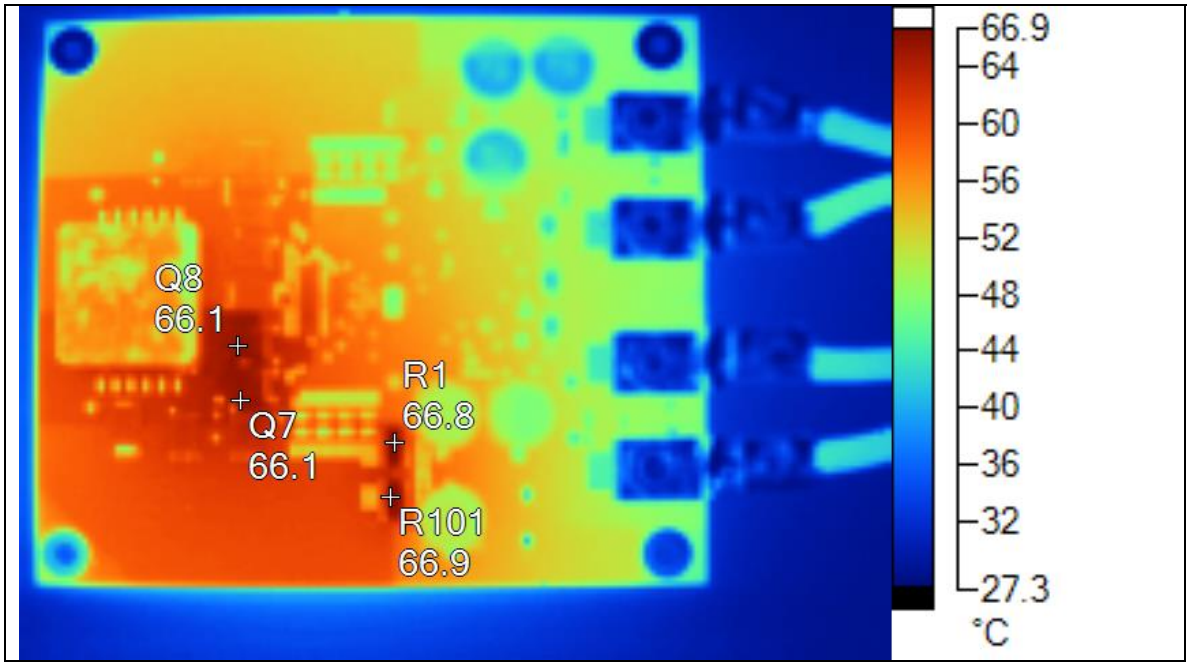


Figure 41

Name	Temperature
R101	66.9°C
Q8	66.1°C
R1	66.8°C
Q7	66.1°C

Figure 43 shows the thermal image at 14V input voltage and 18A output current.

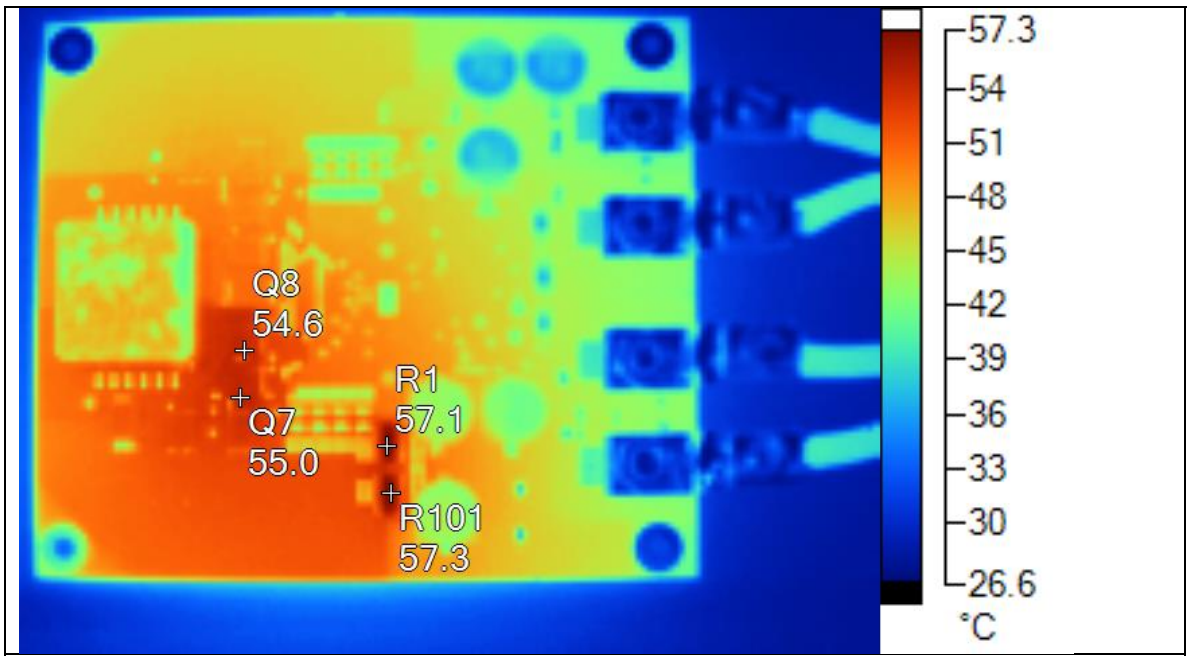


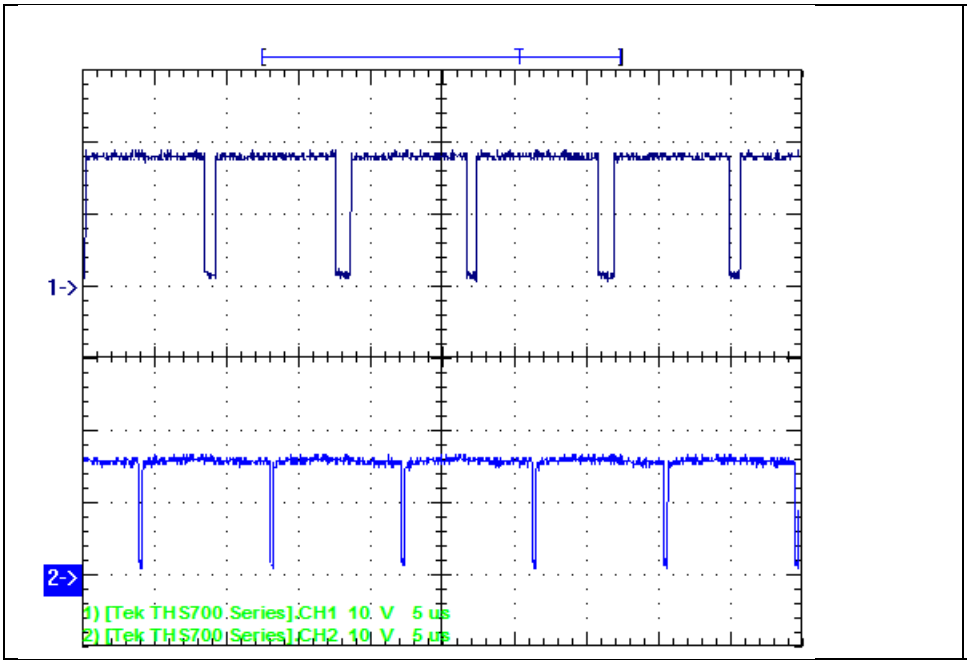
Figure 42

Name	Temperature
R101	57.3°C
Q8	54.6°C
Q7	55.0°C
R1	57.1°C

12 Addendum

12.1 Example of the switching behavior during the buck-boost transition

Figure 43 shows the waveforms of the 2 switchnodes at 16V input voltage



Ch1=> sw2
10V/div

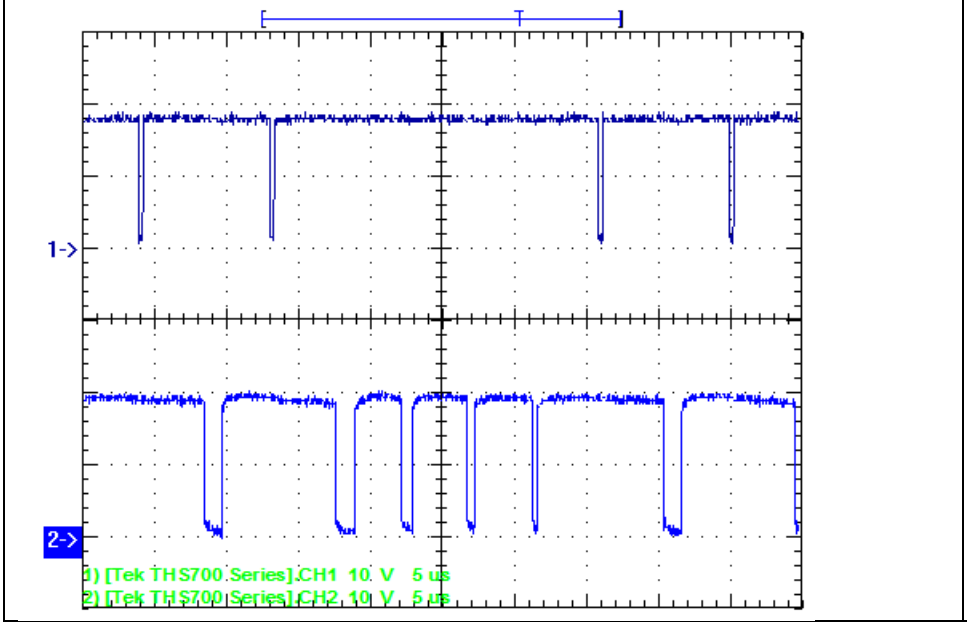
Ch2=> sw1
10V/div

5µs/div

20MHz bw

Figure 43

Figure 44 shows the waveforms of the 2 switchnodes at 19.3V input voltage



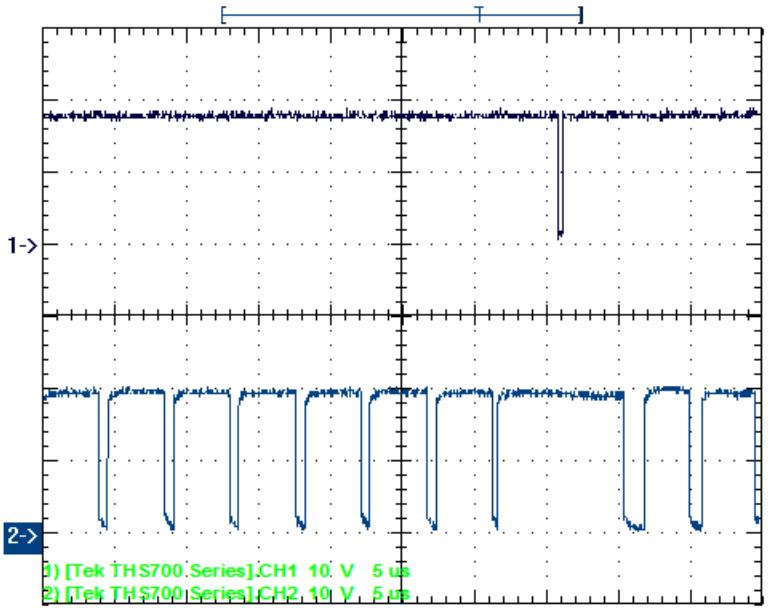
Ch1=> sw2
10V/div

Ch2=> sw1
10V/div

5µs/div

Figure 44

Figure 45 shows the waveforms of the 2 switchnodes at 19.79V input voltage



Ch1=> sw2
10V/div

Ch2=> sw1
10V/div

5µs/div

20MHz bw

Figure 45

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