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Schematic Revision Table

Date	Product number	Revision	Description
18/Feb/2008		0.1	Initial Version
20/Feb/2008		0.2	Add 2 LEDs
			Add TVS protected Diode
			Add Charge Current Calibration Resistance
03/Mar/2008		1.0	Update of schematic
24/Mar/2008		1.1	Redesign to compatible 5.5V Super Cap test
			Add 8 Charge Regulators
18/Nov/2009		2.0	Remove Current test part
			Remove Resistence for Power Supply
			Update of schematic
06/Apr/2011	630-40007-01	2.1	Update of schematic
15/Apr/2011	630-40007-01	03	Update of schematic

SUPER CAP RELIABILITY TEST BOARD

AGIGA TECH
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Super Cap Reliability Test Platform Diagram

Design by: CTU
Date: Jan 31, 2008
Version: 1.2

Navigation

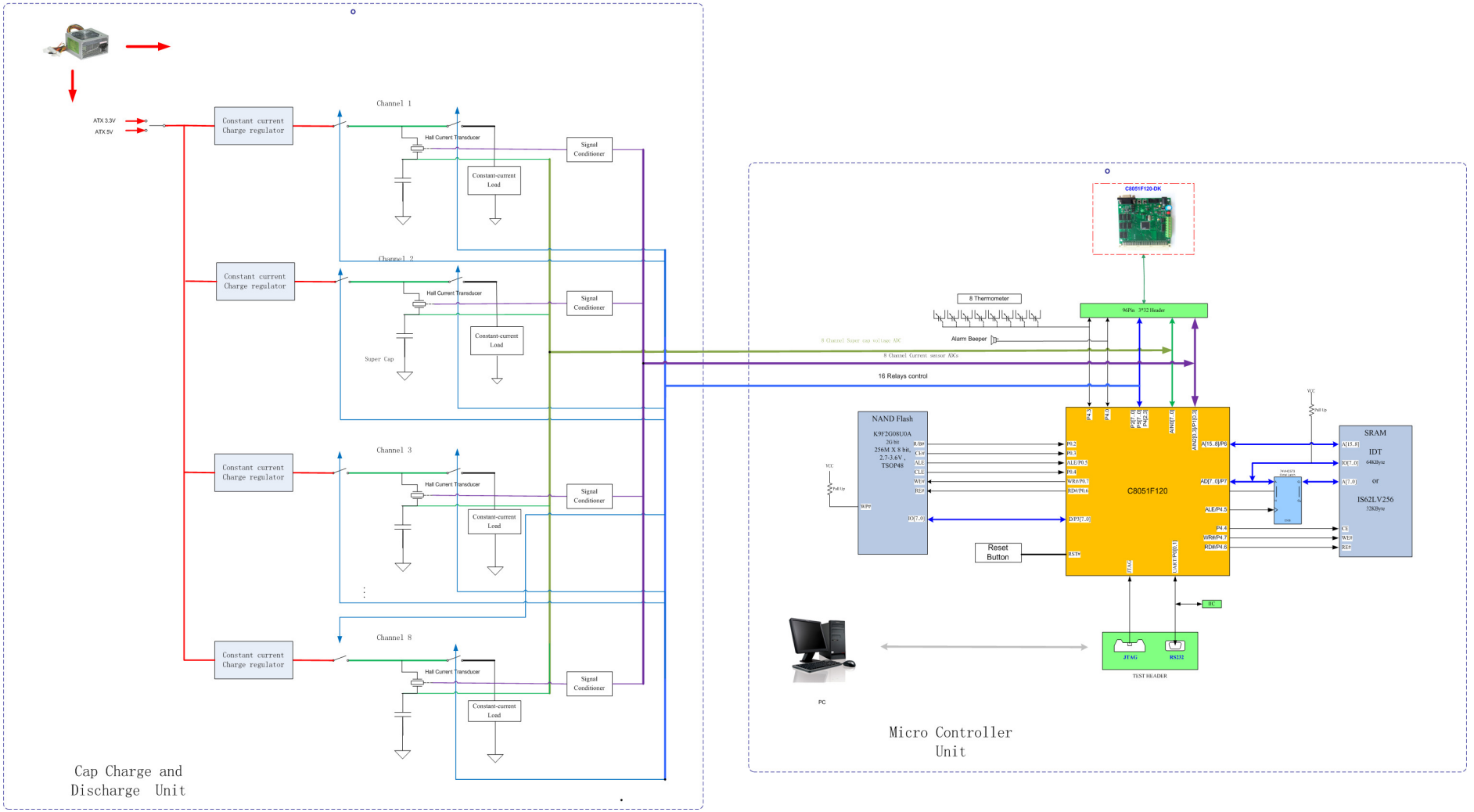
Power | Cap Voltage | Cap Current

Bus

MCU | Other IC | Button

HEADER | NOTE

NOTE
1. Charge Voltage and Current Adjust Manually.
2. Charge Voltage record is used for ADC judge whether charge complete.
3. Discharge current adjust by jumper.
4. In the period of working, protect relay shut down power when temperature Or cap voltage over limit.



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Sheet Title	02-SYSTEM DIAGRAM	
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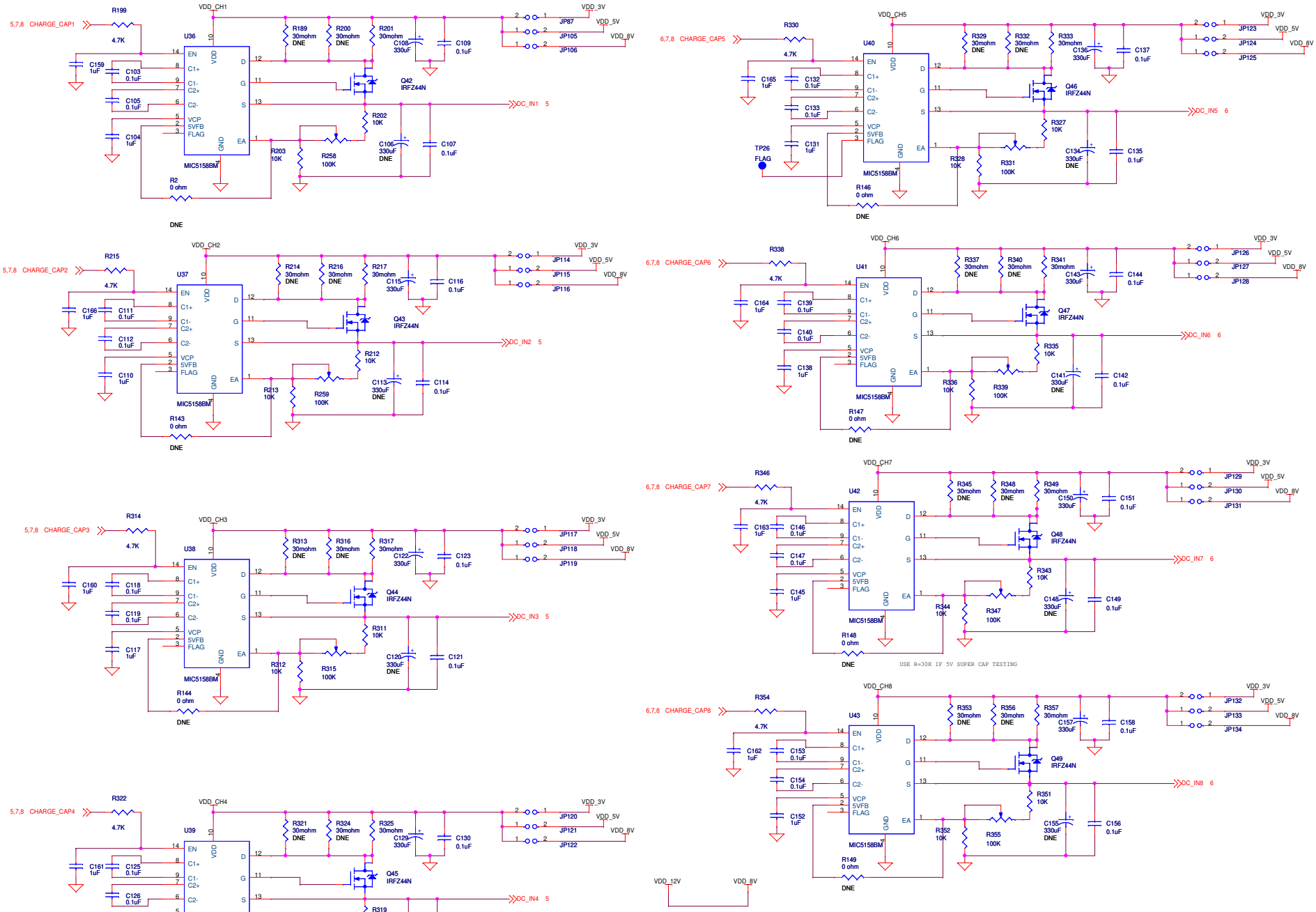

Note:
DNE:Do not install on 2.7V super cap test platform.

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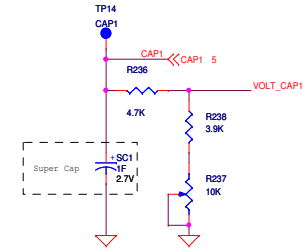

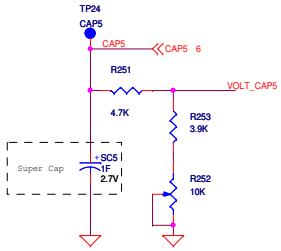

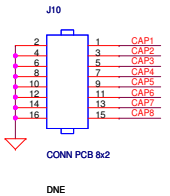

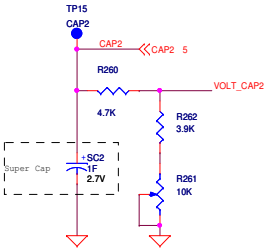

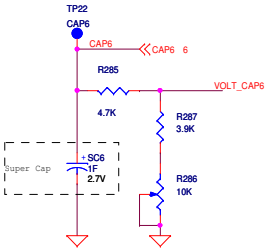

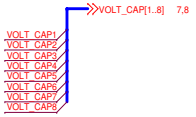

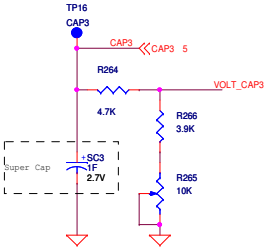

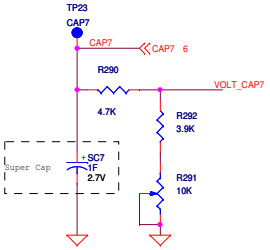

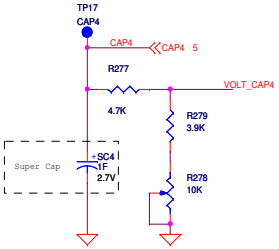

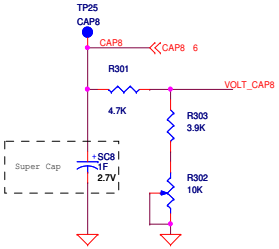

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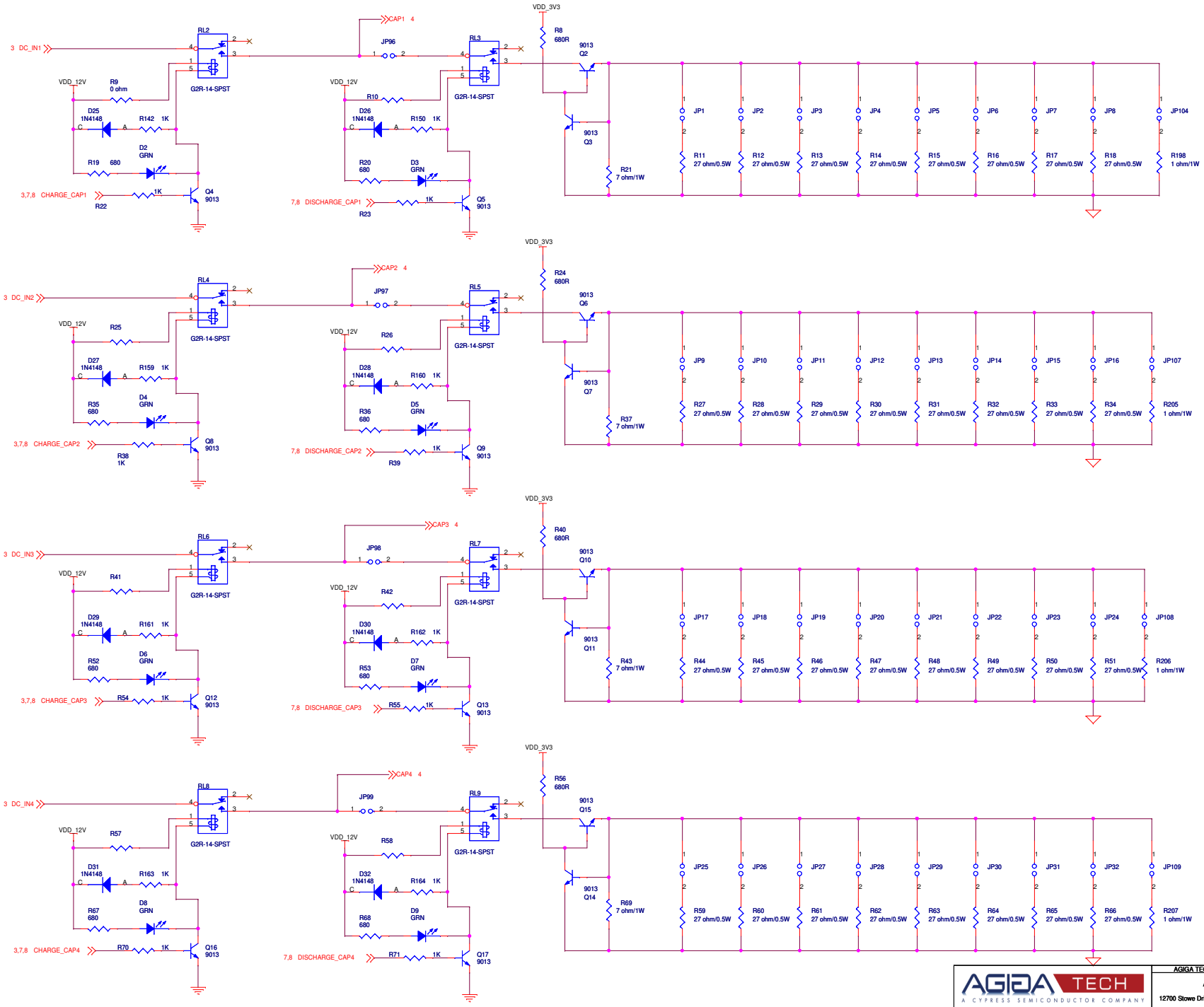

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Sheet Title: 05-CHARGE/DISCHARGE(CHANNEL1-4)

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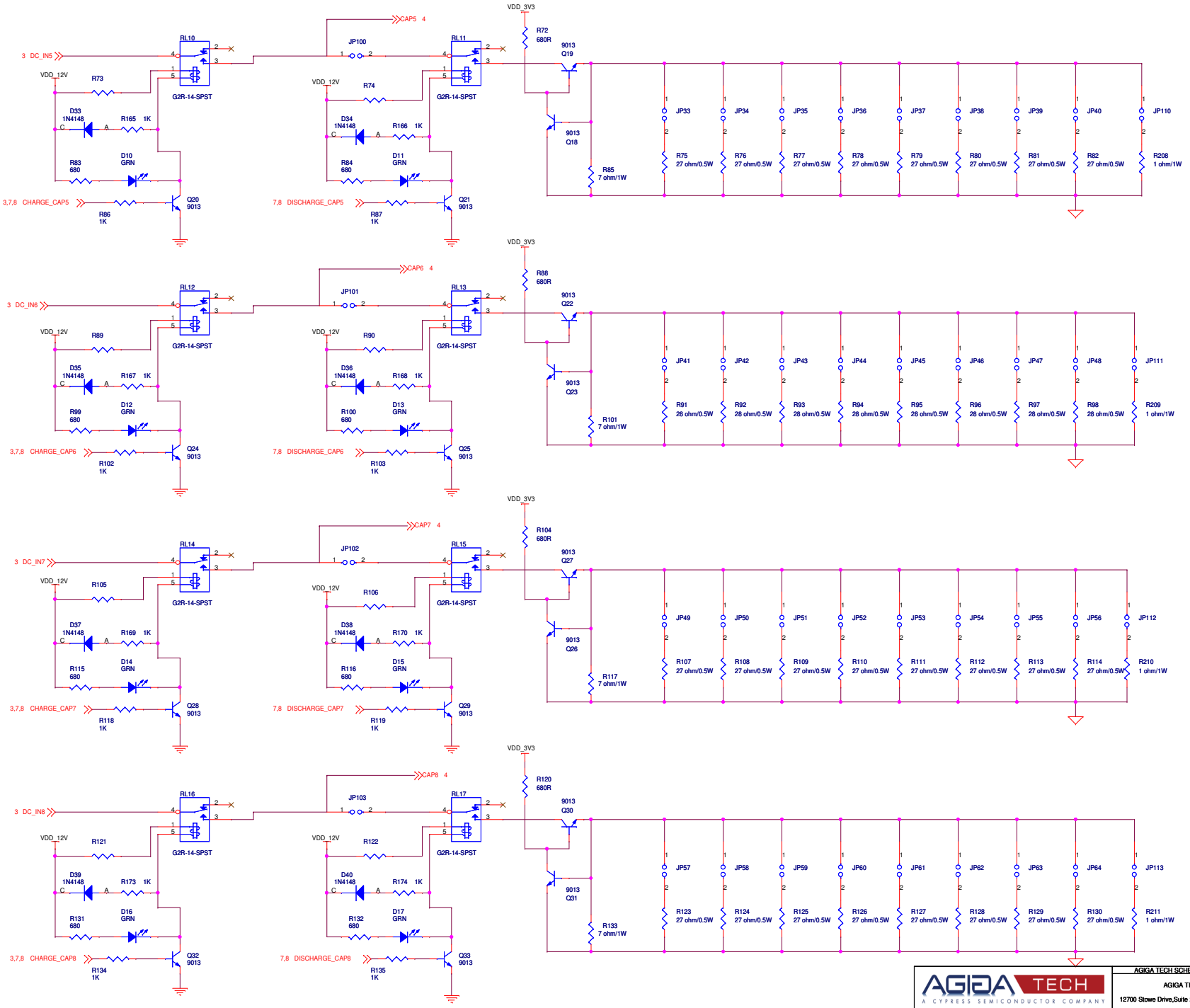

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Sheet Title: **05-CHARGE/DISCHARGE(CHANNEL5-8)**

Size	Document Number	Rev
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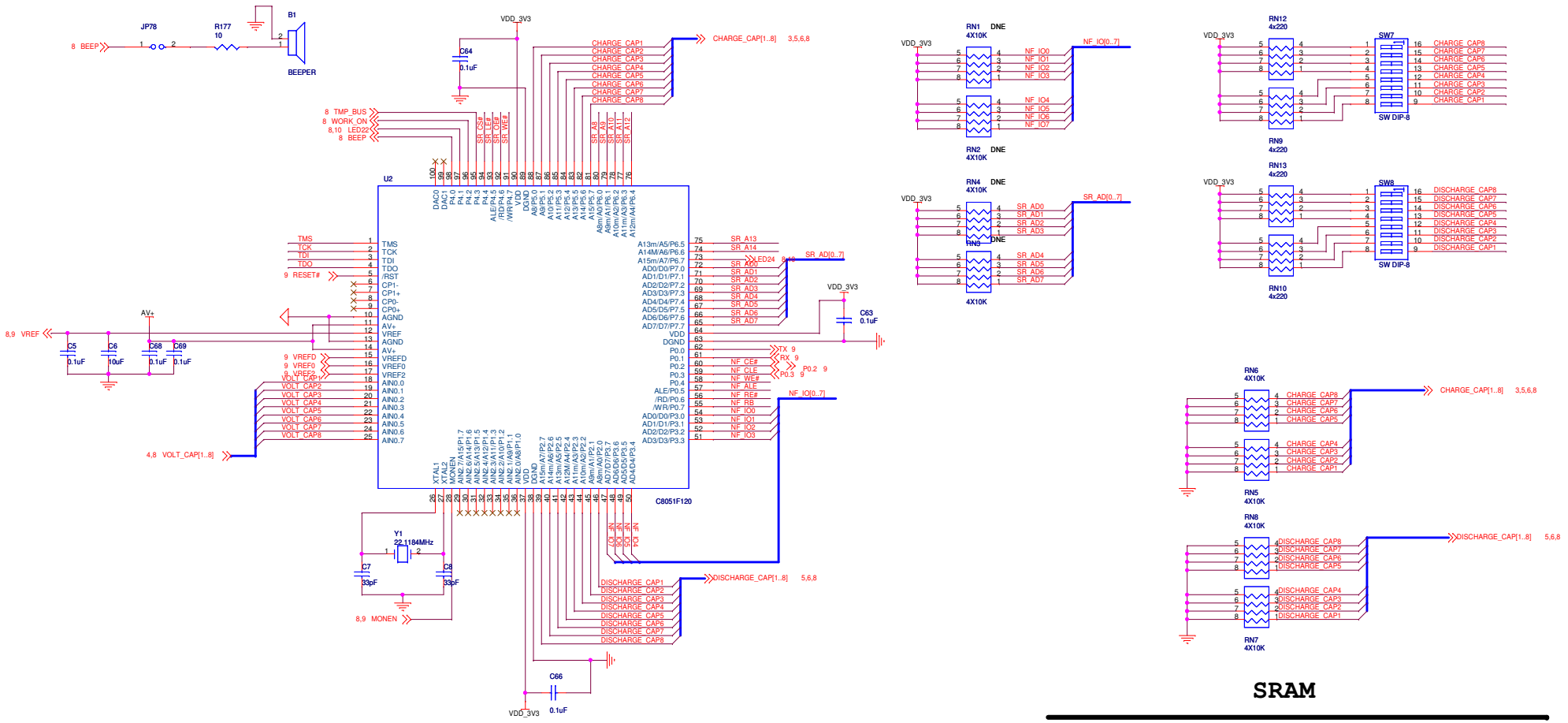
Date	Sheet	of
Thursday, August 04, 2011	6	13



Note:
DNE:Do not install on 2.7V super cap test platform.

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Sheet Title: 07-MCU,SRAM AND NANFLASH

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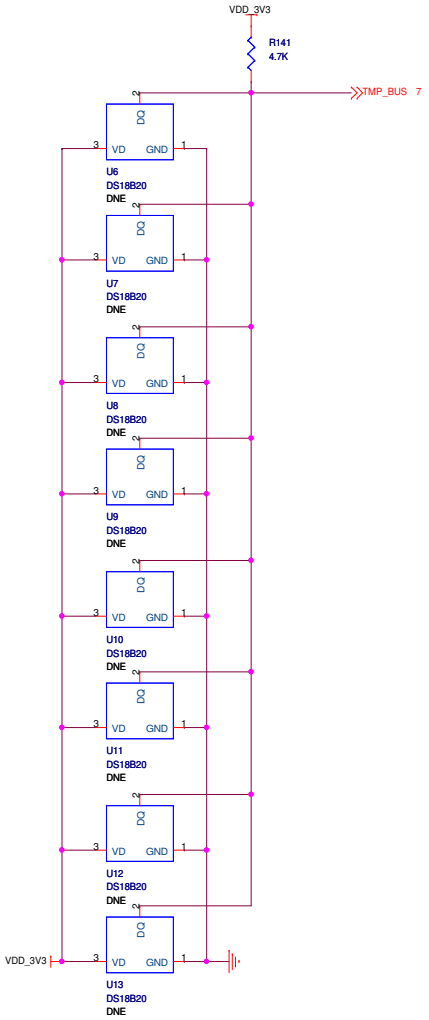
Thermometers

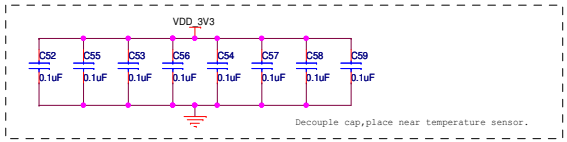


Pin #	Description
A-1	+3 VD2 (+3.3 VDC)
A-2	MONEN
A-3	P1.5
A-4	P1.2
A-5	P2.7
A-6	P2.4
A-7	P2.1
A-8	P3.6
A-9	P3.3
A-10	P3.0
A-11	P0.5
A-12	P0.2
A-13	P7.7
A-14	P7.4
A-15	P7.1
A-16	P6.6
A-17	P6.3
A-18	P6.0
A-19	P5.5
A-20	P5.2
A-21	P4.7
A-22	P4.4
A-23	P4.1
A-24	TCK
A-25	/RST
A-26	AGND (Analog Gnd)
A-27	CP1-
A-28	CP0+
A-29	VREF0
A-30	AIN0.6
A-31	AIN0.3
A-32	AIN0.0

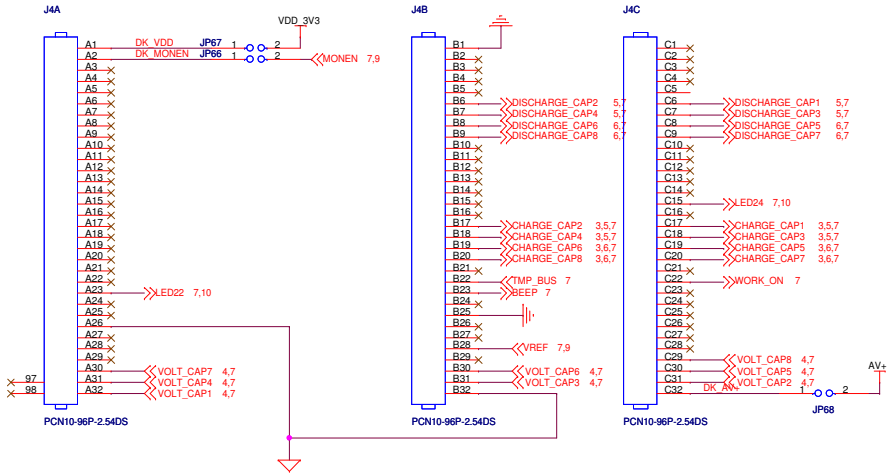
Pin #	Description
B-1	DGND (Digital Gnd)
B-2	P1.7
B-3	P1.4
B-4	P1.1
B-5	P2.6
B-6	P2.3
B-7	P2.0
B-8	P3.5
B-9	P3.2
B-10	P0.7
B-11	P0.4
B-12	P0.1
B-13	P7.6
B-14	P7.3
B-15	P7.0
B-16	P6.5
B-17	P6.2
B-18	P5.7
B-19	P5.4
B-20	P5.1
B-21	P4.6
B-22	P4.3
B-23	P4.0
B-24	TDI
B-25	DGND (Digital Gnd)
B-26	DAC1
B-27	CP1+
B-28	VREF
B-29	VREF1
B-30	AIN0.5
B-31	AIN0.2
B-32	AGND (Analog Gnd)

Pin #	Description
C-1	XTAL1
C-2	P1.6
C-3	P1.3
C-4	P1.0
C-5	P2.5
C-6	P2.2
C-7	P3.7
C-8	P3.4
C-9	P3.1
C-10	P0.6
C-11	P0.3
C-12	P0.0
C-13	P7.5
C-14	P7.2
C-15	P6.7
C-16	P6.4
C-17	P6.1
C-18	P5.6
C-19	P5.3
C-20	P5.0
C-21	P4.5
C-22	P4.2
C-23	TMS
C-24	TDO
C-25	VUNREG
C-26	DAC0
C-27	CP0-
C-28	VREFD
C-29	AIN0.7
C-30	AIN0.4
C-31	AIN0.1
C-32	AV+ (+3.3 VDC Analog)

C8051F120-DK J24 Pin Descriptions



96 PIN Header



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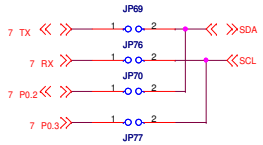
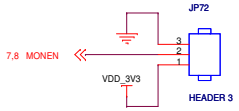
CONFIG

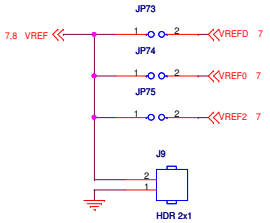


IIC Jumper

J69,J70,J76,J77 Installed:IIC bus on
J69,J70,J76,J77 Removed:IIC bus off

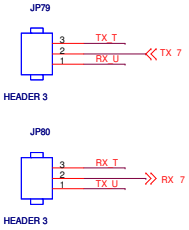


VDD Monitor Hardware Setup
The VDD Monitor of the C8051F120 may be disabled by moving the shorting blockfrom J6 pins 1-2 to pins 2-3

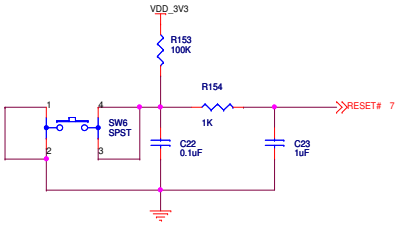


VREF Set Up

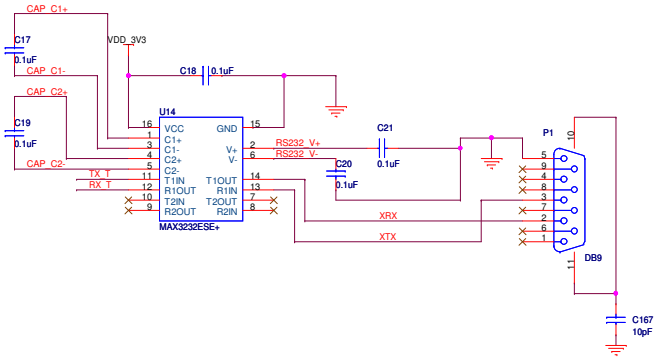
JP73 connect VREF to VREFD
JP74 connect VREF to VREF0
JP75 connect VREF to VREF2



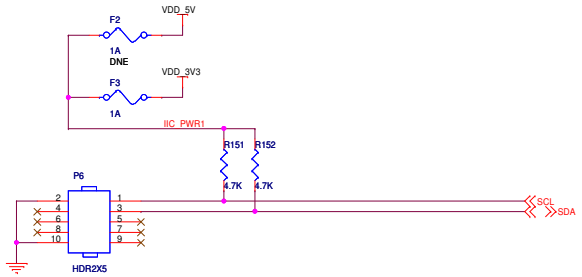
RESET

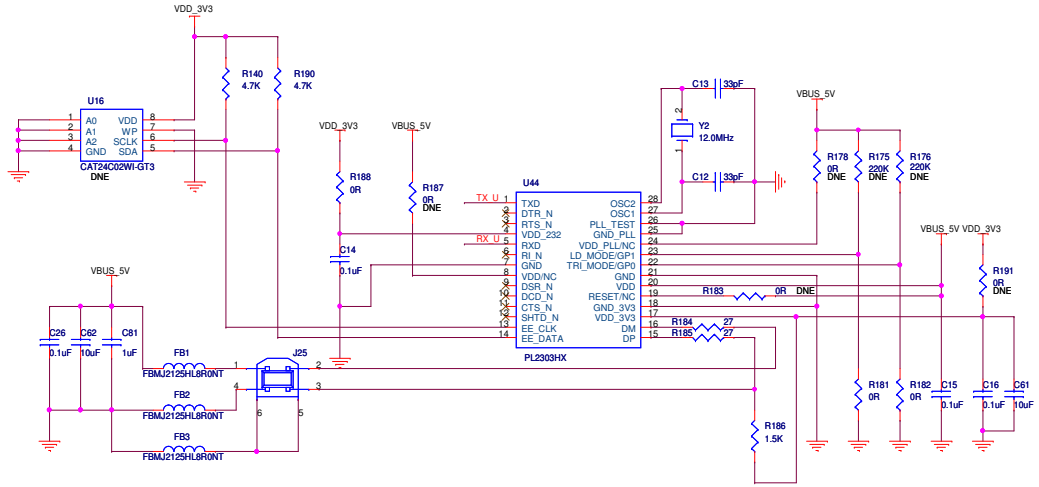


RS232



I2C Access Bus Header





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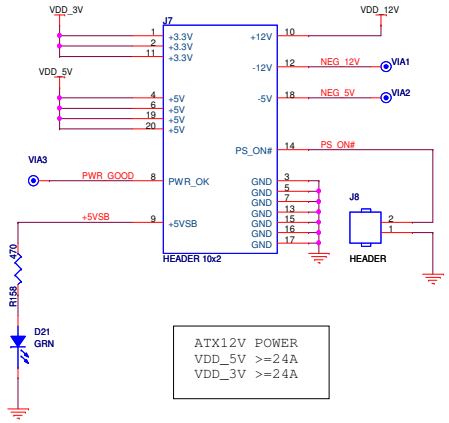
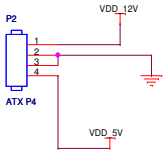
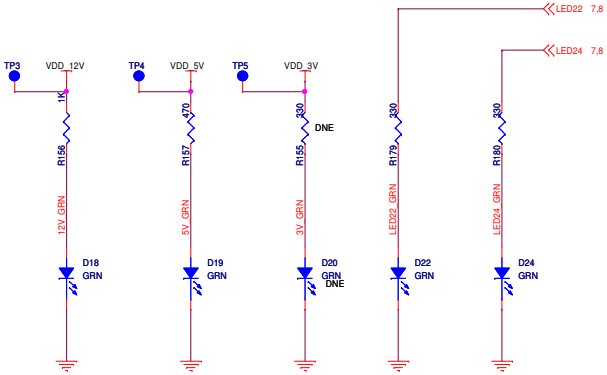
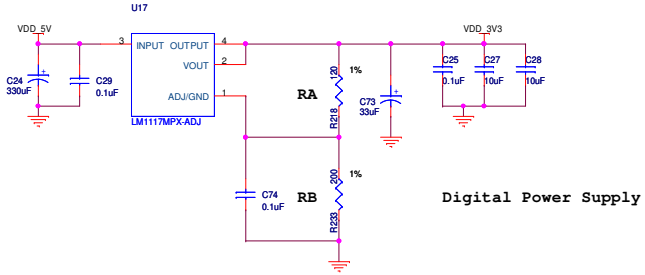
POWER SUPPLY

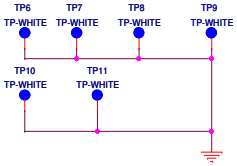




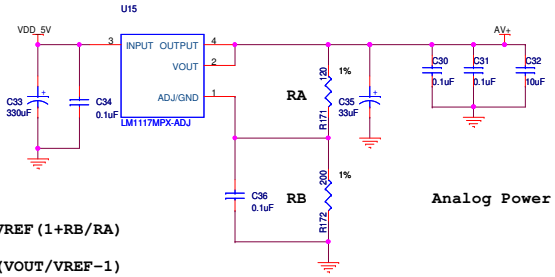




Digital Power Supply

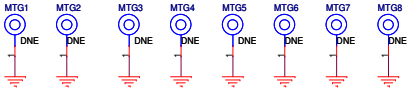


GROUND POINTS

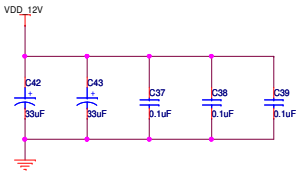


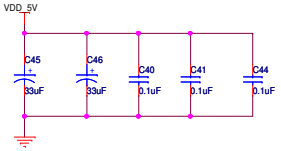
Analog Power Supply

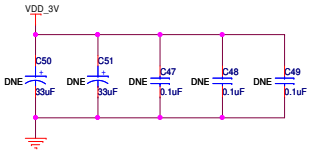
VOUT=VREF(1+RB/RA)
SO
RB=RA(VOUT/VREF-1)
WHERE VREF=1.25VOLT



Mounting holes.







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Title: **SUPER CAP RELIABILITY TEST BOARD**

Sheet Title: **10-POWER SUPPLY**

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GPIO Mapping

PIO Num	Main Function
P0.0	UART TX
P0.1	UART RX
P0.2	NANDFLASH CE#
P0.3	NANDFLASH CLE
P0.4	NANDFLASH WE#
P0.5	NANDFLASH ALE
P0.6	NANDFLASH RE#
P0.7	NANDFLASH RB
P1.0	
P1.1	
P1.2	
P1.3	
P1.4	
P1.5	
P1.6	
P1.7	
P2.0	DISCHARGE CAP1
P2.1	DISCHARGE CAP2
P2.2	DISCHARGE CAP3
P2.3	DISCHARGE CAP4
P2.4	DISCHARGE CAP5
P2.5	DISCHARGE CAP6
P2.6	DISCHARGE CAP7
P2.7	DISCHARGE CAP8
P3.0	NANDFLASH IO0
P3.1	NANDFLASH IO1
P3.2	NANDFLASH IO2
P3.3	NANDFLASH IO3
P3.4	NANDFLASH IO4
P3.5	NANDFLASH IO5
P3.6	NANDFLASH IO6
P3.7	NANDFLASH IO7

PIO Num	Main Function
P4.0	BEEPER
P4.1	LED22
P4.2	WORK ON
P4.3	Temperature Sensor 1 Wire Bus
P4.4	SRAM CS#
P4.5	SRAM LE#
P4.6	SRAM OE#
P4.7	SRAM WE#
P5.0	CHARGE CAP1
P5.1	CHARGE CAP2
P5.2	CHARGE CAP3
P5.3	CHARGE CAP4
P5.4	CHARGE CAP5
P5.5	CHARGE CAP6
P5.6	CHARGE CAP7
P5.7	CHARGE CAP8
P6.0	SRAM A8
P6.1	SRAM A9
P6.2	SRAM A10
P6.3	SRAM A11
P6.4	SRAM A12
P6.5	SRAM A13
P6.6	SRAM A14
P6.7	LED24
P7.0	SRAM A0 OR D0
P7.1	SRAM A1 OR D1
P7.2	SRAM A2 OR D2
P7.3	SRAM A3 OR D3
P7.4	SRAM A4 OR D4
P7.5	SRAM A5 OR D5
P7.6	SRAM A6 OR D6
P7.7	SRAM A7 OR D7

PIO Num	Main Function
AIN0.0	Super cap 1 Voltage input
AIN0.1	Super cap 2 Voltage input
AIN0.2	Super cap 3 Voltage input
AIN0.3	Super cap 4 Voltage input
AIN0.4	Super cap 5 Voltage input
AIN0.5	Super cap 6 Voltage input
AIN0.6	Super cap 7 Voltage input
AIN0.7	Super cap 8 Voltage input

JUMPER SETTINGS

DISCHARGE CURRENT JUMPER

Jumper Num	Installed	Removed
JP1	add 25 mA Super Cap1 discharge current	do not add 25 mA Super Cap1 discharge current
JP2	add 25 mA Super Cap1 discharge current	do not add 25 mA Super Cap1 discharge current
JP3	add 25 mA Super Cap1 discharge current	do not add 25 mA Super Cap1 discharge current
JP4	add 25 mA Super Cap1 discharge current	do not add 25 mA Super Cap1 discharge current
JP5	add 25 mA Super Cap1 discharge current	do not add 25 mA Super Cap1 discharge current
JP6	add 25 mA Super Cap1 discharge current	do not add 25 mA Super Cap1 discharge current
JP7	add 25 mA Super Cap1 discharge current	do not add 25 mA Super Cap1 discharge current
JP8	add 25 mA Super Cap1 discharge current	do not add 25 mA Super Cap1 discharge current
JP9	add 25 mA Super Cap2 discharge current	do not add 25 mA Super Cap2 discharge current
JP10	add 25 mA Super Cap2 discharge current	do not add 25 mA Super Cap2 discharge current
JP11	add 25 mA Super Cap2 discharge current	do not add 25 mA Super Cap2 discharge current
JP12	add 25 mA Super Cap2 discharge current	do not add 25 mA Super Cap2 discharge current
JP13	add 25 mA Super Cap2 discharge current	do not add 25 mA Super Cap2 discharge current
JP14	add 25 mA Super Cap2 discharge current	do not add 25 mA Super Cap2 discharge current
JP15	add 25 mA Super Cap2 discharge current	do not add 25 mA Super Cap2 discharge current
JP16	add 25 mA Super Cap2 discharge current	do not add 25 mA Super Cap2 discharge current
JP17	add 25 mA Super Cap3 discharge current	do not add 25 mA Super Cap3 discharge current
JP18	add 25 mA Super Cap3 discharge current	do not add 25 mA Super Cap3 discharge current
JP19	add 25 mA Super Cap3 discharge current	do not add 25 mA Super Cap3 discharge current
JP20	add 25 mA Super Cap3 discharge current	do not add 25 mA Super Cap3 discharge current
JP21	add 25 mA Super Cap3 discharge current	do not add 25 mA Super Cap3 discharge current
JP22	add 25 mA Super Cap3 discharge current	do not add 25 mA Super Cap3 discharge current
JP23	add 25 mA Super Cap3 discharge current	do not add 25 mA Super Cap3 discharge current
JP24	add 25 mA Super Cap3 discharge current	do not add 25 mA Super Cap3 discharge current
JP25	add 25 mA Super Cap4 discharge current	do not add 25 mA Super Cap4 discharge current
JP26	add 25 mA Super Cap4 discharge current	do not add 25 mA Super Cap4 discharge current
JP27	add 25 mA Super Cap4 discharge current	do not add 25 mA Super Cap4 discharge current
JP28	add 25 mA Super Cap4 discharge current	do not add 25 mA Super Cap4 discharge current
JP29	add 25 mA Super Cap4 discharge current	do not add 25 mA Super Cap4 discharge current
JP30	add 25 mA Super Cap4 discharge current	do not add 25 mA Super Cap4 discharge current
JP31	add 25 mA Super Cap4 discharge current	do not add 25 mA Super Cap4 discharge current
JP32	add 25 mA Super Cap4 discharge current	do not add 25 mA Super Cap4 discharge current
JP33	add 25 mA Super Cap5 discharge current	do not add 25 mA Super Cap5 discharge current
JP34	add 25 mA Super Cap5 discharge current	do not add 25 mA Super Cap5 discharge current
JP35	add 25 mA Super Cap5 discharge current	do not add 25 mA Super Cap5 discharge current
JP36	add 25 mA Super Cap5 discharge current	do not add 25 mA Super Cap5 discharge current
JP37	add 25 mA Super Cap5 discharge current	do not add 25 mA Super Cap5 discharge current
JP38	add 25 mA Super Cap5 discharge current	do not add 25 mA Super Cap5 discharge current
JP39	add 25 mA Super Cap5 discharge current	do not add 25 mA Super Cap5 discharge current
JP40	add 25 mA Super Cap5 discharge current	do not add 25 mA Super Cap5 discharge current
JP41	add 25 mA Super Cap6 discharge current	do not add 25 mA Super Cap6 discharge current
JP42	add 25 mA Super Cap6 discharge current	do not add 25 mA Super Cap6 discharge current
JP43	add 25 mA Super Cap6 discharge current	do not add 25 mA Super Cap6 discharge current
JP44	add 25 mA Super Cap6 discharge current	do not add 25 mA Super Cap6 discharge current
JP45	add 25 mA Super Cap6 discharge current	do not add 25 mA Super Cap6 discharge current
JP46	add 25 mA Super Cap6 discharge current	do not add 25 mA Super Cap6 discharge current
JP47	add 25 mA Super Cap6 discharge current	do not add 25 mA Super Cap6 discharge current
JP48	add 25 mA Super Cap6 discharge current	do not add 25 mA Super Cap6 discharge current
JP49	add 25 mA Super Cap7 discharge current	do not add 25 mA Super Cap7 discharge current
JP50	add 25 mA Super Cap7 discharge current	do not add 25 mA Super Cap7 discharge current
JP51	add 25 mA Super Cap7 discharge current	do not add 25 mA Super Cap7 discharge current
JP52	add 25 mA Super Cap7 discharge current	do not add 25 mA Super Cap7 discharge current
JP53	add 25 mA Super Cap7 discharge current	do not add 25 mA Super Cap7 discharge current
JP54	add 25 mA Super Cap7 discharge current	do not add 25 mA Super Cap7 discharge current
JP55	add 25 mA Super Cap7 discharge current	do not add 25 mA Super Cap7 discharge current
JP56	add 25 mA Super Cap7 discharge current	do not add 25 mA Super Cap7 discharge current
JP57	add 25 mA Super Cap8 discharge current	do not add 25 mA Super Cap8 discharge current
JP58	add 25 mA Super Cap8 discharge current	do not add 25 mA Super Cap8 discharge current
JP59	add 25 mA Super Cap8 discharge current	do not add 25 mA Super Cap8 discharge current
JP60	add 25 mA Super Cap8 discharge current	do not add 25 mA Super Cap8 discharge current
JP61	add 25 mA Super Cap8 discharge current	do not add 25 mA Super Cap8 discharge current
JP62	add 25 mA Super Cap8 discharge current	do not add 25 mA Super Cap8 discharge current
JP63	add 25 mA Super Cap8 discharge current	do not add 25 mA Super Cap8 discharge current
JP64	add 25 mA Super Cap8 discharge current	do not add 25 mA Super Cap8 discharge current

NANDFLASH COUNTROL JUMPER

Jumper Num	Installed	Removed
JP65	NANDFLSH write protected	NANDFLSH write unprotected

CONNECT TO DK BOARD CONNECTER

Jumper Num	Installed	Removed
JP66	connect DK board 3.3V to SCRT board	disconnect DK board 3.3V to SCRT board
JP67	connect DK board MONEN to SCRT board	disconnect DK board MONEN to SCRT board
JP68	connect DK board AV+ to SCRT board	disconnect DK board AV+ to SCRT board

CONNECT TO I2C CONNECTER

Jumper Num	Installed	Removed
JP69	connect I2C SDA to P0.0	disconnect I2C SDA to P0.0
JP70	connect I2C SCL to P0.1	disconnect I2C SCL to P0.1
JP76	connect I2C SDA to P0.2	disconnect I2C SDA to P0.2
JP77	connect I2C SCL to P0.3	disconnect I2C SCL to P0.3

C8051 Config

Jumper Num	1-2 Installed	2-3 Installed
JP72	VDD Monitor enable	VDD Monitor disnable

Jumper Num	Installed	Removed
JP73	connect VREF to VREFD	disconnect VREF to VREFD
JP74	connect VREF to VREF0	disconnect VREF to VREF0
JP75	connect VREF to VREF2	disconnect VREF to VREF2

Charge Current Calibration Jumper

Jumper Num	Installed	Removed
JP78	Current Calibration	Normal

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AGIGA TECH SCHEMATIC TITLE BLOCK

AGIGA TECH INC

12700 Stowe Drive,Suite 280 Poway,CA 92064 USA

Title: SUPER CAP RELIABILITY TEST BOARD

Sheet Title: 11-GPIO INFO AND JUMPER SETTING

Size	Document Number	Rev
B	630-40007-01	03

Date	Sheet
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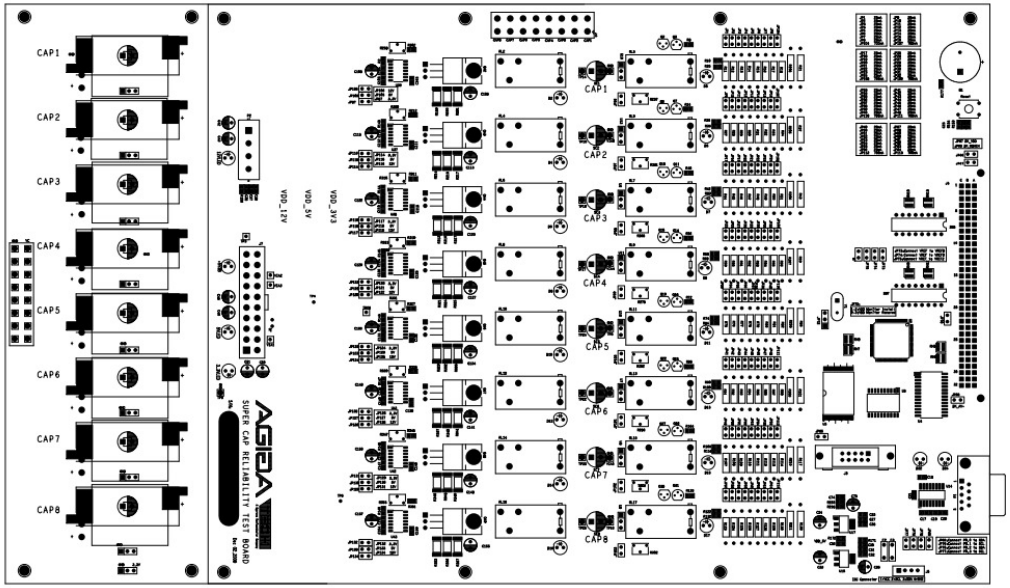
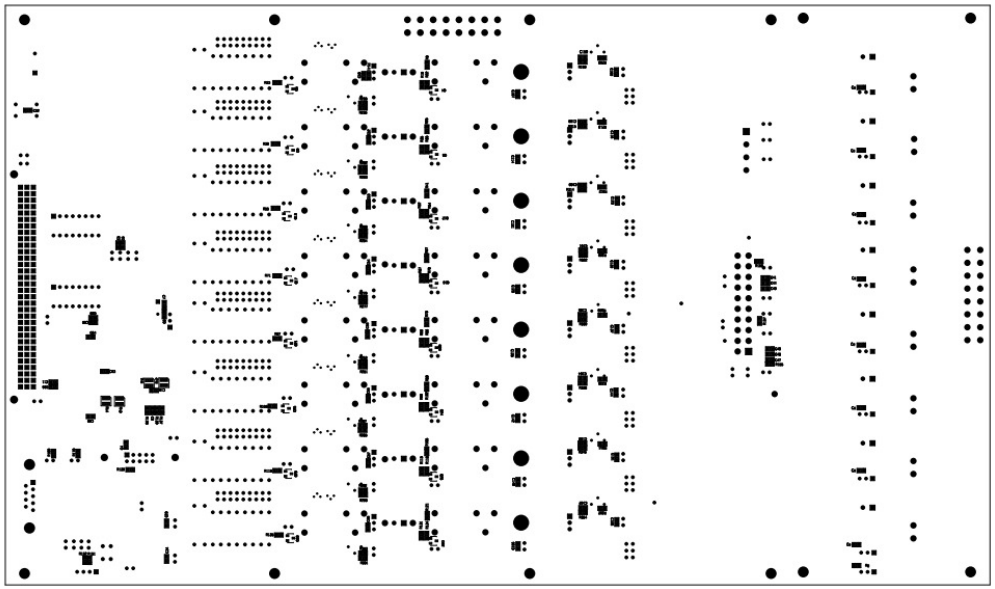


Top Side



Bottom Side

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Title: SUPER CAP RELIABILITY TEST BOARD		
Sheet Title: 12-LAYOUT		
Size: C	Document Number: 630-40007-01	Rev: 03
Date: Thursday, August 04, 2011	Sheet 12 of 13	

Change Log

Date	Description	Revision
1	Change R8,R24,R40,R56,R72,R88,R104,R120 from 1k ohm to 51 ohm.	
2	Add 8 channel Charge Regulators	
3	Compatible test both 5.5V and 2.7V caps.	
4	Add a jumper to jump a bigger discharge current(1A) on each channel.	
5	add 7 Current transducers.	
6	Remove the Current transducers.	
7	Remove Resistence for Power Supply.	
06/Apr/2011	1, Changed project name to 630-40007-01.	2.1
	2, Added U44 and relativet parts for RS232 transfer USB.	
	3, Modefied Q2,3,6,7,10,11,14,15,18,19,22,23,26,27,30,31 pins name.	
	4, Changed R237,252,261,286,265,291,278,302 to 10K.	
	5, Changed R258,331,259,339,315,347,323,355 to 100K.	
	6, Added D25-40, R142,150,159-170,173,174.	
15/Apr/2011	1, Changed title and document number.	03
	2, Changed 4pins J5 to 10pins P6.	

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Title: **SUPER CAP RELIABILITY TEST BOARD**

Sheet Title: **13-CHANGE LOG**

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B	630-40007-01	03

Date	Sheet
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