CORONADO Firmware Specification

Version 0.83

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Revision History

Revision	Date	Description of Changes
0.83	14 Jan 2013	• Removed text from Table 1: EEDATA that indicated the EEPROM address was automatically incremented • Updated Table 1: RELEASENF reg to indicate RW capability, not just W • Updated description of the EEERROR bit in EEBUSY • Added expected duration for canceling a BACKUP or RESTORE • Clarified that the "PGEM Power Present" bit in GTG2 will be 1 only after the Ultracaps are fully charged on PGEMs that do not have an onboard charger • Added a description of the VCAP register • Added a Type column to Table 7: NVDIMM EEPROM Contents and Table 10: PGEM EEPROM Contents • Removed the statement "The maximum reported number is 15" from the UNCORNF description
0.82	13 Dec 2012	• Removed highlighting for CATALINA register backwards compatibility in table 1. • Added EEBUSY timeout information in section 6.2 • Added 2 bits to GTG2, PGEM Power Present[5] and VCAP Error[4] • Updated the description of the I2C RESET command in section 6.33 • Minor corrections to the "source" column of Table 6: CORONADO EEPROM Contents • Removed the statement that during a controlled power-down the BAKRSLT register will be reset. It will maintain its value during a power down. • Removed the description of T_LASTPF • Corrected statement that reserved values in the EEPROM return 0x00 • Added units of Farads to INITIALCAP value in PGEM EEPROM • Numerous grammatical corrections
0.81	13 Nov 2012	• Added back Register 0x07 CMSTAT to report cap measurement status • Corrected VCAP units to 100mV, was 1mV which was incorrect • Removed grayed out formatting, sections that are not implemented in FW will be noted in FW release notes • Added a better description of t_{CKE_LOW} in the ENBKUP section • Added back the CMSTAT register for cap measurement status • Fixed PGEM EEPROM table address range typo • Corrected the Alert Response 7-bit address in Figure 7 • Updated section 10 "I^2C Firmware Upgrade" to correspond to single byte writes
0.80	20 Aug 2012	• SMB BACKUP is now always enabled • Updated ENBKUP table and removed unused rows • Added EESEL to allow access to both NVDIMM EEPROM and PGEM EEPROM and updated the description for accessing EEPROM data • Added error bit to EEBUSY register • Removed programmable CAP measurement delay, fixed at 1/week, but host can command a measurement at any time • Removed PWRCTL and PWRSTAT registers to simplify FW • Added a description for PGEM EEPROM and updated both EEPROM tables • Numerous typo and formatting corrections
0.72	31 July 2012	• Grayed out features not available in current firmware • Added x4 SMB resisters to restore the REGISTER IC RCx values in addition to the Mode Registers if that feature is enabled • Removed bit 2 from CMSTAT register since it's not an NV register • Fixed type in section 6.11, "RELEASENF=0x3F" should be "0x37"

0.71	14 June 2012	• ***Interim review.*** • Added Section 2.4 definition ("BIOS/OS Controlled BACKUP and RESTORE") and made other edits to generalize CORONADO operation. Mentioned that spec focuses on Romley-based systems that use BIOS-controlled B/R. • Incorporated numerous edits by Tom. • Added a footnote to BACKUP enable conditions table to mention *when* CORONADO makes the CKE=0 test after detecting pin 167 assertion.
0.7	8 June 2012	• Rewrote to document single-buffered operation only. Noted that any double-buffered CORONADO will list differences from this spec in its data sheet. • Rewrote to describe motherboard usage, defining and highlighting the role of the motherboard BIOS in power-up sequence • Replaced previous flowcharts with the single new Figure 2 flowchart. • Eliminated GTG2 bit 2 (NF Erased Within Max Allowed Time) and flowchart steps involved with NF erase timeout. • Rearranged a few GTG bits. • Mentioned that plugging in a PowerGEM causes authentication. • Changed authentication trigger from pre-RESTORE to pre-BACKUP. Added clarifying note that we unconditionally try an enabled BACKUP, but if PGEM is not authentic the BACKUP will fail. Removed authentication check bit from Table 3 (Restore Results). • GTG2 bit 4: added statement that if BACKUP fails due to hardware-indicated authentication failure, CORONADO takes no BACKUP steps such as erasing NF blocks. • Removed reference to electrical signal names. • Added statement that if PGEM authentication fails at power-on, we do not turn on the charger. • Repaired Figs 13 and 14. • Removed references to deleted sections in 0.5 version notes. • Moved R0 to R9 and changed byte value to 0xA5 to make it Catalina compatible.
0.6	14 May 2012	• Added explanation of NF single and double buffering in Terminology section. • Clarified "Single Buffer Note" on page 19 to indicate the flowchart difference for single-buffered CORONADOS. • Clarified BACKUP Section 3.2 to add three basic BACKUP rules and to clarify backup sequence. • Clarified statement: "If a NF image is invalid, CORONADO will ignore RESTORE commands until a new successful BACKUP is performed."
0.5	26 April 2012	• Changed BACKUP behavior when GTG=0: Always try the BACKUP regardless of GTG state. • Removed the Interface Signal Table 1 because all signals but one are registers, not interface signals. • Removed remaining question in 0.4; we have implemented this feature. • Added an optional Authentication indication in the GTG factors. • Eliminated Auto-RESTORE feature. • Added authentication information. • Added note to Table 1 that Manufacturing and Debug registers must be removed from this spec for any customer documentation. • Add clarification to Section 6.7 that BACKUP enable comprises the OR of the two possible trigger sources, ANDED with the CKE qualified.
0.4	16 April 2012	• Fixed typos and renumbered several registers as suggested. • One remaining question regarding host trying to write a read-only register (page 40). This spec version states we NACK. If this is not possible, we will replace this with a statement that we ignore writes to read-only registers.

0.3	22 March 2012	• Major rewrite of registers and EEPROM contents. Removed NV registers, moved to EEPROM access. Removed all EEPROM “Data Sheet” entries. Rewrote several sections. • Added EEBUSY register for EEPROM accesses. All I2C accesses now should easily be performed within 25 msec. • Added BUSCHECK register to indicate I2C unit readiness after power-on. • Removed the “reminder” sections on security and partial BACKUPS.
0.2	5 Jan 2012	• Removed bit 0 from BAKRSLT register (Table 6), changed init values of all bits to 0, rewrite section 7.10 to reflect that bit 0 is no longer necessary.
	9 Nov 2011	• Added SMB General Call for simultaneous BACKUP triggers to multiple NVDIMMS using a single SMB transfer. Added GENCALL register to enable or disable this feature. • Changed BAKRSLT section to speculatively set the BACKUP result bits 0 and 2 to the “fail” condition when the BACKUP is enabled (instead of when the BACKUP actually starts). This gives the Coronado HW more time to initialize and store these NV status bits. • Fixed typos.
0.1	25 Oct 2011	Initial Release - LTH

1 Introduction

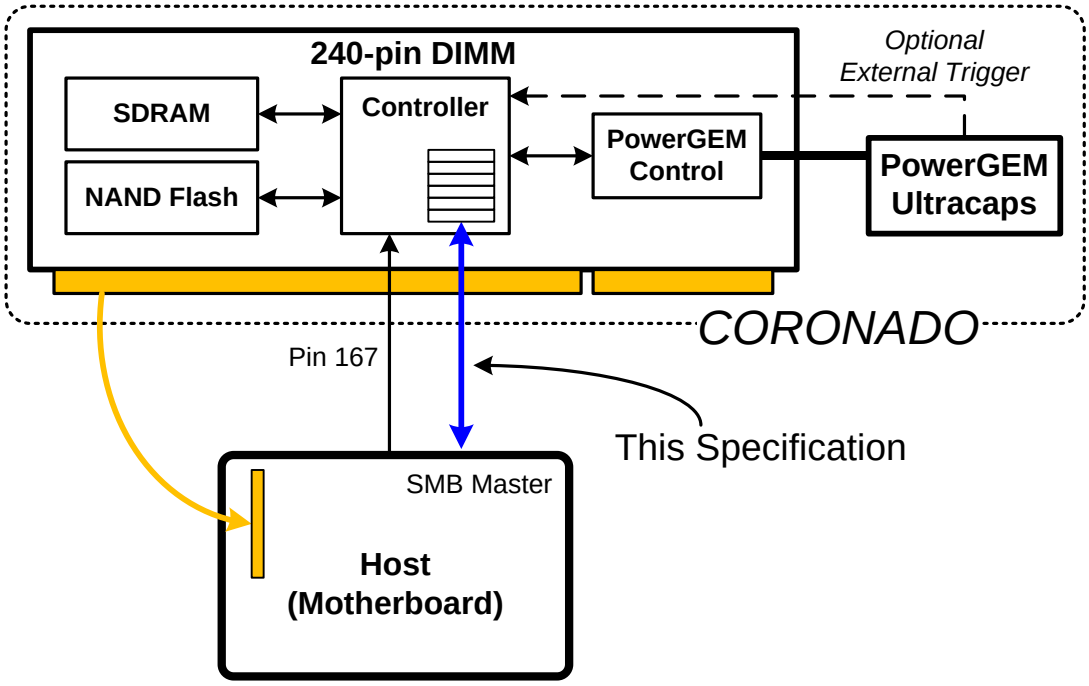

Figure 1. CORONADO Simplified Block Diagram.

CORONADO is a non-volatile Registered DDR3 SDRAM on a standard 240-pin DIMM (Dual Inline Memory Module). It achieves non-volatility by copying SDRAM contents into a non-volatile NAND Flash (NF) memory when host power fails. Because host power is not available for the memory transfer, CORONADO powers the DIMM using a local power supply called a PowerGEM (Figure 1). The PowerGEM uses quick-charging, maintenance-free Ultracapacitors to provide the backup power. When host power returns the CORONADO controller copies the NF data back into SDRAM and returns SDRAM control to the host system.

The host controls CORONADO by accessing a set of registers using the standard SMB bus (solid blue arrow in Figure 1). The CORONADO controller uses the SMB signals SCL and SDA on the DIMM gold fingers to implement an SMB slave. CORONADO shares SCL/SDA with the SPD (Serial Presence Detect) EEPROM on the DDR3 DIMM; therefore the Coronado SMB slave uses a different address than the SPD EEPROM. The Coronado SMB interface conforms to the SMB (System Management Bus) Specification version 2.0.

2 Terminology

2.1 CORONADO

A non-volatile DDR3 Registered SDRAM. CORONADO is a system collection of SDRAM, NF (NAND Flash) memory, a controller to transfer data between SDRAM and NF, and a PowerGEM power supply based on quick-charging Ultracapacitors. When power fails the controller transfers SDRAM data to NF using PowerGEM power. When system power returns CORONADO transfers the NF data back into the SDRAM. An application program therefore sees the same SDRAM contents as before the power failure, making the SDRAM appear to be non-volatile.

2.2 Host

The system which provides the receptacle for the CORONADO DIMM (Dual Inline Memory Module). In most cases the host is a PC/Server/RAID motherboard. The host communicates with the CORONADO register set using the SMB interface and one of two control pins, DIMM pin 167, or an externally supplied BACKUP trigger signal.

2.3 BIOS

Basic Input/Output System.
Motherboards use a non-volatile memory to execute system startup code. The motherboard CPU executes this code to initialize its hardware prior to loading and launching an operating system.

2.4 BIOS/OS Controlled BACKUP and RESTORE

CORONADO supports two different motherboard architectures.

1. **BIOS-Controlled BACKUP and RESTORE.** In this architecture the motherboard has access to its SDRAM controller only at the BIOS level at power-on. Once the OS launches the memory controller cannot be re-configured. A common architecture of this type is the Intel “Romley” platform. In these systems, BACKUP and RESTORE operations are fully automatic:
    a. Enabled BACKUPS are triggered by host power failure.
    b. RESTORES occur automatically at power-on if the BIOS detects a valid saved SDRAM image.

2. **OS-Controlled BACKUP and RESTORE.** In this architecture the host can access its SDRAM controller at the BIOS and OS levels allowing an implementation that

commands both BACKUPS and RESTORES at the OS (application) level, instead of the BIOS level.

Note: This specification focuses on the BIOS-Controlled (e.g. Romley) architecture.

2.5 SMB

System Management Bus.

Present on PC/server motherboards, the SMB is used to monitor and maintain internal resources. The motherboard accesses the CORONADO register set over the SMB. SMB uses the I^2C signaling protocol at 100 KHz clock rate. CORONADO shares the SMB signals with the Serial Presence Detect (SPD) EEPROM on the DIMM using a non-conflicting I^2C address.

2.6 GTG

Good To Go.

CORONADO provides the GTG indication to inform the host that all conditions are satisfied to perform a BACKUP operation. GTG is available as a single register bit that reflects all the individual conditions. Also, the GTG 1-to-0 transition can be indicated by a DIMM signal (EVENT#, pin 187) for hosts that support the SMB ALERT protocol.

CORONADO will attempt a BACKUP operation regardless of the GTG state when an enabled BACKUP is commanded, but BACKUP success is not assured if GTG=0. At the start of a BACKUP, CORONADO saves non-volatile copies of all the GTG condition bits that contribute to the GTG indication. The host therefore can interrogate the individually preserved pre-BACKUP GTG conditions the next time it is powered.

2.7 BACKUP

The process of CORONADO copying the SDRAM contents into NAND Flash. The host normally commands a BACKUP operation by asserting a DIMM pin (167) or an external trigger signal. CORONADO starts a BACKUP operation only if the host has previously enabled the BACKUP and the BACKUP is triggered. Note that the SMB triggered BACKUP is always enabled. If the CORONADO model includes authentication, the CORONADO controller authenticates the PowerGEM before performing a BACKUP. If inauthentic, the BACKUP operation fails.

2.8 RESTORE

The reverse of a BACKUP operation; CORONADO copies the NF contents back into SDRAM.

2.9 SDRAM

Synchronous Dynamic Random Access Memory
The memory type implemented on the CORONADO RDIMM (Registered Dual-Inline Memory Module with ECC). CORONADO uses DDR3 SDRAMS.

2.10 NAND Flash

Non-volatile memory on the CORONADO DIMM, used to store SDRAM images during a BACKUP operation. Abbreviated as “NF”.

2.11 Self-Refresh

The SDRAM state that guarantees data integrity as the SDRAM is switched between the host and the CORONADO memory controllers. The host must insure that the SDRAMS on the CORONADO DIMM are in their self-refresh state before triggering a BACKUP. In addition, the SDRAM controller on the host must be set to “self-refresh” at the end of a RESTORE operation to make its state compatible with the returned SDRAM state. An indicator of the SDRAM being in self-refresh is the SDRAM CKE (clock enable) signal being low.

2.12 SDRAM Mode Registers

SDRAMS have internal write-only mode registers that configure the SDRAMS prior to operation. When CORONADO starts a RESTORE operation, it overwrites host mode register settings to make them compatible with the CORONADO memory controller. Because SDRAM mode registers are write-only, CORONADO cannot preserve the host mode settings prior to changing them. Therefore, following a RESTORE operation, the host must rewrite its mode register settings to conform to its memory controller.

2.13 Single and Double Buffered CORONADOS

A single-buffered CORONADO has enough NAND flash memory to hold a single SDRAM image, while a double-buffered CORONADO has enough NF to hold two SDRAM images. Most CORONADO systems are single-buffered. This specification is based on single-buffering.

Note: The minor differences from this specification for a double-buffered CORONADO are described in its data sheet.

2.14 Authentication (On some CORONADO Versions)

If the CORONADO version has this feature, the CORONADO controller performs an authentication check on the PowerGEM Ultracap board at power-on, when a PowerGEM is

hot-plugged, or before attempting a BACKUP operation. This check validates the Ultracap board as an authentic AgigA board of the correct model. An enabled BACKUP attempt with an inauthentic PowerGEM will report failure.

3 Overview

CORONADO requires coordination with the host system to perform BACKUP and RESTORE operations. This section introduces the basic interactions, and subsequent chapters describe these operations in detail. This specification focuses on mainstream architectures (e.g. Intel "Romley") that perform the coordination at the BIOS level.

3.1 At Power-On

When power is applied, the BIOS can access CORONADO registers after the data sheet specification t_{HW_RDY} has elapsed. The BIOS may check for a positive READY indication by polling the CORONADO BUSCHECK register. This register reads 0xA5 when the CORONADO I^2C unit is initialized and operational.

If the CORONADO model has the PowerGEM Authentication feature, CORONADO hardware checks its PowerGEM for authenticity at power-on, and the result is available in a GTG status bit. CORONADO hardware also does the authentication check if a PowerGEM is hot-plugged into the CORONADO system or prior to starting a BACKUP operation.

3.2 BACKUP

In planning host software, it is important to understand four basic CORONADO rules of operation:

1. If the host has enabled a BACKUP, CORONADO will attempt a BACKUP operation the next time a BACKUP is triggered. CORONADO will attempt a BACKUP even if GTG=0.
2. If the host has not enabled a BACKUP, CORONADO will not attempt a BACKUP unless the BACKUP is triggered by writing to the SMB BACKUP register which is always enabled.
3. CORONADO disables BACKUPS at power-on and at the beginning of a BACKUP operation, so the host must explicitly enable the next BACKUP.
4. CORONADO always does a "best effort" BACKUP. For example, if CORONADO starts a BACKUP operation and detects that there are insufficient erased NAND flash blocks to hold an SDRAM image, it will first erase the required number of NF blocks. In this situation BACKUP success cannot be guaranteed because the NF erase time added to the BACKUP time may exceed the PowerGEM hold-up time. Following the procedure in Section 4 ("Operational Flowchart") eliminates this possibility and ensures successful

BACKUP operations. In any case, the host may determine detailed BACKUP status when power returns.

The host executes the steps listed below to set up CORONADO to do a BACKUP operation. They are listed in the order of typical occurrence:

1. Host issues RELEASE_NF_IMAGE command. CORONADO starts to erase NAND flash blocks.
2. CORONADO asserts GTG (Good To Go), indicating NF erasure is complete.
3. Host issues the ENABLE_BACKUP command.
4. (Host detects its power is failing).
5. Host puts the SDRAMS into self-refresh.
6. Host triggers the BACKUP.

3.2.1 GTG (Good To Go)

CORONADO constantly checks a list of conditions to insure it can perform a successful BACKUP operation when system power fails. The GTG signal indicates that all of these conditions are satisfied. The host can check individual conditions any time in the GTG1 and GTG2 registers. Bit 7 of the GTG1 resister is the “AND” of the individual condition bits, providing a single GTG indication.

CORONADO will attempt an enabled BACKUP even if GTG=0.

For motherboards that implement the SMB_ALERT#” signal, CORONADO can drive a DIMM signal (pin 187, named “EVENT”) whenever GTG makes a 1-to-0 transition, indicating “just became unready”. The host can enable or disable the EVENT signaling using a non-volatile CORONADO control bit. The default state of this bit is to disable EVENT signaling.

3.2.2 RELEASE_NF_IMAGE

The host issues the RELEASE_NF_IMAGE command over SMB to inform CORONADO that the SDRAM image presently residing in NF is no longer needed, and CORONADO may begin to erase the stale image. This command also clears the error status bits from the last BACKUP operation.

If CORONADO is triggered to perform an enabled BACKUP and sufficient NF memory blocks have not been erased to hold the SDRAM image, CORONADO will erase the required NF blocks before starting the BACKUP. However a successful BACKUP operation is not

guaranteed in this case due to the added NF erasure time. See the flowchart in Figure 2 for the recommended host steps to insure a successful BACKUP.

3.2.3 ENABLE_BACKUP

The host writes an SMB register to enable a BACKUP operation. CORONADO clears this register at power-on, so any BACKUP operation must explicitly be enabled by the host unless it is triggered by the SMB BACKUP register. The host sets ENBKUP (Enable BACKUP) register bits to select one or both of two BACKUP *triggers* (DIMM connector pin 167 or external PGEM signal) and one *qualifier* (CKE=0 or CKE is ignored).

3.2.4 START_BACKUP

All motherboard architectures use pin 167 to initiate a BACKUP operation in hardware. In OS-controlled BACKUP architectures (see Section 2.4) a powered host also may write a BACKUP register with a constant to start a BACKUP operation. The host may then poll this register (if the host is still powered) to determine when the BACKUP completes and the SDRAM is again available to the host.

3.3 After a BACKUP

A BACKUP operation starts when the host has detected that it is losing power and has taken the necessary preliminary steps. When power is regained the host may consult various non-volatile CORONADO status bits to learn the detailed results of the last BACKUP operation. These bits are accessed using an EEPROM access mechanism.

3.4 RESTORE

In a BIOS-controlled architecture, at power-on the BIOS commands a RESTORE operation if it finds CORONADO NF contents to be a valid saved SDRAM image. The SDRAM is unavailable to the host during a RESTORE operation. The host (BIOS) may read the RESTORE register to check for completion of the RESTORE operation.

3.5 After a RESTORE

Similar to post-BACKUP, the host may consult CORONADO register bits to determine the detailed outcome of a RESTORE operation.

4 Operational Flowchart

This section illustrates how a host interacts with the CORONADO system at power-on for a BIOS-Controlled architecture (e.g. Intel Romley).

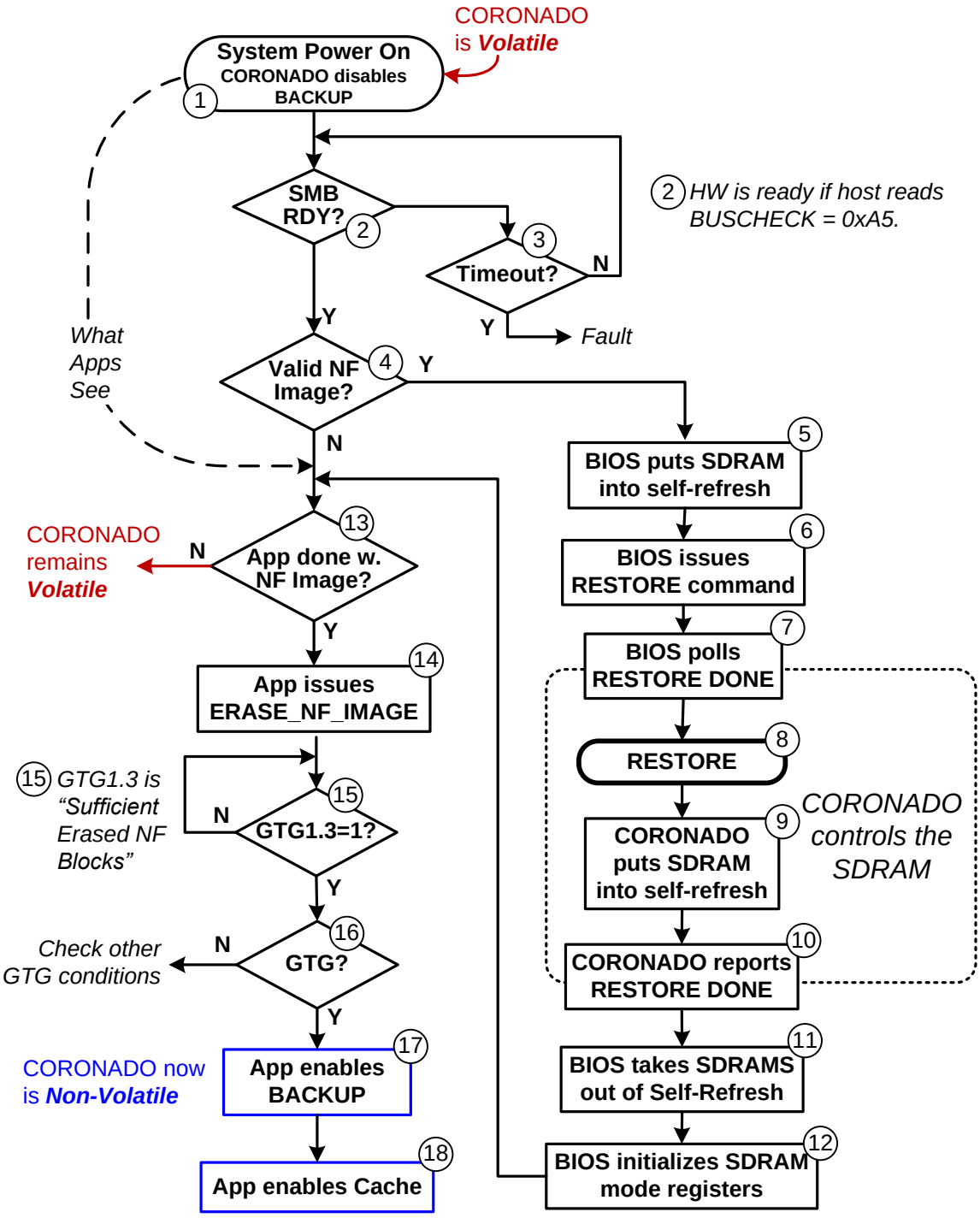

Figure 2. Top-Level Flowchart for CORONADO in a Typical Motherboard.

The motherboard BIOS performs steps ① through ⑫ before the OS loads and application programs begin to run. The dotted arrow from ① to ⑬ indicates what application programs see when they start running, unaware of the BIOS steps taken behind the scenes. In the steps listed below, the term “BIOS” is used to mean the host executing its BIOS code.

4.1 Power-on

At power-on the SDRAM is immediately made available to the host during the time the CORONADO controller initializes its controller and charges its PowerGEM Ultracapacitors. If the CORONADO model includes PowerGEM authentication, CORONADO turns on the charger only if the authentication test passes. If authentication fails CORONADO operates only as a volatile SDRAM.

CORONADO clears the ENBKUP (Enable BACKUP) register at power-on. This prevents an unintentional BACKUP trigger on pin 167 as the system voltages ramp up.

At this stage CORONADO behaves exactly like any volatile SDRAM, uninitialized and with random contents.

Note: In the case that host power returns while a previous BACKUP operation is in progress, the BACKUP continues to completion. In this case CORONADO never lost power due to its local PowerGEM, so it can continue the BACKUP as the host regains power. The host can check a register to determine when the BACKUP finishes. Allowing the BACKUP to complete prevents a partial save that would corrupt NF data.

4.2 BIOS Checks for SMB Communication

The BIOS polls the read-only CORONADO BUSCHECK register to determine SMB slave readiness. When this register returns the value 0xA5 the CORONADO SMB slave is initialized and ready for operation.

4.3 BIOS Tests for SMB Ready Timeout

The CORONADO data sheet parameter T_{HWRDY} specifies the maximum time CORONADO requires to initialize its hardware and make its SMB slave unit available. The BIOS can determine a fault if the readiness test ② exceeds this time.

4.4 BIOS Checks for a Valid NF Image

Once the SMB slave is operational the BIOS can check for a valid SDRAM image in NF, or to see if a BACKUP operation is still in progress (not shown). The valid image check indicates that a previous BACKUP operation has occurred, leaving a NF memory image that can be restored to the SDRAM. If NF contents are valid the BIOS initiates a RESTORE operation by taking the ④ to ⑤ branch.

4.5 BIOS Puts SDRAM into Self-Refresh

The BIOS puts its SDRAM controller into the self-refresh state that allows safe switching between the host and CORONADO controllers.

4.6 BIOS Issues the RESTORE command.

The BIOS commands a RESTORE operation by writing SMB register RESTORE=0x96.

4.7 BIOS Polls for RESTORE DONE

The BIOS polls the RESTORE register to determine when CORONADO completes the RESTORE operation at step ⑩.

4.8 CORONADO does a RESTORE

CORONADO connects its SDRAM controller to the SDRAM, removing SDRAM control from the host. The CORONADO controller then removes the SDRAM from self-refresh, writes new SDRAM mode register values and transfers the NF image into the SDRAM.

4.9 CORONADO Returns the SDRAMS to the Self-Refresh State

The SDRAM contents now are valid, containing the restored NF image. CORONADO puts the SDRAM into the self-refresh state to maintain their contents as the SDRAM is disconnected from the CORONADO controller and re-connected to the host controller.

4.10 CORONADO Reports RESTORE is Done

The BIOS detects the register RESTORE=00, indicating that the RESTORE is complete and the host may re-access the SDRAM.

4.11 BIOS Takes SDRAMS Out Of Self-Refresh

To access the SDRAM, the host controller must be in sync with the SDRAM self-refresh state. This was ensured in step ⑤. The BIOS now takes the SDRAM out of self-refresh in

preparation for host access. The BIOS must ensure that it re-initializes the SDRAM Mode Register settings and enables normal refresh on the host memory controller quickly enough that SDRAM refresh is maintained. Because this step is done in the motherboard BIOS, this timing can be strictly controlled.

4.12 BIOS Initializes SDRAM Mode Registers.

SDRAM contain internal mode registers to set their operating parameters such as CAS Latency and electrical termination settings. These mode registers are write-only, so CORONADO cannot preserve the settings written by the host.

Before a RESTORE operation, CORONADO over-writes the SDRAM mode register values to settings compatible with the CORONADO memory controller. Therefore at step ⑫ the BIOS must re-initialize the SDRAM Mode Register values similar to those used at initialization following power-on but with one important difference. *The host BIOS routine must ensure that its memory controller does not assert the SDRAM RESET# pin, which could result in loss of restored memory contents.*

4.13 (OS Running) App Determines if NF Image No Longer Needed

Steps ① through ⑫ are performed by the motherboard BIOS. At step ⑬ the OS loads and application programs take control. The criteria at step ⑬ ("Done with NF Image?") is up to the application program. A typical scenario should include a validity check of the SDRAM contents using the host's built-in error detection/correction mechanism, followed by safe storage of the SDRAM contents.

If for any reason the host determines that it still needs the SDRAM image held in NF, it exits in ⑬ and CORONADO memory remains volatile *because a new BACKUP is not possible until CORONADO erases the NF memory blocks holding the stale SDRAM image.*

4.14 Host Issues the ERASE_NF_IMAGE Command

Once the host has dealt with the restored SDRAM contents, the host can issue this command to instruct CORONADO to start erasure of the stale SDRAM image.

4.15 Host Waits for NF Erasure

The host polls a specific GTG bit (GTG1.3) to determine when the NF erasure is complete.

4.16 Host Checks All Good To Go Bits

The host checks the main GTG bit (GTG1.7), and if low, the host checks the individual GTG bits to determine why CORONADO may not be ready to perform a BACKUP.

Note: The two dominant GTG factors are NF erasure and PowerGEM charge state. Since the host commands RESTORE operations while powered, it is almost certain that the PowerGEM Ultracapacitors have had sufficient time to charge by the time the host makes this check. Therefore the usual branch in ⑯ will be "Y" (GTG=1), indicating that CORONADO is ready to perform a BACKUP.

4.17 Host Enables a BACKUP

The host enables a BACKUP operation by writing the BACKUP register with a value indicating the trigger source and an optional clock qualifier.

4.18 Host Regards CORONADO as Non-Volatile

CORONADO is now armed to save the SDRAM contents if host system power fails. The host may at this point consider CORONADO non-volatile. A typical host action at this point would be to use CORONADO as a disk cache memory.

4.19 Power Loss During RESTORE

RESTORE operations are done while the host is powered. If the host should lose power during a RESTORE operation, the CORONADO hardware abandons the RESTORE operation. At the next power-on, the host (BIOS) can initiate another RESTORE operation because it has not yet released the SDRAM image in NF (step ⑭).

4.20 Power Fail

When power fails the host must take specific actions to insure a smooth SDRAM handoff to the CORONADO hardware. The host must do any necessary housekeeping such as flushing CPU caches, and then it must put the CORONADO SDRAM into self-refresh. Finally, the host triggers the BACKUP and if enabled, CORONADO starts the BACKUP operation. The BACKUP trigger can occur either by a CORONADO pin (recommended because quick response is critical) or an SMB register (OS-Controlled BACKUP/RESTORE). Note that an SMB register commanded BACKUP is always enabled. At the next power-on the host can determine the status of the last BACKUP by reading EEPROM status bytes.

4.21 Triggering a BACKUP

The host normally asserts DIMM pin 167 to start a BACKUP operation. If the BACKUP is enabled when this pin is asserted, CORONADO starts the BACKUP operation. Once a BACKUP operation starts it continues to completion, regardless of the state of the input power. CORONADO automatically clears the ENABLE_BACKUP bit at the beginning of a BACKUP operation to insure that another BACKUP operation cannot occur unless explicitly enabled by the host. This prevents a new BACKUP operation from overwriting a valid image if, due to power fluctuations as the host regains power, the host cannot reliably drive the trigger signal.

4.22 After a BACKUP

The host can enable a BACKUP operation at any time. If the BACKUP is requested due to a power failure, at the next power-on the host can check the status of the last commanded BACKUP to determine if it was successful using EEPROM data.

5 CORONADO Register Set

Table 1 summarizes the CORONADO register set. The “Reg” column indicates the Register name. The “Acc” column indicates the register access type by the host, R=Read-only, W=Write-only, RW=Read or Write. The “Parameter” column shows the register data written for a write-byte operation or returned for a read byte operation.

All registers in Table 1 are volatile. To access CORONADO non-volatile information such as the results of the last BACKUP operation or temperature/capacitance histories, the host accesses an EEPROM using the four registers EEBUSY, EEADDRL, EEADDRH, and EEDATA.

Table 1. CORONADO Register Set.

Reg	Name	Acc	Parameter	Description
				DIMM Information
0x01	EEBUSY	R	N/A	Poll before EEPROM access. 0x01=busy, 0x00=ready
0x02	EEADDRL	RW	EEPROM Address Pointer L	0x00 – 0xFF
0x03	EEADDRH	RW	EEPROM Address Pointer H	0x00 – 0x03
0x04	EEDATA	RW	EEPROM Data	Read/Write EEPROM
0x05	EESEL	RW	EEPROM Selector	0 = NVDIMM EEPROM, 1 = PGEM EEPROM
				Actions
0x08	ENBKUP	RW	Disable: 0x00 Enable: Various Bytes	Enable or disable BACKUP. CORONADO clears at power-on or when BACKUP starts. See Table 2 for various ways to enable a BACKUP.
0x09	BUSCHECK	R	N/A	Reads 0xA5 when I^2C slave is operational.
0x0A	BACKUP	RW	0x2E = Start BACKUP 0x00 = Cancel Backup	Start BACKUP. Starts BACKUP if enabled in ENBKUP register. Reads 0x2E while BACKUP is in progress, 0x00 when done. Writing 0x00 cancels a BACKUP regardless of how it was initiated.
0x14	BAKRSLT1	R	N/A	BACKUP Results. Results of the last BACKUP operation. Detailed factors are shown in Table 7. BAKRSLT1 Bits.
0x0B	RESTORE	RW	0x96=START_RESTORE 0x00 = Cancel Restore	Start Restore. Reads 0x96 while RESTORE is in progress, 0x00 when done. Cancel operation operates regardless of how the RESTORE was initiated.
0x15	RSTRESLT	R	N/A	RESTORE Results. Results of the last RESTORE operation. Detailed conditions are shown in Table 3.
0x0C	RELEASENF	RW	0x37	Write 0x37 to Release NAND Flash Image (start erasure)
0x06	CAPMEAS	RW		Bit 0: Start Measurement, Bit 1: Clear measurement timer. See EEPROM byte “MCAPINT” to set automatic measurement interval.
0x07	CMSTAT	R	N/A	Capacitance Measurement Status.
				System Status
0x12	GTG1	R	N/A	GTG1. Good To Go Status (1 of 2) as shown in Table . Bit 7=1 if all conditions are right to perform a BACKUP operation. If bit 7=0, check bits 6-0 and GTG2 register for cause.
0x13	GTG2	R	N/A	GTG2. Good To Go Status (2 of 2) as shown in Table . Check this register if GTG1.7=0.
				Power
0x0F	VCAP	R	N/A	Current PGEM Cap Stack Voltage (100mV)
				SDRAM Mode Register Restore Values

Reg	Name	Acc	Parameter	Description
0x1B	MRL	RW	N/A	SDRAM Mode Register MRL
0x1C	MRH	RW	N/A	SDRAM Mode Register MRH
0x1D	EMR1L	RW	N/A	SDRAM Mode Register EMR1L
0x1E	EMR1H	RW	N/A	SDRAM Mode Register EMR1H
0x1F	EMR2L	RW	N/A	SDRAM Mode Register EMR2L
0x20	EMR2H	RW	N/A	SDRAM Mode Register EMR2H
0x21	EMR3L	RW	N/A	SDRAM Mode Register EMR3L
0x22	EMR3H	RW	N/A	SDRAM Mode Register EMR3H
0x23	MDRDVALID	RW	Host sets this register to 0x01 after writing MRH-EMR3H with valid values.	CORONADO controller checks this register when a BACKUP or RESTORE operation completes. If 0x01, CORONADO writes mode register settings R57-R64 to SDRAM before setting SDRAM_RDY=1.
0x24	MRWRSTAT	R	N/A	SDRAM Mode Register Write Status. 0x00=idle, 0x01=SDRAM mode register writes in progress.
0x30	RC0_3	RW	N/A	Register chip Control word 0 - Control word 3
0x31	RC4_7	RW	N/A	Register chip Control word 4 - Control word 7
0x32	RC8_11	RW	N/A	Register chip Control word 8 - Control word 11
0x33	RC12_15	RW	N/A	Register chip Control word 12 - Control word 15
				Miscellaneous
0x10	LEDS	RW	0x00=OFF, 0x01=ON	Amber LED on DIMM
0x11	AUXEEADDR	R	0x00-0x07	*Optional: AUX EEPROM address bits A[2:0].*
0x1A	Reset System	W	0x45	Reset system
				Firmware Update
0x25	STDLD	W	0X67=START	The host writes STDLD =0x67 to start a firmware update (download). Once started, a firmware upgrade should not be interrupted.
0x26	SDD	W	Upgrading data	The host downloads firmware update data by repeatedly writing SDD with 66-byte packets.
0x27	DLDSTAT	R	N/A	Status register for download process

6 Detailed Register Descriptions

6.1 BUSCHECK

CORONADO uses an FPGA which requires initialization time at power-on. The host (BIOS) may determine when the FPGA is initialized and its I^2C slave is operational by reading this register. Only after BUSCHECK returns the value 0xA5 is the FPGA ready for operation.

6.2 EEBUSY

The EEBUSY register must be checked when accessing the EEPROM. During a read the process is, write the ADDRH then ADDRL, wait for EEBUSY = 0, then read EEDATA. For a write to EEPROM the process is write the ADDRH, ADDRL, and EEDATA, then wait for EEBUSY = 0 to verify the write is complete before proceeding. If EEBUSY=1 for more than 30ms, there is an error in the FPGA or EEPROM and the host should issue a RESET command and try again.

Bit 0: EEBUSY

The host must poll the EEBUSY register when accessing the EEPROM. EEBUSY=1 indicates *busy*. When EEBUSY=0 the host may read or write the EEDATA register as described above.

Bit 1: EEERROR

The EEERROR bit is set if there is a failure of the EEPROM IC to respond to an attempted access. For example, EEBUSY = 0 and EEERROR = 1 indicates the EERPOM IC has failed and did not acknowledge the attempted access. EEBUSY = 1 and EEERROR = 1 indicates the EEPROM access timed out.

6.3 EEADDRH

6.4 EEADDRL

6.5 EEDATA

EEPROM Memory Address H/L, Data

These three registers control access to 1 Kilobyte of nonvolatile (NV) CORONADO data and to 1 Kilobyte of NV PGEM data. To read this NV data the host first writes a low address EEADDRL (0x00-0xFF) and then a high address EEADDRH (0x00-0x03). The host then polls the EEBUSY register for it to read back as 0x00 indicating it is not busy. The host then writes the EEPROM data using the EEDATA register. For a write, the host writes to EEADDRL, then EEADDRH, and finally EEDATA. The host then polls for EEBUSY = 0 before doing another

transaction. The host uses the EESEL register to indicate which of the two EEPROM spaces will be accessed as described below.

The NVDIMM EEPROM data space is divided into two halves. The first 512 bytes (addresses 0x0000-0x01FF) comprise uncommitted read-write locations, usable by the host for any purpose. The rest of the address space comprises CORONADO specific data. Aside from a few read-write locations that contain persistent mode values set by the host, most of this region is read-only information.

6.6 EESEL

Bit 0: Select EEPROM

This bit is set to 0 (default) when accessing NVDIMM EEPROM and to 1 when accessing the PGEM EEPROM. EEADRH, EEADRL, and EEDATA are used to access both the NVDIMM EEPROM registers and the PGEM EEPROM based on the value of this bit.

6.7 ENBKUP

Enable BACKUP

The host can enable or disables a BACKUP operation by writing this register. The host may enable a BACKUP operation using one of two trigger sources, the DIMM connector pin 167 or an external trigger connected to the PowerGEM. In addition, the host may specify if and how the SDRAM CKE signal qualifies the BACKUP enable as shown in Table 2. A table entry should be interpreted as the OR of the two BACKUP signals, ANDed with CKE. Note that CKE is active low for the purposes of indicating a BACKUP is qualified.

For example, for ENBKUP = 0xFB, either of the External Signals may initiate a BACKUP, but only if CKE=0. A value of “yes” means the signal is used to determine if a BACKUP should start or not, while “no” means the signal is not used.

About The I2C BACKUP Command

The I2C BACKUP Command does not need to be enabled by writing to the Enable BACKUP register. The I2C BACKUP command is always enabled.

Table 2. Various Ways to Enable a BACKUP.

ENBKUP Value	Action	Pin 167	EXT PGEM Trigger	CKE
0x00	Disable BACKUPS	no	no	no
0xEB	Enable BACKUP	yes	no	no

0x18	Enable BACKUP	yes	no	yes[1]
0x04	Enable BACKUP	no	yes	no
0x53	Enable BACKUP	no	yes	yes[1]
0xBF	Enable BACKUP	no	no	yes[2]

[1]This table shows conditions but not data sheet timing.

[2]Note, in the other two cases with CKE = yes, CKE is used to qualify a BACKUP, the trigger signal AND CKE must be active, but in this case CKE is used as the triggering signal.

In the two cases where CKE is used as an additional qualifier to Pin 167 or EXT PGEM Trigger (0x18 and 0x53), there is an additional timing parameter that must be considered. t_{CKE_LOW} is defined as the time from when the BACKUP trigger is asserted (either on Pin 167 or the EXT PGEM Trigger) to when the DRAM is placed into self-refresh, as indicated by CKE going low. If CKE is not asserted low within t_{CKE_LOW}, the firmware assumes BAKCKUP trigger was not intended and aborts the SAVE. The BACKUP is still enabled for a future event trigger. t_{CKE_LOW} is defined in the CORONADO Datasheet.

Note: It is critical that the DRAM is placed into self-refresh by the host prior to the host losing power regardless of the value of t_{CKE_LOW}. This must be guaranteed by the system or data will be lost during a BACKUP attempt.

The host disables BACKUPS by writing 0x00. CORONADO hardware clears this register to disable the next BACKUP in two circumstances:

1. A BACKUP operation starts
2. Power-on

6.8 BACKUP

Start or Cancel a BACKUP

The host writes BACKUP=0x2E to have the same effect as host hardware asserting the trigger signal. If the External Signal pin is enabled but not used for this purpose, it must be tied to its inactive state. A powered host may check BACKUP status by reading this register:

- BACKUP=0x2E means the BACKUP operation is still in progress
- BACKUP=0x00 means the BACKUP operation has finished, either normally or by the host terminated the BACKUP operation.

The host writes the BACKUP register 0x00 to cancel a BACKUP. This returns the SDRAM to the host and indicates that the host cancelled the BACKUP in the BAKRSLT (BACKUP Result)

register. Canceling a BACKUP does not clear the ENBKUP register—any enabled BACKUP triggers remain enabled. An incomplete BACKUP indicates an invalid NF image, which the host should erase by releasing the NF image (RELEASENF register). Canceling a BACKUP can take up to 1 second to finish.

6.9 BAKRSLT1

Result of the last BACKUP

See the BAKRSLT1 section in the EEPROM chapter for the contents of this register.

CORONADO saves all non-volatile status information, including BACKRSLT1, in its EEPROM. For compatibility with a previous version, CORONADO updates this register (and only this register) with the EEPROM BAKRSLT1 byte at power-on. CORONADO asserts BUSCHECK=0xA5 only after updating this register with the corresponding EEPROM byte. Note that there is a second BACKUP Result byte, BAKRSLT2, in the CORONADO EEPROM.

6.10 RESTORE

Start or Cancel a RESTORE Operation

The host (BIOS) writes RESTORE=0x96 to start a RESTORE operation. CORONADO logic sets RESTORE=0x00 when the RESTORE operation completes. The host can also write RESTORE=0x00 to cancel a RESTORE operation. This returns the SDRAM to the host and indicates the host cancellation in the RSTRESLT register. Canceling a RESTORE can take up to 1 second to finish.

The host may check RESTORE status by reading this register:

- RESTORE=0x96 means the RESTORE operation is still in progress
- RESTORE=0x00 means the RESTORE operation has finished, either normally or if the host terminated the RESTORE operation by writing RESTORE=0x00.

6.11 RSTRESLT

Results of a RESTORE operation

Following a RESTORE operation, the host can determine the success of the operation by reading this register. CORONADO clears these bits at power-on or at the beginning of a RESTORE operation.

Table 3. RESTORE Results.

Bit	Status	Notes

7	Restore SDRAM fault	SDRAM Initialization Fault
6	Invalid RESTORE	RESTORE performed with invalid NF image (BAKRSLT1.1 =0)
5	Reserved, reads 0	Reserved, reads 0.
4	Possible RESTORE fault (see text)	RESTORE started with CKE=1
3	Cancelled RESTORE	RESTORE was cancelled by host
2	Incomplete RESTORE	RESTORE operation did not complete
1	RESTORE NF Read Error	Uncorrectable NF read error during RESTORE
0	RESTORE Succeeded	SDRAM contents are valid.

Bit 0: RESTORE Succeeded

CORONADO sets this bit to indicate the last RESTORE operation was successful and the SDRAM now holds the previously saved SDRAM image. CORONADO clears this bit if any of the bits 1-7 equal 1 indicating a fault.

Bit 1: RESTORE NF Read Error

CORONADO sets this bit in the unlikely event that the CORONADO hardware encountered a read error from the NF during a RESTORE, and was unable to correct the error using its built-in error detection/correction system. In this case a portion of the SDRAM is invalid.

Bit 2: Incomplete RESTORE

CORONADO sets this bit to indicate that a RESTORE operation started but did not complete. This could be caused by a power loss during the RESTORE or by the host cancelling a RESTORE operation. Since the NF contents do not change until explicitly released by the host, a simple corrective host action would be to command another RESTORE and check results.

Bit 3: Cancelled RESTORE

CORONADO sets this bit to indicate that the host canceled a RESTORE operation. This does not alter the NF content, but it does leave the SDRAM with partially restored data.

Bit 4: Possible RESTORE Fault

CORONADO sets this bit to indicate that a RESTORE was requested while CKE=1. This opens the possibility that when CORONADO handed SDRAM control back to the host, the host SDRAM controller was in an operational state that could corrupt the restored SDRAM data.

A remedy would be for the host to put its SDRAM controller into the required self-refresh state (CKE=0) and then command another RESTORE operation

Bits 5 is reserved and reads 0.

Bit 6: Invalid RESTORE
CORONADO sets this bit to indicate that a RESTORE operation was performed with an invalid NF image, as indicated by the BAKRSLT1 register bit 1 = 0). This may be useful for debug purposes.

Bit 7: RESTORE Initialization Fault
CORONADO sets this bit to indicate an SDRAM initialization error by the CORONADO controller.

6.12 RELEASENF

Release NAND Flash Image
The host writes this register with 0x37 to release the last SDRAM image saved in NAND flash. This tells the CORONADO hardware that it may begin to erase the stale image. While erasure is in progress, the register RELEASENF=0x37. When erasure of enough NF blocks to hold the next SDRAM image is complete CORONADO sets RELEASENF=0 and GTG1.3=1 (Sufficient Erased NF Blocks).

6.13 CAPMEAS

Capacitance Measurement
This register controls when CORONADO measures the capacitance of its Ultracapacitor stack. The capacitance is measured automatically once per week (every 7 days). The host may also use the CAPMEAS register to command an instantaneous capacitance measurement, after which the internal measurement timer can be cleared or left running.

Bit[7:2] **Reserved, read 0**

Bit 1: **Clear Timer After Measurement**
The host sets this bit to reset the internal measurement timer after completing an instantaneous capacitance measurement as commanded by bit 0. For example, if the host wishes to do a measurement every day instead of once per week, it can command a measurement using bit 0 of this register and set this bit to reset the timer each day so it doesn't do an extra measurement every seventh day.

Bit 0: **Start a Capacitance Measurement**

Initiate a capacitance measurement now. At the conclusion of the measurement CORONADO consults bit 1 and either clears its automatic measurement timer or leaves it alone.

When the measurement is complete CORONADO updates the percentage capacitance value in the LASTCAP (Last Capacitance Measurement result) EEPROM byte, updates the appropriate capacitance bin in the capacitance history, and clears the CAP_MEAS bit in the CMSTAT register. Note that the appropriate capacitance bin in the capacitance history table should be incremented even if the host has commanded a capacitance measurement. The host must be aware of the time interval if it commands a measurement more frequently than once per week.

If a capacitance measurement is underway when power fails, CORONADO immediately stops the measurement and checks for an enabled BACKUP operation. No capacitance values are updated in this case. CORONADO clears its internal measurement timer when power returns after a power failure, which restarts the automatic measurement interval.

6.14 CMSTAT

Capacitance Measurement Status

The host reads this register to determine capacitor measurement status, as shown in Table 4.

Table 4. Capacitance Status.

Bit	Status	Detail
7	CAP_MEAS	Capacitance measurement is in progress
6	0	Reserved: set to 0
5	0	Reserved: set to 0
4	0	Reserved: set to 0
3	Measurement Fault	Measurement not possible
2	0	Reserved: set to 0
1	0	Reserved: set to 0
0	0	Reserved: set to 0

Bit 7: Capacitance measurement is in progress.

Bits 4-6: Reserved, read 0.

Bit 3: Measurement fault.

CORONADO sets this bit if its capacitance measurement algorithm encounters a problem. In this case, CORONADO updates the percentage capacitance value to 0% in the LASTCAP

(Last Capacitance Measurement result) EEPROM byte, and GTG1 bit 6 (PCT Capacitance Value OK) will be cleared which will immediately drop GTG.

Bit 0-2: Reserved, read 0.

6.15 GTG1

6.16 GTG2

Good To Go #1 and #2

The GTG register bits indicate all the conditions than must be satisfied for the CORONADO system to perform a BACKUP operation. GTG1.7 is the overall GTG bit. GTG=1 only if all non-reserved bits in GTG1 and GTG2 are 1.

The host can poll these registers at any time to determine BACKUP readiness. In addition, if the host writes the register ALERTEN = 0x01, any 1-0 transition of the GTG bit (GTG1.7) asserts the SMB ALERT pin on the DIMM connector.

Table 5. GTG1 and GTG2 Registers.

Bit	GTG1	Bit	GTG2
7	GTG: GTG1=0x7F **AND** GTG2=0x3F	7	Reserved, reads as 0
6	PCT Capacitance Value OK	6	Reserved, reads as 0
5	SDRAM_RDY	5	PGEM Power Present
4	System Initialized Properly	4	VCAP Error
3	Sufficient Erased NF Blocks	3	PowerGEM passed authentication*
2	NF Reserve Pool > 0%	2	Valid PowerGEM Configuration
1	Ultracaps Are Connected	1	Valid FPGA Image
0	Ultracaps Fully Charged	0	Valid FPGA Code

* Not all CORONADO versions.

GTG1 bit 0: Ultracaps Fully Charged

The PowerGEM Ultracaps have charged to the data sheet charge voltage, insuring enough energy to perform a BACKUP operation.

GTG1 bit 1: Ultracaps Are Connected

The Ultracapacitor board is connected to the DIMM.

GTG1 bit 2: NF Reserve Pool > 0%

There are enough reserve NF blocks to guarantee proper operation. This is a very unlikely event, since it would indicate an usual number of NF errors over the product lifetime.

GTG1 bit 3: Sufficient Erased NF Blocks
Sufficient erased NAND Flash memory blocks are available to perform a BACKUP operation.

GTG1 bit 4: System Initialized Properly
No problems were encountered as the CORONADO system powered up and initialized.

GTG1 bit 5: SDRAM_RDY
The SDRAM is connected to the host. This insures that the host can take the mandatory step of putting the SDRAMS into self-refresh before triggering a BACKUP operation.

GTG1 bit 6: PCT Capacitance Value OK
The last capacitance measurement gave a value in the CAPPCT register that insures adequate power delivery for the next BACKUP.

GTG1 bit 7: GTG
Single GTG bit. High only if all defined bits in the GTG1 and GTG2 register are high.

GTG2 bit 0: Valid FPGA Code
The last FPGA update (if applicable) is valid. The upgrade procedure checks this bit after performing an update. If an update fails, CORONADO reverts to its boot loader code and clears this bit.

GTG2 bit 1: Valid FPGA Image
The last FPGA MCU code update (if applicable) is valid. The upgrade procedure checks this bit after performing an update. If an update fails, CORONADO reverts to its boot loader code and clears this bit.

GTG2 bit 2: Valid PowerGEM Configuration
This bit indicates the PowerGEM is a configuration supported by CORONADO.

GTG2 bit 3: PowerGEM Passed Authentication
CORONADO models that implement Authentication check the validity of the PowerGEM UltraCap board at power-on, after a PowerGEM hot-plug, and before every BACKUP operation. This bit is set if the UltraCap board is authentic. *CORONADO versions without authentication permanently set this bit to 1.*

CORONADO hardware makes authentication its highest priority. If a BACKUP fails due to an inauthentic PowerGEM the CORONADO hardware does not perform any BACKUP steps, such as erasing NF blocks.

GTG2 bit 4: VCAP Error
This bit indicates the UltraCap voltage has suddenly dropped below a usable value while GTG is high and the system is armed for a BACKUP. If this bit is triggered by the conditions listed

below, it will stick at 0 indicating an error condition until after the system has been power cycled or after a BACKUP operation. This condition could be caused by several events including opening the PowerGEM resettable fuse, illegal hotplug of a non-charged PowerGEM, or physical damage to the system during operation.

CORONADO sets VCAP Error=0 when all of the following conditions are satisfied:

1. GTG=1
2. 12V power is present (see GTG2 bit 5)
3. The host has enabled a SAVE operation
4. The PowerGEM fuse opens for 100 milliseconds or more before resetting

CORONADO sets VCAP Error=1 at power-on or at the start of a BACKUP operation.

Note: This bit is only valid for PowerGEMs that have an onboard charger, not for systems that use the CORONADO onboard charger. In that case this bit will always be 1.

GTG2 bit 5: PGEM Power Present
This bit indicates that the CORONADO PowerGEM is connected and is supplied by external power (typically 12V). This bit is updated at system power on and once every 10 seconds.

Note: This bit is only valid for PowerGEMs that have an onboard charger, not for systems that use the CORONADO onboard charger. In that case this bit will always be 1 after the Ultracaps are fully charged.

GTG2 bits 4-7: Reserved, set to 0.

6.17 VCAP

VCAP reports the total voltage on the Ultracap stack in 100mV units. This register is updated every 15 seconds except during capacitance measurement.

6.18 MRL

6.19 MRH

6.20 EMR1L

6.21 EMR1H

6.22 EMR2L

6.23 EMR2H

6.24 EMR3L

6.25 EMR3H

SDRAM Mode Register Settings

When CORONADO takes control of the SDRAM at the start of a BACKUP or RESTORE operation, it first writes the mode registers internal to the SDRAM with values compatible with CORONADO's SDRAM controller. *This over-writes the mode register settings written by the host.* Because mode registers inside the SDRAM are write-only, CORONADO cannot read their content and save it prior to over-writing it. For a BACKUP operation this does not matter, because the unpowered host has no means to access the SDRAM until the next power-on.

RESTORE operations are a different matter. The host performs RESTORE operations while powered, and the host expects to access the SDRAM following a RESTORE. But the SDRAM mode register settings during the RESTORE are compatible with the CORONADO controller, not the host SDRAM controller. Before accessing the SDRAM, the host must restore its the SDRAM mode register settings to be compatible with its own memory controller.

How the host rewrites the SDRAM mode registers depends on the system implementation:

- If the host can calibrate its SDRAM at any time (not just at power-on), it can simply command another SDRAM calibration following the RESTORE. The host memory controller would conclude this calibration by writing the host-compatible SDRAM mode register settings. Care should be given to insure that the host (re)calibration does not disrupt the SDRAM contents (for example the SDRAM should not be reset, which would defeat self-refresh) since the SDRAM contain valid restored data from the last power outage.

- In some systems the host cannot command an SDRAM calibration at will, because this operation is performed in the BIOS (or more specifically, the MRC, Memory Reference Code inside the BIOS) and cannot be called after the system boots. In this case the

host must supply mode register restore values in the eight MR-EMR registers. At the end of a RESTORE operation CORONADO checks for the validity of these registers (next register) and if these register contents are valid, CORONADO writes their values into the SDRAMS before releasing them back to the host.

These eight registers are cleared at power-on.

6.26 MDRDVALID

Mode Register Data is Valid

After the host writes the above eight mode registers, it writes 0x01 to this register to signal CORONADO that the register settings are valid. CORONADO checks this register after completing a RESTORE operation, and if 0x01 it copies the eight mode register settings into the SDRAMS. Finally, CORONADO puts the SDRAMS into self-refresh and sets the register RESTORE=0 to indicate the RESTORE is complete and the host had control of the SDRAMS.

This register is cleared at power-on.

6.27 MRWRSTAT

Mode Register Write Status

The host can verify that the mode register settings it provided are being copied into the SDRAMS by monitoring this register. While MRSTAT=1, CORONADO is in the process of copying its eight mode register values to the SDRAMS. MRSTAT returns to 0 when the operation is complete.

6.28 RC0_3

6.29 RC4_7

6.30 RC8_11

6.31 RC12_15

Register IC RCx Values

The Register IC Control words are also restored to the Register IC after a RESTORE operation if MDRDVALID is set to 0x01.

6.32 LEDS

CORONADO DIMM Amber LED

The CORONADO DIMM has three LEDS. Two LEDS are controlled by CORONADO hardware, and the AMBER LED is controlled by the host for any purpose. The host writes 0x01

to this register to turn the amber LED ON, and 0x00 to turn the amber LED off. Reading this register returns the state of the output register, not the buffered LED driver output.

Consult the CORONADO data sheet for the meaning of the other two LEDS.

6.33 AUXEEADDR

Auxilliary EEPROM Address Bits
This is an optional feature, not present on all CORONADO designs. Consult your data sheet to determine if this feature is present.

Some CORONADO systems use an auxiliary EEPROM on the PowerGEM (distinct from the CORONADO EEPROM) for various purposes. In these systems it may be advantageous to determine the pin-defined EEPROM address bits A2 A1 and A0, for example to determine a slot number into which a board is plugged. CORONADO supplies these three address bits if the feature is implemented. Otherwise the contents of this register are undefined.

6.34 RESET

This command resets the CORONADO FPGA causing it to reload the FPGA fabric and firmware image. The reset takes approximately 2 seconds during which time the I2C interface will return NACK for all transactions. The host issues a RESET command by writing 0x45 to register 0x1A.

6.35 Firmware Update Registers

STDLD: Start Firmware Download.
SDD: Send Firmware Download Data
DLDSTAT: Firmware Download Status(DLDSTAT)
Refer to Section 10, “I2C Firmware Upgrade” for a description of these registers.

7 NVDIMM EEPROM Contents

Non-volatile CORONADO data is stored in a 1 Kilobyte (or larger) EEPROM that the host accesses using the EEADDRL/H, EEDATA, and EESEL registers. Multi-byte integers are little-endian: LS byte to MS byte in increasing address order. The Type field indicates if the data should be interpreted as individual bits, an integer, or ASCII characters.

Table 5. CORONADO EEPROM Contents.

Byte	Acc	Name	Address	Contents	Source	Type
512	RW	USER	0x0000-0x01FF	User Read/Write data	Host	-
1	RW	ENABLES	0x0200	SMB alert, Gen Call	Host	Bits
79	-	-	0x0201-0x024F	RESERVED	-	-
1	R	BAKRSLT1	0x0250	Result of last BACKUP	CORONADO	Bits
1	R	BAKRSLT2	0x0251	Result of last BACKUP (cont'd)	CORONADO	Bits
4	R	T_RUN	0x0252-0x0255	Run Time in Hours	CORONADO	Integer
4	-	-	0x0256-0x0259	RESERVED	-	-
2	R	PWRCYCS	0x025A-0x025B	Number of Power Cycles	CORONADO	Integer
1	R	LASTTEMP	0x025C	Last Temperature Measurement °C	CORONADO	Integer
1	R	LASTCAP	0x025D	Last Capacitance Measurement (%)	CORONADO	Integer
1	R	LASTGTG1	0x025E	Last GTG1	CORONADO	Bits
1	R	LASTGTG2	0x025F	Last GTG2	CORONADO	Bits
2	R	T_LASTBU	0x0260-0x0261	Last Backup Time (sec)	CORONADO	Integer
2	R	TOTBACKS	0x0262-0x0263	Total Backup Operations	CORONADO	Integer
2	R	T_LASTCH	0x0264-0x0265	Last Charge Time (sec)	CORONADO	Integer
2	R	V_REMAIN	0x0266-0x0267	Remaining Vcap after last Backup (mV)	CORONADO	Integer
2	R	T_LASTRSTR	0x0268-0x0269	Last Restore Time (sec)	CORONADO	Integer
2	R	UNCORNF	0x026A-0x026B	Uncorrected NF errors, last RESTORE	CORONADO	Integer
1	R	NFPOOL	0x026C	NF reserve pool (%)	CORONADO	Integer
19	-	-	0x026D-0x027F	RESERVED	-	-
5	R	FWVER	0x0280-0x0284	CORONADO FW Version	CORONADO	ASCII
2	R	HWVER	0x0285-0x0286	CORONADO HW Version	Manufact.	ASCII
8	R	SN	0x0287-0x028E	Serial Number	Manufact.	ASCII
2	R	PCBVER	0x028F-0x0290	PCB Version	Manufact.	ASCII
4	R	MFDATE	0x0291-0x0294	Manufacture Date (YYWW)	Manufact.	ASCII
2	R	ENDUSR	0x0295-0x0296	Manufact. Name (End user vendor code)	Manufact.	ASCII
6	R	PCA	0x0297-0x029C	PC Assembly Number	Manufact.	ASCII
2	R	DENSITY	0x029D-0x029E	NVDIMM Density (GB)	Manufact.	Integer
2	R	CHARGEVOL	0x029F-0x02A0	Fully charge V of charger circuit (mV)	Manufact.	Integer
2	R	CHGMAXVOL	0x02A1-0x02A2	Highest V for cap measurement (mV)	Manufact.	Integer
93	-	-	0x02A3-0x02FF	RESERVED	-	-
256	R	FWCFG	0x0300-0x03FF	FW configuration	CORONADO	-

If the host attempts to write a read-only address (“R” in the Acc column) the CORONADO I^2C controller returns the NACK handshake.

7.1 USER

The host may write and read this uncommitted 512 byte EEPROM space for any purpose.

7.2 ENABLES

The host enables various CORONADO features using this register. Note that CORONADO ships with these bits set to 0.

Table 6. CORONADO Enable Bits.

Bit	Function
7:2	Reserved, read 0
1	General Call Enable
0	SMB Alert Enable

7.2.0 Bit 0: SMB Alert Enable

If this bit is set, CORONADO asserts the SMB ALERT mechanism when the CORONADO Good To Go indication negates (GTG.7 makes a 1-0 transition). This mechanism is described in Section 9.4.

7.2.1 Bit 1: General Call Enable

This bit enables “General Call” writes to CORONADO.

There are two methods the host can use to start a register-commanded BACKUP operation:

1. The usual way is for the host to write the BACKUP register with the value 0x2E using the CORONADO I^2C address.
2. A second way is for the host to write the same BACKUP register, but instead to I^2C address 0. This I^2C General Call mechanism allows the host simultaneously to initiate BACKUP operations to multiple CORONADOS in a system without having to send individual commands to each CORONADO.

In either case a BACKUP starts if enabled. If ENABLES.2=0, CORONADO ignores host writes to I^2C address 0.

7.3 BAKRSLT1

Result of the last BACKUP

Table 7. BAKRSLT1 Bits.

Bit	Status
7	Pin 167 started BACKUP
6	BACKUP was cancelled by host
5	Register started BACKUP
4	BACKUP was requested with CKE=1
3	BACKUP was requested with GTG=0
2	BACKUP did not complete
1	BACKUP Succeeded: Valid NF Image
0	External PGEM Signal started BACKUP

The host can determine status of the last BACKUP by reading this register. These register bits are non-volatile because the BACKUP results normally are checked when the host re-powers following power interruption. The host clears this register (invalidating previous BACKUP results) by issuing the RELEASE_NF_IMAGE command.

If the host performs a controlled power-down, it must clear ENABLE_SAVE if it wishes to inhibit a BACKUP operation.

Bit 0: External Signal Started BACKUP
On CORONADO versions that support an external BACKUP trigger, this bit indicates that the BACKUP started as a result of the host asserting this external trigger signal.

Bit 1: BACKUP Succeeded: Valid NF Image
CORONADO sets this bit after completing a successful BACKUP operation.
CORONADO clears this bit:

- When the host releases the previous NF image by writing RELEASENF=0x37.
- If a BACKUP started but did not complete, leaving the NF with a mixture of new and stale data.

Bit 2: BACKUP Did Not Complete
CORONADO hardware sets this bit if the last BACKUP operation did not complete for any reason.

Bit 3: BACKUP started while GTG=0
CORONADO performed a BACKUP with GTG=0. The host should consult the individual GTG bits to determine BACKUP success.

Bit 4: BACKUP started with CKE=1
This indicates that the SDRAMS were not in self-refresh when CORONADO took control of the SDRAMS. In this case the NF image should be considered suspect, and the host should take its own error detection/correction measures to validate the SDRAM data after a RESTORE.

Bit 5: BACKUP register requested the last BACKUP
This indicates that the host requested the last backup with software, by the host writing the BACKUP register. This does not indicate that the BACKUP actually started; the host can consult other bits to determine the BACKUP outcome.

After a successful BACKUP (Valid NF Image = 1), if bits 5 and 7 are zero, the BACKUP was initiated by CKE=0.

Bit 6: BACKUP was canceled by host
This is a very unlikely event, because the BACKUP probably started because the host lost power, and is unable to cancel a BACKUP. This status is provided mainly to indicate errant host behavior. If CORONADO sets this bit, it also sets bit 2, BACKUP Did Not Complete.

Bit 7: Pin 167 requested the last BACKUP
This indicates that the host requested the last backup with hardware, by asserting DIMM pin 167. This does not indicate that the BACKUP actually started; the host can consult other bits to determine the BACKUP outcome.

After a successful BACKUP (Valid NF Image = 1), if bits 5 and 7 are zero, the BACKUP was initiated by CKE=0.

7.4 BAKRSLT2

Pre-BACKUP Faults

This register collects fault conditions that would impair a BACKUP operation.

Table 8. BAKRSLT2 Bits.

Bit	Status
7	Reserved, reads 0
6	Reserved, reads 0
5	Reserved, reads 0
4	Reserved, reads 0
3	Reserved, reads 0
2	Reserved, reads 0
1	General Fault
0	SDRAM Initialization Fault

Bit 0: SDRAM Initialization Fault

This bit indicates that the CORONADO controller was unable to initialize the SDRAM.

Bit 1: General Fault

Any fault that prevents a BACKUP; module requires service.

7.5 T_RUN

Total RunTime

This 32-bit integer indicates the total hours CORONADO has operated.

7.6 PWRCYCS

Number of Power Cycles

This 16-bit integer indicates how many times CORONADO has been power-cycled.

7.7 LASTTEMP

Result of last PowerGEM temperature measurement.

This byte indicates the last PowerGEM temperature measurement taken by CORONADO.

7.8 LASTCAP

Result of last capacitance measurement (PCT)

CORONADO updates this byte after performing a capacitance measurement. The value represents the percentage of Ultracapacitor initial measured value. CAPPCT has a range of 0-100.

The CORONADO PowerGEM is rated to operate over its specified lifetime by taking into account the fact that capacitors gradually lose capacitance over long time periods. CORONADO performance ratings are conservatively specified using “end-of-life” capacitance instead of beginning capacitance values. To give an example, capacitance measurements could give percentage values ranging from 110% (new) to 82% (after 5 years). A value of 82% at end-of-life would be perfectly adequate if the CORONADO PowerGEM is rated to deliver its rated power with, for example, 70% of its initial capacitance.

After a capacitance measurement CORONADO compares this register with the data sheet specification for minimum percentage of data sheet capacitance to insure operation. If this measurement indicates less than the data sheet minimum percentage, CORONADO clears the GTG bit GTG1.6 (PCT Capacitance Value OK).

7.9 LASTGTG1

7.10 LASTGTG2

GTG1 and GTG2 BACKUP States
These registers the GTG1 and GTG2 register bits when a BACKUP operation starts. The host may inspect these saved registers at the next power-on to determine detailed pre-BACKUP conditions.

7.11 T_LASTBU

Last BACKUP Time
Time taken to perform the last BACKUP in seconds.

7.12 TOTBACKS

Total BACKUP Operations
Total number of BACKUP operations. This count increments for every BACKUP attempt, regardless of the outcome of the BACKUP.

7.13 T_LASTCH

Last Charge Time

Time taken after the last power-on for the PowerGEM to fully charge its Ultracapacitors, in seconds.

7.14 V_REMAIN

Remaining Cap Voltage After Last BACKUP

After CORONADO completes a BACKUP operation it measures the voltage to which the PowerGEM decreased to perform the BACKUP. These registers indicate the remaining voltage in millivolts.

7.15 T_LASTRSTR

Last RESTORE Time

Time CORONADO took to perform the last RESTORE in seconds.

7.16 UNCORNF

Uncorrected NF Errors

In the rare event that the CORONADO controller encounters an uncorrectable read error from the NAND flash during a restore, CORONADO sets bit 1 (Uncorrectable NF read error during RESTORE) of the Restore Results register RSTRESLT, and writes the number of encountered errors to this register.

CORONADO products employ extensive error detection and correction for their internal NAND Flash (NF) devices. Robust error detection/correction insures that over the product lifetime, any defective NF blocks are automatically detected, taken out of service, and replaced with reserve blocks. Nevertheless, the possibility exists that during a NF read, an uncorrectable error could be encountered. This means that the corresponding SDRAM memory area is not valid, since NF data is copied into SDRAM during the RESTORE operation.

7.17 NFPOOL

Remaining NF Reserve Blocks

NAND Flash vendors guarantee a maximum number of blocks that will require replacement due to wear over the device lifetime. CORONADO adds some margin to this figure and sets aside the resulting pool of NF reserve blocks. This register returns the percentage of the pool that remains available. If this number ever decreases to zero (an unlikely event), CORONADO clears the GTG1.2 bit (NF Reserve Pool > 0%).

7.18 Manufacturing Data

FWVER, HWVER, DENSITY, SN, PCBVER, MFDATE, ENDUSR and PCA

Manufacturing data is stored in these 2 to 8-character strings, which read left to right in ascending EEPROM addresses.

7.19 Reserved for Internal Use

Reserved for AGIGARAM internal use. The host cannot read or write these locations: Writes are ignored, and reads return the value 0x00.

8 PGEM EEPROM Contents

Non-volatile PowerGEM data is stored in a 256 Byte EEPROM that the host accesses using the EEADDRL/H, EEDATA, and EESEL registers. Multi-byte integers are little-endian: LS byte to MS byte in increasing address order.

Table 9. PGEM EEPROM Contents.

Byte	Acc	Name	Address	Contents	Source	Type
32	R	TEMPHIST	0x000-0x01F	Temperature History	CORONADO	Integer
1	-	---	0x020	RESERVED	-	-
32	R	CAPHIST	0x021-0x040	Capacitance History	CORONADO	Integer
1	R	CHARGER	0x041	0=Charger on NVDIMM; 1=Charger on PGEM	Manufacturer	Bits
1	R	CAPACITANCE	0x042	Spec CAP value of PGEM in Farads	Manufacturer	Integer
2	R	CHARGEVOL	0x043-0x044	Full chg V of chg circuit; 0xFFFF if no charger	Manufacturer	Integer
2	R	CHGMAXVOL	0x045-0x046	Highest voltage for cap measurement; 0xFFFF if no charger	Manufacturer	Integer
1	R	POWERDET	0x047	Power fail detection avail; 0 = no, 1 = yes	Manufacturer	Bits
2	R	CHARGECUR	0x048-0x049	Cap charge current (mA); 0xFFFF if no charger	Manufacturer	Integer
2	R	HWVER	0x04A-0x04B	PGEM HW Version	Manufacturer	ASCII
16	R	CAPPN	0x04C-0x05D	Capacitor Part Number	Manufacturer	ASCII
8	R	SN	0x05E-0x63	Product Serial Number	Manufacturer	ASCII
2	R	PCBVER	0x064-0x065	PCB Version	Manufacturer	ASCII
4	R	MFDATE	0x066-0x069	Manufacture Date (YYWW)	Manufacturer	ASCII
2	R	ENDUSR	0x06A-0x06B	Manufacturer Name (End user vendor code)	Manufacturer	ASCII
11	R	PCA	0x06C-0x076	PC Assembly Number	Manufacturer	ASCII
1	R	INITIALCAP	0x077	Initial measured CAP value during Manufacture in Farads	Manufacturer	Integer
TBD	R	---	TBD	RESERVED	-	-

8.1 TEMPHIST

Temperature History.

Table 10. Data Format for Temperature History.

TEMPHIST Byte Offset	Temperature History *Hours between these temperatures*	
0-1	Over 70°C	
2-3	65°C	70°C
4-5	60°C	65°C
6-7	55°C	60°C
8-9	50°C	55°C

10-11	45°C	50°C
12-13	40°C	45°C
14-15	35°C	40°C
16-17	30°C	35°C
18-19	25°C	30°C
20-21	20°C	25°C
22-23	15°C	20°C
24-25	10°C	15°C
26-27	5°C	10°C
28-29	0°C	5°C
30-31	Under 0°C	

CORONADO takes a PowerGEM temperature measurement every hour of operation. Each time CORONADO measures temperature it updates the LASTTEMP EEPROM value and the EEPROM Temperature History data. Each 16-bit integer (in L-H order) represents the number of hours CORONADO PowerGEM has run in the indicated temperature range. For example, if bytes 15:14 = 150, CORONADO PowerGEM has experienced a temperature between 35°C and 40°C for 150 hours. The host can use the 32 values (16 integers) to construct a histogram of temperature “bins”, each 5°C wide, with cumulative hours spent in each bin. Figure 3 shows what a Temperature Histogram might look like after an extended run time.

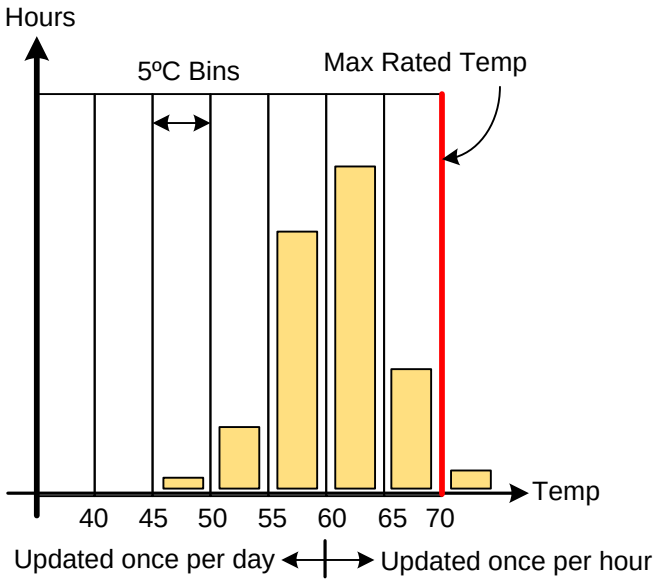

Figure 3. An Example PowerGEM Temperature Histogram.

CAPHIST

Capacitance measurement history.

Table 11. Data Format for Capacitance History.

CAPHIST Byte Offset	Capacitance History *Days between these % capacitance values*	
0-1	Over 120%	
2-3	115%	120%
4-5	110%	115%
6-7	105%	110%
8-9	100%	105%
10-11	95%	100%
12-13	90%	95%
14-15	85%	90%
16-17	80%	85%
18-19	75%	80%
20-21	70%	75%
22-23	65%	70%
24-25	60%	65%
26-27	55%	60%
28-29	50%	55%
30-31	Under 50%	

CORONADO measures the capacitance of its Ultracapacitor stack once per week, or whenever commanded by the host. A unique CORONADO feature is that it can perform the capacitance measurement without depleting the charge in the Ultracapacitors, so that GTG can remain asserted during the measurement.

Each byte pair in the Capacitance History represents the number of times the Ultracap stack capacitance measurement fell into a particular capacitance range. If the host does not command more regular measurements, each measurement represents a week of time. The range numbers represent percentage of initial (time of manufacture) measured capacitance. For example, bytes 11:10 = 200 indicates 200 measurements at 95-100% of initial capacitance. An additional EEPROM byte (LASTCAP) indicates the result of the last capacitance measurement, again given as the percentage of initial capacitance.

8.2 Measurements at Bin Boundaries

A temperature or capacitance value at a bin boundary is tallied in the upper bin. For example a 40°C temperature goes into the 40°C to 45°C bin, not the 35°C to 40°C bin.

9 SMB Communication

COROADO implements an SMB-compatible I^{2}C slave unit as the interface to its register file. The CORONADO controller shares the SMB connections with the onboard SPD (Serial Presence Detect) EEPROM and temperature sensor as shown in Figure 4.

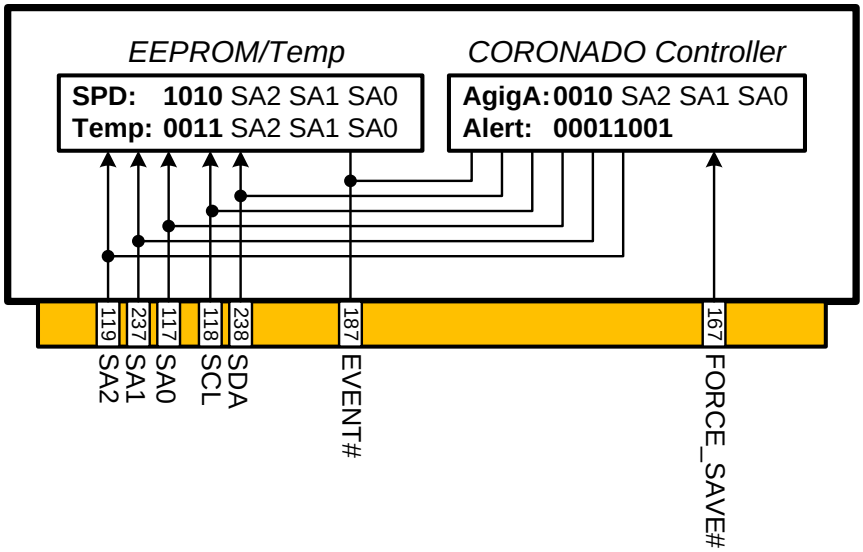

Figure 4. CORONADO shares the DIMM SMB connections.

The CORONADO SMB slave controller recognizes four transfer formats:

- Write Byte
- Read Byte
- Alert Response
- General Call

9.1 Slave Address Byte ACK and NACK

The SMB specification states that an SMB slave must always ACK its own address. Lack of the ACK signal indicates that the SMB slave at the requested address is not present. Because CORONADO implements an FPGA controller, the CORONADO SMB slave logic is not available until the FPGA loads its configuration bits and MCU code. This power-on readiness delay is specified in the CORONADO data sheet as T_{HW_RDY}.

The SMB master can detect that the CORONADO hardware is ready by reading a register (BUSCHECK) that is hard-coded to the value 0xA5. Just after power-on this register reads 0xFF due to the uninitialized I^{2}C drivers and the bus pull-up resistors. The host should poll this register until it returns the value 0xA5 before conducting any I^{2}C traffic.

9.2 Write-Byte

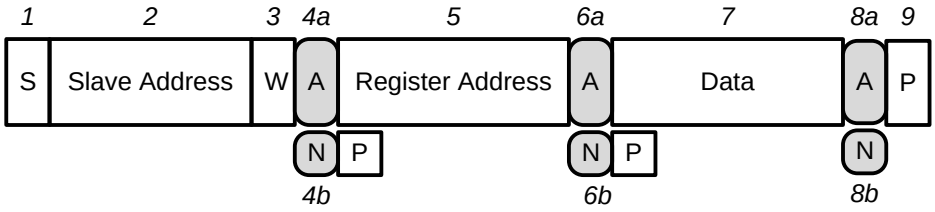

Figure 5. SMB Write Byte Transfer.

An SMB master **Write Byte** operation comprises the following steps. In Figure 5 and Figure 6 the un-shaded items represent the SMB bus master driving the bus and the shaded items represent the SMB slave logic driving the bus. The following steps correspond to the numbers in Figure 5:

1. SMB master sends the START signal.
2. SMB master sends the 7-bit SMB slave address.
3. SMB master sends the direction bit set to WRITE (0).
4. CORONADO SMB slave sends ACK or NACK:
    a. Immediately sends ACK (no clock stretch) if the address matches CORONADO's slave address. The transfer continues with step 5
    b. NACK if the address does not match CORONADO's slave address. CORONADO enters an idle state and removes the drive from its SCL-SDA pins, causing the bus to pull high due to the I^2C pullup resistors. The CORONADO slave controller remains in this idle state until it detects the next START signal.
5. SMB master sends a byte containing an SMB register number.
6. CORONADO SMB slave sends ACK or NACK:
    a. ACK if the requested SMB register number is valid.
    b. NACK if the requested register number is invalid. In this case CORONADO enters an idle state and removes the drive from its SCL-SDA pins, causing the bus to pull high due to the I^2C pullup resistors. The CORONADO slave controller remains in this idle state until it detects the next START signal.
7. SMB master sends a data byte to be written to the SMB register requested in (5).
8. CORONADO immediately sends ACK or NACK (no clock stretch):
    a. ACK if the requested SMB register can be written.
    b. NACK if the requested register number is read-only. In this case CORONADO enters an idle state and removes the drive from its SCL-SDA pins, causing the bus to pull high due to the I^2C pullup resistors. The CORONADO slave controller remains in this idle state until it detects the next START signal.
9. SMB master sends the STOP signal.

9.3 Read-Byte

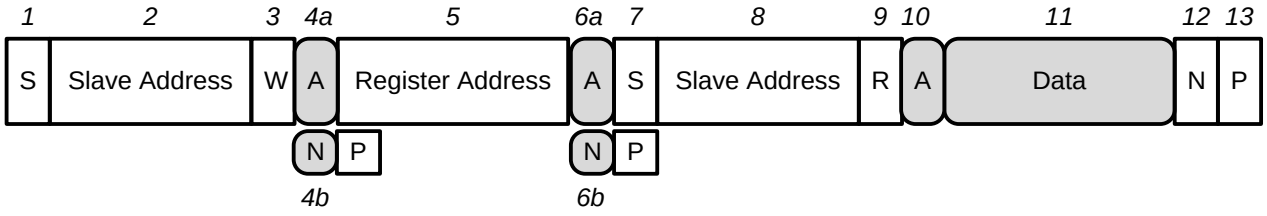

Figure 6. SMB Read Byte Transfer.

An SMB master **Read Byte** operation comprises the following steps. The steps correspond to the numbers in Figure 6.

1. SMB master sends the START signal.
2. SMB master sends the 7-bit SMB slave address.
3. SMB master sends the direction bit set to WRITE (0).
4. CORONADO SMB slave sends ACK or NACK:
    a. Immediately sends ACK (no clock stretch) if the address matches CORONADO's slave address. The transfer continues with step 5
    b. NACK if the address does not match CORONADO's slave address. CORONADO enters an idle state and removes the drive from its SCL-SDA pins, causing the bus to pull high due to the I^2C pullup resistors. The CORONADO slave controller remains in this idle state until it detects the next START signal.
5. SMB master sends a byte containing an SMB register number.
6. CORONADO SMB slave sends ACK or NACK:
    a. ACK if the requested SMB register number is valid.
    b. NACK if the requested register number is invalid. In this case CORONADO enters an idle state and removes the drive from its SCL-SDA pins, causing the bus to pull high due to the I^2C pullup resistors. The CORONADO slave controller remains in this idle state until it detects the next START signal.
7. SMB master sends a *repeated START* signal.
8. SMB master re-sends the 7-bit SMB slave address.
9. SMB master sends the direction bit set to READ (1).
10. CORONADO immediately sends ACK (no clock stretch).
11. CORONADO SMB slave sends the requested register data.
12. SMB master sends the NACK signal to indicate it is finished receiving.
13. SMB master sends the STOP signal.

9.4 Alert Response

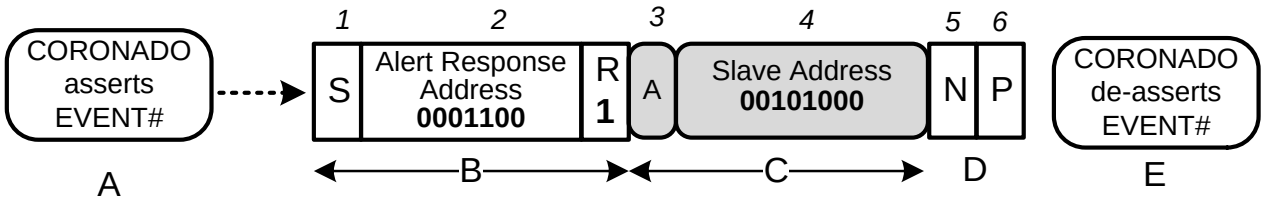

Figure 7. SMB Alert Response.

CORONADO indicates its readiness to perform a BACKUP operation using the GTG bit. The host system may periodically check the state of this bit by polling the CORONADO register GTG1 over the SMB. For quicker response, the host system may implement an optional SMB interrupt feature which uses a hardware signal called SMBALERT# in the SMB spec. On a DIMM, this signal is called ALERT#. ALERT# is commonly used for motherboard temperature control. For host systems that implement the SMB Alert mechanism, CORONADO implements the “Modified Receive Byte” protocol shown in Figure 7.

If SMB Alert is enabled, whenever the CORONADO GTG signal makes a 1-0 transition, the CORONADO hardware asserts the SMBALERT# signal by pulling it low with an open-drain driver (A). The EVENT# signal is wire-ANDED with any other SMB devices on the bus that can drive EVENT# low. Any device can assert the EVENT# line low, and only when all devices de-assert their drive does EVENT# go inactive (high).

When EVENT# = 0 the SMB master knows that one or more slaves is requesting service, but it does not yet know the address of the requesting slave(s). To discover the address of the requestor the SMB master sends out an SMB-reserved address called the Alert Response Address (B). Any slave unit that asserted the EVENT# signal is required to reply with its own slave address. This informs the SMB master which SMB slave to query to discover the cause of the interrupt. CORONADO sends back its own address in (C), and the special single-byte read operation terminates in (D). Following the STOP bit in (D), CORONADO then automatically de-asserts its EVENT# signal (E).

The de-assertion requirement (E) is the reason CORONADO asserts EVENT# on a 1-to-0 transition of the GTG signal. Holding this signal low for an extended time (for example as the Ultracapacitors charge) would lock out other contributors to the EVENT# signal.

If two or more SMB slaves assert their EVENT# signals at the same time, the conflict is resolved using the standard SMB (I^2C) arbitration mechanism. Specifically, the CORONADO

SMB slave logic monitors the SMB_SDA line whenever it is driving SMB_SDA and SMB_SCL is high. In Figure 7, this is during interval (C). If, during this interval, CORONADO detects a logic LOW while it is sending HI, it knows that another slave is driving the bus. In this case the CORONADO logic immediately removes its drive signals, keeps its EVENT# signal asserted (low), and waits for the next START bit.

9.5 General Call

Figure 8. I²C General Call Format.

The host normally sets the Coronado BACKUP register (0x0A) to 0x2E to initiate a BACKUP operation. The I²C specification, on which the SMB spec is based, defies a reserved address of 00000000 as a General Call address. The master can use this special address to send information to multiple slaves using a single transfer. Coronado uses this feature to allow multiple Coronado NVDIMMS to receive the BACKUP command in parallel, saving critical time in the power-loss program execution.

The SMB master sets the register GENCALL (General Call) to 0x99 to enable this feature. The feature defaults to disabled at power-on.

Note: It is preferable for hosts to use pin 167 to initiate a BACKUP operation due to its superior speed compared with the 100 KHz SMB signaling rate. The General Call feature is provided for systems that cannot support pin 167.

Note: To use the General Call feature, the SMB master (host) must insure that no other SMB slaves on its bus respond to the general call address 00000000 with the second byte defined as 0x0A.

9.6 Multi-byte Data

The host reads and writes only single bytes in every SMB transfer. The host reads multi-precision integers by accessing consecutive registers, low-byte first in incrementing order. The host must send the register address for each byte; there is no automatic register incrementing.

Note: In order to minimize firmware upgrade times, the CORONADO SMB interface may operate in a manner that does not adhere to the one-byte-per-transfer protocol. Refer to the Firmware Upgrade section for details.

9.7 SMB Compatibility

The SMB slave unit conforms to the SMB Specification version 2.0. In addition to SMB electrical specifications in the data sheet, this implies the following timing conditions [SMD spec parameters in brackets]:

- CORONADO operates with SCL = 100 KHz [f_{SMB} = 10KHz to 100 KHz].
- CORONADO continuously monitors the SCL and SDA lines. If either line is held low for more than 25 milliseconds, either by CORONADO or anything else on the bus, the SMB slave resets, unconditionally removing drive (if any) from SCL and SDA.

10 I²C Firmware Upgrade

CORONADO systems have two programmable units included in the firmware upgrade image:

1. FPGA logic (i.e. FPGA fabric)
2. Firmware for the FPGA CPU and controllers that comprise the System Control Unit (SCU).

Headers at the beginning of the update image file include information about each unit that is to be updated. An update image file may contain data for the either the FPGA logic or the SCU firmware or both.

10.1 Update Sequence

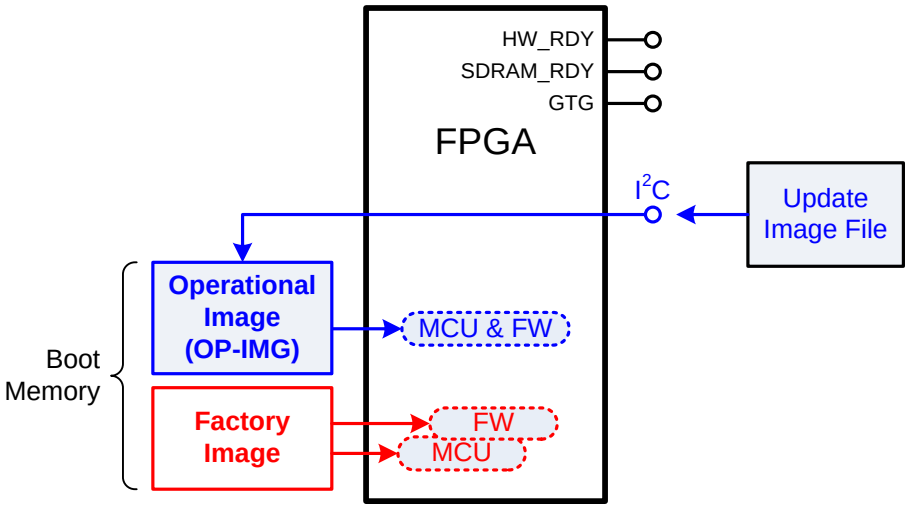

Figure 8. FPGA can initialize from two images.

A non-volatile memory outside the FPGA ("Boot Memory") contains two digital images as shown in Figure 8. The machines they create are shown with dotted lines to indicate that only one of these images can reside in the FPGA at a time. The function of the two images is as follows:

- The Factory Image, shown in red, comprises a loader plus enough of the I²C control interface to allow host-commanded firmware updates. This image is unalterable, and always loads when power is applied or the FPGA comes out of RESET.
- The Operational Image (OP-IMG), shown in blue, contains the image for the fully operational AGIGARAM system plus updated firmware code. Only this image can be altered in the field (updated) using the I²C protocol described in this Appendix.

For purposes of understanding the load/update state diagram, it is convenient to think in terms of a “red machine” (configured by the factory image) and a “blue machine” (configured by the operational image) corresponding to the colors in Figure 8. The states in Figure 9 are color-coded to indicate which of these machines is loaded and operating. Green blocks indicate host actions.

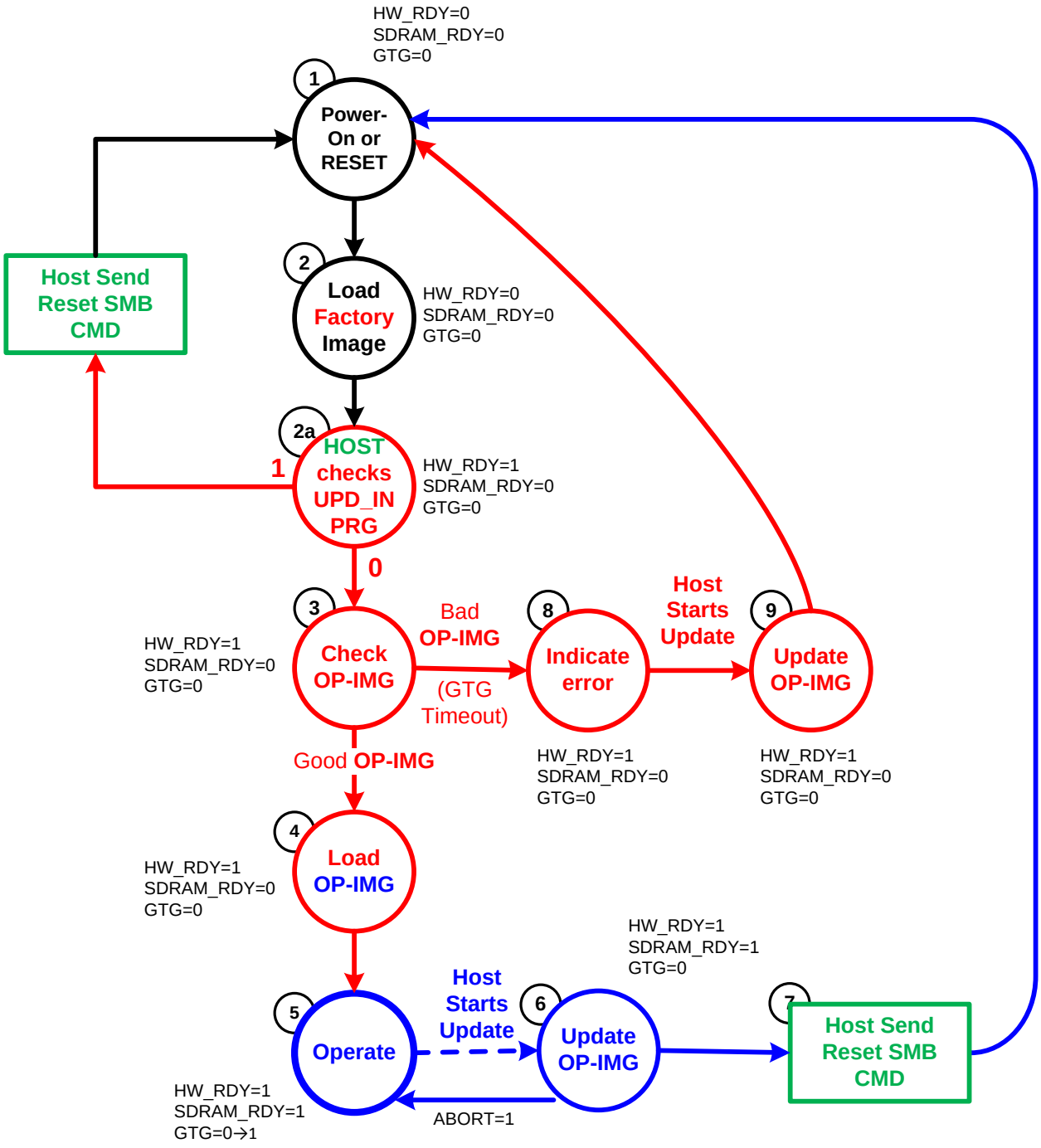

Figure 9. Firmware Load & Update State Diagram

Routine operation proceeds as states 1-2-3-4-5, terminating in the fully operational AGIGARAM state 5. State 4 is shown in red to indicate that the machine created by the factory

image does the loading of the (blue) operational image from the boot memory. Once in operational state 5 the host may initiate a firmware update at any time, indicated by the dotted line.

A firmware update follows the state sequence 5-6-7, 1-2-3-4-5. State 6 writes the new (updated) OP-IMG into the boot memory using the Update Image File sent by the SMB host. This new image is loaded into the FPGA as the updated OP-IMG in state 4.

The host test in state 2a handles the condition that the host momentarily loses-then-regains power in the middle of an update, but before the new image is written to the boot memory. In this case the FPGA needs hardware reset because it did not see the host power loss--it remained powered due to PowerGEM backup power.

States 8 and 9 handle another exceptional condition, where the firmware download and re-programming of the boot loader memory is interrupted because of any abnormal condition during the update. This leaves a corrupt OP-IMG in the boot loader memory. The purpose for state 3 is to verify the integrity of the OP-IMG before loading it into the FPGA and using it. This verification is done by the red machine in state 3 by reading the flag of OP-IMG. If the flag is invalid, state 8 is entered and the host must re-do the download operation. The host detects that the previous update failed by observing that the GTG signal does not assert within its maximum specified timeout value (t_{GTG}) and then get the bits in GTG2 (bit 0-2 for image valid).

Note that states 6 and 9 are the only states that can write the boot memory via I^2C. They are shown as distinct states because the loader exists in both the red Factory Machine and the blue Operating Machine.

Three FPGA output signals become invalid during a firmware update process. The states of these signals are shown for each state in Figure 9:

1. HW_RDY
2. SDRAM_RDY
3. GTG (Good To Go)

Note: The SDRAM_RDY signal should be considered invalid while PMODE = 1. Although the FPGA pulls its outputs low as its configuration bits are loaded, the host can access the SDRAM while PMODE = 1 even though SDRAM_RDY = 0.

10.2 SMB Block Write

The Coronado firmware update process uses the SMB “block write” format with 1 byte payloads. This format is shown in Figure 9.

Figure 9. SMB Block Write format.

The SMB command code slot is set to the Coronado register number 38, indicating a code download. The byte count is fixed as 1 in order to transmit the maximum bytes per block allowed by the SMB specification. 1 data bytes follow the byte count.

10.3 Update Protocol

The downloader uses internal SCU memory as a buffer for download data. A handshake mechanism (using the READY signal) is used for each packet to be programmed. The host sends download data in 1 byte packets (Every 32 packets verify the data whether correct. The 32 packets have 30 data bytes plus 2 checksum bytes) by repeating write-block command to R38 until all data is transmitted.

R37: Start Firmware Download

The host writes R37=0x67 to start a firmware upgrade (download).

R38: Send Firmware Download Data

The host downloads firmware update data by repeatedly writing R38 with 32-byte packets. Data flow is coordinated by the READY bit in status register R39. The first two packets after the ‘start firmware download’ command is the headers shown in Table 12.

The Data Bytes comprise two formats, headers and data. The headers are transmitted first, followed by the data blocks as shown in Table 12.

Table 12. Coronado Update Image Format.

0	1	2	3	4 5 6 7	8 9 10 11 12 13	14 15
8C	8C	8C	01 FPGA	FPGA Byte Count	FPGA Version String	
FPGA Image Checksum				00		Packet checksum
8C	8C	8C	02 SCU	SCU Byte Count	SCU Version String	
SCU Image Checksum				00		Packet checksum
16 data bytes						
14 data bytes						2 bytes Packet checksum
32-byte blocks						
16 data bytes						
14 data bytes						2 bytes Packet checksum

Note: The firmware update header represents multi-byte integers in big-endian format.

The first three 32-byte blocks in Table 12 are headers for the three update units, FPGA and SCU. All two headers are required, even if the full code image does not contain code for all two update units. An absent code unit is indicated by a zero Byte Count field.

The headers are followed by update data. The update data must be in the order shown,

R39: Firmware Download Status

The host downloader coordinates delivery of update packets by reading R39 to determine various status bits.

Table 13. Firmware Up/Download Status Bits.

Bit	Meaning	Comments
7	ABORT	
6	0	
5	0	
4	0	
3	UPD_INPRG	Update is in progress
2	TX_ERROR	SMB transmit error
1	READY	Coronado is ready to receive next 1 byte packet
0	PMODE	Programming Mode

PMODE: Programming Mode

PMODE = 1 indicates that the programming unit is ready to accept download data. PMODE goes high at the beginning of a download/programming operation, and low when the programming operation terminates.

READY: Ready to accept the next packet.

READY is the handshake signal between the host and the programming unit. When the CORONADO programming unit receives one byte of a packet it sets READY = 0 to indicate it is busy. After finishing with the block the programming unit sets READY = 1. When READY makes its 0-1 transition the TR_ERR bit indicates the result of the operation.

READY is also used to hold off downloading while the CORONADO loader erases its internal memories to prepare for the download. After the host sends the initial 32 packets with header, the READY signal goes low while the CORONADO loader determines which of the internal memories are to be updated, and erases the appropriate memories. When erasure is complete the CORONADO loader sets READY = 1 to indicate the programming unit is ready to accept update data.

TX_ERROR: SMB Transmit Error

TX_ERROR is valid when READY makes a 0-1 transition.

Every received 32 packets contains 30 data bytes and a 2-byte checksum. The CORONADO loader computes a checksum over the 32 data bytes and compares with the checksum. If they do not match the loader sets TX_ERROR =1 to indicate the block should be re-sent. If TX_ERROR =1 for three tries of the same block, the loader sets ABORT = 1 and the download terminates, (PMODE = 0).

ABORT: Abort Firmware Update Process

If ABORT = 1 a download process has terminated abnormally. If the host loader detects ABORT = 1 it should wait for the CORONADO loader to exit the programming mode (indicated by PMODE = 0). Then the host should read the GTG2 register to get details about the aborted download.

UPD_INPRG : Firmware Update Is In-Progress

The host should check this bit at every power-on to insure that an update did not abort before the host lost and regained power. Refer to Figure 9 for details.

10.4 Incomplete Updates

Unfinished downloads and any data errors are all called incomplete updates. For example, power loss during the update or some bits inverted. Incomplete updates will result in Coronado reverting to the factory image that was installed when the unit was manufactured the next time it is powered up. Coronado will verify the image after downloading all data. This prevents a corrupted code image (some old code, some new) from executing.

At that point, only completely upgrading the firmware will restore a valid FPGA image.

10.5 After Update Completes

Note: After the firmware upgrade completes, the host must wait 2 minutes to allow Coronado to rebuild the system parameters.

The host must reset the CORONADO system after a firmware update completes. It is recommended that the host power cycle the CORONADO board, but the reset command R1A can also be used.

Write 0x45 to R1A to reset CORONADO.

Resetting allows firmware to be reloaded and checks whether the upgrade was performed correctly or not.