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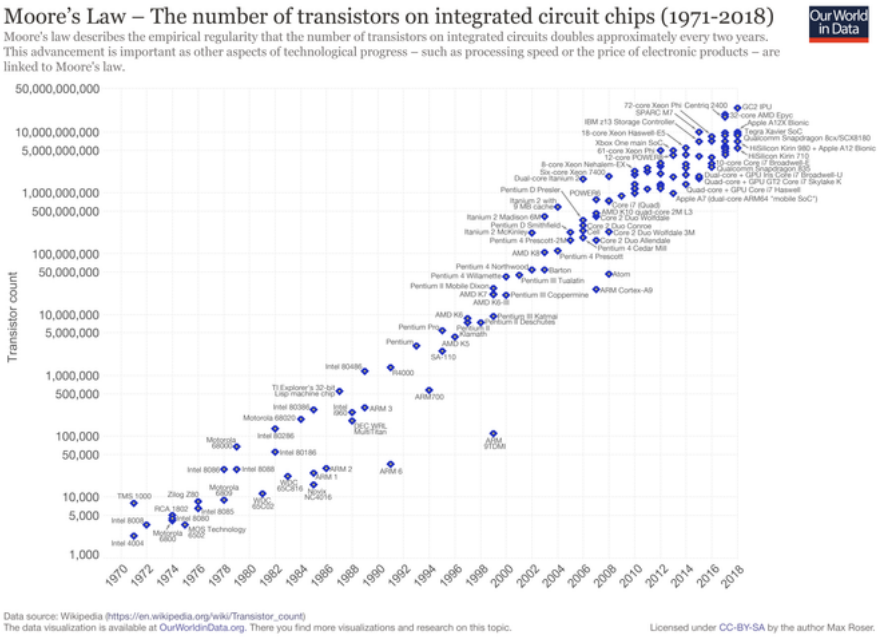
Moore's law

Moore's law is the observation that the number of transistors in a dense integrated circuit doubles about every two years. The observation is named after Gordon Moore, the co-founder of Fairchild Semiconductor and CEO of Intel, whose 1965 paper described a doubling every year in the number of components per integrated circuit,[2] and projected this rate of growth would continue for at least another decade.[3] In 1975,[4] looking forward to the next decade,[5] he revised the forecast to doubling every two years, a compound annual growth rate (CAGR) of 41.4%.[6][7][8]



A plot (logarithmic scale) of MOSFET transistor counts for microprocessors against dates of introduction, nearly doubling every two years.

The doubling period is often misquoted as 18 months because of a prediction by Moore's colleague, Intel executive David House. In 1975, House noted that Moore's revised law of doubling transistor count every 2 years in turn implied that computer chip performance would roughly double every 18 months (with no increase in power consumption).[9] Moore's law is closely related to MOSFET scaling, also known as Dennard scaling,[10] as the rapid scaling and miniaturization of silicon MOSFETs (metal-oxide-semiconductor field-effect transistors, or MOS transistors)[11][12] is the key driving force behind Moore's law.[10][13]

Moore's prediction proved accurate for several decades and has been used in the semiconductor industry to guide long-term planning and to set targets for research and development (R&D).[14] Advancements in digital electronics are strongly linked to Moore's law: quality-adjusted microprocessor prices,[15] memory capacity (RAM and flash), sensors, and even the number and size of pixels in digital cameras.[16] Digital electronics has contributed to world economic growth in the late twentieth and early twenty-first centuries.[17] Moore's law describes a driving force of technological and social change, productivity, and economic growth.[18][19][20][21]

Moore's law is an observation and projection of a historical trend. It is an empirical relationship and not a physical or natural law. Although the rate held steady from 1975 until around 2012, the rate was faster during the first decade. In general, it is not logically sound to extrapolate from the historical growth rate into the indefinite future. For example, the 2010 update to the International Technology Roadmap for Semiconductors predicted that growth would slow around 2013,[22] and in 2015, Gordon Moore foresaw that the rate of progress would reach saturation: "I see Moore's law dying here in the next decade or so."[23]

Experts in microprocessor architecture report that semiconductor advancement has slowed industry-wide since around 2010, below the pace predicted by Moore's law.[24] Brian Krzanich, the former CEO of Intel, announced, "Our cadence today is closer to two and a half years than two."[25] Intel stated in 2015 that improvements in device have slowed, starting at the 22 nm feature width around 2012, and continuing at 14 nm.[26] Brian Krzanich, the former CEO of Intel, announced, "Our cadence today is closer to two and a half years than two."[27] Intel also stated in 2017

that hyperscaling would be able to continue the trend of Moore's law and offset the increased cadence by aggressively scaling beyond the typical doubling of transistors.[28] Krzanich cited Moore's 1975 revision as a precedent for the current deceleration, which results from technical challenges and is "a natural part of the history of Moore's law".[29][30][31] Leading semiconductor manufacturers, TSMC and Samsung Electronics, have 10 nm and 7 nm semiconductor nodes in production.[32][33]

Contents

History of the concept

In 1959, Douglas Engelbart discussed the projected downscaling of integrated circuit (IC) size in the article "Microelectronics, and the Art of Similitude".[34][35] Engelbart presented his ideas at the 1960 International Solid-State Circuits Conference, where Moore was present in the audience.[36]


Gordon Moore in 2004

The MOSFET (metal-oxide-semiconductor field-effect transistor), also known as the MOS transistor, was invented by Mohamed Atalla and Dawon Kahng at Bell Labs in 1959, and demonstrated in 1960.[37] It was the first truly compact transistor that could be miniaturised and mass-produced for a wide range of uses,[38] due to its high scalability,[11] and low power consumption, leading to increasing transistor density.[13] This made it possible to build high-density IC chips,[39] enabling what would later be known as Moore's law.[13] In the early 1960s, Gordon E. Moore recognized that the ideal electrical and scaling characteristics of MOSFET devices would lead to rapidly increasing integration levels and unparalleled growth in electronic applications.[40]

For the thirty-fifth anniversary issue of *Electronics* magazine, which was published on April 19, 1965, Gordon Moore, who was working as the director of research and development at Fairchild Semiconductor at the time, was asked to predict what was going to happen in the semiconductor components industry over the next ten years. His response was a brief article entitled, "Cramming more components onto integrated circuits".[41] Within his editorial, he speculated that by 1975 it would be possible to contain as many as 65,000 components on a single quarter-square-inch semiconductor.

> The complexity for minimum component costs has increased at a rate of roughly a factor of two per year. Certainly over the short term this rate can be expected to continue, if not to increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least 10 years.

His reasoning was a log-linear relationship between device complexity (higher circuit density at reduced cost) and time.[42][43]

In 1974, Robert H. Dennard at IBM recognized the rapid MOSFET scaling technology and formulated what became known as Dennard scaling. It states that, as MOS transistors get smaller, their power density stays constant, so that the power use stays in proportion with area.[44][45] MOSFET scaling and miniaturization has been the key driving force behind Moore's law.[10] According to experts in microprocessor design, Dennard scaling ended in the 2000s, so power density no longer scales inversely with areal density.[24]

At the 1975 IEEE International Electron Devices Meeting, Moore revised the forecast rate.[6][46] Semiconductor complexity would continue to double annually until about 1980 after which it would decrease to a rate of doubling approximately every two years.[46] He outlined several contributing factors for this exponential behavior:[42][43]

- Die sizes were increasing at an exponential rate and as defective densities decreased, chip manufacturers could work with larger areas without losing reduction yields.
- Simultaneous evolution to finer minimum dimensions.
- What Moore called "circuit and device cleverness".
- The advent of metal-oxide-semiconductor (MOS) technology.

Shortly after 1975, Caltech professor Carver Mead popularized the term "Moore's law".[47][48]

Despite a popular misconception, Moore did not predict a doubling "every 18 months". Rather, David House, an Intel colleague, had factored in the increasing performance of transistors to conclude that integrated circuits would double in *performance* every 18 months.[49] Mathematically, Moore's Law predicted that transistor count would double every 2 years due to shrinking transistor dimensions, increased area and other improvements. As a consequence of shrinking dimensions, Dennard Scaling predicted that transistor frequency would rise exponentially. Combining these effects, David House deduced that computer chip performance would roughly double every 18 months. Also due to Dennard Scaling, this increased performance would not be accompanied by increased power i.e. the energy-efficiency of silicon-based computer chips roughly doubles every 18 months. Dennard scaling ended in the 2000s.[24] Much later, Koomey showed that a similar rate of efficiency improvement predated silicon chips and Moore's Law, covering technologies such as vacuum tubes used to build early computers.

Moore's law came to be widely accepted as a goal for the industry, and it was cited by competitive semiconductor manufacturers as they strove to increase processing power. Moore viewed his eponymous law as surprising and optimistic: "Moore's law is a violation of Murphy's law. Everything gets better and better."[50] The observation was even seen as a self-fulfilling prophecy.[14][51] However, the rate of improvement in physical dimensions known as Dennard scaling (MOSFET scaling) has come to an end for most semiconductor manufacturers in recent years, with much of the industry shifting, *circa* 2016, from using semiconductor scaling as a driver to more of a focus on meeting the needs of major computing applications.[14][52][24]

In April 2005, Intel offered US$10,000 to purchase a copy of the original *Electronics* issue in which Moore's article appeared.[53] An engineer living in the United Kingdom was the first to find a copy and offer it to Intel.[54]

In the late 2010s, only two semiconductor manufacturers have been able to produce semiconductor nodes that keep pace with Moore's law, TSMC[55] and Samsung Electronics, with 10 nm, 7 nm and 5 nm nodes in production (and plans for 3 nm nodes), whereas the pace has slowed down for Intel and other semiconductor manufacturers.[56][57][58]

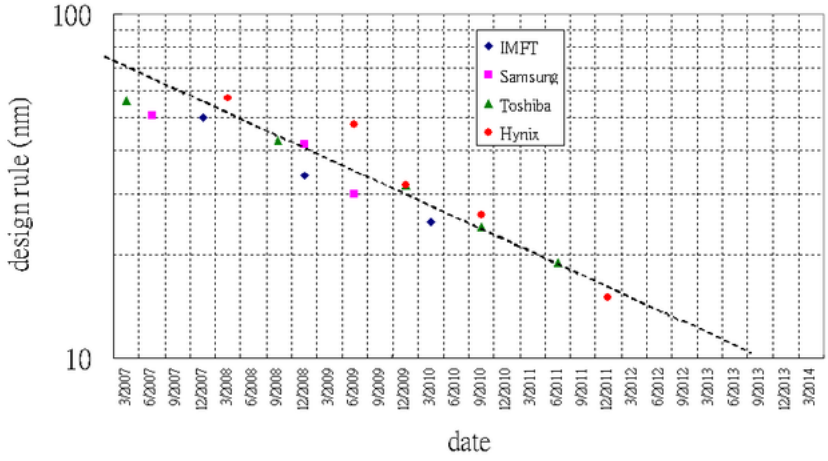
Moore's second law

As the cost of computer power to the consumer falls, the cost for producers to fulfill Moore's law follows an opposite trend: R&D, manufacturing, and test costs have increased steadily with each new generation of chips. Rising manufacturing costs are an important consideration for the sustaining of Moore's law.[59] This had led to the formulation of Moore's second law, also called Rock's law, which is that the capital cost of a semiconductor fab also increases exponentially over time.[60][61]

An Osborne Executive portable computer, from 1982, with a Zilog Z80 4 MHz CPU, and a 2007 Apple iPhone with a 412 MHz ARM11 CPU; the Executive weighs 100 times as much, is nearly 500 times the volume, costs approximately 10 times as much (adjusted for inflation), and has 1/103rd the clock frequency of the smartphone.

History of major enabling factors

Numerous innovations by scientists and engineers have sustained Moore's law since the beginning of the integrated circuit (IC) era. Some of the key innovations are listed below, as examples of breakthroughs that have advanced integrated circuit and semiconductor device fabrication technology, allowing transistor counts to grow by more than seven orders of magnitude in less than five decades.



The trend of MOSFET scaling for NAND flash memory allows the doubling of floating-gate MOSFET components manufactured in the same wafer area in less than 18 months.

- Integrated circuit (IC) – The *raison d'être* for Moore's law. The germanium hybrid IC was invented by Jack Kilby at Texas Instruments in 1958,[62] followed by the invention of the silicon monolithic IC chip by Robert Noyce at Fairchild Semiconductor in 1959,[63] which was enabled by Jean Hoerni's planar process (1959)[64] and Mohamed Atalla's silicon surface passivation process (1957).[65][66][67]
- MOSFET (metal–oxide–semiconductor field-effect transistor) – Also known as the MOS transistor, this is the key driving force behind Moore's law.[13][10] It was invented by Mohamed Atalla and Dawon Kahng at Bell Labs in 1959.[37] It was the first transistor that could be miniaturised and mass-produced for a wide range of uses,[38] due to high scalability (known as MOSFET scaling, or Dennard scaling),[11] making it possible to build high-density IC chips.[39] It is the most widely manufactured device in history, with an estimated total of 13 sextillion MOS transistors manufactured as of 2018.[68][69]
  - CMOS (complementary metal-oxide-semiconductor) – The CMOS process, a form of MOSFET fabrication, was invented by Chih-Tang Sah and Frank Wanlass at Fairchild Semiconductor in 1963.[70][71][72] A number of advances in CMOS technology by researchers in the semiconductor field since then have enabled the extremely dense and high-performance ICs that the industry makes today.

- Dynamic random-access memory (DRAM) – Bipolar DRAM was developed by Toshiba in 1965,[73][74] and then MOS DRAM was independently developed by Robert H. Dennard at IBM in 1967.[75] MOS DRAM made it possible to fabricate single-transistor memory cells on IC chips.
- Microprocessor – The first commercial single-chip microprocessor, the Intel 4004, released in 1971.[76] It was designed by Intel engineers Federico Faggin, Marcian Hoff, and Stan Mazor, and Busicom engineer Masatoshi Shima,[77] using Faggin's MOS silicon-gate technology (SGT).[78]
- Flash memory – Invented by Fujio Masuoka at Toshiba *circa* 1980,[79][80][81] using floating-gate MOSFET (FGMOS) technology.[82][83] This led to low-cost, high-capacity memory in diverse electronic products. NAND flash memory has since become the most rapidly scaling technology among electronic devices.
- 3D integrated circuit (3D IC) chip – Research and development (R&D) on 3D ICs was initiated in 1981 by the Research and Development Association for Future (New) Electron Devices in Japan,[84] and the earliest 3D IC to be fabricated was a CMOS chip by a Fujitsu research team led by S. Kawamura in 1983.[85]
- Multi-gate MOSFET (MuGET) and 3D transistor – A double-gate MOSFET was first demonstrated by Electrotechnical Laboratory researchers Toshihiro Sekigawa and Yutaka Hayashi in 1984,[86][87] and a non-planar double-gate 3D transistor by Digh Hisamoto's Hitachi team in 1989.[88][89] The FinFET (fin field-effect transistor) 3D transistor was developed by Hisamoto with a team of TSMC and UC Berkeley researchers, who achieved 17 nm fabrication in 1998 and 10 nm fabrication in 2002.[90]

- Chemically-amplified photoresist – Invented by Hiroshi Ito, C. Grant Willson and J. M. J. Fréchet at IBM *circa* 1980,[91][92][93] which was 5-10 times more sensitive to ultraviolet light.[94] IBM introduced chemically amplified photoresist for DRAM production in the mid-1980s.[95][96]
- Deep UV excimer laser photolithography – Invented by Kanti Jain[97] at IBM *circa* 1980.[98][99][100] Prior to this, excimer lasers had been mainly used as research devices since their development in the 1970s.[101][102] From a broader scientific perspective, the invention of excimer laser lithography has been highlighted as one of the major milestones in the 50-year history of the laser.[103][104]
- Interconnect innovations – Interconnect innovations of the late 1990s, including chemical-mechanical polishing or chemical mechanical planarization (CMP), trench isolation, and copper interconnects—although not directly a factor in creating smaller transistors—have enabled improved wafer yield, additional layers of metal wires, closer spacing of devices, and lower electrical resistance.[105][106][107]

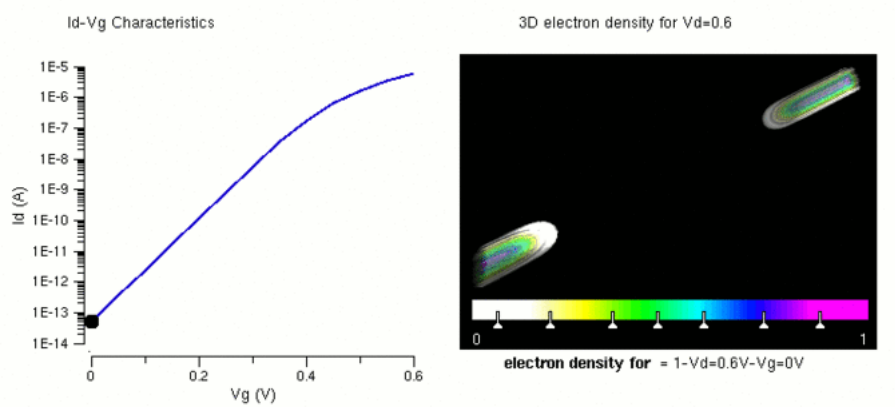
Computer industry technology road maps predicted in 2001 that Moore's law would continue for several generations of semiconductor chips. Depending on the doubling time used in the calculations, this could mean up to a hundredfold increase in transistor count per chip within a decade. The semiconductor industry technology roadmap used a three-year doubling time for microprocessors, leading to a tenfold increase in a decade.[108] Intel was reported in 2005 as stating that the downsizing of silicon chips with good economics could continue during the following decade,[note 1] and in 2008 as predicting the trend through 2029.[109]

Recent trends

One of the key challenges of engineering future nanoscale transistors is the design of gates. As device dimension shrinks, controlling the current flow in the thin channel becomes more difficult. Compared to FinFETs, which have gate dielectric on three sides of the channel, gate-all-around MOSFET (GAAFET) structure has even better gate control. By 2016, the smallest features in MOSFETs (metal-oxide-semiconductor field-effect transistors) had shrunk down to 10 nanometers.[110]

- A gate-all-around MOSFET was first demonstrated in 1988, by a Toshiba research team led by Fujio Masuoka, who demonstrated a vertical nanowire GAAFET which he called a "surrounding gate transistor" (SGT).[111][112] Masuoka, best known as the inventor of flash memory, later left Toshiba and founded Unisantis Electronics in 2004 to research surrounding-gate technology along with Tohoku University.[113]
- In 2006, a team of Korean researchers from the Korea Advanced Institute of Science and Technology (KAIST) and the National Nano Fab Center developed a 3 nm transistor, the world's smallest nanoelectronic device, based on FinFET technology.[114][115]

- In 2010, researchers at the Tyndall National Institute in Cork, Ireland announced a junctionless transistor. A control gate wrapped around a silicon nanowire can control the passage of electrons without the use of junctions or doping. They claim these may be produced at 10-nanometer scale using existing fabrication techniques.[116]



An atomistic simulation for electron density as gate voltage (Vg) varies in a nanowire MOSFET. The threshold voltage is around 0.45 V. Nanowire MOSFETs lie toward the end of the ITRS road map for scaling devices below 10 nm gate lengths. A FinFET has three sides of the channel covered by gate, while some nanowire transistors have gate-all-around (GAA) structure, providing better gate control.[108]

- In 2011, researchers at the University of Pittsburgh announced the development of a single-electron transistor, 1.5 nanometers in diameter, made out of oxide based materials. Three "wires" converge on a central "island" that can house one or two electrons. Electrons tunnel from one wire to another through the island. Conditions on the third wire result in distinct conductive properties including the ability of the transistor to act as a solid state memory.[117] Nanowire transistors could spur the creation of microscopic computers.[118][119][120]
- In 2012, a research team at the University of New South Wales announced the development of the first working transistor consisting of a single atom placed precisely in a silicon crystal (not just picked from a large sample of random transistors).[121] Moore's law predicted this milestone to be reached for ICs in the lab by 2020.
- In 2015, IBM demonstrated 7 nm node chips with silicon-germanium transistors produced using EUVL. The company believes this transistor density would be four times that of current 14 nm chips.[122]
- In 2020, Samsung Electronics plans to begin commercial production of a 5 nm process, using FinFET and EUV technology.[33]
- Samsung and TSMC have presented plans to manufacture 3 nm GAAFET nodes by 2021–2022.[123][124] Note that node names, such as 3 nm, have no relation to the physical size of device elements (transistors).
- A Toshiba research team including T. Imoto, M. Matsui and C. Takubo developed a "System Block Module" wafer bonding process for manufacturing 3D integrated circuit (3D IC) packages in 2001.[125][126] In April 2007, Toshiba introduced an eight-layer 3D IC, the 16 GB THGAM embedded NAND flash memory chip which was manufactured with eight stacked 2 GB NAND flash chips.[127] In September 2007, Hynix introduced 24-layer 3D IC, a 16 GB flash memory chip that was manufactured with 24 stacked NAND flash chips using a wafer bonding process.[128]
- V-NAND, also known as 3D NAND, allows flash memory cells to be stacked vertically using charge trap flash technology, significantly increasing the number of transistors on a flash memory chip. 3D NAND was first announced by Toshiba in 2007.[129] V-NAND was first commercially manufactured by Samsung Electronics in 2013.[130][131][132]
- In 2008, researchers at HP Labs announced a working memristor, a fourth basic passive circuit element whose existence only had been theorized previously. The memristor's unique properties permit the creation of smaller and better-performing electronic devices.[133]
- In 2014, bioengineers at Stanford University developed a circuit modeled on the human brain. Sixteen "Neurocore" chips simulate one million neurons and billions of synaptic connections, claimed to be 9,000 times faster as well as more energy efficient than a typical PC.[134]
- In 2015, Intel and Micron announced 3D XPoint, a non-volatile memory claimed to be significantly faster with similar density compared to NAND. Production scheduled to begin in 2016 was delayed until the second half of 2017.[135][136][137]

- In 2017, Samsung combined its V-NAND technology with eUFS 3D IC stacking to produce a 512 GB flash memory chip, with eight stacked 64-layer V-NAND dies.[138] In 2019, Samsung produced a 1 TB flash chip with eight stacked 96-layer V-NAND dies, along with quad-level cell (QLC) technology (4-bit per transistor),[139][140] equivalent to 2 trillion transistors, the highest transistor count of any IC chip.

While physical limits to transistor scaling such as source-to-drain leakage, limited gate metals, and limited options for channel material have been reached, new avenues for continued progress without physical scaling are open. The most promising of these approaches rely on using the spin state of electron spintronics, tunnel junctions, and advanced confinement of channel materials via nano-wire geometry. Available device choices shows that a wide range of device options is open for continuing Moore's law into the next few decades.[141] Spin-based logic and memory options are being developed actively in industrial labs,[142] as well as academic labs.[143]

Alternative materials research

The vast majority of current transistors on ICs are composed principally of doped silicon and its alloys. As silicon is fabricated into single nanometer transistors, short-channel effects adversely change desired material properties of silicon as a functional transistor. Below are several non-silicon substitutes in the fabrication of small nanometer transistors.

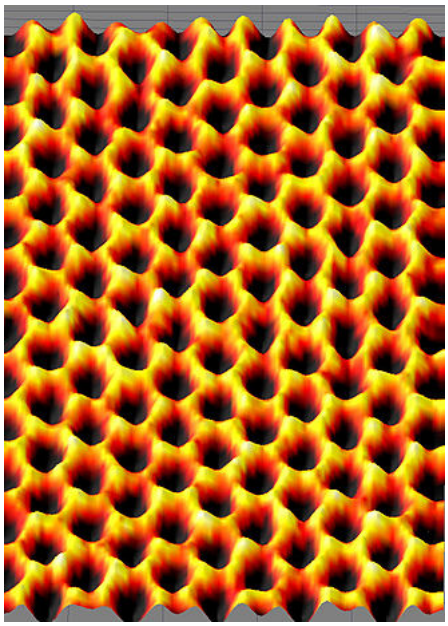
One proposed material is indium gallium arsenide, or InGaAs. Compared to their silicon and germanium counterparts, InGaAs transistors are more promising for future high-speed, low-power logic applications. Because of intrinsic characteristics of III-V compound semiconductors, quantum well and tunnel effect transistors based on InGaAs have been proposed as alternatives to more traditional MOSFET designs.

- In the early 2000s, the atomic layer deposition high-k film and pitch double-patterning processes were invented by Gurtej Singh Sandhu at Micron Technology, extending Moore's law for planar CMOS technology to 30 nm class and smaller.[88]
- In 2009, Intel announced the development of 80-nanometer InGaAs quantum well transistors. Quantum well devices contain a material sandwiched between two layers of material with a wider band gap. Despite being double the size of leading pure silicon transistors at the time, the company reported that they performed equally as well while consuming less power.[144]
- In 2011, researchers at Intel demonstrated 3-D tri-gate InGaAs transistors with improved leakage characteristics compared to traditional planar designs. The company claims that their design achieved the best electrostatics of any III-V compound semiconductor transistor.[145] At the 2015 International Solid-State Circuits Conference, Intel mentioned the use of III-V compounds based on such an architecture for their 7 nanometer node.[146][147]
- In 2011, researchers at the University of Texas at Austin developed an InGaAs tunneling field-effect transistors capable of higher operating currents than previous designs. The first III-V TFET designs were demonstrated in 2009 by a joint team from Cornell University and Pennsylvania State University.[148][149]
- In 2012, a team in MIT's Microsystems Technology Laboratories developed a 22 nm transistor based on InGaAs which, at the time, was the smallest non-silicon transistor ever built. The team used techniques currently used in silicon device fabrication and aims for better electrical performance and a reduction to 10-nanometer scale.[150]

Research is also showing how biological micro-cells are capable of impressive computational power while being energy efficient.[151]

Various forms of graphene are being studied for graphene electronics, e.g. Graphene nanoribbon transistors have shown great promise since its appearance in publications in 2008. (Bulk graphene has a band gap of zero and thus cannot be used in transistors because of its constant conductivity, an inability to turn off. The zigzag edges of the nanoribbons introduce localized energy states in the conduction and valence bands and thus a bandgap that enables switching when fabricated as a transistor. As an example, a typical GNR of width of 10 nm has a desirable bandgap energy of 0.4eV.[152][153]) More research will need to be performed, however, on sub 50 nm graphene layers, as its resistivity value increases and thus electron mobility decreases.[152]

Driving the future via an application focus



Scanning probe microscopy image of graphene in its hexagonal lattice structure

Most semiconductor industry forecasters, including Gordon Moore,[154] expect Moore's law will end by around 2025.[155][156][157]

In April 2005, Gordon Moore stated in an interview that the projection cannot be sustained indefinitely: "It can't continue forever. The nature of exponentials is that you push them out and eventually disaster happens." He also noted that transistors eventually would reach the limits of miniaturization at atomic levels:

> In terms of size [of transistors] you can see that we're approaching the size of atoms which is a fundamental barrier, but it'll be two or three generations before we get that far—but that's as far out as we've ever been able to see. We have another 10 to 20 years before we reach a fundamental limit. By then they'll be able to make bigger chips and have transistor budgets in the billions.[158]

In 2016 the International Technology Roadmap for Semiconductors, after using Moore's Law to drive the industry since 1998, produced its final roadmap. It no longer centered its research and development plan on Moore's law. Instead, it outlined what might be called the More than Moore strategy in which the needs of applications drive chip development, rather than a focus on semiconductor scaling. Application drivers range from smartphones to AI to data centers.[156]

A new initiative for a more generalized roadmapping was started through IEEE's initiative Rebooting Computing (http://rebootingcomputing.ieee.org/), named the International Roadmap for Devices and Systems (IRDS).[159]

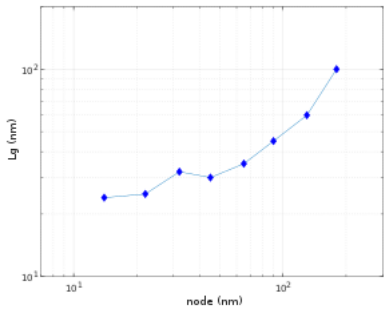
Consequences

Technological change is a combination of more and of better technology. A 2011 study in the journal *Science* showed that the peak of the rate of change of the world's capacity to compute information was in 1998, when the world's technological capacity to compute information on general-purpose computers grew at 88% per year.[160] Since then, technological change clearly has slowed. In recent times, every new year allowed humans to carry out roughly 60% more computation than possibly could have been executed by all existing general-purpose computers in the year before.[160] This still is exponential, but shows that the rate of technological change varies over time.[161]

The primary driving force of economic growth is the growth of productivity,[20] and Moore's law factors into productivity. Moore (1995) expected that "the rate of technological progress is going to be controlled from financial realities".[162] The reverse could and did occur around the late-1990s, however, with economists reporting that "Productivity growth is the key economic indicator of innovation."[21]

An acceleration in the rate of semiconductor progress contributed to a surge in U.S. productivity growth,[163][164][165] which reached 3.4% per year in 1997–2004, outpacing the 1.6% per year during both 1972–1996 and 2005–2013.[166] As economist Richard G. Anderson notes, "Numerous studies have traced the cause of the productivity acceleration to technological innovations in the production of semiconductors that sharply reduced the prices of such components and of the products that contain them (as well as expanding the capabilities of such products)."[167]

An alternative source of improved performance is in microarchitecture techniques exploiting the growth of available transistor count. Out-of-order execution and on-chip caching and prefetching reduce the memory latency bottleneck at the expense of using more transistors and increasing the processor complexity. These increases are described empirically by Pollack's Rule, which states that performance increases due to microarchitecture techniques approximate the square root of the complexity (number of transistors or the area) of a processor.



Intel transistor gate length trend – transistor scaling has slowed down significantly at advanced (smaller) nodes

For years, processor makers delivered increases in clock rates and instruction-level parallelism, so that single-threaded code executed faster on newer processors with no modification.[168] Now, to manage CPU power dissipation, processor makers favor multi-core chip designs, and software has to be written in a multi-threaded manner to take full advantage of the hardware. Many multi-threaded development paradigms introduce overhead, and will not see a linear increase in speed vs number of processors. This is particularly true while accessing shared or dependent resources, due to lock contention. This effect becomes more noticeable as the number of processors increases. There are cases where a roughly 45% increase in processor transistors has translated to roughly 10–20% increase in processing power.[169]

On the other hand, processor manufacturers are taking advantage of the 'extra space' that the transistor shrinkage provides to add specialized processing units to deal with features such as graphics, video, and cryptography. For one example, Intel's Parallel JavaScript extension not only adds support for multiple cores, but also for the other non-general processing features of their chips, as part of the migration in client side scripting toward HTML5.[170]

A negative implication of Moore's law is obsolescence, that is, as technologies continue to rapidly "improve", these improvements may be significant enough to render predecessor technologies obsolete rapidly. In situations in which security and survivability of hardware or data are paramount, or in which resources are limited, rapid obsolescence may pose obstacles to smooth or continued operations.[171]

Because of the toxic materials used in the production of modern computers, obsolescence, if not properly managed, may lead to harmful environmental impacts. On the other hand, obsolescence may sometimes be desirable to a company which can profit immensely from the regular purchase of what is often expensive new equipment instead of retaining one device for a longer period of time. Those in the industry are well aware of this, and may utilize planned obsolescence as a method of increasing profits.[172]

Moore's law has affected the performance of other technologies significantly: Michael S. Malone wrote of a Moore's War following the apparent success of shock and awe in the early days of the Iraq War. Progress in the development of guided weapons depends on electronic technology.[173] Improvements in circuit density and low-power operation associated with Moore's law also have contributed to the development of technologies including mobile telephones[174] and 3-D printing.[175]

Other formulations and similar observations

Several measures of digital technology are improving at exponential rates related to Moore's law, including the size, cost, density, and speed of components. Moore wrote only about the density of components, "a component being a transistor, resistor, diode or capacitor",[162] at minimum cost.

Transistors per integrated circuit – The most popular formulation is of the doubling of the number of transistors on integrated circuits every two years. At the end of the 1970s, Moore's law became known as the limit for the number of transistors on the most complex chips. The graph at the top shows this trend holds true today.

- As of 2017, the commercially available processor possessing the highest number of transistors is the 48 core Centriq with over 18 billion transistors.[176]

Density at minimum cost per transistor – This is the formulation given in Moore's 1965 paper.[3] It is not just about the density of transistors that can be achieved, but about the density of transistors at which the cost per transistor is the lowest.[177] As more transistors are put on a chip, the cost to make each transistor decreases, but the chance that the chip will not work due to a defect increases. In 1965, Moore examined the density of transistors at which cost is minimized, and observed that, as transistors were made smaller through advances in photolithography, this number would increase at "a rate of roughly a factor of two per year".[3]

Dennard scaling (MOSFET scaling) – This suggests that power requirements had been proportional to area (both voltage and current being proportional to length) for transistors. Combined with Moore's law, performance per watt would grow at roughly the same rate as transistor density, doubling every 1–2 years. According to Dennard scaling transistor dimensions would be scaled by 30% (0.7x) every technology generation, thus reducing their area by 50%. This would reduce the delay by 30% (0.7x) and therefore increase operating frequency by about 40% (1.4x). Finally, to keep electric field constant, voltage would be reduced by 30%, reducing energy by 65% and power (at 1.4x frequency) by 50%.[note 2] Therefore, in every technology generation transistor density would double, circuit becomes 40% faster, while power consumption (with twice the number of transistors) stays the same.[178] Dennnard scaling came to end in 2005–2010, due to device physics effects.[24]

The exponential processor transistor growth predicted by Moore does not always translate into exponentially greater practical CPU performance. Since around 2005–2007, Dennard scaling has ended, so even though Moore's law continued for several years after that, it has not yielded dividends in improved performance.[44][179] The primary reason cited for the breakdown is that at small sizes, current leakage poses greater challenges, and also causes the chip to heat up, which creates a threat of thermal runaway and therefore, further increases energy costs.[44][179][24]

The breakdown of Dennard scaling prompted a switch among some chip manufacturers to a greater focus on multicore processors, but the gains offered by switching to more cores are lower than the gains that would be achieved had Dennard scaling continued.[180][181] In another departure from Dennard scaling, Intel microprocessors adopted a non-planar tri-gate FinFET at 22 nm in 2012 that is faster and consumes less power than a conventional planar transistor.[182] The rate of performance improvement for single-core microprocessors has slowed significantly.[183] Single-core performance was improving by 52% per year in 1986–2003 and 23% per year in 2003–2011, but slowed to just seven percent per year in 2011–2018."[183]

Quality adjusted price of IT equipment – The price of information technology (IT), computers and peripheral equipment, adjusted for quality and inflation, declined 16% per year on average over the five decades from 1959 to 2009. [184][185] The pace accelerated, however, to 23% per year in 1995–1999 triggered by faster IT innovation,[21] and later, slowed to 2% per year in 2010–2013.[184][186]

The rate of quality-adjusted microprocessor price improvement likewise varies, and is not linear on a log scale. Microprocessor price improvement accelerated during the late 1990s, reaching 60% per year (halving every nine months) versus the typical 30% improvement rate (halving every two years) during the years earlier and later.[187][188] Laptop microprocessors in particular improved 25–35% per year in 2004–2010, and slowed to 15–25% per year in 2010–2013.[189]

The number of transistors per chip cannot explain quality-adjusted microprocessor prices fully.[187][190][191] Moore's 1995 paper does not limit Moore's law to strict linearity or to transistor count, "The definition of 'Moore's Law' has come to refer to almost anything related to the semiconductor industry that when plotted on semi-log paper approximates a straight line. I hesitate to review its origins and by doing so restrict its definition."[162]

Hard disk drive areal density – A similar observation (sometimes called Kryder's law) was made in 2005 for hard disk drive areal density.[192] Several decades of rapid progress in areal density advancement slowed significantly around 2010, because of noise related to smaller grain size of the disk media, thermal stability, and writability using

available magnetic fields.[193][194]

Fiber-optic capacity – The number of bits per second that can be sent down an optical fiber increases exponentially, faster than Moore's law. **Keck's law**, in honor of Donald Keck.[195]

Network capacity – According to Gerry/Gerald Butters,[196][197] the former head of Lucent's Optical Networking Group at Bell Labs, there is another version, called Butters' Law of Photonics,[198] a formulation that deliberately parallels Moore's law. Butters' law says that the amount of data coming out of an optical fiber is doubling every nine months.[199] Thus, the cost of transmitting a bit over an optical network decreases by half every nine months. The availability of wavelength-division multiplexing (sometimes called WDM) increased the capacity that could be placed on a single fiber by as much as a factor of 100. Optical networking and dense wavelength-division multiplexing (DWDM) is rapidly bringing down the cost of networking, and further progress seems assured. As a result, the wholesale price of data traffic collapsed in the dot-com bubble. Nielsen's Law says that the bandwidth available to users increases by 50% annually.[200]

Pixels per dollar – Similarly, Barry Hendy of Kodak Australia has plotted pixels per dollar as a basic measure of value for a digital camera, demonstrating the historical linearity (on a log scale) of this market and the opportunity to predict the future trend of digital camera price, LCD and LED screens, and resolution.[201][202][203]

The great Moore's law compensator (TGMLC), also known as Wirth's law – generally is referred to as software bloat and is the principle that successive generations of computer software increase in size and complexity, thereby offsetting the performance gains predicted by Moore's law. In a 2008 article in InfoWorld, Randall C. Kennedy,[204] formerly of Intel, introduces this term using successive versions of Microsoft Office between the year 2000 and 2007 as his premise. Despite the gains in computational performance during this time period according to Moore's law, Office 2007 performed the same task at half the speed on a prototypical year 2007 computer as compared to Office 2000 on a year 2000 computer.

Library expansion – was calculated in 1945 by Fremont Rider to double in capacity every 16 years, if sufficient space were made available.[205] He advocated replacing bulky, decaying printed works with miniaturized microform analog photographs, which could be duplicated on-demand for library patrons or other institutions. He did not foresee the digital technology that would follow decades later to replace analog microform with digital imaging, storage, and transmission media. Automated, potentially lossless digital technologies allowed vast increases in the rapidity of information growth in an era that now sometimes is called the Information Age.

Carlson curve – is a term coined by *The Economist*[206] to describe the biotechnological equivalent of Moore's law, and is named after author Rob Carlson.[207] Carlson accurately predicted that the doubling time of DNA sequencing technologies (measured by cost and performance) would be at least as fast as Moore's law.[208] Carlson Curves illustrate the rapid (in some cases hyperexponential) decreases in cost, and increases in performance, of a variety of technologies, including DNA sequencing, DNA synthesis, and a range of physical and computational tools used in protein expression and in determining protein structures.

Eroom's law – is a pharmaceutical drug development observation which was deliberately written as Moore's Law spelled backwards in order to contrast it with the exponential advancements of other forms of technology (such as transistors) over time. It states that the cost of developing a new drug roughly doubles every nine years.

Experience curve effects says that each doubling of the cumulative production of virtually any product or service is accompanied by an approximate constant percentage reduction in the unit cost. The acknowledged first documented qualitative description of this dates from 1885.[209][210] A power curve was used to describe this phenomenon in a 1936 discussion of the cost of airplanes.[211]

Edholm's law – Phil Edholm observed that the bandwidth of telecommunication networks (including the Internet) is doubling every 18 months.[212] The bandwidths of online communication networks has risen from bits per second to terabits per second. The rapid rise in online bandwidth is largely due to the same MOSFET scaling that enables

Moore's law, as telecommunications networks are built from MOSFETs.[213]

See also

- Accelerating change
- Beyond CMOS
- Ephemeralization
- List of eponymous laws
- List of laws § Technology
- Microprocessor chronology

Notes

1. The trend begins with the invention of the integrated circuit in 1958. See the graph on the bottom of page 3 of Moore's original presentation of the idea.[1]
2. Active power = CV^2f

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Further reading

- *Moore's Law: The Life of Gordon Moore, Silicon Valley's Quiet Revolutionary.* Arnold Thackray, David C. Brock, and Rachel Jones. New York: Basic Books, (May) 2015.
- *Understanding Moore's Law: Four Decades of Innovation.* Edited by David C. Brock. Philadelphia: Chemical Heritage Foundation, 2006. ISBN 0-941901-41-6. OCLC 66463488 (https://www.worldcat.org/oclc/66463488).
- Mody, Cyrus (December 2016). *The long arm of Moore's law : microelectronics and American science*. The MIT Press. ISBN 978-0262035491.

External links

- Intel press kit (http://www.intel.com/pressroom/kits/events/moores_law_40th/index.htm) – released for Moore's Law's 40th anniversary, with a 1965 sketch (ftp://download.intel.com/pressroom/images/events/moores_law_40th/Moores_Law_Original_Graph.jpg) by Moore
- The Lives and Death of Moore's Law (http://firstmonday.org/ojs/index.php/fm/article/view/1000/921) – by Ilkka Tuomi; a detailed study on Moore's Law and its historical evolution and its criticism (http://www.kurzweilai.net/meme/frame.html?main=/articles/art0593.html) by Kurzweil
- No Technology has been more disruptive... (http://www.slideshare.net/Christiansandstrom/no-technology-has-been-more-disruptive-presentation/) Slide show of microchip growth
- Intel (IA-32) CPU speeds 1994–2005 (http://wi-fizzle.com/compsci/) – speed increases in recent years have seemed to slow down with regard to percentage increase per year (available in PDF or PNG format)
- International Technology Roadmap for Semiconductors (ITRS) (https://web.archive.org/web/20151228041321/http://www.itrs.net/)
- Gordon Moore His Law and Integrated Circuit, Dream 2047 October 2006 (http://www.vigyanprasar.gov.in/dream/oct2006/English.pdf)
- A C|net FAQ about Moore's Law (https://archive.today/20130102082556/http://news.com.com/FAQ+Forty+years+of+Moores+Law/2100-1006_3-5647824.html?tag=nefd.lede) at Archive.today (archived 2013-01-02)
- ASML's 'Our Stories', Gordon Moore about Moore's Law, (https://www.youtube.com/watch?v=EzyJxAP6AQo)ASML Holding