MT612X RF Transceiver IC
Data Sheet

Table of contents

Introduction

1.1 Features

- **Receiver**
  - Very low IF architecture
  - Quad band differential input LNAs
  - Quadrature RF mixers
  - Fully integrated channel filter
  - More than 100 dB gain
  - More than 110 dB control range
  - Image-reject down conversion to baseband
- **Transmitter**
  - Precision IQ modulator
  - Translation loop architecture
  - Fully integrated wideband TX VCO
  - Fully integrated TX loop filter
- **Frequency Synthesizer**
  - Single integrated, fully programmable fractional-N synthesizer
  - Fully integrated wideband RF VCO
  - Fast settling time suitable for multi-slot GPRS application
- **Voltage Control Crystal Oscillator (VCXO)**
  - 26 MHz crystal oscillator capable of supporting 13 MHz / 26 MHz output clock
  - Programmable capacitor array for coarse tuning
  - Internal varactor for fine tuning
- **Regulators**
  - Built-in low-noise, low-dropout (LDO) regulators
- **Low power consumption**
- **QFN (Quad Flat Non-lead) Package 56-pin SMD**
- **3-wire serial interface**
- **MT612X is fabricated using a 0.35 μm BiCMOS process**

1.2 Applications

E-GSM 900 / DCS 1800 dual-band handsets
E-GSM 900 / PCS 1900 dual-band handsets
GSM 850 / PCS 1900 dual -band handsets
EGSM 900 / DCS 1800 / PCS 1900 triple-band handsets
GSM 850 / DCS 1800 / PCS 1900 triple-band handsets
GSM 850 / E-GSM 900 / DCS 1800 / PCS 1900 quad-band handsets

1.3 General Description

MT612X is a highly integrated RF transceiver IC for multi-band Global Systems for Mobile communication (GSM) and General Packet Radio Service (GPRS) cellular system applications. The MT612X includes four LNAs, two RF quadrature mixers, an integrated channel filter, programmable gain amplifiers (PGA), an IQ demodulator for the receiver, a precision IQ modulator with offset PLL for the transmitter, two internal TX VCOs, a VCXO, on-chip regulators, and a fully programmable sigma-delta fractional-N synthesizer with an on-chip RF VCO. The MT612X also includes control circuits to enable different operating modes. The device is housed in a 56-pin QFN SMD package with a downset paddle for additional grounding.

A functional block diagram of the MT612X and its pin assignment are shown in Figure 1.

1.4 MT612X Function Block Diagram

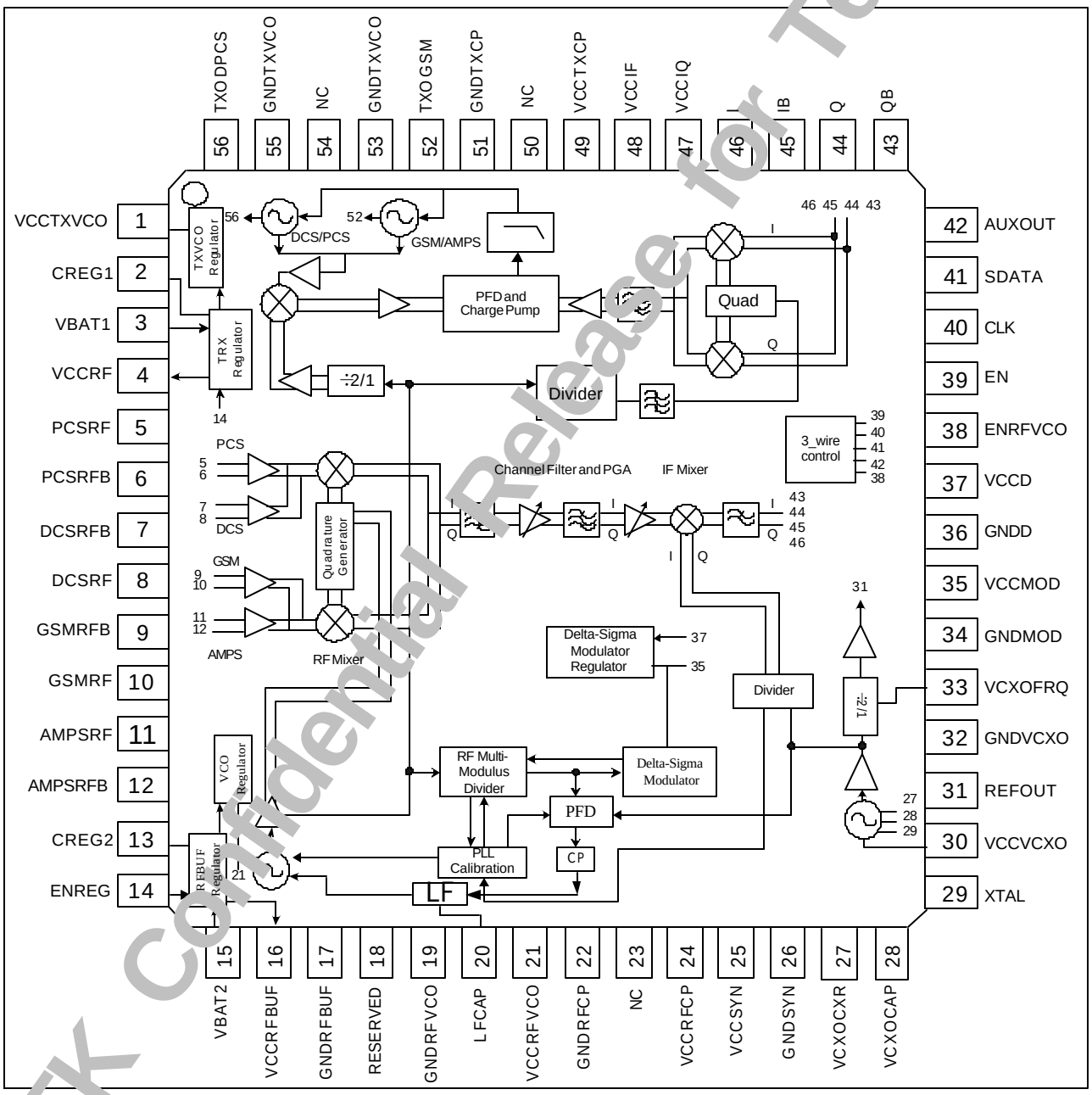

Figure 1 MT612X Function Block Diagram

1.5 Pin Description

Pin No.	Pin Name	Description
1	VCCTXVCO	TX VCO supply voltage and Regulator 1 (TX VCO) voltage output
2	CREG1	Regulator 1 external noise bypass capacitor
3	VBAT1	Battery supply for Regulator 1
4	VCCRF	TRX RF and TX BUF block supply voltage and Regulator 1 (TRX) voltage output
5	PCSRF	Receiver PCS 1900 RF differential positive input
6	PCSRFB	Receiver PCS 1900 RF differential negative input
7	DCSRFB	Receiver DCS 1800 RF differential negative input
8	DCSRF	Receiver DCS 1800 RF differential positive input
9	GSMRFB	Receiver E-GSM 900 RF differential negative input
10	GSMRF	Receiver E-GSM 900 RF differential positive input
11	AMPSRF	Receiver GSM 850 RF differential negative input
12	AMPSRFB	Receiver GSM 850 RF differential positive input
13	CREG2	Regulator 2 external noise bypass capacitor
14	ENREG	Regulator 1 & 2 enable input for TRX/ RFVCO buffer/ Synthesizer/VCXO
15	VBAT2	Battery supply for Regulator 2
16	VCCRFBUF	RF VCO buffer supply voltage and Regulator 2 (SX) voltage output
17	GNDRFBUF	RF VCO buffer ground
18	Reserved	Keep this pin floating
19	GNDRFVCO	RF VCO ground
20	LFCAP	Loop filter main capacitor input
21	VCCRFVCO	RF VCO supply voltage and Regulator 2 (RF VCO) voltage output
22	GNDRFCP	Synthesizer charge pump and PFD ground
23	NC	No connection
24	VCCRFCP	Synthesizer charge pump and PFD supply voltage
25	VCCSYN	Synthesizer supply voltage
26	GNDSYN	Synthesizer ground
27	VCXOCXR	VCXO internal / external output buffer control
28	VCXOCAP	VCXO coarse tuning capacitor and fine tuning varactor

29	XTAL	26 MHz crystal reference input
30	VCCVCXO	VCXO supply voltage
31	REFOUT	13 MHz / 26 MHz reference buffer output
32	GNDVCXO	VCXO ground
33	VCXOFRQ	Reference output buffer 13 MHz / 26 MHz selection
34	GNDMOD	Synthesizer Sigma-Delta modulator ground
35	VCCMOD	Synthesizer Sigma-Delta modulator supply voltage and Regulator 3 output
36	GNDD	3-wire digital circuit ground
37	VCCD	Supply voltage for 3 -wire digital circuit and supply voltage for Regulator 3
38	ENRFVCO	Regulator 2 enable input for RFVCO
39	EN	3-wire serial bus enable input
40	CLK	3-wire serial bus clock input
41	SDATA	3-wire serial bus data input
42	AUXOUT	Auxiliary test output
43	QB	Q path negative baseband input / output
44	Q	Q path positive baseband input / output
45	IB	I path negative baseband input / output
46	I	I path positive baseband input / output
47	VCCIQ	IF circuit supply voltage
48	VCCIF	Transmitter PFD and Receiver IF circuit supply voltage
49	VCCTXCP	Transmitter charge pump supply voltage
50	NC	No connection
51	GNDTXCP	Transmitter charge pump ground
52	TXOGSM	TX VCO buffer transmit output for GSM
53	GNDTXVCO	TX VCO ground
54	NC	No connection
55	GNDTXVCO	TX VCO ground
56	TXODPCS	TX VCO buffer transmit output for DCS/PCS

Table 1 MT612X Pin Description

2 Functional Description

2.1 Receiver

The receiver section of MT612X includes Quad-band low noise amplifiers (LNAs), RF quadrature mixers, an on-chip channel filter, Programmable Gain Amplifiers (PGAs), quadrature second mixers, and a final low-pass filter. The very low-IF MT612X uses image-rejection mixers and filters to eliminate interference. With accurate RF quadrature signal generation and mixer matching techniques, the image rejection of the MT612X can reach 35 dB for all bands. The fully integrated channel filters rejects interference, blocking signals, and images without any external components. Compared to a direct conversion receiver (DCR), MT612X' s very low-IF architecture improves the blocking rejection, AM suppression, as well as the adjacent channel interference performance. Moreover, the very low-IF architecture eliminates the need for complicated DC offset calibration that is necessary in a DCR architecture. In addition, the common-mode balance requirement of the SAW filter input is relaxed. The MT612X provides the analog IQ baseband output without any extra frequency conversion components.

The MT612X includes four differential LNAs for GSM 850 (869 MHz – 893 MHz), E-GSM 900 (925 MHz-960 MHz), DCS 1800 (1805 MHz-1880 MHz) and PCS 1900 (1930 MHz –1990 MHz). The differential inputs are matched to 200 Ω SAW filters using LC networks. The gain of the LNAs can be controlled either high or low for an additional 35 dB dynamic range control. Following the LNAs are the image-rejection quadrature RF mixers that down-convert the RF signal to the IF frequency. No external components are needed at the output of the RF mixers.

The IF signal is then filtered and amplified through an image-rejection filter and a PGA. The multi-stage PGA is implemented between filtering stages to control the gain of the receiver. With 2 dB gain steps, a 78 dB dynamic range of the PGA ensures a proper signal level for demodulation. The quadrature 2 nd mixers are provided on-chip to down convert IF signal to baseband in an analog differential IQ format.

2.2 Transmitter

The MT612X transmitter section consists of two on-chip TX VCOs, buffer amplifiers, a down-converting mixer, a quadrature modulator, an analog phase detector (PD) and a digital phase frequency detector (PFD), each with a charge pump output and on chip loop filter. The dividers and loop filters are used to achieve the desired IF frequency from the down-conversion mixer and quadrature modulator. For a given transmission channel, the transmitter will select one of the two different TX reference dividing numbers. These built-in components, along with an internal voltage controlled oscillator (TX VCO) and a loop filter, implement a translation loop modulator. The TX VCO output is fed to the power amplifier (PA). A control loop, implemented externally, is used to control the PA' s output power level.

2.3 TX VCO

Two power VCOs are integrated with OPLL to form a complete transmitter circuit. The TX VCO output power is typically 9 dBm with +/- 2.5dB variation in E-GSM900/ GSM850 bands and +8 dBm output power with +/- 2dB variation in DCS1800 / PCS1900 bands over extreme temperature conditions. Inside the chip, the VCO differential output signals are fed into the output buffer, the OPLL input feedback buffer, and the calibration circuit. The off chip signal is

transformed into a single ended output which needs impedance matching to 50 Ω to drive the power amplifier. Like RF VCO, the oscillation bandwidth is partitioned into 128 (or 64) sub-bands for DCS/ PCS (for E-GSM900/ GSM850) TX VCO to cover the process and temperature variation. Calibration process begins after a period of programmable time when the on chip TX VCO regulator is turned on. Total calibration time needs about 60us maximally and the frequency error after calibration is within +/-5 MHz. For Vtune=1.2 V, the variation of kvco is about 14% and 40% for GSM and DCS/PCS TX VCO, respectively, across the desired frequency range.

2.4 Frequency Synthesizer

2.4.1 Synthesizer System Description

The MT612X includes a frequency synthesizer with a fully integrated RF VCO to generate RX and TX local oscillator frequencies. The PLL locks the RF VCO to a precision reference frequency at 26 MHz. In order to reduce the inherent spur caused by fractional-N synthesizers, a 3rd-order sigma-delta modulator with dithering function is used to generate the prescaler divider number N. The prescaler is based on a multi-modulus architecture with programmable divider numbers ranging from 64 to 127. A conventional digital-type PFD with a charge pump is used for phase comparison in the PLL. By changing the output current of the charge pump, the phase detector gain can be programmed from 75/π μA/rad to 600/π μA/rad.

To reduce the acquisition time or to enable fast settling time for multi-slot data services such as GPRS, a digital loop (calibration loop) along with a fast-acquisition system are implemented in the synthesizer. Once the synthesizer is programmed, the RF VCO is pre-set to the vicinity of the desired frequency by a digital calibration loop. After the calibration, a fast-acquisition system is utilized for a period of time to facilitate fast locking. Once the acquisition is done, the PLL reverts back to the normal operation mode.

2.4.2 Synthesizer Frequency Programming for RX Mode

The frequency ranges of the synthesizer for RX mode are

RX mode	GSM 850	1737 MHz ~ 1788 MHz
	E-GSM900	1850 MHz ~ 1920 MHz
	DCS 1800	1805 MHz ~ 1880 MHz
	PCS 1900	1930 MHz ~ 1990 MHz.

And the divider number N can be decided by the following procedure.

1. Calculate LO frequency f_{VCO} from RX channel frequency f_{CH}

   $f_{VCO} = 2 * f_{CH} - 200k$ for GSM 850 and E-GSM 900

   $f_{VCO} = f_{CH} - 100k$ for DCS 1800 and PCS 1900

2. Calculate N_{int} and N_{frac}

   $N = 64 + N_{int} + N_{frac}/5200 = f_{VCO}/26M$ N_{int} and N_{frac} are integers

   $0 \le N_{frac} < 5200$

3. Use the binary equivalents of N_{int} and N_{frac} to program registers CW1-N_INT and CW1 -N_FRA.

2.4.3 Synthesizer Frequency Programming for TX Mode

The frequency ranges of the synthesizer for TX mode are

TX mode	GSM850	1813 MHz ~ 1868 MHz
	EGSM900	1936 MHz ~ 2059 MHz
	DCS1800	1881 MHz ~ 2008 MHz
	PCS1900	2035 MHz ~ 2149 MHz

And the divider number N can be decided by the following procedure.

1. Set the divider ratio D1 of TX reference divider = 11
2. Calculate LO frequency f_{VCO} from TX channel frequency f_{CH}

   $f_{VCO} = 2 * D1 * f_{CH} / (D1-1)$ for GSM850 and E GSM900

   $f_{VCO} = D1 * f_{CH} / (D1-1)$ for DCS1800 and PCS1900
3. Calculate N_{int} and N_{frac}

   $N = 64 + N_{int} + N_{frac}/5200 = f_{VCO}/26M$ N_{int} and N_{frac} are integers

   $0 \le N_{frac} < 5200$
4. If $N_{fra} < 400$ or $N_{fra} > 4800$, re-set D1 = 9 and repeat Step 2 and 3 to get new N_{int} and N_{frac}.
5. Use the binary equivalents of N_{int} and N_{frac} to program registers CW1-N_INT and CW1 -N_FRA.

2.4.4 Digital Calibration Loop

The MT612X uses a digital calibration technique to reduce the PLL settling time. Once the RF synthesizer is programmed through a 3-wire serial interface, the calibration loop is activated. The main function of the calibration loop is to preset the RF VCO to the vicinity of the desired frequency quickly and correctly, thus aiding the PLL to settle faster. On the other hand, since a large portion of initial frequency error is dealt with by the integrated calibration loop, the overall locking time can be drastically reduced, irrespective of the desired frequency.

2.4.5 Fast-Acquisition System

After the digital calibration loop presets the RFVCO, the RF synthesizer reverts to the PLL operation and a fast-acquisition system is activated. For faster settling, the charge pump current is set to a higher current than normal setting for a period of time, typically, 20 µs or 60 µs.

2.5 Voltage Control Crystal Oscillator

Voltage Control Crystal Oscillator (VCXO) consists of an amplifier, a buffer, and a programmable capacitor array. The VCXO provides the MT612X with a selectable reference frequency of either 13 MHz or 26 MHz.

The amplifier is designed to be in series resonance with a standard 26 MHz crystal. The crystal is connected from the input pin XTAL of amplifier to ground through a series load capacitance. The buffer provides a typical 600 mVpp voltage swing at either 13 MHz or 26 MHz. It is designed to drive a tuned load to improve harmonic contents and reduce the oscillator current consumption. The capacitor array, from 0.0625 pF to 4 pF in steps of 0.0625 pF, is used to shunt the series load capacitor for coarse tuning and remove any fixed offsets due to crystal manufacturing variations. An internal varactor that provides fine tuning combines with the capacitor array. As an alternative, the reference frequency can be provided by an external 26 MHz VCTCXO module. When pin VCXOCXR is tied to the VCCVCXO supply, the XTAL pin will accept an external signal. Furthermore, the VCXO control pin can be tied to VCCVCXO to prevent the current leakage during the sleep mode operation.

2.6 Regulator

The MT612X internal regulators provide low noise, stable, temperature and process independent supply voltages to critical blocks in the transceiver. An internal P-channel MOSFET pass transistor is used to achieve a low dropout (LDO) voltage of less than 150 mV in all regulators.

3 MT612X Hardware Control Pin Descriptions

A description of MT612X hardware control pins and their functionality are shown in the table below.

MT612X has an internal VCXO and its control.

Name	Setting	Description
ENREG	0	Power off Regulator1 and 2
	1	Power on Regulator 1 and 2
ENRFVCO	0	Power off RFVCO
	1	Power on RFVCO
VCXOCXR	0	Select internal VCXO
	1	Select external TCVCXO Note: Connect to VCCVCXO
VCXOFRQ	0	Reference output buffer 13 MHz
	1	Reference output buffer 26 MHz Note: Connect to VCCVCXO

Table 2 Hardware Control Pin Description

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Prolonged exposure to absolute maximum ratings may reduce device reliability. Functional operation at these maximum ratings is not implied.

Item	Symbol	Min.	Max.	Unit
Power supply voltage (VBAT)	VBAT	-0.3	5.5	V
Pin voltage	V_T	-0.3	VBAT+0.3(4.0max)	V
Maximum power dissipation	P_T		529	mW
Operating temperature	T_{opr}	-20	80	°C
Storage temperature	T_{stg}	-55	125	°C

Table 3 Absolute Maximum Ratings

4.2 Recommended Operating Range

Item	Symbol	Min.	Typ.	Max	Unit
Power supply voltage (VBAT)	VBAT	3.1	3.6	4.6	V
Power supply voltage (VCCD)	VCCD	2.5	2.8	3.1	V
Operating ambient temperature	T_{opr}	-20	25	75	°C

Table 4 Recommended Operating Range

4.3 DC Specifications

VBAT = 3.6 V, VCCD = 2.8 V, Ta = 25 °C unless otherwise specified.

Item	Mode	Test condition	Min.	Typ.	Max.	Unit
Power supply voltage (VBAT)	ALL[1]		3.1	3.6	4.6	V
Power supply voltage (VCCD)	ALL		2.5	2.8	3.1	V
Power supply current (RX)	ALL			68		mA
Power supply current (TX)	GSM850			116		mA
	GSM900			116		mA
	DCS			100		mA
	PCS			100		mA
Power supply current (Warm-up)	ALL	Including VCXO		33		mA
Power supply current (Standby)	ALL	2 regulators + internal RFVCO + VCXO		11.9		mA
Power supply current (VCXO)	ALL	Regulator 2 + VCXO		3.1		mA
Saving mode power supply current (Sleep)	ALL	ENREG = 0 V, SDATA = 0 V, CLK = 0 V, EN = 0 V		1.0		µA
Serial data VH (CLK, SDATA, EN)	ALL	VCCD = 2.8 V	2.5			V
Serial data VL (CLK, SDATA, EN)	ALL	VCCD = 2.8 V			0.3	V
Control pin VH (ENREG)	ALL		2.5			V
Control pin VL (ENREG)	ALL				0.3	V
Control pin VH (ENRFVCO)	ALL		2.5			V
Control pin VL (ENRFVCO)	ALL				0.3	V
IQ common mode DC output voltage	ALL	Receiver output DC	0.95	1.1	1.25	V
IQ common mode DC input voltage	ALL	Transmitter input DC		1.2		V

Table 5 DC specification

[1] ALL mode is GSM850 / E-GSM900 / DCS1800 / PCS1900 mode

5 Receiver Specifications

VBAT = 3.6 V, VCCD = 2.8 V, Ta = 25 °C unless otherwise specified.

Item	Mode	Test condition	Min	Typ	Max	unit
Receiver input frequency	GSM850		869		894	MHz
	GSM900		925		960	MHz
	DCS		1805		1880	MHz
	PCS		1930		1990	MHz
Receiver max differential voltage gain	GSM850	LNA = high gain RF = 882 MHz PGA = 78 dB	102	104	106	dB
	GSM900	LNA = high gain RF = 940 MHz PGA = 78 dB	103	105	107	dB
	DCS	LNA = high gain RF = 1842 MHz PGA = 78 dB	101	103	105	dB
	PCS	LNA = high gain RF = 1960 MHz PGA = 78 dB	100	102	104	dB
LNA differential input impedance	GSM850	Zin, RF = 882 MHz		71-j73 (146// 1.2 pF)		O
	GSM900	Zin, RF = 945 MHz		71-j73 (146// 1.2 pF)		O
	DCS	Zin, RF = 1842 MHz		33-j85 (252// 885 fF)		O
	PCS	Zin, RF = 1960 MHz		37-j81 (214// 830 fF)		O
Front-end LNA gain difference	GSM850	LNA = high gain to low gain RF = 882 MHz	37	39	41	dB
	GSM900	LNA = high gain to low gain RF = 940 MHz	37	39	41	dB
	DCS	LNA = high gain to low gain RF = 1842 MHz	37	39	41	dB

	PCS	LNA = high gain to low gain RF = 1960 MHz	37	39	41	dB
Receiver gain variation over temperature	ALL	-20 to 70 °C All gain settings			3.5	dB

2nd order input intercept point	GSM850		30	45		dBm
	GSM900		30	45		dBm
	DCS		22	28		dBm
	PCS		22	28		dBm
High gain 3rd order input intercept point	GSM850		-14	-12		dBm
	GSM900		-15	-13		dBm
	DCS		-14	-12		dBm
	PCS		-14	-11		dBm
Receiver noise figure	GSM850	LNA = high gain		4	5	dB
	GSM900			3.5	4.5	dB
	DCS			4.5	6.5	dB
	PCS			4.5	6.5	dB
	GSM850	LNA = low gain PGA=78 dB Note 3.		37	39	dB
	GSM900			37	39	dB
	DCS			40	42	dB
	PCS			40	42	dB
Receiver S/N with 3 MHz blocker	GSM850	Blocker= –23 dBm.	9	12		dB
	GSM900		9	12		dB
	DCS		9	11		dB
	PCS		9	11		dB
Receiver image rejection ratio	GSM850		30	40		dB
	GSM900		30	40		dB
	DCS		30	33		dB
	PCS		30	33		dB
Receiver channel response attenuation	ALL	@ +/-200 kHz offset	+17			dB
		@ +/-400 kHz offset	+40			dB
		@ +/-600 kHz offset	+62			dB
		@ +/-1.6 MHz offset	+80			dB
		@ +/-3.2 MHz offset	100			dB
Receiver group delay variation	ALL	For all gain settings 0-67.7 kHz		1.6	2	dB
Receiver channel filter 3 -dB BW	ALL	For all gain settings	90		130	kHz

PGA gain linearity	ALL	In any 20 dB setting		0.5	1	dB
		For all gain settings		0.8	1.5	dB
PGA gain step	ALL		1.75	2	2.25	dB
PGA dynamic range	ALL	PGA = 0 dB to 78 dB	77	78		dB
Receiver dynamic range	ALL		110			dB
Output DC offset voltage	ALL	For all gain settings		10	25	mV
2nd LO leakage	ALL	For all gain settings I+jQ measurement		6	11.3	mVrms
PGA gain setting transient time	ALL	+-30 dB Gain setting			25	µSec
IQ maximum output swing	ALL	For all gain settings	1.4	1.5		V_{p-p}
IQ common mode output voltage	ALL	For all gain settings	0.9	1.05	1.2	V

Table 6 AC Specification of Receiver

6 Transmitter Specifications

VBAT = 3.6 V, VCCD = 2.8 V, Ta = 25 °C unless otherwise specified.

Item	Mode	TestConditions	Min.	Typ.	Max.	Unit
Frequency(RF)	GSM850		824		849	MHz
	GSM900		880		915	MHz
	DCS		1710		1785	MHz
	PCS		1850		1910	MHz
Phaseaccuracy	ALL	RMS value, 200 kHz BW		1.5	3	degree
		Peak value, 200 kHz BW		3.0	9	degree
Carrier suppression ratio	ALL	All ‘ 1’ GMSK (Differential encode: off) (baseband frequency = 67.7 kHz) IQ input swing = 0.5 Vp-p IQ common mode input voltage = 1.2 V	30	40		dBc
Side-band suppression ratio			35	40		dBc
IM3attenuation			50	55		dBc
Averagemodulation spectrum	ALL	200 kHz offset (30 kHz bandwidth)		-36	-34	dBc
	GSM850/ GSM900	400 kHz offset (30 kHz bandwidth)		-66	-64	dBc
	DCS			-65	-63	
	PCS			-64	-63	
	ALL	600 kHz offset (30 kHz bandwidth)		-68	-65	dBc
	ALL	1.2 MHz to 1.8 MHz offset (30 kHz bandwidth)		-72		dBc
	ALL	1.8 MHz to 3 MHz offset (100 kHz bandwidth)		-73.5		dBc
	ALL	3 MHz to 6 MHz offset (100 kHz bandwidth)		-77		dBc
	ALL	6 MHz upward offset (100 kHz bandwidth)		-77		dBc
TX noise in RX band	GSM850	925 MHz to 935 MHz 10 MHz up from TX band			-156	dBc/Hz
	GSM900	935 MHz to 960 MHz 20 MHz up from TX band			-162	dBc/Hz

	DCS	1805 MHz to 1880 MHz 20 MHz up from TX band			-154	dBc/Hz
	PCS	1930 MHz to 1990 MHz 20 MHz up from TX band			-154	dBc/Hz
IQ input swing	ALL	Single ended	0.4	0.5	0.6	Vp-p
IQ common mode input voltage	ALL		1.0	1.2	1.4	V
Lock up time	ALL			20		µSec

Table 7 AC Specification of OPLL

7 Specification for TX VCO and Buffer

VBAT = 3.6 V, VCCD = 2.8 V, Ta = 25 °C unless otherwise specified.

Item	Mode	Test condition	Min.	Typ.	Max.	Unit
Frequency range	GSM850		824		849	MHz
	GSM900		824		915	
	DCS		1710		1785	
	PCS		1850		1910	
Phase noise	GSM850/ GSM900	@ 400 kHz offset			-120	dBc/Hz
		@ 20 MHz offset			-162	
	DCS/PCS	@ 400 kHz offset			-120	
		@ 20 MHz offset			-154	
Tuning sensitivity (K_{vco})	GSM850/ GSM900	Vtune = 1.2 V	11.2		15.6	MHz/V
	DCS/PCS		10.1		13.9	
Tuning sensitivity variation	GSM850/ GSM900	All channels, all Vtune	8		19.2	MHz/V
	DCS/PCS		7.9		16.1	
Pulling figure	ALL	VSWR = 2:1 for all phase			2.5	MHz
Pushing figure	ALL	VBAT = 2.8 ± 0.1 V			1	MHz
Output power level	GSM	R_{load} = 50 Ω	7.5	9.5	11.5	dBm
	DCS/PCS		7	8.5	10	
Output harmonics	ALL				-30	dBc

Table 8 Specification of TX VCO and Buffer

8 Frequency Synthesizer Specifications

VBAT = 3.6 V, VCCD = 2.8 V, Ta = 25 °C unless otherwise specified.

Item	Mode	Test condition	Min.	Typ.	Max.	Unit
Frequency range	ALL		1738		2150	MHz
Reference frequency	ALL			26		MHz
Frequency step resolution	ALL			5		kHz
Phase detector gain	ALL	CW0-SYNCP[2] = 00		75/π		µA /rad
		CW0-SYNCP = 01		150/π		
		CW0-SYNCP = 10		300/π		
		CW0-SYNCP = 11		600/π		
Phase detector sink versus source mismatch	ALL	V_{CPO} = VCCRFCP/2		5		%
Phase detector gain versus voltage	ALL	0.4 < V_{CPO} < VCCRFCP – 0.4		10		%
In-band phase noise	ALL	@10 kHz offset		-85		dBc /Hz
Phase noise	ALL	@400 kHz offset		-118		dBc /Hz
		@3 MHz offset		-138		
Calibration time	ALL			32		µs
Spurious performance	GSM850/ GSM900 RX	@200 kHz offset		-37		dBc
		@600 kHz offset		-61		
		@1.6 MHz offset		-77		
		@ >3MHz offset		-87		
	DCS/PCS RX	@100 kHz offset		-25		
		@300 kHz offset		-49		
		@500 kHz offset		-58		
		@700 kHz offset		-64		
		@1.5 MHz offset		-70		
		@> 2.9 MHz offset		-84		
	TX	@1.6 MHz offset		-82		
		@> 3 MHz offset		-92		
Lock time	ALL	Frequency error < 1 kHz			200	µs
Varactor tuning voltage range	ALL		0.4		2.4	V

[2] Please refer to MT612X 3-wire programming guide - control word register part descriptions

K_{vco} variation for Vtune 0.4 ~1.6 V	ALL	1738 MHz < f_{vco} < 1872 MHz	6		18	MHz /V
		1872 MHz < f_{vco} < 1950 MHz	7		20	
		1950 MHz < f_{vco} < 2054 MHz	8		24	
		2054 MHz < f_{vco} < 2129 MHz	9		27	
RFVCO Pulling figure	ALL	VSWR = 2:1 for all phase			1	MHz
RFVCO Pushing figure	ALL	VBAT = 3.1~ 3.6 V			1	MHz
RFVCO long time frequency drift	ALL	60ms after digital calibration is finished, under, temperature –20 ℃ ~ 65 ℃			3	MHz

Table 9 Specifications of RF Frequency Synthesizer

9 Voltage Control Crystal Oscillator (VCXO) Specifications

VBAT = 3.6 V, VCCD = 2.8 V, Ta = 25 °C unless otherwise specified.

Item	Test condition	Min.	Typ.	Max.	Unit
Operating frequency	Internal resonance (crystal Cload = 9.5 pF / Res = 35 O max.) / external Input		26		MHz
Output frequency	Baseband clock, VCXOFRQ = 0		13		MHz
	Baseband clock, VCXOFRQ = 1		26		MHz
Switched capacitor value	6 bits switch control from 0 to 63	0.0625		4	pF
Switched capacitor step			0.0625		pF
Varactor	Vbias=0 V		10		pF
	Vbias=3 V		5		pF
Buffer output level	13 MHz baseband clock (Load = 148 - j1206 O@ Frequency = 13 MHz)	400	600		mVpp
	26 MHz baseband clock (Load = 37 - j610 O@ Frequency = 26 MHz)				
Duty cycle	13 MHz / 26 MHz baseband clock	45		55	%
Buffer output 2 nd harmonic	Load = 20 pF		-20	-5	dBc
Buffer output 3 rd harmonic	Load = 20 pF		-10	-5	dBc
Input level	AC coupled by external 26 MHz	0.2		1	Vpp
Input resistance	Shunt by external 26 MHz clock	5	7.5		kO
Input capacitance	Shunt by external 26 MHz clock		5	10	pF
Start-up time	Including Regulator 2 power on time by ENREG pull high			5	ms

Table 10 Specification of VCXO

10 Regulator Specifications

V_{IN} = 3.6 V, Ta = 25 °C, C_{out} = 2.2 µF, C_{bp} = 0.1 µF

Item	Test condition	Min.	Typ.	Max.	Unit
Input voltage		3.1	3.6	4.6	V
Output voltage		2.7	2.8	2.9	V
Dropout voltage	V_{in}-V_{out} when V_{out} = ($V_{out, nominal}$-100 mV)			150	mV
Line regulation	V_{in} = 3.1 V to 4.6 V			10	mV
Load regulation	I_{out} = 1 mA to I_{max}			10	mV
Output voltage noise	Frequency = 10 Hz to 100 kHz		30	60	μV_{rms}
Power supply ripple rejection	Frequency = 216.7 Hz	50	60		dB
Temperature coefficient	V_{in} = 3.6 V, TC = ?V_{OUT}/[$V_{out, nominal}$*?T], ?T = 80-(-20)=100 ℃		50		ppm/° C
Turn-on time of regulator	V_{out} step from 0 to $V_{out, nominal}$ ± 4 %		20	40	µSec

Table 11 Specification of Regulator

11 OrderInformation

Part Number	Band specification	Note
MT6120	Quad-band	GSM850/GSM900/DCS1800/PCS1900
MT6126	Dual-band	GSM 850//PCS1900
MT6127	Tri-band	GSM850/DCS1800/PCS1900
MT6128	Dual-band	GSM900/DCS1800
MT6129	Tri-band	GSM900/DCS1800/PCS1900

12 Package Dimensions

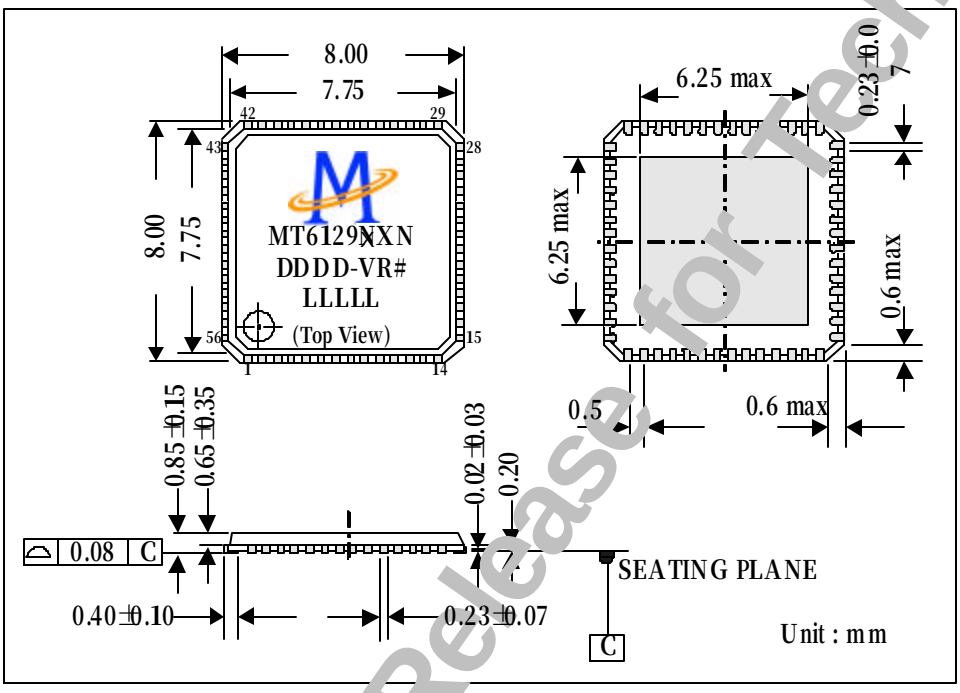

Figure 2 Package dimension

13 Footprint Dimension

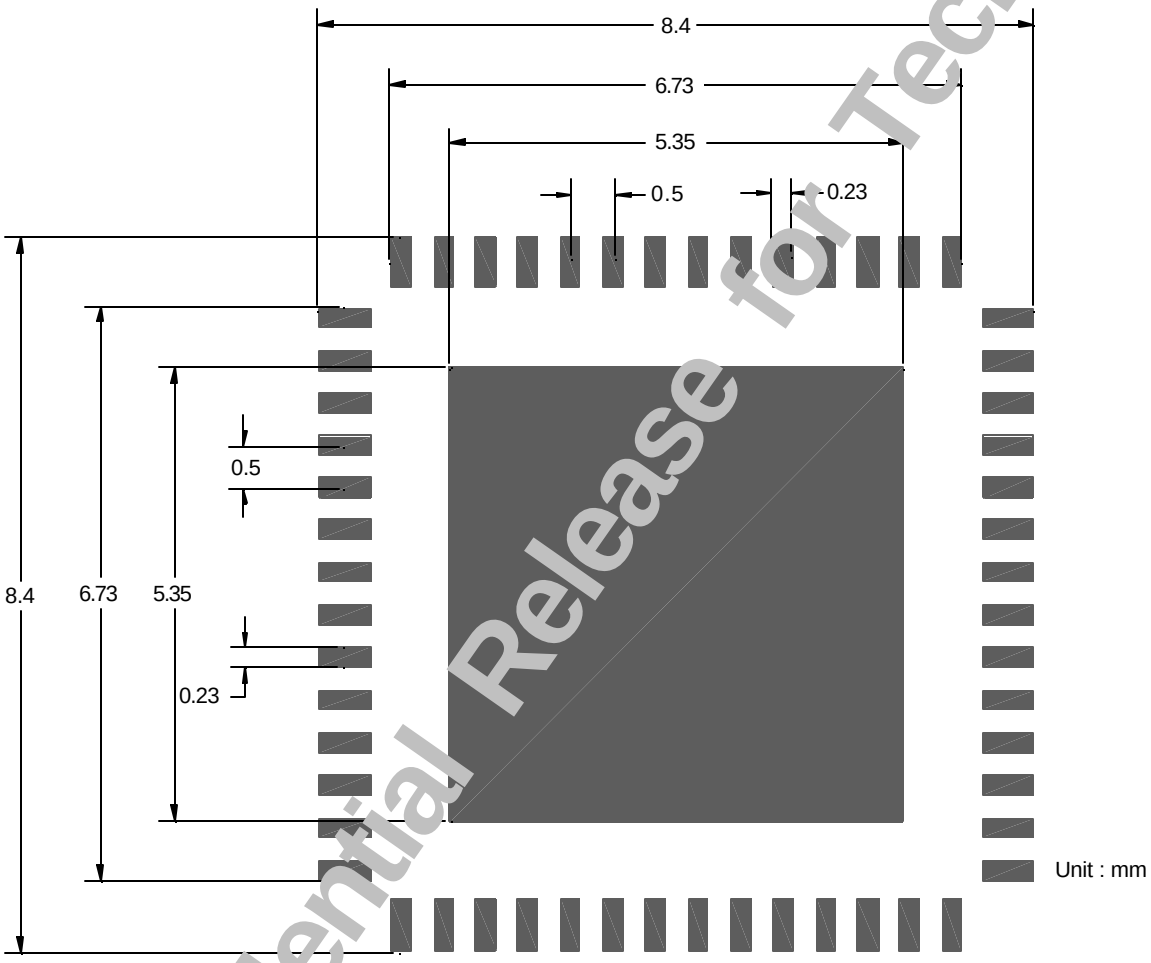

Figure 3 QFN-56 Footprint Dimensions

14 ReferenceApplicationCircuit

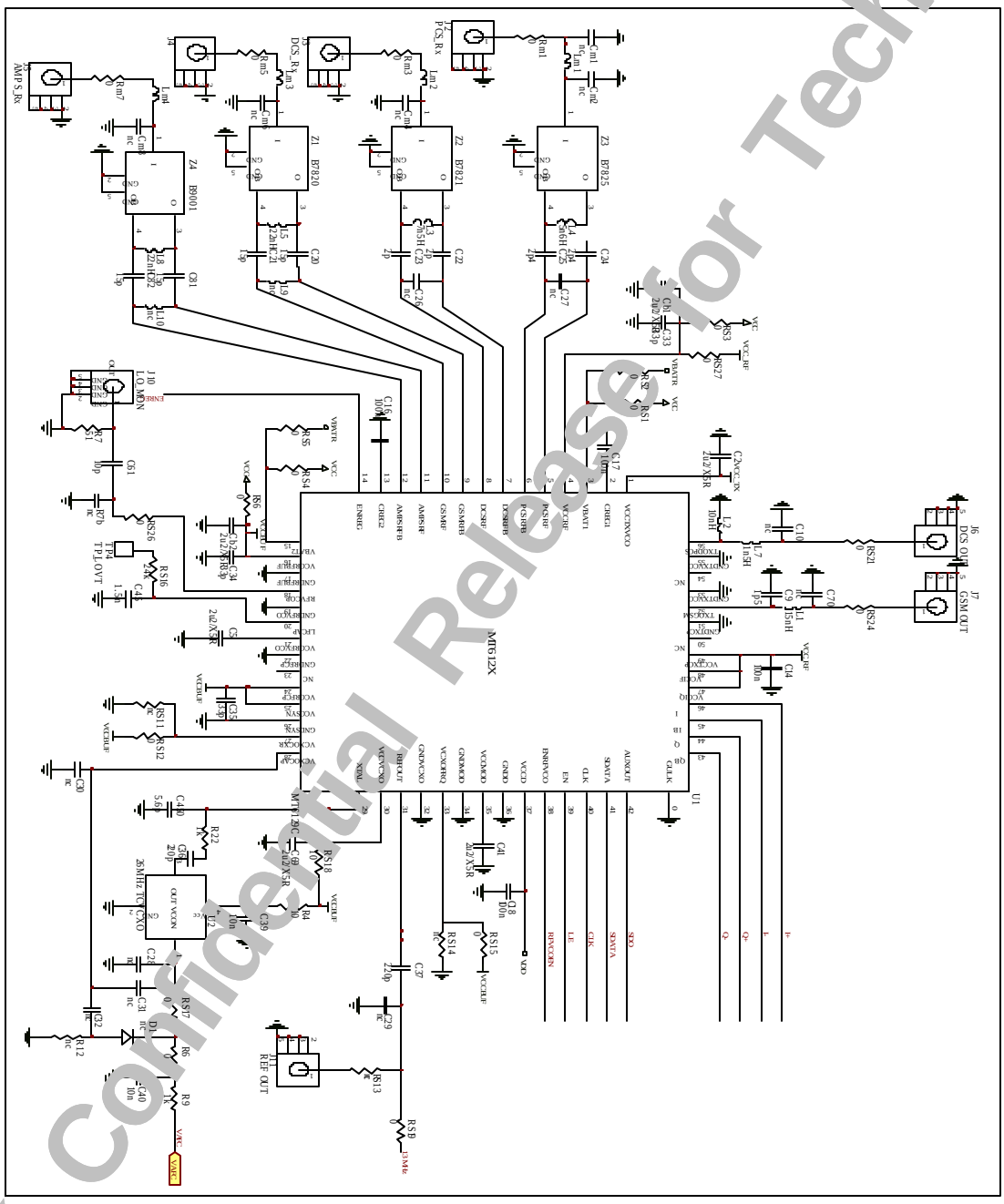

Figure 4 MT612XReferenceApplicationcircuit