MT6189 Application Notes

MediaTek Inc.

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21 December 2005

V2.4

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1. Introduction

1.1 Features

- Fully integrated single-chip for FM radio
- Cover EURO/US/Japan FM bands
- Low power consumption 9mA
- Power supply 2.5V~3.6V
- I^2C/3-wire serial interface
- Internal RF AGC control circuit
- Power down mode
- Fully integrated FM demodulator
- Fully integrated channel filter and limiter
- Signal dependent stereo blend and soft mute
- High cut control
- Adjust-free stereo decoder
- Stereo audio outputs for audio amplifiers
- Fewer external components
- No manually tunable parts required
- 10-bit IF counter
- 4-bit RSSI register
- High SNR
- High sensitivity
- Low distortion
- Integrated VCO circuit with only one external inductor
- Operates with a standard 32.768kHz crystal or externally applied 32.768k/13/26MHz clock
- Small 6x6 mm^2 40-pin QFN Package

1.2 Applications

Flash MP3, Cell Phone, Portable Radio.

1.3 General Descriptions

MT6189 is a highly integrated FM radio IC for low power portable devices. The radio can tune the EURO/US/Japan FM bands. The MT6189 includes LNA and mixer with AGC, integrated channel filter, limiter amplifier, 4bit RSSI indicator, IF counter, FM demodulator, stereo decoder, and an integrated VCO with only one off-chip inductor. The MT6189 includes control circuits to implement different operating modes. The device is housed in a small size 40-pin QFN SMD package.

A functional block diagram of the MT6189 and its pin assignment is shown in Figure 1.

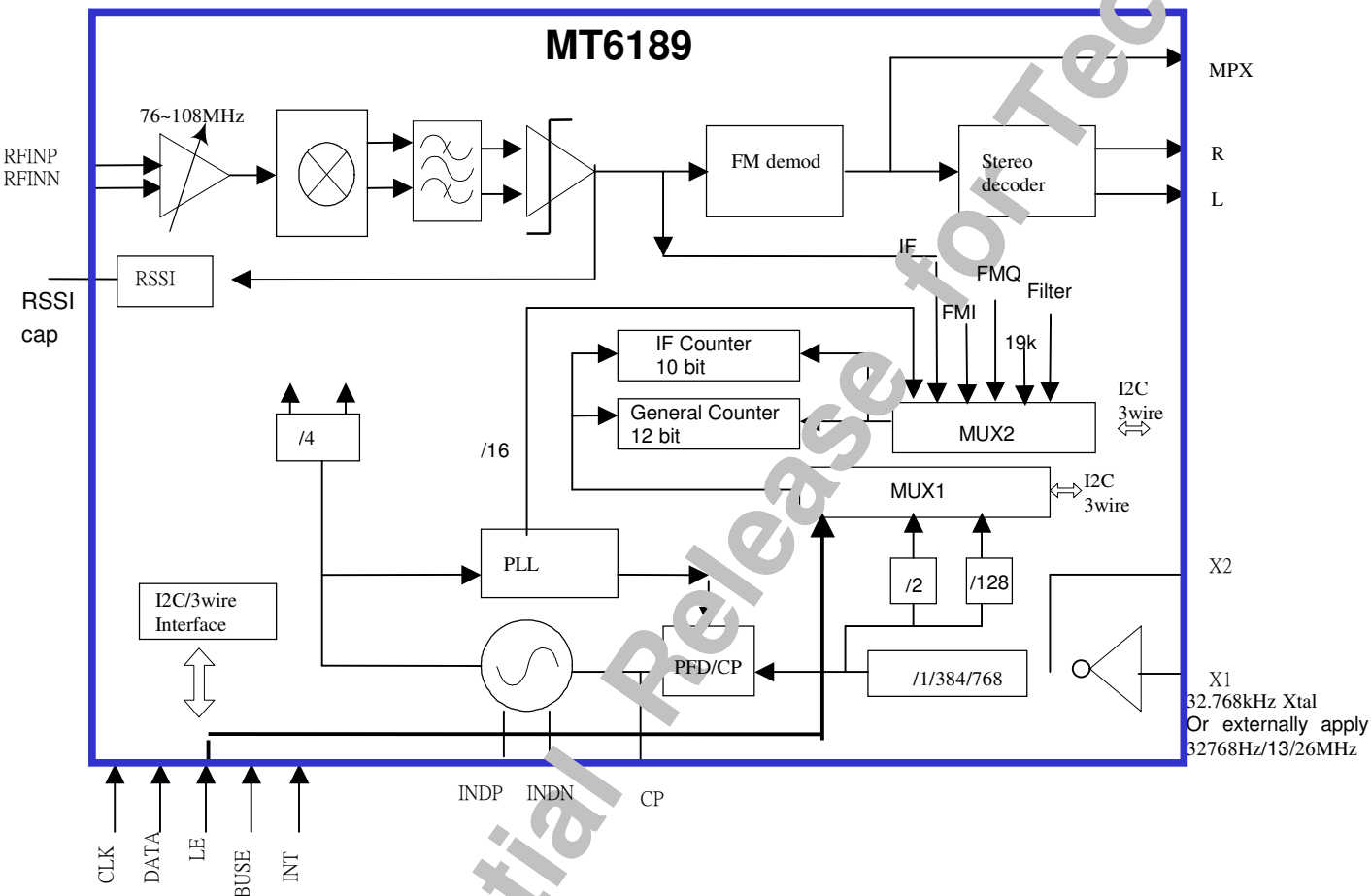


Figure 1 MT6189 Function Block Diagram

2. Register Table

Addr.	Name	Data 1								Data 0							
		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CW0	Reserve																
CW1	INT FLG		RST	PWD	0	CNTMK	0	RSSIMK	SARMK				0	CNTFG	0	RSSIFG	SARIFG
CW2	RFPLL_2	0	0	Ns_5	Ns_4	Ns_3	Ns_2	Ns_1	Ns_0	N2_7	N2_6	N2_5	N2_4	N2_3	N2_2	N2_1	N2_0
CW3	RFPLL_1	1	1	1	0	0	CAL_PLL	0	0	S_div_256	S_div_128	S_div_3	Idn1	Idn0	Iup1	Iup0	pd_rfpll
CW4	RSSI	1	1	0	0	RSSI3	RSSI2	RSSI1	RSSI0	HSIDE	1	0	0	0	1	1	1
CW5	LNA/MIXER									0	0	0	1	0	1	1	RFAGC_P
CW6	VCO	TAR3	TAR2	TAR1	TAR0	CNT_S2	CNT_S1	CNT_S0	WIN_EN							WIN_S1	WIN_S0
CW7	VCO							CAL1	CAL0				0	0	1	1	1
CW8	Demod part	DMRG_GAINSEL1	DMRG_GAINSEL0	0	0	0	DMGAIN1	DMGAIN0	Dmcali					0	0	DMNB1	DMNB0
CW9	Demod part						MPXGAIN1	MPXGAIN0	DMCALQ					0	0	FRNB1	FRNB0
CW10	Demod part	0	0	FRPTGAIN1	FRPTGAIN0		1	0	0	0	DMRSB	0	FRTUPD	DMPD	MPXPD	0	FRPTPD
CW11	Pilot filter	0	0	DMRESV5	0	0	0	0	0	0	0	0	0	0	0	0	0
CW12	PLL19K	0	0	0	0	0	0	pd_vco_19k	Sel_19k	mode_12_19k	cal_vco_19k	test_vco_19k	Idn1_19k	Idn0_19k	Iup1_19k	Iup0_19k	pd_pll19K
CW13		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
CW14	Stereo 1	PD_SD1	PD_SD2	PD_SD3	PD_SD4	PD_SD5	PD_SD6	1	1	S_AUTO	SBLEND	SC_DIS	STEREO	SMUTE	DEEM_USA	DEEM	HCC
CW15	Stereo 2	1	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0
CW16	Stereo 3	LCHGAIN1 [2:0]				LCHGAIN2 [3:0]					RCHGAIN1 [2:0]			RCHGAIN2 [3:0]			
CW17	Stereo 4	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0
CW18	Stereo 5	0	0	0	0	0	LCHF3DB [2:0]			0	0	0	0	0	RCHF3DB [2:0]		
CW19	Stereo 6	0	0	0	0	0	0	0	PD_SD7	PI_AMP [1:0]		1	0	SM_GAIN [1:0]		SB_GAIN [1:0]	
CW20	IF counter	CNT[9:0]															
CW21		DREF [3:0]								0		PD_SD8	1	1	1	1	0
CW23		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CW24	PLL19K1	0	0	0	REFDI_2_	REFDI_1_	REFDI_0_	FBDI_2_	FBDI_1_	FBDI_0_	0	0	0	0	0	0	0
CW25	Count Target					CNT_T_11	CNT_T_10	CNT_T_9	CNT_T_8	CNT_T_7	CNT_T_6	CNT_T_5	CNT_T_4	CNT_T_3	CNT_T_2	CNT_T_1	CNT_T_0
CW97	filterosc	FRTUNE1[4:0]												FRTUNE2[3:0]			
CW98	Dmtunei	DMTUNE1I[4:0]												DMTUNE2I[3:0]			
CW99	Dmtuneq	DMTUNE1Q[4:0]												DMTUNE2Q[3:0]			
CW100	PLL19Kosc	Fb_19k1[2:0]										Iband_19k1[5:0]					
CW101	PLL19Klpf														LPF[2:0]		
CW103	PLL19Kosc1	Fb_19k2[2:0]										Iband_19k2[5:0]					

Table 1 Register Control Table

3. Register Descriptions

CW1

Whole Chip Power Down (Read/Write)

PWD	Power Down
0	Power up
1	Power down (default)

This will turn off the whole chip.

Manual Reset (Read/Write)

RST	Reset Register
0	Off (default)
1	Reset

When 'RST' bit is set, a reset pulse will send to all digital circuits. This will reset the value of the registers.

RSSI Change Interrupt (Read Only)

RSSIFG	RSSI Change Interrupt
0	RSSI has not change
1	RSSI changes two step

RSSIFG will set when RSSI register changes two steps in 4.4ms.

Counter Counting Finished Interrupt (Read Only)

CNTFG	Counter Counting Finished Interrupt
0	No Counter Interrupt
1	Counter Interrupt

Counter Counting Finished Interrupt Mask (Read/Write)

CNTMK	Counter Counting Finished Interrupt Mask
0	Disable counter Interrupt (default)
1	Enable counter Interrupt

CW2~3

Selection of Calibration Coarse Tune or PLL Fine Tune

CAL_PLL	Mode
0	PLL Fine Tune

1	Calibration Circuit (default)

External Reference Clock Selection

S_div_256	S_div_128	S_div_3	Mode
0	0	1	32.768kHz Xtal or External 32768Hz Clock (default)
0	1	0	External 13MHz Clock
1	1	0	External 26MHz Clock

Charge Pump Current

Idn1	Idn0	Iup1	Charge Pump Current
0	0	0	10uA
0	0	1	20uA
0	1	0	30uA
0	1	1	40uA
1	0	0	50uA
1	0	1	60uA
1	1	0	70uA
1	1	1	80uA

Crystal Amplifier Power Down

Iup0	Crystal Amplifier Power Down
0	Normal
1	Power down (default)

RFPLL Power Down

pd_rfpll	RFPLL Power Down
0	Enable (default)

CW4 and CW20

Lo High Side Injection (Read/Write)

HSIDE	Lo High Side Injection
0	Low Side
1	High Side (default)

This will set the LO in high (low) side injection.

Receive Signal Strength Indicator (Read only)

RSSI3	RSSI2	RSSI1	RSSI0	Receive Signal Strength Indicator
0	0	0	0	< 0dBuVemf
0	0	0	1	0 ~ 5dBuVemf
0	0	1	0	5 ~ 10dBuVemf
0	0	1	1	10 ~ 15dBuVemf
0	1	0	0	15 ~ 20dBuVemf
0	1	0	1	20 ~ 25dBuVemf
0	1	1	0	25 ~ 30dBuVemf
0	1	1	1	30 ~ 35dBuVemf
1	0	0	0	35 ~ 40dBuVemf
1	0	0	1	40 ~ 46dBuVemf
1	0	1	0	46 ~ 52dBuVemf
1	0	1	1	52 ~ 60dBuVemf
1	1	0	0	> 60dBuVemf

Table 2 Receive signal strength indication

Table 3

These bits are updated every 4.4ms and can be read only for receive signal strength indication.

IF counter (Read only/Write to clear)

CNT[9:0]	10 bits IF Counter
x	Read IF counting value
0	Write to clear counter

Write the register value CW20:CNT[9:0] to clear the counter. Select counter source CW6 [11:9] and timing window source CW6 [1:0] and enable the counter CW6 [8]. Read the register value CW20:CNT[9:0] and calculate IF frequency.

CW5

RFAGC enable (Read/Write)

RFAGC_P	RFAGC Power
0	Off
1	On (default)

This will turn on the bias of RFAGC.

CW6~7

Calibration Result Target Register Selection (Read/Write)

TAR[3:0]	Window Source	Counter Source	Target Register
0000	Ref. Clock ÷2	VCO	**N/A**

0001	Ref. Clock ÷128 / LE	IF_CNT (default)	CNT[9:0]
0010	**N/A**	**N/A**	**N/A**
0011	Ref. Clock ÷128 / LE	PLL19K	Fb_19k1[2:0]
0100	Ref. Clock ÷128 / LE	PLL19K	Iband_19k1[5:0]
0101	Ref. Clock ÷128 / LE	PLL19K	LPF[2:0]
0110	Ref. Clock ÷128 / LE	PLL19K	Fb_19k2[2:0]
0111	Ref. Clock ÷128 / LE	PLL19K	Iband_19k2[5:0]
1000	**N/A**	**N/A**	**N/A**
1001	**N/A**	**N/A**	**N/A**
1010	Ref. Clock ÷128 / LE	FMI	DMTUNE1I[4:0]
1011	Ref. Clock ÷128 / LE	FMI	DMTUNE2I[3:0]
1100	Ref. Clock ÷128 / LE	FMQ	DMTUNE1Q[4:0]
1101	Ref. Clock ÷128 / LE	FMQ	DMTUNE2Q[3:0]
1110	Ref. Clock ÷128 / LE	FILTER	FRTUNE1[4:0]
1111	Ref. Clock ÷128 / LE	FILTER	FRTUNE2[3:0]

Table 4 Window Source, Counter Source And Target Register Mapping Table

Counter Source Selection (Read/Write)

CNT_S2	CNT_S1	CNT_S0	Counter Source Selection
0	0	0	VCO (default)
0	0	1	**N/A**
0	1	0	IF
0	1	1	PLL19K
1	0	0	**N/A**
1	0	1	FMI
1	1	0	FMQ
1	1	1	FILTER

See the 6-to-1 MUX2 for IF counter and general counter in Figure 1.

Start / Stop Counter Window (Read/Write)

WIN_EN	Start / Stop Counter Window
0	Window close (default)
1	Window open / Start Calibration

Once counter window is open, calibration mechanism starts immediately.

Counter Window Source Selection (Read/Write)

WIN_S1	WIN_S0	Counter Window Source
0	0	Ref. Clock ÷2 (default)
0	1	Ref. Clock ÷128

1	X	3-wire LE

Table 5 Counter Window Source Selection Table

See the 3-to-1 MUX1 for IF counter and general counter in Figure 1.
These should be set corresponding to Table 4.

Calibration Enable (Read/Write)

CAL1	CAL0	Calibration Enable
0	0	Calibration OFF (default)
1	1	Calibration Stand-by

CW8~11

Demodulator Output Gain1 Adjustment (Read/Write)

DMRG_GAINSEL[1:0]	Demodulator Gain1 Control
00	1/3
01	1/2(default)
1X	1

Demodulator Output Gain2 Adjustment (Read/Write)

DMGAIN[1:0]	Demodulator Gain2 Control
00	0.6
01	0.8
10	1
11	1.2(default)

Demodulator Channel I Delay Calibration (Read/Write)

Dmcali	Demodulator I Calibrate
0	Off(default)
1	ON

Demodulator Bias Current Adjustment (Read/Write)

DMNB[1:0]	Bias Current
00	5u
01	7.5u
10	10u
11	12.5u

MPX Output Gain Adjustment (Read/Write)

MPXGAIN[1:0]	Demodulator Gain Control
00	0.6
01	0.8
10	1(default)
11	1.2

Demodulator Channel Q Delay Calibration (Read/Write)

DMCALQ	Demodulator Q Calibration
0	Off(default)
1	ON

Pilot Filter Bias Current Adjustment (Read/Write)

FRNB[1:0]	Bias Current
00	5u
01	7.5u
10	10u(default)
11	12.5u

Pilot SC Filter Gain Adjustment (Read/Write)

FRPTGAIN[1:0]	Pilot filter Gain Control
00	0.6
01	0.8
10	1(default)
11	1.2

Demodulator Calibration Reset (Read/Write)

DMRSB	Demodulator Q Calibration
0	Reset(default)
1	Non reset

SC Filter Tuning Circuit Power Down (Read/Write)

FRTUPD	SC Filter Tuning Circuit PD
0	Power on
1	Power down(default)

Demodulator Power Down (Read/Write)

DMPD	Demodulator Q PD
0	Power on
1	Power down(default)

MPX Buffer Circuit Power Down (Read/Write)

MPXPD	MPXout Buffer Circuit PD
0	Power on
1	Power down(default)

Pilot SC Filter Power Down (Read/Write)

FRPTPD	Pilot SC Filter Circuit PD
0	Power on
1	Power down(default)

DMRESV5 (read/write)

DMRESV5	Reset Pilot Filter Clock
0	Reset (default)
1	Enable

CW12 & 24

PLL19K VCO Reset

pd_vco_19k	PLL19K VCO Reset
0	Normal (default)
1	Reset

PLL19K Mode Selection

Sel_19k	Mode
0	mixer
1	Pfd (default)

PLL19K Divider Value

Mode_12_19k	N
0	8
1	12

PLL19K VCO Calibration

test_vco_19k	cal_vco_19k	Calibration Mode
0	0	Normal (default)
0	1	Normal
1	0	Ext. input

1	1	Calibration

Charge Pump Current Mismatch

Iup1_19k	Iup0_19k	Up Current Mismatch
0	0	Normal (default)
0	1	1uA
1	0	2uA
1	1	3uA

Idn1_19k	Idn0_19k	Down Current Mismatch
0	0	Normal (default)
0	1	1uA
1	0	2uA
1	1	3uA

PLL19K Power Down

pd_pll19K	PLL19K Power Down
0	Enable PLL19K (default)
1	Disable PLL19K

PLL19K REF Delay Selection

REFDI_2_	REFDI_1_	REFDI_0_	Delay Selection
0	0	0	0us
0	0	1	0.5us
0	1	0	1us
0	1	1	1.5us
1	0	0	2us
1	0	1	2.5us
1	1	0	x
1	1	1	x

PLL19K Feedback Delay Selection

FBDI_2_	FBDI_1_	FBDI_0_	Delay Selection
0	0	0	0us
0	0	1	0.5us
0	1	0	1us
0	1	1	1.5us
1	0	0	2us
1	0	1	2.5us
1	1	0	x
1	1	1	x

CW14~CW19, CW21

(CW14)
Stereo Decoder Power Down 1~6

PD_SD1	Power Down Stereo Decoder Circuit Subblock1
0	Circuit On (default)
1	Circuit OFF

PD_SD2	Power Down Stereo Decoder Circuit Subblock2
0	Circuit On (default)
1	Circuit OFF

PD_SD3	Power Down Stereo Decoder Circuit Subblock3
0	Circuit On (default)
1	Circuit OFF

PD_SD4	Power Down Stereo Decoder Circuit Subblock4
0	Circuit On (default)
1	Circuit OFF

PD_SD5	Power Down Stereo Decoder Circuit Subblock5
0	Circuit On (default)
1	Circuit OFF

PD_SD6	Power Down Stereo Decoder Circuit Subblock6
0	Circuit On (default)
1	Circuit OFF

Stereo / Mono Mode Auto Detection

S_AUTO	Status
0	Auto Detection Disable
1	Auto Detection Enable (default)

Stereo Blend Function

SBLEND	Status
0	Function Disable
1	Function Enable (default)

Short Circuit Protection Function

SC_DIS	Status
0	Short Circuit Protection Enable
1	Short Circuit Protection Disable

	(default)

Stereo

STEREO	Stereo Status
0	Mono State
1	Stereo State (default)

Soft Mute Index

SMUTE	Soft Mute Status
0	Soft Mute Disable
1	Soft Mute Enable (default)

De-emphasis Type

DEEM_USA	De-emphasis Type
0	Japan/Eurp (50-us)
1	USA (75-us) (default)

De-emphasis Mode

DEEM	De-emphasis Enable
0	Disable De-emphasis
1	Enable De-emphasis (default)

High-Cut Control Mode

HCC	HCC Enable
0	Disable HCC (default)
1	Enable HCC

(CW16)
L-Channel Output Gain Control 1

LCHGAIN1 [2:0]	L-Channel Gain Control 1
000	
001	
010	
011	(default)
100	
101	
110	
111	

R-Channel Output Gain Control 1

RCHGAIN1 [2:0]	L-Channel Gain Control 1
000	
001	
010	
011	(default)
100	
101	
110	
111	

L-Channel Output Gain Control 2

LCHGAIN2 [3:0]	L-Channel Gain Control 2
0000	0 dB (default)
0001	1.25 dB
0010	2.50 dB
0011	3.75 dB
0100	5.00 dB
0101	6.25 dB
0110	7.50 dB
0111	8.75 dB
1000	10.00 dB
1001	11.25 dB
1010	12.50 dB
1011	13.75 dB
1100	15.00 dB
1101	16.25 dB
1110	17.50 dB
1111	18.75 dB

R-Channel Output Gain Control 2

RCHGAIN2 [3:0]	R-Channel Gain Control 2
0000	0 dB (default)
0001	1.25 dB
0010	2.50 dB
0011	3.75 dB
0100	5.00 dB
0101	6.25 dB
0110	7.50 dB
0111	8.75 dB
1000	10.00 dB
1001	11.25 dB
1010	12.50 dB
1011	13.75 dB
1100	15.00 dB

1101	16.25 dB
1110	17.50 dB
1111	18.75 dB

(CW18)

AAF F3dB Control (L-Channel)

LCHF3DB [2:0]	L-Channel AAF 3dB Control
000	
001	
010	
011	(default)
100	
101	
110	
111	

AAF F3dB Control (R-Channel)

RCHF3DB [2:0]	R-Channel AAF 3dB Control
000	
001	
010	
011	(default)
100	
101	
110	
111	

(CW19)

Stereo Decoder Power Down 7

PD_SD7	Power Down Stereo Decoder Circuit Subblock7
0	Circuit On (default)
1	Circuit OFF

Pilot Amplitude Detection Threshold Voltage

PI_AMP [1:0]	Descriptions
10	(default)
Other	TBD

Soft-Mute Amplifier Gain Control

SM_GAIN [1:0]	Soft-Mute Gain Control
00	TBD

01	TBD
10	(default)
11	TBD

Stereo Blend Amplifier Gain Control

SB_GAIN [1:0]	Stereo Blend Gain Control
00	TBD
01	TBD
10	(default)
11	TBD

(CW21)
Pilot Signal Detector Threshold

DREF [3:0]	Select Stereo Clock
1100	(default)
…	
…	

Stereo Decoder Power Down 8

PD_SD8	Power Down Stereo Decoder Circuit Subblock8
0	Circuit On (default)
1	Circuit OFF

4. Function Descriptions

4.1 3wire/I2C interface

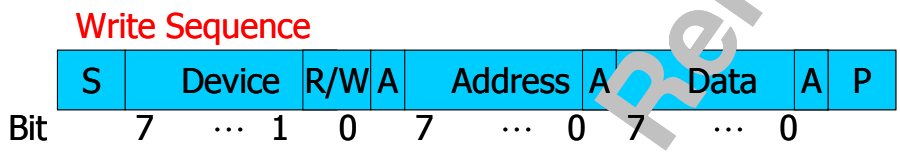
The serial interface is used as the control interface from the host. The host can send command or read status by this interface. The host interface of MT6189 has two modes. One is the I^{2}C mode and the other is the 3-wire mode. The I^{2}C mode uses two pins SDA, SCL and the 3-wire mode has an extra LE pin besides the SDA and SCL. The selection of the two modes is by a pin MODE. When the pin MODE is pull to Vdd, the serial interface is in I^{2}C mode. When MODE is pull to GND, the serial interface is in 3-wire mode.

4.1.1 The I^{2}C mode

The I^{2}C mode is compatible to the standard I^{2}C defined by Philips. There are two pins, SCL and SDA. The SCL is driven by HOST and the SDA is a bi-directional signal. The signal of I^{2}C when reading or writing a register will be shown in the following sections.

i. The I^{2}C write sequence

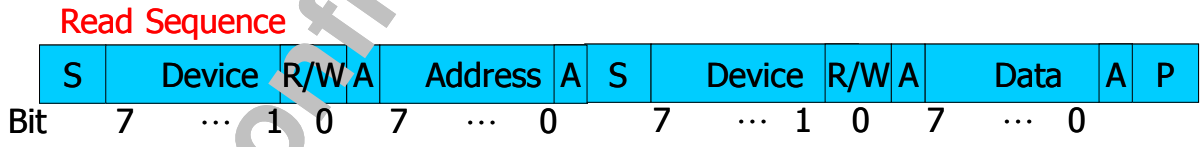
The I^{2}C write cycle is as the following graph.



The “S” is the start bit as defined in I^{2}C spec. . The “Device” is the Device ID, our device ID is “1100000”. R/W is read/write flag of the following byte. 1 means read and 0 means write. A is the acknowledge bit. P is the stop bit. The number below the blue bar is the bit order. The Device has 7 bits from 7 to 1, and the bit 0 is R/W. The “Address” and “Data” both have 8 bits. After this write sequence the data in “Data” will be written to address “Address”.

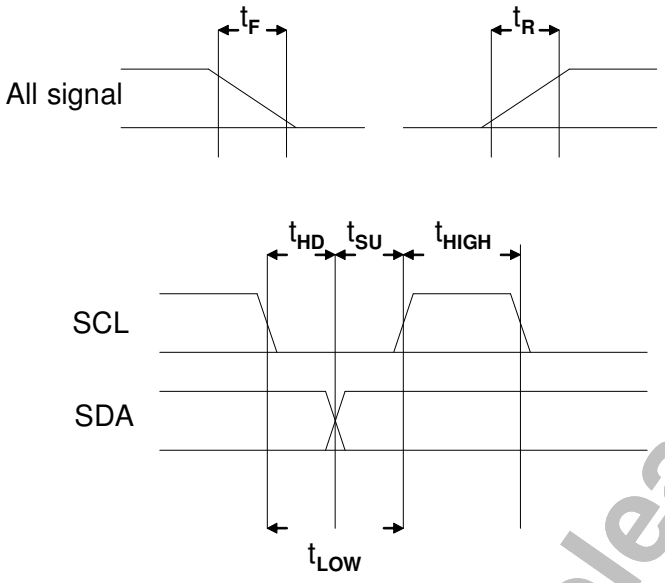
ii. The I2C read sequence

The I^{2}C read cycle is as the following graph.



The write sequence has 3 byte of data, but he read sequence has 4 byte. In read sequence, the device and R/W are sent twice, and the R/W is 0(write) at the first time and 1(read) at the second time. There are also two start bits. The second start bit means the Device will be sent again and the read/write mode can be switched. The Address is sent from the Host and the Data will be given from the device.

iii. Timing constraint



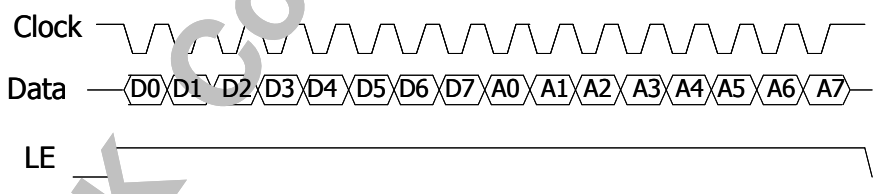
Constraint	Minimum	Maximum	Description
tF	25ns	100ns	Fall time
tR	25ns	100ns	Rise time
tHD	100ns	-	The hold time of SDA to SCL
tSU	100ns	-	The setup time of SDA to SCL
tHIGH	100ns	-	The period when SCL is high
tLOW	100ns	-	The period when SCL is low

4.1.2 The 3-wire mode

In the 3-wire mode, the Host uses three wires to control the Device. The three wires are CLOCK (SCL) DATA (SDA) and LE. At the rising edge of the CLOCK pin, the value on DATA pin will be sampled by the Device. The LE has two meanings. One is the I/O direction of the DATA pin, and the other is to indicate a read or write command. The sequences of read/write command will be shown in the following sections.

i. The 3-wire write sequence

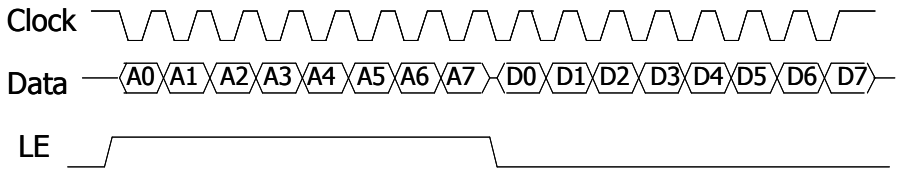
The 3-wire write sequence is:



At every rising edge of Clock pin, the value on Data pin is latched. The data sequence start from the LSB of data, and end at the MSB of address. During the write sequence, the LE pin keeps high to allow the value on Data pin to be fed into device.

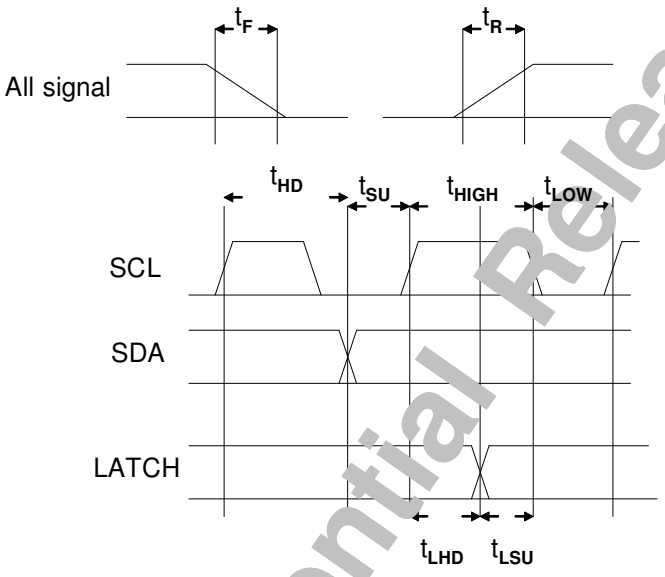
ii. The 3-wire read sequence

The 3-wire read sequence is:



The data sequence on Data pin in read command is different to the write command. After the address is sent, the LE will become low. Then, the data will be sent from the device.

iii. Timing constraint



Constraint	Minimum	Maximum	Description
tF	25ns	100ns	Fall time
tR	25ns	100ns	Rise time
tHD	100ns	-	The hold time of SDA to SCL
tSU	100ns	-	The setup time of SDA to SCL
tLHD	100ns	-	The hold time of LATCH to SCL
tLSU	100ns	-	The setup time of LATCH to SCL
tHIGH	100ns	-	The period when SCL is high
tLOW	100ns	-	The period when SCL is low

4.2 Interrupts

There are 3 interrupt sources in MT6189 chip. Each of them has an interrupt flag and an interrupt mask in the register CW1. D0, D1 and D3 are the flags and D8, D9 and D11 are the masks. If anyone of the interrupt sources triggers, the flag will become 1. If the corresponding mask of the triggered flag is set as 1, the interrupt pin will be pull to high to notify the host for interrupt service. If the mask is set as 0, the flag will still become high but the interrupt pin will not trigger. Writing any value to the lower byte (D0~D7) will clear all of the interrupt flags.

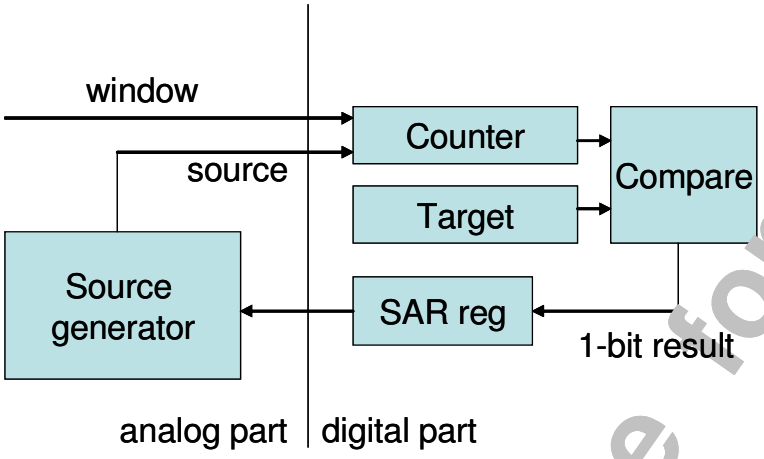
The SARIFG (D0) and corresponding SARMK (D8) are the flag and the mask of the SAR interrupt. The SAR interrupt will be triggered when a SAR calibration is finished. This interrupt can notify the host to get the result of SAR calibration and issue another calibration.
The RSSIFG (D1) and corresponding RSSIMK (D9) are the flag and the mask of the RSSI interrupt. This interrupt is triggered when the RSSI value changes larger than 1. For example, if the RSSI value changes from 1 to 3, the difference is larger then 1, the interrupt will be triggered. If the value changes from 1 to 2, the interrupt will not be triggered.
The CNTFG (D3) and corresponding CNTMK (D11) are the flag and the mask of the IF counter interrupt. This interrupt is triggered when the IF counter finish the counting. The CNTFG is also used to stop the IF counter counting, thus the host should read the counter result before clearing this flag.

4.3 Initialization

- Set all registers to default value
- Power up MT6189 according to 4.5.6
- Proceed pilot PLL 19KHz calibration (reference to 4.5.7)
- Proceed calibration for demodulator (reference to 4.7.5)
- Set the operation mode (stereo/mono) according 4.5.6

4.4 Calibrations

The SAR calibration is an auto counting and comparing system for adjusting the frequency of internal signals. There are many signals in the chip that need to be set to a target frequency. The frequency of these signals can be controlled by a corresponding register. We will calibrate the frequency and use binary decision to modify the value of register to make the frequency approaching the target frequency. The calibration is done by counting the signal's rising edge inside a window signal. The result is compared with the value in the counter target register. If the counting result of the calibrated signal is higher than the target value, the register bit under calibration will be set to 0 to make the frequency lower. Thus, the target frequency is decided by the length of window and the value in the counter target register.



The selection of source and window can be programmed by setting registers. The flow of setting a calibration will be introduced in the following section.

i. The Algorithm of SAR Calibration

During the SAR calibration, the SAR register is set as 1000000 (in binary representation). This value means the source will be set in the middle frequency. Then according to the calibration result, the MSB of the SAR register will be programmed as 1 or 0 to make the frequency faster or slower, and the bit next to MSB in SAR register will be set to 1. After the second calibration, the second bit is also decided by the same way. This loop is continued until all the bits in the SAR register is decided. The bit number of the SAR register is decided by the TAR3~TAR0 (in CW6) register recorded in the register map.

ii. The Programming Steps

The programming steps of a SAR calibration are:

1. Enable SAR calibration by setting CAL [1:0] = 11.
2. Setting CW6 to select the window type (WIN_S1, WIN_S0) calibration source (CNT_S2, CNT_S1, CNT_S0) and SAR register (TAR3, TAR2, TAR1, TAR0). The meaning of these registers can be found in register map.
3. Setting the counter target in CW25.
4. Enable window by setting 1 to WIN_EN.
5. If the selection of window type is 3-wire latch, the host needs to send a sequence of window from the latch pin.
6. The SAR calibration circuit will start to calibrate the frequency. The result will be stored into the register indexed by the TAR3~TAR0 register.

4.5 Control Method

4.5.1 General Parameter – Window Time for Calibration

For all calibration procedures, a counter window is needed as a reference, which can be selected via register CW6 [1:0] (WINS [1:0]) in Table 5. VCO can only use 32,768Hz reference (or 13M / 26MHz) as counter window, while the other ones can use other slower clock from LE pin. Hence the counter window is different according to different reference clock setting. The setting for VCO is listed with VCO calibration, and the window time for the other part is listed below.

1. 32768 / 13M / 26M Hz Reference Clock (CW6[1:0] = 01)

Reference Clock Type	CW3[7:5] Setting	**Window Time**
32768Hz	001	1.9531 ms
13MHz	010	1.8905 ms
26MHz	110	1.8905 ms

2. LE Pin (CW6[1:0] = 1X)

Because the SAR counter is high-level enable, the signal given to LE pin should satisfy the following specifications:

Items	Condition	Min.	Typ.	Max	Unit
Clock HIGH Level	Comply with VDD	2.5	2.8	3.6	V
Clock Frequency		140	256	360	Hz
Duty Cycle	Square Wave	45	50	55	%
Clock Jitter	Peak-to-Peak Jitter			50	µs

As a result, **Window Time** = Time Duration of LE Pin HIGH Level.

4.5.2 LNA/MIXER

1. RFAGC Control:

	Address	Data	Value	Function
1	CW5	[0:0]	1/0	RFAGC is on/off

If RF signal is strong than 70dBuV, RFAGC would react and decrease LNA gain. The RFAGC range is about 28dB.

4.5.3 IF

Set CW4 as Table 6 to make IF circuit operates normally.

1. Read RSSI Value

	Address	Data	Value	Function
1	CW12	[9:9]	0	Make sure 456kHz VCO is on
2	CW12	[0:0]	0	Make sure 456kHz VCO is on
3	CW14	[12:12]	0	Make sure 456kHz VCO is on
4	CW4	[11:8]	XXXX	read 4bit RSSI value

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CW4	1	1	0	0	RSSI3	RSSI2	RSSI1	RSSI0	HSIDE	1	0	0	0	1	1	1
	1	1	0	0	x	x	x	x	1	1	0	0	0	1	1	1

Table 6 IF Circuit Register

2. Read RSSI Interrupt

Set CW1 [RSSIMK] =1 to enable the RSSI interrupt.
RSSI value is updated every 4.491ms. If RSSI value changes larger than 2 steps in 4.491ms, then RSSI interrupt occur. INT pin will pull low and CW1 [RSSIFG] =1.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CW1		RST	PWD	0	CNTMK	0	RSSIMK	SARMK				0	CNTFG	0	RSSIFG	SARIFG
		0	0	0	0	0	1	0				0	x	0	x	x

Table 7 Interrupt Register

3. Read IF Counter Value

	Address	Data	Value	Function
1	CW20	[9:0]	0000000000	Write to clear the IF counter
2	CW6	[15:8]	00010100	counter data source set to IF signal and disable time window
3	CW7	[9:8]	00	Make sure calibration is OFF
4	CW6	[2:0]	01	time window source set to xtal clock
5	CW1	[3:0]	XXXX	Read the interrupt and check if need to do other job or not.
6	CW1	[3:0]	0000	write to clear the interrupt
7	CW1	[11:11]	1	Enable IF counter interrupt
8	CW6	[8:8]	1	enable time window
9				INT pin will pull low and read IF count interrupt will be set to '1'.
10	CW1	[3:3]	X	Read IF counter interrupt flag. It will set to '1', if IF counter is finished. Read the interrupt and check if need to do other job or not.
11	CW6	[8:8]	0	disable time window
12	CW1	[3:0]	0000	write to clear the interrupt
13	CW20	[9:0]	XXXXXXXXXX	Read the IF counter value **IF count**.
				IF frequency=**IFcount** / (**Window Time**)

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CW20							CNT9	CNT8	CNT7	CNT6	CNT5	CNT4	CNT3	CNT2	CNT1	CNT0
							x	x	x	x	x	x	x	x	x	x

Table 8 IF Counter Register

4.5.4 VCO

VCO Frequency Set-up Procedure

1	CW12_0	[0:0] = 0	Preparing for VCO calibration.
2	CW12_1	[1:1] = 0	
3	CW7_0	[4:0] = 7	
4	CW4_0	[7:7] =	Choose high/low side IF;
5			Divider Number = (Radio Freq.† +- IF) x 4 / Ref. Freq. …(round to integer) +: High-side injection -: Low-side injection IF = 140kHz ……corresponding to IF block setting Ref. Freq. = 32,768 Hz: 32,768Hz crystal 33,854.167 Hz: 13MHz or 26MHz reference
6	CW2_1	[5:0] = 0	Fix VCO divider value for calibration
7	CW2_0	N2	N2 = Divider Number / 64 …(round-down to integer)
8	CW3_1	[2:2]=1	Xtal setting.
9	CW3_1	[7:5] = 7	
10	CW3_0	[1:0] = 2	
11	CW3_0	[7:5] =	1 for 32.768KHz; 2 for 13MHz; 6 for 26MHz
12	CW7_1	[1:0] = 3	Calibration stand-by
13	CW25	Target	Target = Divider Number / 16 …(round to integer)
14	CW6_0	[1:0] = 0	Select calibration window for calibration
15	CW1_0	[7:0] = 0	Clear interrupt flag
16	CW5_0	[4:4]=	1 for 32.768KHz; 0 for 13 & 26MHz
17	CW6_1	[7:0] = 1	Select calibrate and start calibration
18	wait until SARFG=1, reset CW1_0, read CW6_1		
19	CW2_1	Ns	Ns = Divider Number – 64 x N2
20	CW3_1	[2:2] = 0	Connect RFPLL & VCO
21	CW6_1	[7:4] = 1	Reset to default without calibration
22	CW7_1	[7:0] = 0	Reset to default without calibration
23	Check CW96_0; set CW96_0 = CW96_0 +1 if CW96_0 < 64		

†: Radio Freq. represents the destination radio channel frequency.

4.5.5 Demodulator

1. Calibration
   a. FMI

1	CW1_1	[5:5] = 0	
2	CW10_0	[3:3] = 0	
3	CW8_1	[3:3] = 0	Preparing for demodulator calibration.
4	CW8_1	[0:0] = 1	Enable calibration mode of I channel demodulator
5	CW9_1	[0:0] = 1	Enable calibration mode of Q channel demodulator
6	CW10_0	[6:6] = 0	Reset demodulator
7	CW10_0	[6:6] = 1	Reset demodulator
8	CW3_0	[1:0] = 2	
9	CW3_1	[7:5] = 7	Xtal setting.
10	CW3_0	[7:5] =	1 for 32.768KHz; 2 for 13MHz; 6 for 26MHz
11	CW12_1	[1:1] = 0	
12	CW12_0	[0:0] = 0	PLL setting.
13	CW6_1	[7:0] = 26	Set clock source and target register
14	CW7_1	[1:0] = 0	Disable calibration process
15	CW98_1	[4:0] = 0	
16	CW98_0	[3:0] = 0	Pre-set for calibration.
17	CW7_1	[1:0] = 3	Enable calibration process
18	CW6_0	[1:0] = 1	Set window source
19	CW6_1	[7:0] = 170	Set clock source and target register
20	CW25_0	[7:0] = 34	
21	CW25_1	[7:0] = 2	target= 140 * 2 * 64 / p = CW25_1 * 256 + CW25_0; p = 32.768 or 13000 / 384 for 13 & 26MHz
22	CW1_0	[7:0] = 0	Clear all FLG registers
23	CW5_0	[4:4]=	1 for 32.768KHz; 0 for 13 & 26MHz
24	CW6_1	[0:0] = 1	Start calibration process
25	wait until SARFG=1, reset CW1_0, read CW6_1		
26	CW98_0	[7:0] = 0	Pre-set initial value of resistor array
27	CW25_0	[7:0] = 34	
28	CW6_1	[7:4] = 11	Set clock source and target register
29	CW7_1	[7:0] = 3	Enable calibration
30	CW6_0	[1:0] = 1	Set window source
31	CW1_0	[7:0] = 0	Clear all FLG registers
32	CW5_0	[4:4]=	1 for 32.768KHz; 0 for 13 & 26MHz
33	CW6_1	[0:0] = 1	Start calibration process

34	wait until SARFG=1, reset CW1_0, read CW6_1		

b. FMQ

1	CW1_1	[5:5] = 0	
2	CW10_0	[3:3] = 0	
3	CW8_1	[3:3] = 0	Preparing for demodulator calibration.
4	CW8_1	[0:0] = 1	Enable calibration mode of I channel demodulator
5	CW9_1	[0:0] = 1	Enable calibration mode of Q channel demodulator
6	CW10_0	[6:6] = 0	Reset demodulator
7	CW10_0	[6:6] = 1	Reset demodulator
8	CW3_0	[1:0] = 2	
9	CW3_1	[7:5] = 7	Xtal setting.
10	CW3_0	[7:5] =	1 for 32.768KHz; 2 for 13MHz; 6 for 26MHz
11	CW12_1	[1:1] = 0	
12	CW12_0	[0:0] = 0	PLL setting.
13	CW6_1	[7:0] = 28	Set clock source and target register
14	CW7_1	[1:0] = 0	Disable calibration process
15	CW99_1	[4:0] = 0	
16	CW99_0	[3:0] = 0	Pre-set for calibration.
17	CW7_1	[1:0] = 3	Enable calibration process
18	CW6_0	[1:0] = 1	Set window source
19	CW6_1	[7:0] = 204	Set clock source and target register
20	CW25_0	[7:0] = 34	
21	CW25_1	[7:0] = 2	target= 140 * 2 * 64 / k = CW25_1 * 256 + CW25_0; p = 32.768 or 13000 / 384 for 13 & 26MHz
22	CW1_0	[8:2] = 0	Clear all FLG registers
23	CW5_0	[4:4]=	1 for 32.768KHz; 0 for 13 & 26MHz
24	CW6_1	[0:0] = 1	Start calibration process
25	wait until SARFG=1, reset CW1_0, read CW6_1		
26	CW99_0	[7:0] = 0	Pre-set initial value of resistor array
27	CW25_0	[7:0] = 34	
28	CW6_1	[7:4] = 13	Set clock source and target register
29	CW7_1	[7:0] = 3	Enable calibration
30	CW6_0	[1:0] = 1	Set window source
31	CW1_0	[7:0] = 0	Clear all FLG registers
32	CW5_0	[4:4]=	1 for 32.768KHz; 0 for 13 & 26MHz
33	CW6_1	[0:0] = 1	Start calibration process

34	wait until SARFG=1, reset CW1_0, read CW6_1

c. SCF Filter Oscillator

1	CW10_1	[2:2] = 0	
2	CW10_0	[7:7] = 1	
3	CW10_0	[4:4] = 0	
4	CW11_1	[5:5] = 0	
5	CW11_1	[5:5] = 1	
6	CW1_1	[5:5] = 0	Preparing for SCF calibration.
7	CW3_0	[1:0] = 2	
8	CW3_1	[7:5] = 7	Xtal setting.
9	CW3_0	[7:5] =	1 for 32.768KHz; 2 for 13MHz; 6 for 26MHz
10	CW12_1	[1:1] = 0	
11	CW12_0	[0:0] = 0	PLL setting.
12	CW6_1	[7:0] = 30	Set clock source and target register
13	CW7_1	[1:0] = 0	Disable calibration process
14	CW97_1	[4:0] = 0	
15	CW97_0	[3:0] = 0	Pre-set for calibration.
16	CW7_1	[1:0] = 3	Enable calibration process
17	CW6_0	[1:0] = 1	Set window source
18	CW6_1	[7:0] = 238	Set clock source and target register
19	CW25_1	[3:0] = 3	
20	CW25_0	[7:0] = 122	target= 456 * 64 / p = CW25_1 * 256 + CW25_0; p = 32.768 or 13000 / 384 for 13 & 26MHz
21	CW1_0	[7:0] = 0	Clear all FLG registers
22	CW5_0	[4:4]=	1 for 32.768KHz; 0 for 13 & 26MHz
23	CW6_1	[0:0] = 1	Start calibration process
24	wait until SARFG=1, reset CW1_0, read CW6_1		
25	CW25_0	[7:0] = 122	
26	CW6_1	[7:4] = 15	Set clock source and target register
27	CW7_1	[1:0] = 3	Enable calibration process
28	CW1_0	[7:0] = 0	Clear all FLG registers
29	CW5_0	[4:4]=	1 for 32.768KHz; 0 for 13 & 26MHz
30	CW6_1	[0:0] = 1	Start calibration process
31	wait until SARFG=1, reset CW1_0, read CW6_1; read CW97_0; set K = min (CW97_0 + 1 & 15)		
32	CW6_1	[7:4] = 1	Set clock source and target register

33	CW7_1	[1:0] = 0	Disable calibration process
34	CW97_0	[4:0] = K	refer to step 31
35	CW3_0	[7:5] =	1 for 32.768KHz; 2 for 13MHz; 6 for 26MHz
36	CW3_1	[2:2] = 0	Disable RFPLL calibration mode
37	CW8_1	[0:0] = 0	Disable Demodulation I channel mode
38	CW9_1	[0:0] = 0	Disable Demodulation Q channel mode Check CW97_1; set T according to: CW97-1 T >= 13 3 = 12 4 = 11 5 = 10 6
39	CW4_0	[6:4] = T	< = 9 7

2. Demodulator Function

Register setup:
DMPD (CW10 [D3]) →0, power on demodulator
DMCALI (CW8 [D8]) →0, disable calibration loop I
DMCALQ (CW9 [D8]) →0, disable calibration loop Q
DMRSB (CW10 [D6]) 0→1, disable demodulator reset
DMGAIN_1 (CW8 [D10]) →1, demodulator fine gain select
DMGAIN_0 (CW8 [D9]) →0, demodulator fine gain select
DMRG_GAINSEL_1 (CW8 [D15) →0, demodulator coarse gain select
DMRG_GAINSEL_0 (CW8 [D14]) →0, demodulator coarse gain select

a. MPXOUT

Register setup
FRRDSPD (CW10 [D1]) →0, power on mpxout amplifier
MPXPD→0 (CW10 [D2]), power on mpxout amplifier
MPXGAIN<1:0> (CW9 [D10:D9]) →10, MPXGAIN adjust

b. PTfrosc(SCF filter oscillator)

Register setup
FRTUPD (CW10 [D10]) →0, power on oscillator
FRCKTEST (CW10 [D9]) →0, disable test
DMRESERV<5> (CW11 [D13) →0→1, reset oscillator to make oscillation

c. Pilot Filter

Register setup:
FRPTPD (CW10 [D0]) →0, power on pilot filter
FRPTTEST (CW10 [D5]) →0, disable test mode
FRPTGAIN<1:0> (CW10 [D13:D12]) →10, adjust pilot filter gain

4.5.6 Stereo Decoder

MONO and STEREO mode has different setup as following descriptions

- MONO Mode:
  - Make sure OSC in Pilot PLL is enable and calibrated to guarantee de-emphasis filter works properly (de-emphasis filter is SCF need 456-KHz clock)
  - Turn-OFF (Set to '0') **S_AUTO** (CW14:D7) and **STEREO** (CW14:D4) if you need force MT6189 operated in MONO Mode. If you need MT6189 to automatic determine MONO or STEREO mode, Turn ON **S_AUTO** Bit.
  - Set **FRPTPD** (CW10:D0) to high.
  - Whenever **S_AUTO** Bit is set high, **STEREO** Bit is no function
  - Turn-ON **SMUTE** (CW14:D3) if you need Soft-Mute Function Enable.
  - Turn-ON **HCC** (CW14:D0) if you need to enable High-Cut Control Function
  - To Disable De-emphasis Filter, you need to set **DEEM** to '0' and **PD_SD4** to '1'
- Stereo Mode:
  - Make sure Pilot PLL and Pilot Filter is enable and calibrated to guarantee Stereo Function works properly
  - Turn-OFF (Set to '0') **S_AUTO** (CW14:D7) and Turn-ON (Set to '1') **STEREO** (CW14:D4) if you need force MT6189 operated in Stereo Mode. If you need MT6189 to automatic determine MONO or STEREO mode, Turn ON **S_AUTO** Bit.
  - Set **FRPTPD** (CW10:D0) to low.
  - Whenever **S_AUTO** Bit is set high, **STEREO** Bit is no function
  - Turn-ON **SMUTE** (CW14:D3) if you need Soft-Mute Function Enable.
  - Turn-ON **SBLEND** (CW14:D6) if you need Stereo Blend Function Enable.
  - Turn-ON **HHC** (CW14:D0) if you need to enable High-Cut Control Function
  - To Disable De-emphasis Filter, you need to set **DEEM** to '0' and **PD_SD4** to '1'
- Power Down Mode:
  - Set CW14 [D15:D8] = [11 11 11 11]
  - Set CW14 [D7:D0] = [01 01 11 10]
  - Set CW19 [D8] = '1'
  - Set CW21 [D5] = '1'
- Power On Mode:
  - Set CW14 [D15:D8] = [00 00 00 11]
  - Set CW19 [D8] = '0'
  - Set CW21 [D5] = '0'

4.5.7 Pilot PLL 19k

1. Calibration Process

1	CW1_1	[5:5] = 0	Global power ON
2	CW3_0	[5:5] = 1	
3	CW3_0	[1:1] = 1	Power down internal active resistor and Set dived value =3
4	CW6_1	[7:4] = 1	Set target register
5	CW7_1	[1:0] = 0	Disable calibration process
6	CW3_0	[1:0] = 2	
7	CW3_1	[7:5] = 7	Xtal setting.
8	CW3_0	[7:5] =	1 for 32.768KHz; 2 for 13MHz; 6 for 26MHz
9	CW103_1	[2:0] = 4	
10	CW103_0	[5:0] = 32	
11	CW101_0	[2:0] = 4	Pre-set for calibration.
12	CW12_0	[0:0] = 0	
13	CW12_0	[6:5] = 3	Power on and set calibration mode.
14	CW12_1	[0:0] = 1	Power on VCO
15	CW14_0	[7:7] = 0	
16	CW14_0	[4:4] = 1	Enforce stereo mode
17	CW6_0	[1:0] = 1	Set window source
18	CW7_1	[1:0] = 3	Enable calibration
19	CW6_1	[7:0] = 102	Set clock source
20	CW25_1	[3:0] = 3	Set target value
21	CW25_0	[7:0] = 122	Set target value
22	CW1_0	[7:0] = 0	Clear all FLG registers
23	CW5_0	[4:4]=	1 for 32.768KHz; 0 for 13 & 26MHz
24	CW6_1	[0:0] = 1	Start calibration
25	wait until SARFG=1, reset CW1_0, read CW6_1		
26	CW6_1	[7:4] = 1	Set target register
27	CW7_1	[1:0] = 0	Disable calibration process
28	CW3_0	[0:0] = 0	
29	CW3_0	[7:5] =	1 for 32.768KHz; 2 for 13MHz; 6 for 26MHz
30	CW12_0	[0:0] = 0	
31	CW12_0	[6:5] = 3	Power on and set calibration mode.
32	CW12_1	[0:0] = 1	Power on VCO.
33	CW14_0	[7:7] = 0	Enforce stereo mode

34	CW14_0	[4:4] = 1	
35	CW6_0	[1:0] = 1	Set window source
36	CW7_1	[1:0] = 3	Enable calibration
37	CW6_1	[7:0] = 118	Set clock source
38	CW25_1	[3:0] = 3	
39	CW25_0	[7:0] = 122	target= 456 * 64 / p = CW25_1 * 256 + CW25_0; p = 32.768 or 13000 / 384 for 13 & 26MHz
40	CW1_0	[7:0] = 0	Clear all FLG registers
41	CW5_0	[4:4]=	1 for 32.768KHz; 0 for 13 & 26MHz
42	CW6_1	[0:0] = 1	Start calibration
43	wait until SARFG=1, reset CW1_0, read CW6_1		
44	CW6_1	[7:4] = 1	Set target register
45	CW7_1	[1:0] = 0	Disable calibration process
46	CW3_0	[0:0] = 0	
47	CW3_0	[7:5] =	1 for 32.768KHz; 2 for 13MHz; 6 for 26MHz
48	CW12_0	[0:0] = 0	
49	CW12_0	[6:5] = 3	Power on and set calibration mode for PLL19K
50	CW12_1	[0:0] = 1	Power on VCO in PLL19K
51	CW14_0	[7:7] = 0	
52	CW14_0	[4:4] = 1	Enforce stereo mode
53	CW6_0	[1:0] = 1	Set window source
54	CW6_1	[7:0] = 86	Enable calibration
55	CW7_1	[1:0] = 3	Set clock source
56	CW25_1	[3:0] = 3	
57	CW25_0	[7:0] = 122	target= 456 * 64 / p = CW25_1 * 256 + CW25_0; p = 32.768 or 13000 / 384 for 13 & 26MHz
58	CW1_0	[7:0] = 0	Clear all FLG registers(Should be CW1_0 [7:0]=0)
59	CW5_0	[4:4]=	1 for 32.768KHz; 0 for 13 & 26MHz
60	CW6_1	[0:0] = 1	Start calibration
61	wait until SARFG=1, reset CW1_0, read CW6_1		
62	CW14_0	[7:7] = 1	
63	CW14_0	[4:4] = 0	Set Automatic mode
64	CW12_0	[7:5] = 4	Set Divided value=24 and disable calibration mode of PLL19K
65	CW12_1	[5:5] = 0	Disable test mode of PLL19K
66	CW13_0	[7:7] = 0	Disable test mode of PLL19K
67	CW23_1	[4:2] = 0	Disable test mode of PLL19K

5. Application of MT6189

5.1 Layout of MT6189

The PCB layout of MT6189 application can be simply done if the few critical portions are well positioned.

- The 15nH inductor is a part of the VCO tank, it requires the Q factor to ≧25, the connection from MT6189 to the inductor need to be symmetric and short to reduce the unwanted parasitic effect.
- The loop filter (1 resister and 2 capacitance) connected to pin 17 is the controlling point the RF VCO; these should be placed close to MT6189.
- For the application with antenna matching network, the components of the matching network also need to be placed near to MT6189.

5.2 Reference application circuit

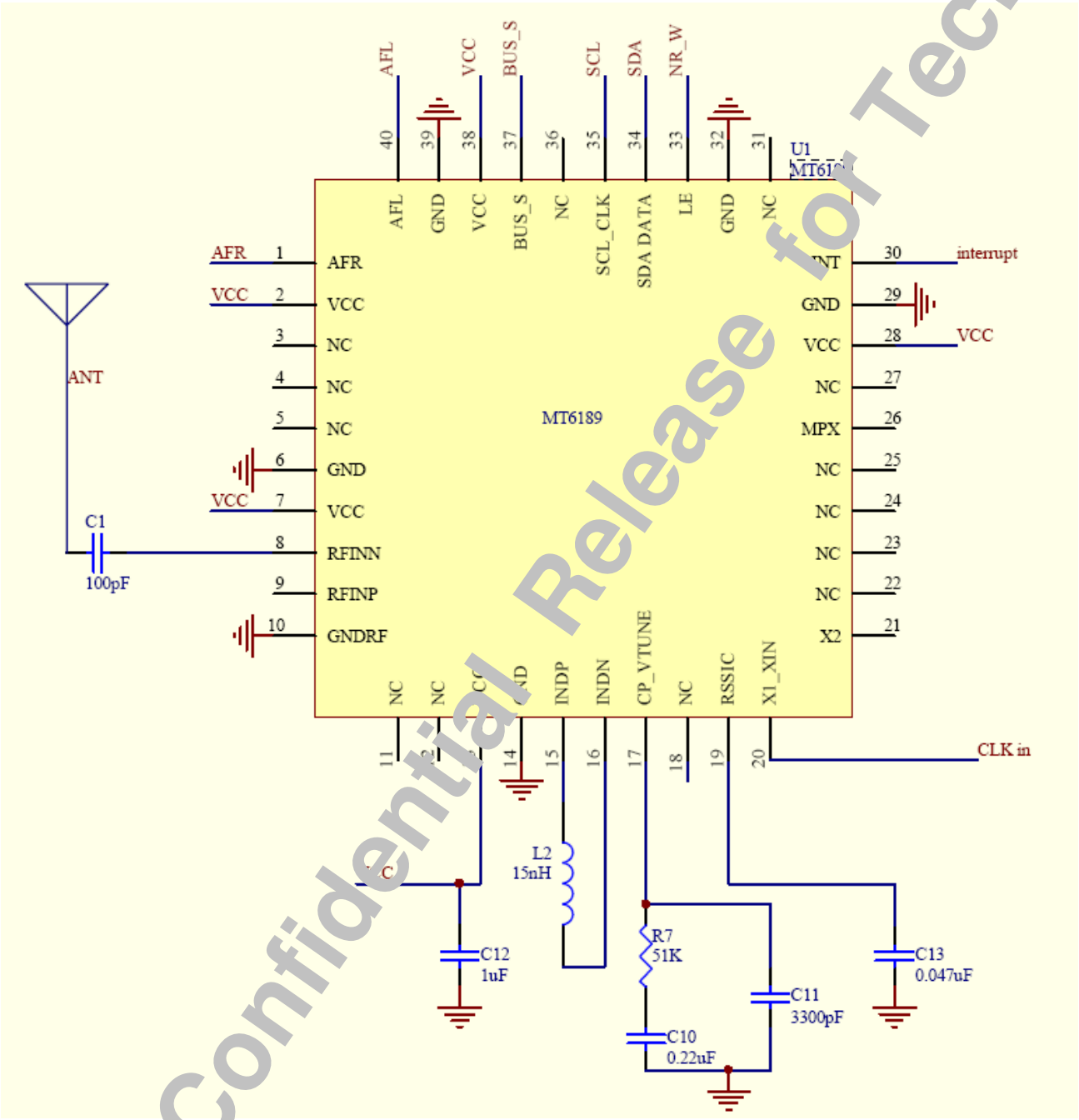


Figure 2 MT6189 with external clock & without antenna matching circuit

*note that circuits without antenna matching may cause sensitivity degradation.

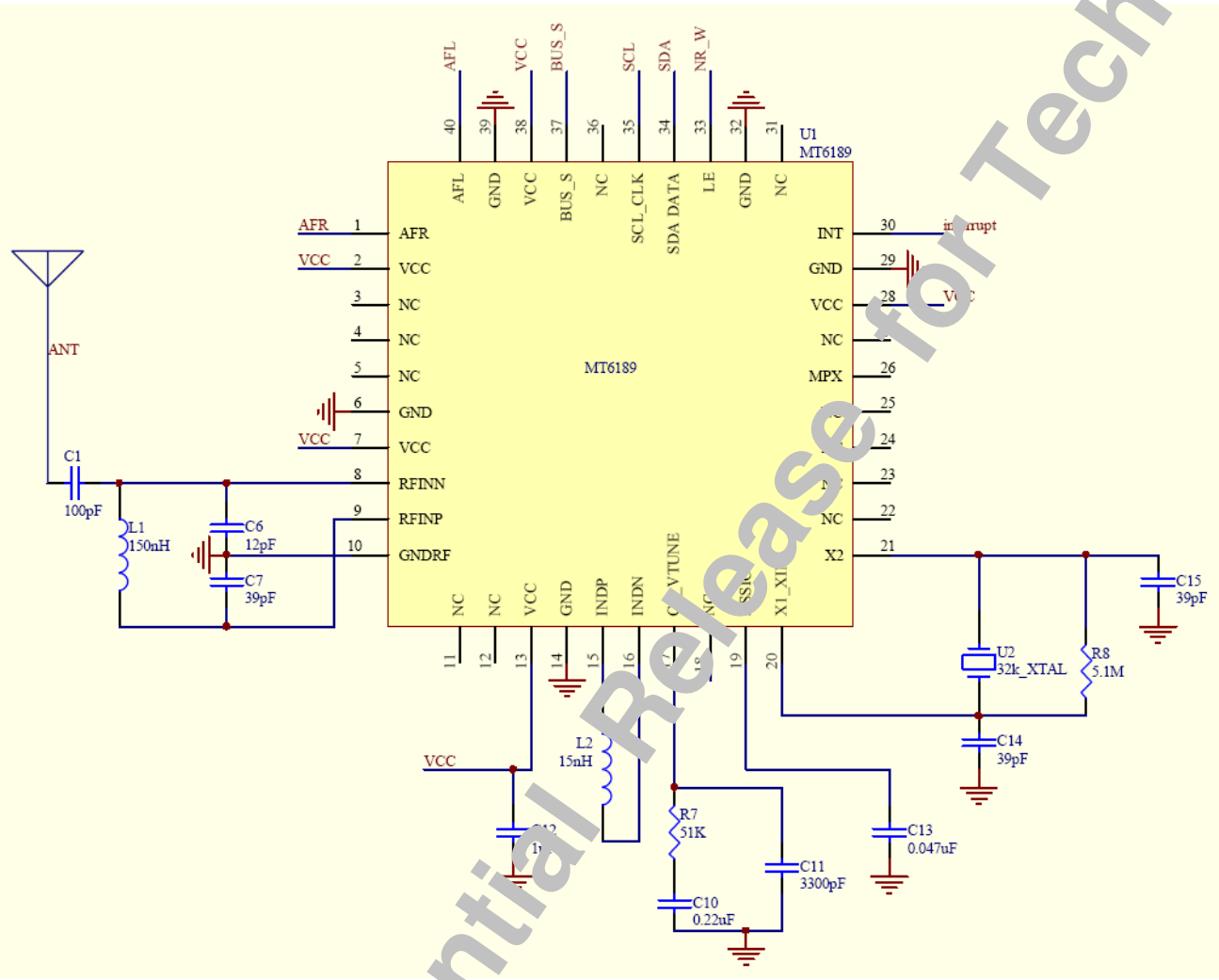
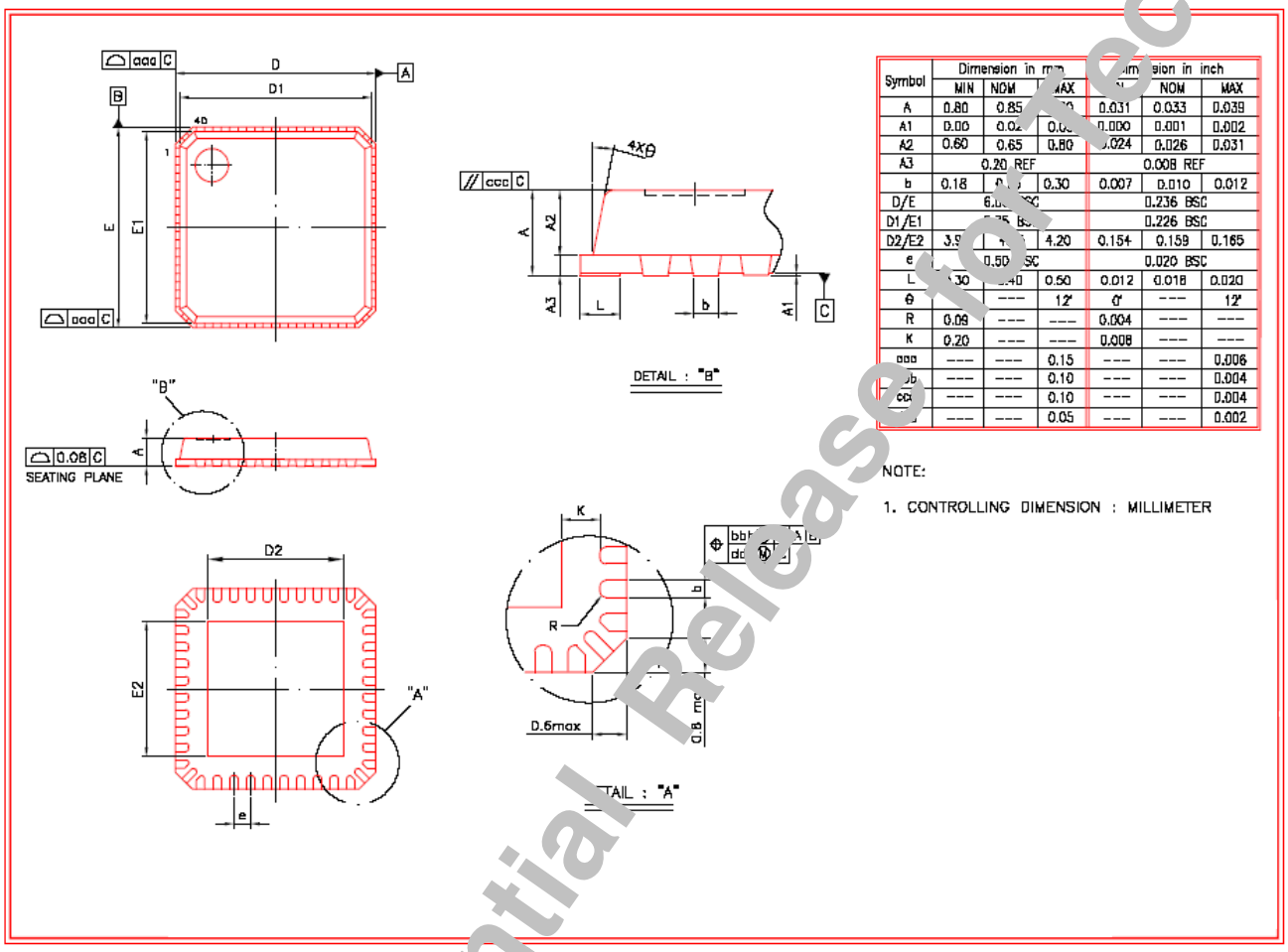


Figure 3 MT6189 with crystal oscillator & antenna matching circuit

5.3 Bill of Materials

components	Value	Description	Annotations
U1		MT6189 FM Tuner	necessary
C12	1uF	0402; supply bypass	necessary
C13	0.047uF	0402; RSSI cap.	necessary
C11	3300pF	0402; loop filter	necessary
R7	51K		
C10	0.22uF		
L2	15nH	0402; inductor	Necessary; Q≧25 is required.
L1	150nH	0402; RF input matching	could be removed with little degradation on sensitivity
C6	12pF		
C7	39pF		

5.4 Package dimensions



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	[illegible]	0.031	0.033	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.60	0.65	0.80	0.024	0.026	0.031
A3		0.20 REF			0.008 REF	
b	0.18	[illegible]	0.30	0.007	0.010	0.012
D/E		6.00 BSC			0.236 BSC	
D1/E1		[illegible] BSC			0.226 BSC	
D2/E2	3.9	[illegible]	4.20	0.154	0.159	0.165
e		0.50 BSC			0.020 BSC	
L	[illegible]	[illegible]	0.50	0.012	0.018	0.020
θ		---	12°	0°	---	12°
R	0.09	---	---	0.004	---	---
K	0.20	---	---	0.008	---	---
aaa	---	---	0.15	---	---	0.006
bbb	---	---	0.10	---	---	0.004
ccc	---	---	0.10	---	---	0.004
[illegible]	---	---	0.05	---	---	0.002

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER

Figure 4 Package dimensions