Om Prakash Singh

Professional Summary

Software Engineer with 7+ years of specialized experience in AI/ML system validation, firmware development, and test automation across Microsoft, Intel, and L&T Technology Services. Expert in building scalable validation frameworks for next-generation AI features, with proven track record of reducing test execution time by 40% and post-silicon bugs by 25%. Passionate about advancing AI technologies through robust system-level validation, having contributed to Copilot+ PCs and Windows Studio Effects. Recognized for driving engineering velocity through innovative tooling, infrastructure improvements, and end-to-end ownership of complex cross-platform integrations.

Experience

Software Engineer 2(Device Validation) Microsoft

Hyderabad, India June 2024 – Present

- Developed PowerShell-based test automation frameworks for validating AI camera features in Windows Studio Effects on Intel, AMD, and QNN IHVs, supporting millions of Copilot+ PC users.
- Reduced test suite run time by 40% through dynamic synchronization and optimization of execution logic, saving 15+ hours weekly across validation cycles.
- Led validation for MEP v1 releases across LNL, STRX, and Cadmus platforms; authored comprehensive infra-setup guides adopted by 3 validation teams.
- Built EdgeOptimizer, an AI agent to track on-device model power usage and CPU/NPU utilization, enabling real-time performance monitoring for Windows AI workloads.
- Implemented semaphore-based synchronization, enabling concurrent multi-model execution across test applications while maintaining resource isolation.
- Performed deep concurrency profiling using WPR/WPA traces, identifying and resolving timing bottlenecks, resource contention, and execution gaps in AI model pipelines.
- Contributed to Copilot+ PCs by building new API-level model validation pipelines and fixing 15+ critical issues across IHV integration, ensuring seamless user experience.
- Integrated and shipped content moderation capability into Phi models used in Copilot, enhancing AI safety and compliance across Microsoft's AI ecosystem.
- Enhanced code coverage by 25% and reliability by integrating AppVerifier into CI flows, reducing production bugs in device validation workflows.
- Owned PS API test pipeline, added cache validation layers, and independently triaged 20+ issues across 10+ release cycles, maintaining 99% pipeline reliability.

Emulation Engineer (Pre-Silicon Validation) Intel

Bangalore, India July 2021 – June 2024

- Owned firmware integration for ADR (Asynchronous DRAM Refresh) flow in the CXL interface and low-power entry/exit scenarios across Xeon platforms.
- Developed 10+ PCIe Gen6 transactor enhancements in C++ and debugged integration with testbench flows.
- Created and maintained Perspec-based test content for reset and power management validations, improving test reuse and automation.
- Validation for idle PM and reset flows, ensuring early bug capture across emulation stages with Simics and Zebu platforms.
- Diagnosed and fixed 15+ cross-IP bugs involving silicon interface failures, platform timeouts and firmware issues.
- Contributed to a 25% reduction in post-silicon bugs by improving validation coverage and speeding up triage by using AI tools.

L&T Technology Services

Bangalore, India Sep 2018 – July 2021

- Designed and implemented a modular test automation suite in Python for thermal and power management of NVMe-based storage platforms.
- Developed 25+ test scenarios to evaluate power states, thermal thresholds, and firmware transitions.
- Conducted post-silicon debugging using JTAG and Metaware, analyzing register maps and firmware traces for system-level failures.
- Performed NVMe 1.3 protocol validation using Lecroy analyzers, OakGate, and Exercisers, ensuring spec compliance across firmware revisions.
- Collaborated with FW and validation teams to resolve 10+ power-related issues.

Key Projects

- EdgeOptimizer AI Agent (Microsoft, 2025) Developed an intelligent monitoring system to track ondevice model power usage and CPU/NPU utilization across Windows Studio Effects, enabling real-time performance optimization and resource management for AI workloads.
- Copilot+ PC Validation Infrastructure (Microsoft, 2024) Built comprehensive API-level model validation pipelines for Copilot+ PCs, ensuring seamless integration across Intel, AMD, and QNN IHVs while resolving critical compatibility issues.
- CXL Firmware Integration Platform (Intel, 2023-2024) Owned end-to-end firmware integration for Asynchronous DRAM Refresh (ADR) flows in CXL interface, covering low-power scenarios and reset management across Xeon server platforms.
- NVMe Thermal Management Suite (L&T/SanDisk, 2020-2021) Designed and implemented modular Python-based automation framework for thermal and power management validation of NVMe storage platforms, covering 25+ test scenarios and firmware transition states.

Education

- o M.Tech in CSE, National Institute of Technology (NIT), Durgapur 2018
- o B.Tech in CSE, RGPV, Bhopal 2015

Technical Skills

- o Programming Languages: Python, PowerShell, C, C++, Perl, Shell Scripting
- o AI/ML Frameworks: ONNX Runtime, LLM Phi Models, Content Moderation APIs
- o Development Areas: Firmware Development, System Validation, Performance Optimization, API
- o Tools & Platforms: JTAG, WinDbg, WPR/WPA, Metaware, VS Code, AppVerifier, Simics, Zebu
- o System Technologies: Windows Internals, PCIe, NVMe, SOC Architecture, Power Management
- o Domain Expertise: LLM Integration, Agentic AI, Silicon Validation, Device Validation, Storage Protocols
- o Version Control & CI/CD: Git, GitHub, PowerShell-based CI flows, Automated Testing Pipelines

Awards & Recognition

- o Microsoft
 - Jan 2025 Recognized for performance optimization efforts that reduced test execution time by ~40%.
 - Sep 2024 Awarded for building and setting up validation infrastructure for Copilot+ PCs.
- o Intel
 - Received "Star of the Month" for early bug discovery and validation of CXL firmware flows.
- o L&T Technology Services (Client: SanDisk)
 - Awarded Spot Awards for SDExpress POC validation in power/reset flows.