Wen Fan

Email: fan372@purdue.edu
Homepage: https://fanweneddie.github.io/

EDUCATION

Purdue University West Lafayette, USA
Major: Electrical and Computer Engineering *Aug. 2024 – Present*
Degree: PhD
Advisor: Prof. Jenna DiVincenzo

University of Science and Technology of China (USTC) Hefei, China
Major: Computer Science and Technology *Sept. 2018 – Jun. 2022*
Degree: Bachelor
GPA: 3.75/4.3

RESEARCH INTEREST

Program Verification, Software Engineering

PUBLICATIONS

Evaluating the Ability of Large Language Models to Generate Verifiable Specifications in VeriFast [paper]
Marilyn Rego*, Wen Fan*, Xin Hu, Sanya Dod, Zhaorui Ni, Danning Xie, Jenna DiVincenzo, Lin Tan. The 2nd ACM international conference on AI Foundation Models and Software Engineering (FORGE 2025).

PROJECTS

Evaluating LLMs on Generating Specifications for Separation Logic Purdue University
Advisor: Prof. Jenna DiVincenzo *Sept. 2024 – Now*
Program verification checks whether a program satisfies a specification. Given a program and partial specification, we evaluate how well LLMs can generate full specification in Separation Logic, including the number of errors and the preservation of functional behavior of the specification and source code.

Optimizing Gradual C0 Program Verifier by Adding Parallelism Purdue University
Advisor: Prof. Jenna DiVincenzo *Jun. 2024 – Aug. 2024*
The Gradual C0 verifier uses symbolic execution to verify C0 program. However, its execution on branches is in a sequential manner, which limits the performance on a large program. In this work, I added parallelism on its execution and reduced the static verification time by 41% on cparser.c0. [poster]

- Discovered that the performance of Gradual C0 is bottlenecked in sequentially executing branches
- Designed and Implemented the parallel execution on branching
- Discovered that static verification is accelerated by enabling parallelism, but doesn't scale well.

DSLAB (Sharded and Fault Tolerant Distributed Key-Value Store) CS505 project at Purdue University
DSLAB is a framework for building and debugging distributed systems for educational purposes. I did this lab with my friend and passed most of the tests.

- Implemented Primary-Backup, Paxos and Two Phase Commit protocols.
- Debugged to pass more than 90% of tests (including searching tests on corner cases).

Tiny MIPS Pipelined CPU Computer Organization and Design Project at USTC

This lab builds a 5-staged pipelining CPU of simplified MIPS instruction set on FPGA, which runs a Fibonacci Number calculator as a simple application.

- Implemented the circuit in VeriLog
- Tested both on waveform and FPGA

TALKS

[2025/4] Presented our work "Evaluating the Ability of Large Language Models to Generate Verifiable Specifications in VeriFast" on PurPL seminar and FORGE conference

[2024/10] Presented the poster on "Optimizing Gradual C0 Program Verifier by Adding Parallelism" in Purdue ECE Symposium

TEACHING ASSISTANT EXPERIENCE

Mathematical Logic, USTC *Spring 2021*

CS252 Systems Programming, Purdue University *Fall 2022, Spring 2023, Spring 2024*

CS251 Data Structures, Purdue University *Fall 2023*

AWARDS

Huawei Scholarship *Nov. 2020*

Huaxia Talent Program at USTC *Jun. 2022*

SKILLS

Programming Languages: C, C++, Java, Python, Go
Tools: Git, Linux, Docker, JetBrains IDE, LaTeX, Google Docs/Slides/Sheets
Algorithms: Leetcode 100+
Languages: English, Chinese