

# The ANCHOR Verifier for Blocking and Non-Blocking Concurrent Software

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Verifying the correctness of performance critical concurrent software with subtle synchronization is notoriously challenging, and many existing verifiers are either inadequately expressive or excessively burdensome to use. We present the ANCHOR verifier, which is based on a new, expressive formalism for specifying synchronization disciplines that naturally matches how programmers should think about reduction-based correctness arguments. ANCHOR proves concurrent components are race-free; do not go wrong; respect their synchronization disciplines; and are preemptive/cooperative equivalent, meaning that thread interference only happens at explicit yield annotations. Experiments on textbook concurrent data structures and the FASTTRACK analysis demonstrate that ANCHOR significantly reduces the burden of concurrent verification.

## 1 INTRODUCTION

Building maximally performant concurrent systems necessitates using a wide variety of synchronization disciplines, ranging from locks, read-only data structures, and thread-local exclusive access to sophisticated non-blocking algorithms based on atomic compare-and-swap. Additionally, synchronization disciplines may vary over time, depending on the values of flags or other data structures, may provide different access permissions to reads and writes, and may restrict permissible writes to, for example, enforce monotonically increasing updates. Reasoning about the correctness of algorithms based on such subtle synchronization is tricky and error-prone, particularly in the presence of an unbounded number of preemptive threads.

Much prior work has produced tools for verifying concurrent software [Brookes 2007; Chajed et al. 2018; Cohen et al. 2009; Elmas 2010; Feng 2009; Flanagan et al. 2008, 2002, 2005; Freund and Qadeer 2004; Gu et al. 2018; Hawblitzel et al. 2015a; Jung et al. 2015; Leino et al. 2009; Lorch et al. 2020,?; O’Hearn 2004; Xu et al. 2016; Yi et al. 2012]. However, using such tools remains a daunting task in practice. Some tools are limited in the types of synchronization they can effectively reason about, while others present programming models far from typical programming languages or require much time and effort to write a verifiable specification or proof script. Diagnosing verification failures and addressing them is also difficult if the verifier is not carefully designed to provide meaningful feedback.

This paper presents the ANCHOR concurrent software verifier that is designed to address two central challenges in concurrent software verification:

- (1) How to clearly and concisely *specify* the kinds of often-sophisticated synchronization mechanisms used in concurrent software.
- (2) How to *verify* that each thread in a system behaves correctly, under the assumption that interleaved operations of other threads obey the documented synchronization discipline.

Clearly, these specification and verification challenges are interdependent. At one extreme, standard model checking avoids the need for synchronization specifications but has trouble scaling to large numbers of threads. Conversely, scalable verification necessitates precise, intuitive, and expressive synchronization specifications.

ANCHOR utilizes Lipton’s theory of reduction [Lipton 1975], which employs a commuting argument to verify that thread interference can be safely assumed to occur only at yield annotations. ANCHOR’s reduction analysis is enabled by synchronization specifications documenting the commutativity of each heap access as one of Left-moving, Right-moving, Both-moving, Non-moving,

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or `Error` (for prohibited accesses). For example, a lock acquire operation right-commutes across a subsequent operation of a different thread; a race-free memory access both right- and left-commutes across preceding operations of other threads; and accessing a lock protected memory location without holding the lock is an Error. The commutivity of a memory access may depend on a variety of conditions, including which locks are held, whether the location is thread-local, whether the access is a read or a write, whether a particular flag is set to true, and so on. To support these dependencies ANCHOR supports conditional synchronization disciplines of the form

$$\text{SyncDiscipline} ::= B \mid R \mid L \mid N \mid E \\ \mid \text{expr} ? \text{SyncDiscipline} : \text{SyncDiscipline}$$

ANCHOR's synchronization specifications are more expressive than prior tools (e.g. [Flanagan et al. 2008, 2002; Freund and Qadeer 2004; Hawblitzel et al. 2015a,b; Yi et al. 2012]) in that they support conditional synchronization disciplines and they explicitly specify how each access commutes with concurrent operations by other threads. This expressiveness enables ANCHOR to

- check synchronization specifications for self-consistency properties even before the first line of implementation code is written;
- verify more complex algorithms;
- provide a better intuitive model of which code fragments are reducible; and
- provide better diagnostic error messages to the programmer.

The ANCHOR guarantees that thread interference is only observable at yield annotations. As such, ANCHOR ensures that concurrent programs exhibit the same behavior under both

- a *preemptive* scheduler that context switches at any point, and
- a *cooperative* scheduler that context switches only at yield annotations.

We call this guarantee *preemptive/cooperative (P/C) equivalence*. It enables subsequent higher-level (formal or informal) reasoning to be based on the more intuitive cooperative scheduler, even though the code runs on standard, preemptive hardware. In addition, code without yields is guaranteed to be atomic, so P/C equivalence can be seen as an extension of atomicity supporting complex synchronization with intentional thread interference [Yi et al. 2012].

ANCHOR supports verification of cas-based non-blocking algorithms, such as the cas-based atomic counter shown in Figure 2. For that counter, ANCHOR can infer that a read from `n` followed by a successful cas is reducible, because knowing that `n` is free of ABA problems [Michael 2004] rules out the possibility of intervening concurrent writes. This cas support complicates our formal development and implementation but is critical for verifying high-performance non-blocking algorithms that rely on ABA-freedom arguments for correctness.

Our correctness argument for ANCHOR is formalized as a stack of three operational semantics for an idealized subset of Java. The first is a *standard semantics* formalizing the execution behavior programs. The second is an *instrumented semantics* extending the standard semantics to check that the synchronization discipline is respected and that each yield-free code fragment is reducible. The final is a *thread-modular semantics* that executes one thread of the instrumented semantics in isolation, using the synchronization specifications to model possible behaviors of interleaved threads at yield points, which enables ANCHOR to scale to an unbounded number of threads. These three semantics are related by appropriate notions of simulation.

The ANCHOR implementation analyzes the behavior of code under the thread-modular semantics via a translation to Boogie [Barnett et al. 2005]. If Boogie shows the thread-modular semantics does not go wrong, then the original program

- does not go wrong under the standard preemptive semantics,
- is free of data race conditions and hence exhibits sequentially-consistent behavior,

- satisfies its synchronization specification,
- satisfies its method specifications, and
- is P/C equivalent.

We have evaluated ANCHOR on a variety of examples ranging from textbook data structures and algorithms [Herlihy and Shavit 2008] to the FASTTRACK race detection algorithm [Flanagan and Freund 2010; Wilcox et al. 2018]. Our experience shows that ANCHOR is readily able to verify programs using subtle and complex synchronization disciplines without an excessive specification or proof burden. For example, verifying P/C equivalence for the complex FASTTRACK algorithm required adding about 50 lines of specification to 220 lines of implementation code. Verifying functional correctness required adding about 150 lines of specification to those 220 lines. Prior work verifying those functional requirements in CIVL necessitated adding over 500 lines of specification to 250 lines of CIVL code [Flanagan et al. 2017; Wilcox et al. 2018].

In summary, the contributions of this paper include:

- A concise and expressive notation for synchronization specifications that describes how memory accesses commute with concurrent operations. (Sections 2 and 4)
- A set of self-consistency checks to detect errors in synchronization specifications early in the development process, even before the first line of concurrent code is written. (Section 5)
- A verification technique that uses synchronization specifications to perform reduction and thread-modular reasoning to verify concurrent code with sophisticated synchronization and an unbounded number of threads. (Sections 6 and 7)
- A correctness argument based on three related operational semantics. (Sections 6 and 7)
- The ANCHOR verifier, an implementation of our technique for a Java-like language, as well as a compiler that generates executable code directly from verified ANCHOR source. (Section 8)
- An evaluation of ANCHOR demonstrating its effectiveness on a variety of concurrent algorithms. (Section 9)

## 2 BACKGROUND AND EXAMPLES

**Review: Lipton’s Theory of Reduction.** To verify P/C-equivalence, ANCHOR leverages Lipton’s theory of reduction [Lipton 1975], which is based on classifying how operations of one thread  $t$  commute with concurrent operations of another thread  $u$ .

- A  $t$ -operation is a *right-mover* (denoted R) if it commutes “to the right” of any subsequent  $u$ -op, in that performing the steps in the opposite order (i.e.  $u$  followed by  $t$ ) does not change the resulting state. For example, a lock acquire by  $t$  is a right-mover because any subsequent  $u$ -op cannot modify that lock.
- Conversely, a  $t$ -operation is a *left-mover* (denoted L) if it commutes “to the left” of a preceding  $u$ -operation. For example, a lock release by  $t$  is a left-mover because any preceding  $u$ -op cannot modify that lock.
- An operation is a *both-mover* (B) if it is both a left- and a right-mover, and it is a *non-mover* (N) if neither a left- nor a right-mover. For example, a race-free memory access is a both-mover because there are no concurrent, conflicting accesses, but an access to a race-prone variable is a non-mover since there may be concurrent writes.

Consider a sequence of steps performed by a particular thread that consists of zero or more right-movers (R); at most one non-mover (N); and zero or more left-movers (L). Such a sequence is said to be *reducible*; any interleaved steps of other threads can be “commuted out” to yield an execution in which the steps run in a cooperative fashion without interleaved steps other threads. For example, a lock acquire followed by a race-free access and a lock release is reducible. ANCHOR

```

1  class SyncSpecs {
2    volatile int x    moves_as N;
3    volatile int y    moves_as B; // <-- invalid
4    int z             moves_as holds(this) ? B : E;
5
6    public void double() {
7      R  acquire(this);
8      B  int t = this.z;
9      B  this.z = 2 * t;
10     L  release(this);
11   }
12 }

```

Fig. 1. ANCHOR synchronization specification examples.

uses this theory to show that each method is P/C equivalent by verifying that all execution paths consist of reducible sequences separated by yields.

**Synchronization specifications.** To leverage Lipton’s theory, ANCHOR relies on a synchronization specification that describes when each thread can access each memory location and how each access commutes with steps from other threads. In addition to the four movers listed above, we use the error-mover (E) to denote accesses are not permitted. Thus, our language of movers, and their partial ordering based on decreasing commutativity.

$$m \in \text{Mover} ::= B \mid L \mid R \mid N \mid E$$

$$B \sqsubset \{L, R\} \sqsubset N \sqsubset E$$

These movers are the basic building blocks of our conditional synchronization disciplines:

$$\text{SyncDiscipline} ::= m$$

$$\mid \text{expr} ? \text{SyncDiscipline} : \text{SyncDiscipline}$$

Here, *expr* may be any boolean expression, and it may refer to the following special variables and predicates.

*this*: The object being accessed.

*tid*: The unique thread identifier of the accessing thread.

*isRead()*: Whether the access is a read.

*newValue*: The value being written, if the access is a write.

*holds(l)*: Whether lock for object *l* is held, where *l* is a path expression (*i.e.* a local variable optionally followed by field or array accesses, such as *x*, *x.f*, *a[i]*, or *y.f.g*).

*isLocal(l)*: Whether *l* is local to the current thread.

*isShared(l)*: Whether *l* is potentially shared.

Figure 1 illustrates these synchronization specifications. The *moves\_as* specification on the volatile field *x* on line 3 indicates that *x* can be accessed by any thread at any time, and that all accesses are thus non-movers (N), as they may not commute with concurrent accesses. ANCHOR requires any fields exhibiting N, R, or L commutivity must be declared volatile to ensure race freedom and sequentially-consistent behavior.

```

197 13 class AtomicInt {
198 14     noABA volatile int n  moves_as isRead() ? N
199 15                               : (newValue == this.n + 1 ? N : E)
200 16     yields_as newValue >= this.n;
201 17
202 18     ensures this.n == old(this.n) + 1;
203 19     public int inc() {
204 20         while (true) {
205 21             N/R   int x = this.n;
206 22             B/N   if (cas(this.n,x,x+1)) { return n+1; }
207 23                 yield;
208 24         }
209 25     }
210 26 }

```

Fig. 2. AtomicInt example.

In contrast, the specification on the field *y* claims that unrestricted accesses to *y* are all both-movers (B). This specification is not valid since a write to *y* cannot commute with a concurrent write. ANCHOR detects such errors even before any code using *y* is written.

Field *z* is only accessible by a thread holding the lock of the enclosing object, specified using the `holds(this)` predicate. Such lock-protected accesses are both-movers (B) as there are no concurrent accesses. Accesses without holding the lock are errors (E).

These specifications document the synchronization discipline and also facilitate reduction arguments. For example, method `double()` on line 6 is atomic because it consists of a lock acquire (R), a race-free read (B), a race-free write (B), and a lock release (L). Figure 1 includes these movers to the left of the code for clarity.

ANCHOR supports abbreviations for common synchronization idioms including the following:

```

225         immutable  ≡  isRead() ? R : E
226         readonly   ≡  isRead() ? B : E
227         thread_local ≡  isLocal(this) ? B : E
228         guarded_by l ≡  holds(l) ? B : E
229         write_guarded_by l ≡ isRead() ? (holds(l) ? B : N)
230                               : (holds(l) ? N : E)
231
232

```

Writes to immutable fields are forbidden (E), but reads are okay and are right-movers due to the absence of subsequent writes. Reads of immutable fields are not left-movers, however, as an immutable field could have changed before reaching its immutable state. The `readonly` abbreviation is for cases when a field's value is fixed from the moment the field becomes accessible. Reads of `readonly` fields are thus both-movers. For thread-local fields of an object, the allocating thread initially has exclusive access (B). If the object ever becomes shared between threads, subsequent accesses are not allowed (E).

The `guarded_by` abbreviation captures lock-based exclusive access, as for the field *z* on line 4. The `write_guarded_by` abbreviation captures a more subtle discipline where a lock must be held for writes but not necessarily for reads. Reads while holding the lock are both-movers (B) since there cannot be concurrent writes; reads without holding the lock are non-movers (N) since there may be concurrent writes; and writes are non-movers (N) since there may be concurrent reads.

**AtomicInt Example.** As an illustration of ANCHOR's cas-based reasoning, consider class AtomicInt in Figure 2. The synchronization specification for volatile field n

```
moves_as isRead() ? N
      : (newValue == this.n + 1) ? N : E
```

indicates that the field can be read by any thread at any time (N) and that writes (also N) must increment n. Consequently, the field n is ABA-free [Michael 2004], meaning that the field is never changed from a value A to B and then back to A again.

The last loop iteration in inc() consists of a read of n into x, followed by a successful cas changing this.n from x to x+1. Since n is ABA-free, no other thread could have written to n between the read and the successful cas. As such, ANCHOR considers the read operation to be a right-mover, provided it is followed by a successful cas [Wang and Stoller 2005]. On all earlier iterations, the read of this.n is followed by a failed cas. We permit cas to fail non-deterministically, meaning that we can treat failed cas operations as both-movers. Thus, any call to inc() performs the following sequence of heap operations:

$$\left[ \underbrace{x = \text{this}.n; \text{failed-cas}; \text{yield}}_{N \quad B} \right]^* \underbrace{x = \text{this}.n; \text{successful-cas}}_{R \quad N}$$

The sequence  $[N; B; \text{yield}]^* R; N$  consists of reducible sequences separated by yields and is P/C equivalent. Moreover, the reducible sequences are all no-ops, except for the last, which has the heap effect of atomically incrementing this.n, as required by inc()'s specification.

This cas-based reasoning is critical for verifying the correctness of many concurrent algorithms, including various non-blocking algorithms. It involves verifying ABA-free fields and treating reads from them differently depending on whether they or not they are followed by a successful cas operation. To the best of our knowledge ANCHOR is the first SMT-based verifier that automates this kind of reasoning.

**LockBasedStack and LockFreeStack Examples.** The LockBasedStack class in Figure 3 contains a head node with initial value null. The push() method allocates a new Node, initializes its item and next fields via the constructor, and then stores it in head. To respect the synchronization discipline, the push() method acquires the lock on the stack object prior to accessing head. The pop() method similarly acquires the stack's lock, but then busy waits until the stack has at least one element in it. While waiting, it releases and re-acquires the lock. Since other threads may change head between the release and acquire, we include a yield at that point. Since yield annotations are part of a program's specification, they do not affect the run-time behavior of the code.

The alternative LockFreeStack implementation in Figure 3 uses a cas operation for optimistic concurrency control. Other threads may change head between the read and cas operation, necessitating the inclusion of a yield between those operations. Unlike the inc example in Figure 2, a successful cas operation does not rule out the possibility that head changed after the read, since another thread could call push and then pop, resulting in head being changed and then restored to the original value. Consequently, head cannot be declared ABA-free.

We discuss method specifications for push() and pop() below. Interestingly, despite using different synchronization disciplines, both stack implementations satisfy the same method specifications.

**ANCHOR Error Messages.** A key feature of ANCHOR is its ability to provide understandable and actionable error messages. To this end, ANCHOR embeds auxiliary information in the generated Boogie code for mapping Boogie errors and counterexamples back to meaningful messages in the original code. We illustrate the types of messages ANCHOR reports for synchronization and reduction errors below. We have simplified and reformatted some parts of these examples for

```

295 class Node {
296     int item moves_as
297         isLocal(this) ? B : readonly;
298     Node next moves_as
299         isLocal(this) ? B : readonly;
300
301     Node(int item, Node next) {
302         this.item = item; this.next = next;
303     }
304 }
305
306 class LockBasedStack {
307     Node head moves_as
308         isLocal(this) ? B : guarded_by this;
309
310     public int push(int item) {
311         R acquire(this);
312         B Node node = new Node(item, this.head);
313         B this.head = node;
314         L release(this);
315     }
316
317     public int pop() {
318         while (true) {
319             R acquire(this);
320             B if (this.head != null) break;
321             L release(this);
322             yield;
323         }
324         B int value = this.head.item;
325         B this.head = this.head.next;
326         L release(this);
327         return value;
328     }
329 }
330
331 class LockFreeStack {
332     volatile Node head moves_as
333         isLocal(this) ? B : N;
334
335     public void push(int item) {
336         while (true) {
337             N Node next = this.head;
338             B Node nu = new Node(item, next);
339             yield;
340             B/N if (cas(this.head, next, nu) {
341                 break;
342             }
343         }
344     }
345
346     public int pop() {
347         while (true) {
348             N Node top = this.head;
349             if (top != null) {
350                 B Node next = top.next;
351                 yield;
352                 B/N if (cas(this.head, top, next)) {
353                     return top.item;
354                 }
355             }
356             yield;
357         }
358     }
359 }

```

Fig. 3. LockBasedStack and LockFreeStack examples.

clarity and brevity, but they embody the key aspects how ANCHOR reports errors. We first consider the following synchronization error trace reported when the following method is added to the LockBasedStack class from Figure 3.

<pre> 335 public void buggy() { 336     this.push(10); 337     // must acquire lock here 338     assert this.head.item == 10; 339 } </pre>	<pre> call this.push(10) [R] acquire(this); ... [L] release(this); [E] tmp1 = this.head; [!isLocal(this) &amp;&amp; !holds(this) =&gt; E] </pre>
--	--

The trace contains the commutivity of each synchronization and memory access, as well as how that commutivity was computed. Such traces are often sufficient to immediately identify a synchronization specification violation, as indicated by the error commutivity E for the access to this.head



without holding the lock. After inserting the necessary synchronization, ANCHOR reports the following reduction error trace.

```

public void buggy() {
  this.push(10);
  // yield necessary here
  acquire(this);
  assert this.head.item == 10;
  release(this);
}

call this.push(10)
[R]  acquire(this);
    node = new Node();
[B]  tmp = this.head; [!isLocal(this) && holds(this) => B]
[B]  node.item = 10;  [isLocal(node) => B]
[B]  node.next = tmp; [isLocal(node) => B]
[B]  this.head = node; [!isLocal(this) && holds(this) => B]
[L]  release(this);
[R]  acquire(this); // R cannot follow L in reducible trace

```

As before, the reduction error message allows us to readily identify either a missing yield or a situation in which the synchronization specification fails to ensure the necessary commuting properties. Once the missing yield is inserted, ANCHOR reports that the assertion may fail, again providing a failing trace:

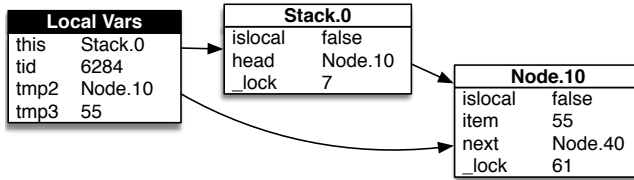
```

public void buggy() {
  this.push(10);
  yield; // added
  acquire(this);
  assert this.head.item == 10;
  release(this);
}

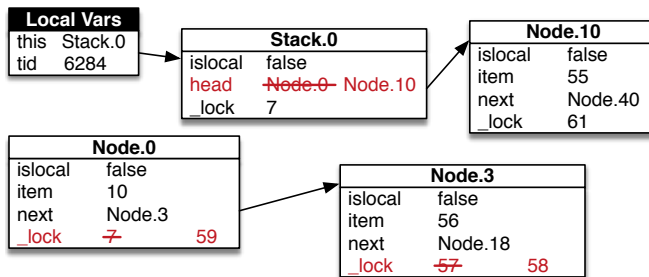
call this.push(10)
[R]  acquire(this);
[B]  ... as before ...
[L]  release(this);
=== yield;
[R]  acquire(this);
[B]  tmp2 = this.head; [!isLocal(this) && holds(this) => B]
[B]  tmp3 = tmp2.item; [!isLocal(tmp2) && isRead() => B]
    assert tmp3 == 10;

```

As in some other verification tools [Le Goues et al. 2011], ANCHOR provides a way to visually inspect the program state via memory snapshots for each line of the trace. The snapshot immediately before the assert is:



The record for the object Node.10 includes its item and next fields, whether it is thread-local, and the tid of the thread holding its lock (if any). From this snapshot, we see that the head node stores 55 instead of the expected value 10. Inspecting the snapshot for the earlier yield indicates that this is where the change occurred.





```

393 147 class VarState {
394 148     volatile int readEpoch moves_as (this.readEpoch != SHARED) ? write_guarded_by this
395 149                                     : immutable;
396 150     int[moves_as (this.readEpoch != SHARED) ? guarded_by this
397 151                 : isRead() ? (holds(this) || tid == index ? B:E)
398 152                 : (holds(this) && tid == index ? B:E)]
399 153     vc moves_as (this.readEpoch != SHARED) ? guarded_by this : write_guarded_by this;
400 154 }

```

Fig. 4. FASTTRACK VarState synchronization specification.

That snapshot shows the pre-*yield* state and any changes that occurred during the *yield*. Some changes are irrelevant, such as for lock holders, but we can also see that `this.head` was changed to object `Node.10` instead of `Node.0` during the *yield*. Snapshots like these, coupled with the detailed traces, have proven effective for debugging errors both in specifications and in code.

**FASTTRACK VarState Synchronization Discipline.** We conclude this section with the class `VarState` in Figure 4 that shows a more involved synchronization discipline derived from the FASTTRACK dynamic data race detector [Flanagan and Freund 2010; Wilcox et al. 2018]. The field `readEpoch` is initially *write\_guarded\_by this*, as shown on line 147, but becomes *immutable* once it is set to the special value `SHARED`. The array declaration on lines 149–152 has the form

```
int[moves_as SyncDiscipline] vc moves_as SyncDiscipline';
```

to indicate that the field `vc` is protected by *SyncDiscipline'* and the array element `vc[index]` is protected by *SyncDiscipline* (which may mention `index`). According to this declaration, the array entry `vc[index]` is initially *guarded\_by this* (line 149). However, once `readEpoch` becomes `SHARED`, the synchronization discipline for `vc[index]` changes. That memory location can then be read by any thread holding the lock *this* or by the thread with thread identifier `tid == index` (line 150). Writes to `vc[index]` require both holding the lock *and* having `tid == index` (line 151). Under this discipline, all permitted accesses to `vc[index]` are both-movers.

These complex synchronization specifications are necessary to verify the reducibility of the fast-path code from the core FASTTRACK algorithm, shown below, which elides locking to maximize performance.

```

424     public boolean read(VarState sx) {
425     B     int e = ...; // e cannot be SHARED
426
427         // fast path:
427     N/R    int r = sx.readEpoch;
428         if (r == e) return true;
429         if (r == SHARED &&
430     N       sx.vc[tid] == e) return true;
431         yield;
432         // slow path:
433     R       acquire(sx);
434     N       ...
435     L       release(sx);
436     }

```

If `sx.readEpoch` is not `SHARED`, the fast-path code is clearly reducible since it only reads `sx.readEpoch` (N). If `sx.readEpoch` is `SHARED`, the code reads `sx.readEpoch` (now R because it is *immutable*), reads `vc` (N because it is *write\_guarded\_by* a lock that is not held, line 152), and reads `vc[tid]` (B because `tid` is the index being accessed). Thus, this sequence is also reducible.

### 3 RELATED WORK

ANCHOR and Calvin-R [Freund and Qadeer 2004] both verify concurrent software using reduction and thread-modular reasoning. ANCHOR improves on Calvin-R in terms of expressiveness and usability: it permits different synchronization specifications for reads and writes; its synchronization specifications explicitly describe the mover status of each access, enabling additional self consistency checks; it supports explicit yields to a document thread interference; it verifies P/C equivalence; and it provides better error messages with traces and heap snapshots upon verification failure. Unlike Calvin-R, ANCHOR can support method calls via inlining, thus avoiding the burden and complexity of specifying all methods. Most of our benchmarks could not be verified with Calvin-R.

ANCHOR is inspired by CIVL [Hawblitzel et al. 2015a] (and its predecessor QED [Elmas 2010]), and by the difficulties we encountered while verifying complex algorithms in CIVL. CIVL verifies software through a series of layers of repeated abstraction and reduction, but its expressiveness introduces significant user-visible complexity. Indeed, its acronym “Concurrent Intermediate Verification Language” suggests that it is not targeted towards user-level verification. Moreover, the CIVL source language is not executable. In contrast, ANCHOR supports standard imperative object-oriented code enriched with specifications in order to achieve both expressiveness and usability. Section 9 compares verifying the FastTrack data race detector in both ANCHOR and CIVL.

Like ANCHOR, Armada [Lorch et al. 2020] also focuses on SMT-based verification of concurrent programs via a combination of reduction and thread-modular reasoning. Armada also supports additional strategies such as data abstraction, which facilitates simpler (higher-level) method specifications. A key difference between Armada and ANCHOR is our emphasis on formally specifying synchronization disciplines, checking them for consistency and appropriate commuting properties independently from the code, and only then checking that code conforms to those specifications. In contrast, Armada checks commuting properties for all pairs of operations in the code itself. We believe our approach offers several benefits, including a better documentation, more modular development methodology (outlined in Section 9), more understandable errors messages, and potentially better scalability. In addition, Armada does not include the built-in support for cas that ANCHOR does, including verification of ABA-free fields and automatically upgrading any read followed by a successful matching cas to be a right-mover. One avenue for future work is to leverage our expressive synchronization specifications in tools like Armada that support data abstraction.

CSpec [Chajed et al. 2018] is a Coq library for verifying concurrent systems modeled in Coq [Coq 2019] using movers and reduction. It is very expressive, particularly because additional proof techniques can be added as additional Coq code, but that flexibility comes at the price of needing to write significant Coq code for both specifications and proofs.

CCAL [Gu et al. 2018] provides a compositional semantic model in Coq for composing multi-threaded layers of software and for verifying the correctness of software components. It focuses on rely-guarantee reasoning rather than reduction.

Lipton [Lipton 1975] first proposed reduction as a way to reason about concurrent programs without considering all possible interleavings. Doeppner [Jr. 1977], Back [Back 1989], and Lamport and Schneider [Lamport and Schneider 1989] extended this work to proofs of general safety properties, Misra [Misra 2001] to programs built with monitors [Hoare 1974] communicating via procedure calls, and Cohen and Lamport [Cohen and Lamport 1998] to proofs of liveness properties.

Azedah and Vandikas [Farzan and Vandikas 2019] recently extended these ideas to encompass a search for a sound reduction strategy, thus enabling automatic safety proofs of complex systems for which non-reduction proofs are not feasible. ANCHOR currently assumes that reducible code blocks are explicitly delimited with yield statements, but incorporating a search for optimal yields is an interesting topic for future work.

A large body of prior work has addressed the important problem of the current software verification. Much work is focused on concurrent software model checking [Chamillard et al. 1996; Musuvathi et al. 2008; Yahav 2001], which is hard to apply to concurrent components with an unbounded number of threads. Partial-order methods [Godefroid 1997; Godefroid and Wolper 1991; Peled 1994] have also been used to limit state-space explosion while model checking concurrent programs. Type-based techniques [Abadi et al. 2006; Agarwal and Stoller 2004; Boyapati and Rinard 2001; Grossman 2003] have proven useful for systems with simpler synchronization disciplines than those studied here. Dynamic concurrency analyses [Christiaens and Bosschere 2001; Flanagan and Freund 2010; Nishiyama 2004; Pozniansky and Schuster 2007; Savage et al. 1997; Schonberg 1989; von Praun and Gross 2001; Wilcox et al. 2018; Yu et al. 2005,?] are also very useful in practice but they do not provide ANCHOR's strong correctness guarantees. The notion of atomicity is a useful and concise method specification [Flanagan and Freund 2004], but it is often not applicable to concurrent software with intentional thread interference. P/C equivalence is a natural extension of atomicity that uses yields to document intentional interference between threads [Adya et al. 2002; Amadio and Zilio 2004; Boudol 2007; Cerný et al. 2017; Yi et al. 2015].

#### 4 THE ANCHORJAVA CONCURRENT LANGUAGE: SYNTAX AND SEMANTICS

We formalize ANCHOR's verification methodology for the idealized concurrent language ANCHOR-JAVA shown in Figure 5. Each class definition includes field and method declarations. Each method declaration  $mn(\bar{x}) \{ s; \text{return } z \}$  includes a unique method name  $mn$ , formal parameters  $\bar{x}$ , and a body  $s$  followed by a return statement. (We discuss method specifications in Section 8 below.) We omit static types and local variable declarations, which are orthogonal to our development. Statements are mostly in A-normal form [Flanagan et al. 1993; ?].

States  $\Sigma$  consist of a heap  $H$  and a collection of threads  $T$ , where each thread  $(s, \sigma)$  combines a statement  $s$  with its thread local environment  $\sigma$ . Expressions  $e$  are left abstract, and we use  $\sigma(e)$  to denote the evaluation of  $e$  with respect to a given thread local environment  $\sigma$ . The heap  $H$  maps locations to values, where each location  $\rho.f$  combines an object address  $\rho$  with a field name  $f$ . The heap also maps each object address  $\rho$  to the thread identifier (or *Tid*) of the thread holding the object's lock, or  $\perp$  if the lock is not held. We use  $\mathcal{E}$  to range over evaluation contexts and say that a thread  $(\mathcal{E}[\text{wrong}], \sigma)$  has *gone wrong*. Rather than include a special statement `assert  $e$` , we encode it as `if ( $e$ ) skip wrong`.

The state evaluation relation  $\Sigma \rightarrow_t \Sigma'$  performs a step of thread  $t$  via an auxiliary relation  $(s \cdot \sigma) \cdot H \rightarrow_t (s' \cdot \sigma') \cdot H'$  for threads. Those rules are mostly straightforward. Updates to functions are written as, for example,  $\sigma[z := \text{true}]$ , which extends  $\sigma$  to map  $z$  to `true`.

The compare-and-set operation  $z = \text{cas}(y.f, x, w)$  compares  $y.f$  to  $x$ , and if they match, sets  $y.f$  to  $w$  and  $z$  to `true` via [STD CAS+]. Alternatively, the `cas` operation can fail non-deterministically and set  $z$  to `false` via [STD CAS-]. We identify certain locations  $\rho.f$  as being *ABA-free*, which means they never change from a value  $A$  to  $B$  and then back to  $A$  again. For such locations, we assume there is some ordering  $\sqsubseteq_{\rho.f}$  that is respected by writes to  $\rho.f$  and the rules [STD CAS+] and [STD WRITE] check that this ordering is respected.

We define two different evaluation relations (or schedulers) for ANCHORJAVA programs, as shown in Figure 5. The relation  $\Sigma \rightarrow \Sigma'$  models *preemptive* scheduling; it performs a step of an arbitrary thread  $t$ . The relation  $\Sigma \mapsto \Sigma'$  models *cooperative* scheduling where once one thread  $t$  is running, it keeps running (without interleaved steps of other threads) until it reaches a yield point. We say that thread  $t$  with state  $(s, \sigma)$  is *yielding* if it is at a yield statement ( $s = \mathcal{E}[\text{yield}]$ ), has gone wrong ( $s = \mathcal{E}[\text{wrong}]$ ), or has terminated ( $s = \text{skip}$ ). Thus, the relation  $\Sigma \mapsto \Sigma'$  only performs a step of thread  $t$  if all other threads  $u \neq t$  are yielding. In particular, context switches only happen at *yielding states* in which all threads are yielding.

**Syntax:**

$s \in \text{Stmt} ::= x = y.f \mid y.f = x$   
 $\quad \mid z = \text{cas}(y.f, x, w)$   
 $\quad \mid x = e \mid x = \text{new } c$   
 $\quad \mid \text{acq}(x) \mid \text{rel}(x) \mid \text{yield}$   
 $\quad \mid z = y.mn(\bar{x}) \mid \text{while } e \text{ } s$   
 $\quad \mid \text{if } e \text{ } s \mid s; s \mid \text{skip} \mid \text{wrong}$   
 $\text{meth} \in \text{Method} ::= mn(\bar{x}) \{ s; \text{return } z \}$   
 $D \in \text{Defn} ::= \text{class } c \{ \bar{f} \text{ meth} \}$   
 $w, x, y, z \in \text{Var} \quad f \in \text{FieldName}$   
 $e \in \text{Expr} \quad mn \in \text{MethodName}$   
 $c \in \text{ClassName}$

**Standard State:**

$H \in \text{Heap} = (\text{Location} \rightarrow \text{Value})$   
 $\quad \cup (\text{Address} \rightarrow \text{Tid}_{\perp})$   
 $k, l \in \text{Location} = \rho.f$   
 $\rho \in \text{Address}$   
 $v \in \text{Value} ::= \rho \mid \text{true} \mid \text{false} \mid \text{null} \mid \dots$   
 $\sigma \in \text{Env} = \text{Var} \rightarrow \text{Value}$   
 $T \in \text{Threads} = \text{Tid} \rightarrow (\text{Stmt} \times \text{Env})$   
 $\Sigma \in \text{State} = T \cdot H$   
 $t, u \in \text{Tid}$   
 $\mathcal{E} \in \text{EvalCtxt} = [\bullet] \mid \mathcal{E}; s$

$$(s \cdot \sigma) \cdot H \rightarrow_t (s' \cdot \sigma') \cdot H'$$

$$[\text{STD ACQ/REL}] \quad \frac{\sigma(x) = \rho \quad H(\rho) = \perp}{(\text{acq}(x) \cdot \sigma) \cdot H \rightarrow_t (\text{skip} \cdot \sigma) \cdot H[\rho := t]} \quad \frac{\sigma(x) = \rho \quad H(\rho) = t}{(\text{rel}(x) \cdot \sigma) \cdot H \rightarrow_t (\text{skip} \cdot \sigma) \cdot H[\rho := \perp]}$$

$$[\text{STD YIELD}] \quad \frac{}{(\text{yield} \cdot \sigma) \cdot H \rightarrow_t (\text{skip} \cdot \sigma) \cdot H}$$

$$[\text{STD NEW}] \quad \frac{\rho \text{ is fresh}}{(x = \text{new } c \cdot \sigma) \cdot H \rightarrow_t (\text{skip} \cdot \sigma[x := \rho]) \cdot H}$$

$$[\text{STD READ}] \quad \frac{\sigma(y) = \rho}{(x = y.f \cdot \sigma) \cdot H \rightarrow_t (\text{skip} \cdot \sigma[x := H(\rho.f)]) \cdot H}$$

$$[\text{STD WRITE}] \quad \frac{\sigma(y) = \rho \quad \sigma(x) = v \quad \text{if } \rho.f \text{ is ABA-free then } H(\rho.f) \sqsubseteq_{\rho.f} v}{(y.f = x \cdot \sigma) \cdot H \rightarrow_t (\text{skip} \cdot \sigma) \cdot H[\rho.f := v]}$$

$$[\text{STD CAS+}] \quad \frac{\sigma(y) = \rho \quad H(\rho.f) = \sigma(x) \quad \sigma(w) = v \quad \text{if } \rho.f \text{ is ABA-free then } H(\rho.f) \sqsubseteq_{\rho.f} v}{(z = \text{cas}(y.f, x, w) \cdot \sigma) \cdot H \rightarrow_t (\text{skip} \cdot \sigma[z := \text{true}]) \cdot H[\rho.f := v]}$$

$$[\text{STD CAS-}] \quad \frac{}{(z = \text{cas}(y.f, x, w) \cdot \sigma) \cdot H \rightarrow_t (\text{skip} \cdot \sigma[z := \text{false}]) \cdot H}$$

$$[\text{STD EXPR/SKIP}] \quad \frac{}{(x = e \cdot \sigma) \cdot H \rightarrow_t (\text{skip} \cdot \sigma[x := \sigma(t, e)]) \cdot H} \quad \frac{}{(\text{skip}; s \cdot \sigma) \cdot H \rightarrow_t (s \cdot \sigma) \cdot H}$$

$$[\text{STD IF-TRUE/IF-FALSE}] \quad \frac{\sigma(e) = \text{true}}{(\text{if } e \text{ } s_1 \text{ } s_2 \cdot \sigma) \cdot H \rightarrow_t (s_1 \cdot \sigma) \cdot H} \quad \frac{\sigma(e) = \text{false}}{(\text{if } e \text{ } s_1 \text{ } s_2 \cdot \sigma) \cdot H \rightarrow_t (s_2 \cdot \sigma) \cdot H}$$

$$[\text{STD WHILE}] \quad \frac{}{(\text{while } x \text{ } s \cdot \sigma) \cdot H \rightarrow_t (\text{if } e \text{ } (s; \text{while } e \text{ } s) \text{ skip} \cdot \sigma) \cdot H}$$

$$[\text{STD CALL}] \quad \frac{\begin{array}{l} mn(\bar{x}') \{ s; \text{return } z' \} \in \bar{D} \\ \forall w \in FV(s) \setminus \{ \bar{x}', \text{this}, z' \}. \theta(w) \text{ is fresh} \quad \theta(\bar{x}') = \bar{x} \quad \theta(\text{this}) = y \quad \theta(z') = z \end{array}}{(z = y.mn(\bar{x}) \cdot \sigma) \cdot H \rightarrow_t (\theta(s) \cdot \sigma) \cdot H}$$

$$\boxed{\Sigma \rightarrow_t \Sigma'}$$

[STD THREAD]

$$\boxed{\Sigma \rightarrow \Sigma'}$$

[STD PREEMPTIVE]

$$\boxed{\Sigma \mapsto \Sigma'}$$

[STD COOPERATIVE]

$$\frac{(s \cdot \sigma) \cdot H \rightarrow_t (s' \cdot \sigma') \cdot H'}{T[t := (\mathcal{E}[s], \sigma)] \cdot H \rightarrow_t T[t := (\mathcal{E}[s'], \sigma')] \cdot H'}$$

$$\frac{\Sigma \rightarrow_t \Sigma'}{\Sigma \rightarrow \Sigma'}$$

$$\frac{\Sigma \rightarrow_t \Sigma' \quad \forall u \neq t. T_u \text{ is yielding}}{\Sigma \mapsto \Sigma'}$$

Fig. 5. ANCHORJAVA syntax and standard semantics.

## 5 SYNCHRONIZATION SPECIFICATIONS

As shown in Section 2, the synchronization discipline for a field access  $\rho.f$  can depend on the  $\text{tid}$  of the accessing thread and on the state of other data or locks in the heap. As such, we formalize the read synchronization discipline<sup>1</sup> for each location  $\rho.f$  as a function  $R_{\rho.f}$ :

$$R_{\rho.f} \in \text{ReadMover} = \text{Tid} \times \text{Heap} \rightarrow \text{Mover}$$

Thread  $t$  can read  $\rho.f$  in heap  $H$  provided that  $R_{\rho.f}(t, H) \neq \text{E}$ . In addition,  $R_{\rho.f}(t, H)$  specifies the appropriate mover for each permitted read access.

For writes, the synchronization discipline can restrict the value written (e.g., to enforce that a variable is monotonically increasing or that the new value is always a freshly-allocated object). Thus, the function  $W_{\rho.f}$  for  $\rho.f$ 's write synchronization discipline also takes the value being written:

$$W_{\rho.f} \in \text{WriteMover} = \text{Tid} \times \text{Heap} \times \text{Value} \rightarrow \text{Mover}$$

These synchronization specifications help identify specification errors early, even before the first line of code is written.

Suppose a read of  $\rho.f$  by thread  $t$  in heap  $H$  is a right-mover, i.e.  $R_{\rho.f}(t, H) \sqsubseteq \text{R}$ . Then the synchronization discipline must prohibit a subsequent write to  $\rho.f$  by any other thread  $u$ , i.e.  $W_{\rho.f}(u, H, \_) = \text{E}$ , because the read would not right-commute over such a write. The *validity* condition [VALID READ-R] below enforces this restriction. The erroneous synchronization specification on line 3 of Figure 1, where  $R_{\rho.y}(t, H) = W_{\rho.y}(u, H, v) = \text{B}$  is prohibited by this rule.

Similarly, the second condition [VALID WRITE-R] ensures that a right-mover write of  $v$  to  $\rho.f$  is not followed by a conflicting read or write by another thread in the post state  $H[\rho.f := v]$ . The final two conditions address left-mover reads and writes, respectively, and prohibit conflicting accesses in the pre-state.

**Definition 5.1** (Validity). *Specification  $R, W$  is valid if for all  $l = \rho.f, t, H, v$ , and  $u$  where  $u \neq t$ :*

$$[\text{VALID READ-R}] \quad R_{\rho.f}(t, H) \sqsubseteq \text{R} \Rightarrow W_{\rho.f}(u, H, \_) = \text{E}$$

$$[\text{VALID WRITE-R}] \quad W_{\rho.f}(t, H, v) \sqsubseteq \text{R} \Rightarrow W_{\rho.f}(u, H[\rho.f := v], \_) = \text{E} \wedge R_{\rho.f}(u, H[\rho.f := v]) = \text{E}$$

$$[\text{VALID READ-L}] \quad R_{\rho.f}(t, H) \sqsubseteq \text{L} \Rightarrow W_{\rho.f}(u, H[\rho.f := \_], H(l)) = \text{E}$$

$$[\text{VALID WRITE-L}] \quad W_{\rho.f}(t, H, v) \sqsubseteq \text{L} \Rightarrow W_{\rho.f}(u, H[\rho.f := \_], H(l)) = \text{E} \wedge R_{\rho.f}(u, H) = \text{E}$$

Additionally, suppose thread  $t$  is permitted to write  $v$  to  $\rho.f$  in heap  $H$ , i.e.  $W_{\rho.f}(t, H, v) \neq \text{E}$ . This permission should be *stable* on an interleaved write  $\rho'.g = v'$  of another location by another thread  $u$  such that  $W_{\rho'.g}(u, H, v') \neq \text{E}$ . That is, the interleaved write should not change  $W_{\rho.f}(t, H, v)$ . We refer to this correctness requirement on specifications as *strict stability*. Read permissions may similarly be required to be invariant under interleaved writes, giving us the following requirement.

**Definition 5.2** (Strict Stability). *Specification  $R, W$  is strictly stable if for all  $\rho, \rho', t, H, v, v'$ , and  $u$  where  $W_{\rho'.g}(u, H, v') \neq \text{E}$  and  $u \neq t$ :*

$$\begin{aligned} & W_{\rho.f}(t, H, v) = W_{\rho.f}(t, H[\rho'.g := v'], v) \\ & \wedge R_{\rho.f}(t, H) = R_{\rho.f}(t, H[\rho'.g := v']) \end{aligned}$$

This strict stability condition works well for most programs. To support more subtle synchronization disciplines, ANCHOR actually enforces a more relaxed notion of stability that is weaker than Definition 5.2 yet still sufficiently strong to support reduction-based verification. That more complex definition appears in the Supplementary Appendix.

<sup>1</sup>For technical convenience, we formalize the read and write synchronization disciplines separately.

**Instrumented State:**

$p$	$\in$	$Phase$	$::=$	$PRE \mid POST \mid ERR$
$P$	$\in$	$PhaseMap$	$=$	$Tid \rightarrow Phase$
$C$	$\in$	$CasSet$	$=$	$\mathcal{P}(Location \times Tid \times Value)$
$\Pi$	$\in$	$InstState$	$=$	$T \cdot H \cdot C \cdot P$

$$(s, \sigma) \cdot H \cdot C \cdot p \Rightarrow_t (s', \sigma') \cdot H' \cdot C' \cdot p'$$

$$[INST\ ACQ] \frac{\sigma(x) = \rho \quad H(\rho) = \perp}{(acq(x) \cdot \sigma) \cdot H \cdot C \cdot p \Rightarrow_t (skip \cdot \sigma) \cdot H[\rho := t] \cdot C \cdot (p \triangleright R)}$$

$$[INST\ REL] \frac{\sigma(x) = \rho \quad H(\rho) = t}{(rel(x) \cdot \sigma) \cdot H \cdot C \cdot p \Rightarrow_t (skip \cdot \sigma) \cdot H[\rho := \perp] \cdot C \cdot (p \triangleright L)}$$

$$[INST\ YIELD] \frac{}{(yield \cdot \sigma) \cdot H \cdot C \cdot p \Rightarrow_t (skip \cdot \sigma) \cdot H \cdot C \cdot PRE}$$

$$[INST\ READ] \frac{\sigma(y) = \rho \quad m = (CASable_{\rho, f}(t, H, C) ? R : R_{\rho, f}(t, H))}{(x = y.f \cdot \sigma) \cdot H \cdot C \cdot p \Rightarrow_t (skip \cdot \sigma[x := H(\rho.f)]) \cdot H \cdot C \cdot (p \triangleright m)}$$

$$[INST\ WRITE] \frac{\sigma(y) = \rho \quad \sigma(x) = v \quad \text{if } \rho.f \text{ is ABA-free then } H(\rho.f) \sqsubseteq_{\rho.f} v \quad ValidWrite_{\rho, f}(C, v) \quad m = W_{\rho, f}(t, H, v)}{(y.f = x \cdot \sigma) \cdot H \cdot C \cdot p \Rightarrow_t (skip \cdot \sigma) \cdot H[\rho.f := v] \cdot C \cdot (p \triangleright m)}$$

$$[INST\ CAS+] \frac{\sigma(y) = \rho \quad H(\rho.f) = \sigma(x) \quad \sigma(w) = v \quad \text{if } \rho.f \text{ is ABA-free then } H(\rho.f) \sqsubseteq_{\rho.f} v \quad ValidWrite_{\rho, f}(C, v) \quad m = W_{\rho, f}(t, H, v) \quad p \triangleright m \neq ERR}{(z = cas(y.f, x, w) \cdot \sigma) \cdot H \cdot (C \cup \{(\rho.f, t, \sigma(x))\}) \cdot p \Rightarrow_t (skip \cdot \sigma[z := true]) \cdot H[\rho.f := v] \cdot C \cdot (p \triangleright m)}$$

$$[INST\ CAS+ \text{ WRONG}] \frac{\sigma(y) = \rho \quad \sigma(w) = v \quad m = W_{\rho, f}(t, H[\rho.f := \sigma(x)], v) \quad p \triangleright m = ERR}{(z = cas(y.f, x, w) \cdot \sigma) \cdot H \cdot (C \cup \{(\rho.f, t, \sigma(x))\}) \cdot p \Rightarrow_t (z = cas(y.f, x, w) \cdot \sigma) \cdot H \cdot C \cdot ERR}$$

$$[INST\ CAS-] \frac{}{(z = cas(y.f, x, w) \cdot \sigma) \cdot H \cdot C \cdot p \Rightarrow_t (skip \cdot \sigma[z := false]) \cdot H \cdot C \cdot p}$$

$$[INST\ STD] \frac{(s \cdot \sigma) \cdot H \rightarrow_t (s' \cdot \sigma') \cdot H \quad s \in \{x = new\ c, x = e, \text{if } e\ s_1\ s_2, \text{while } e\ s_1, z = y.mn(\bar{x}), skip; s_1\}}{(s \cdot \sigma) \cdot H \cdot C \cdot p \Rightarrow_t (s' \cdot \sigma') \cdot H \cdot C \cdot p}$$

$$\Pi \Rightarrow_t \Pi'$$

$$[INST\ THREAD] \frac{p \neq ERR \quad (s \cdot \sigma) \cdot H \cdot C \cdot p \Rightarrow_t (s' \cdot \sigma') \cdot H' \cdot C' \cdot p' \quad p' \neq ERR}{T[t := (\mathcal{E}[s], \sigma)] \cdot H \cdot C \cdot P[t := p] \Rightarrow_t T[t := (\mathcal{E}[s'], \sigma')] \cdot H' \cdot C' \cdot P[t := p']}$$

$$[INST\ THREAD \text{ WRONG}] \frac{p \neq ERR \quad (s \cdot \sigma) \cdot H \cdot C \cdot p \Rightarrow_t (s' \cdot \sigma') \cdot H' \cdot C' \cdot ERR}{T[t := (\mathcal{E}[s], \sigma)] \cdot H \cdot C \cdot P[t := p] \Rightarrow_t T[t := (\mathcal{E}[s], \sigma)] \cdot H \cdot C \cdot P[t := ERR]}$$

$$\Pi \Rightarrow \Pi'$$

$$\Pi \Rightarrow \Pi'$$

$$[INST\ PREEMPTIVE] \frac{\Pi \Rightarrow_t \Pi'}{\Pi \Rightarrow \Pi'} \quad [INST\ COOPERATIVE] \frac{\Pi \Rightarrow_t \Pi' \quad \forall u \neq t. u \text{ is yielding in } \Pi}{\Pi \Rightarrow \Pi'}$$

Fig. 6. ANCHORJAVA instrumented semantics.



## 6 CHECKING REDUCTION

### 6.1 Instrumented Semantics

We now extend the standard semantics to check that (1) all accesses satisfy the synchronization specification and (2) the execution is P/C-equivalent. The resulting instrumented semantics is shown in Figure 6, which uses shading to highlight the major changes over the standard semantics.

The instrumented semantics records, for each thread  $t$ , a *phase*  $p \in \text{Phase}$  indicating whether  $t$  is in the PRE or POST commit phase of a reducible block. The operation

$$\cdot \triangleright \cdot : \text{Phase} \times \text{Mover} \rightarrow \text{Phase}$$

computes the updated phase  $p \triangleright m$  for  $t$  when it performs a heap access with mover  $m$  in phase  $p$ . Essentially, in the PRE-commit phase, mover steps B and R are permitted; L and N transition a thread from PRE to POST (this is called the *commit point*); and in the POST-commit phase only B and L steps are permitted. The special phase ERR indicates a reduction error occurred.

$\triangleright$	B	R	L	N	E
PRE	PRE	PRE	POST	POST	ERR
POST	POST	ERR	POST	ERR	ERR
ERR	ERR	ERR	ERR	ERR	ERR

An instrumented state  $\Pi = T \cdot H \cdot C \cdot P$  extends a standard state  $\Sigma = T \cdot H$  with a phase map  $P : \text{Tid} \rightarrow \text{Phase}$  and also with a *CasSet*  $C$  (described below). Thread  $t$  is *wrong* in  $T \cdot H \cdot C \cdot P$  if either  $T_t = (\mathcal{E}[\text{wrong}], \sigma)$  or  $P_t = \text{ERR}$ .

The instrumented relation  $\Pi \Rightarrow_t \Pi'$  performs a step of thread  $t$  via an auxiliary relation  $(s \cdot \sigma) \cdot H \cdot C \cdot p \Rightarrow_t (s' \cdot \sigma') \cdot H' \cdot C' \cdot p'$  for threads. (See [INST THREAD].) If  $p' = \text{ERR}$ , the thread and heap state are left unchanged via [INST THREAD WRONG] to facilitate our correctness proofs. The relations  $\Pi \Rightarrow \Pi'$  and  $\Pi \Rightarrow \Pi'$  define steps of the instrumented semantics under preemptive and cooperative schedulers, respectively.

The new rule [INST ACQ] extends [STD ACQ] to update the phase from  $p$  to  $p \triangleright R$ , reflecting that the acquire is a right-mover. Rule [INST YIELD] resets the phase to PRE, thus initiating a separate new reducible sequence.

As illustrated by `inc()` in Figure 2, the commutivity of a read depends critically on whether a future `cas` operation is successful. For this reason, the instrumented semantics maintains a *CasSet*  $C \in \mathcal{P}(\text{Location} \times \text{Tid} \times \text{Value})$ , where  $(\rho.f, t, v) \in C$  means that, in the future, thread  $t$  will perform a successful `cas` in which  $\rho.f$  is compared to  $v$ . In this situation, thread  $t$  reading  $v$  from an ABA-free location  $\rho.f$  is a right-mover provided the read does not violate the synchronization discipline, i.e.  $R_{\rho.f}(t, H) \neq E$ . We summarize these conditions via the following predicate:

$$\text{CASable}_{\rho.f}(t, H, C) \stackrel{\text{def}}{=} \rho.f \text{ is ABA-free} \wedge (\rho.f, t, H(\rho.f)) \in C_{\rho.f} \wedge R_{\rho.f}(t, H) \neq E$$

Rule [INST READ] uses this predicate to upgrade the commutivity  $m$  of a read from  $R_{\rho.f}(t, H)$  to R where appropriate.

Rule [INST WRITE] extends [STD WRITE] to update the thread's phase to  $p \triangleright m$  where  $m = W_{\rho.f}(t, H, v)$ . For ABA-free locations  $\rho.f$ , the rule requires that the ordering  $\sqsubseteq_{\rho.f}$  is respected. In particular,  $H(\rho.f) \sqsubseteq_{\rho.f} v$  and for all values  $v'$  appearing in  $C$  because they are read by a later successful `cas`,  $v \sqsubseteq_{\rho.f} v'$ . We formalize the second requirement via the following predicate:

$$\text{ValidWrite}_{\rho.f}(C, v) \stackrel{\text{def}}{=} \rho.f \text{ is ABA-free} \Rightarrow \forall (\rho.f, \_, v') \in C. v \sqsubseteq_{\rho.f} v'$$

Rule [INST CAS+] similarly extends [STD CAS+] with a *ValidWrite* check. It also updates the *CasSet*  $C$  in the pre-state to reflect this successful `cas` on  $\rho.f$ , and it updates the phase  $p$  to  $p \triangleright m$  in the post-state. Thus, a successful read-cas sequence



$x = y.f; z = \text{cas}(y.f, x, w)$

is reducible as follows, where we assume  $R_{\rho.f}(\_, \_) = W_{\rho.f}(\_, \_) = N$  and  $\sigma = [y \mapsto \rho, w \mapsto 2]$ :

$$\begin{array}{c} T \quad H \quad C \quad P \\ \Rightarrow_t^* [t \mapsto ((x = y.f; z = \text{cas}(y.f, x, w)), \sigma) \cdot [\rho.f \mapsto 1] \cdot \{(\rho.f, t, 1)\} \cdot [t \mapsto \text{PRE}] \\ \Rightarrow_t [t \mapsto ((z = \text{cas}(y.f, x, w), \sigma[x := 1]) \cdot [\rho.f \mapsto 1] \cdot \{(\rho.f, t, 1)\} \cdot [t \mapsto \text{PRE}] \\ \Rightarrow_t [t \mapsto ((\text{skip}, \sigma[x := 1, z := \text{true}]) \cdot [\rho.f \mapsto 2] \cdot \emptyset \cdot [t \mapsto \text{POST}]) \end{array}$$

Rule [INST CAS+ WRONG] addresses the case where  $p \triangleright m = \text{ERR}$ . Two subtleties are worth noting. First, in order to establish the desired commutivity properties for our correctness argument below, this rule needs to left-commute across concurrent writes to  $\rho.f$ . Therefore we compute the commutivity  $m = W_{\rho.f}(t, H[\rho.f := \sigma(x)], v)$  in the heap  $H[\rho.f := \sigma(x)]$ . This heap is identical to  $H$  if the cas could have succeeded. Second, rule [INST CAS+ WRONG] must update the CasSet  $C$  in the pre-state to be  $C \cup \{(\rho.f, t, v)\}$ . If we were to omit this update to  $C$ , then ANCHOR could not verify the read-cas sequence above. Specifically, the read would be a non-mover if  $C$  were empty, transitioning the thread to the POST state. The cas operation would then execute via [INST CAS+ WRONG] due to the reduction error as  $\text{POST} \triangleright N = \text{ERR}$ , as illustrated below.

$$\begin{array}{c} T \quad H \quad C \quad P \\ [t \mapsto ((x = y.f; z = \text{cas}(y.f, x, w)), \sigma) \cdot [\rho.f \mapsto 1] \cdot \emptyset \cdot [t \mapsto \text{PRE}] \\ \Rightarrow_t^* [t \mapsto ((z = \text{cas}(y.f, x, w), \sigma[x := 1]) \cdot [\rho.f \mapsto 1] \cdot \emptyset \cdot [t \mapsto \text{POST}] \\ \Rightarrow_t [t \mapsto ((z = \text{cas}(y.f, x, w), \sigma[x := 1]) \cdot [\rho.f \mapsto 1] \cdot \emptyset \cdot [t \mapsto \text{ERR}]) \end{array}$$

## 6.2 Correspondence to the Standard Semantics

The instrumented semantics ( $\Rightarrow$ ) behaves the same as a standard semantics ( $\rightarrow$ ), except it may go wrong as a result of detecting a violation of the synchronization specifications or reducibility. In proving this correspondence, we assume that specification  $R, W$  is valid and stable;  $P_0$  denotes the initial phase map  $\lambda t. \text{PRE}$ ; and that the initial program state  $\Sigma_0 = T_0 \cdot H_0$  is yielding and *nonblocking*, meaning that any reducible code sequence reaching its commit point must terminate.

Note that the initial CasSet  $C_0$  needs to be appropriately chosen to reflect the successful cas operations that will be performed during the run. A CasSet  $C$  is *valid* for a heap  $H$  if  $C$  contains only values for future cas operations that properly ordered with respect to the current values in  $H$ :

$$C \text{ is valid for } H \quad \text{iff} \quad \forall \rho.f, v. \rho.f \text{ is ABA-free} \wedge \forall (\rho.f, \_, v) \in C \Rightarrow H(\rho.f) \sqsubseteq_{\rho.f} v$$

**Theorem 1.** If  $T_0 \cdot H_0 \rightarrow^* T \cdot H$  then there exists a valid  $C_0$  for  $H_0$  such that either:

- (1) there exists  $P$  such that  $T_0 \cdot H_0 \cdot C_0 \cdot P_0 \Rightarrow^* T \cdot H \cdot \emptyset \cdot P$ , or
- (2)  $T_0 \cdot H_0 \cdot C_0 \cdot P_0 \Rightarrow^* \Pi$  where  $\Pi$  is wrong.

Consequently, if the standard semantics can go wrong then so does the instrumented semantics.

**Corollary 1.** If  $T_0 \cdot H_0$  goes wrong under  $\rightarrow$  then there exists a valid  $C_0$  for  $H_0$  such that  $T_0 \cdot H_0 \cdot C_0 \cdot P_0$  goes wrong under  $\Rightarrow$ .

Finally, any cooperative run of the instrumented semantics is also cooperative under the standard semantics.

**Theorem 2.** If  $T_0 \cdot H_0 \cdot C_0 \cdot P_0 \Rightarrow^* T \cdot H \cdot C \cdot P$  for some  $C_0, T, H, C$ , and  $P$ , then  $T_0 \cdot H_0 \mapsto^* T \cdot H$ .

## 6.3 Reducibility of the Instrumented Semantics

We next show that the instrumented semantics is P/C-equivalent, *i.e.* that any preemptive run ( $\Rightarrow$ ) is reducible to a cooperative run ( $\Rightarrow$ ), under the assumption that cooperative runs do not go wrong.

**Theorem 3 (Reduction).** If  $\Pi = T_0 \cdot H_0 \cdot C_0 \cdot P_0$  and  $\Pi_0$  does not go wrong under  $\Rightarrow$ , then:

**Thread-Modular State:**

$$\Theta \in \text{ThreadModularState} = (s \cdot \sigma) \cdot H \cdot C \cdot p$$

$$\boxed{\Theta \models_t \Theta'}$$

[TM STEP]

$$\frac{(s \cdot \sigma) \cdot H \cdot C \cdot p \Rightarrow_t (s' \cdot \sigma') \cdot H' \cdot C' \cdot p' \quad p' \neq \text{ERR}}{(\mathcal{E}[s] \cdot \sigma) \cdot H \cdot C \cdot p \models_t (\mathcal{E}[s'] \cdot \sigma') \cdot H' \cdot C' \cdot p'}$$

[TM STEP WRONG]

$$\frac{(s \cdot \sigma) \cdot H \cdot C \cdot p \Rightarrow_t (s' \cdot \sigma') \cdot H' \cdot C' \cdot \text{ERR}}{(\mathcal{E}[s] \cdot \sigma) \cdot H \cdot C \cdot p \models_t (\mathcal{E}[s] \cdot \sigma) \cdot H \cdot C \cdot \text{ERR}}$$

[TM YIELD]

$$\frac{\text{Yield}(t, H, H')}{(\mathcal{E}[\text{yield}] \cdot \sigma) \cdot H \cdot C \cdot p \models_t (\mathcal{E}[\text{yield}] \cdot \sigma) \cdot H' \cdot C \cdot p}$$

$$\begin{aligned} \text{where } \text{Yield}(t, H, H') &= \forall x. H(x) \neq H'(x) \Rightarrow (\exists u \neq t. W_x(u, H, H'(x)) \neq E) \\ &\wedge \forall l. H(l) = t \Leftrightarrow H'(l) = t \end{aligned}$$

Fig. 7. ANCHORJAVA thread-modular semantics.

- (1)  $\Pi_0$  does not go wrong under  $\Rightarrow$ .
- (2) If  $\Pi_0 \Rightarrow^* \Pi$  where  $\Pi$  is yielding, then  $\Pi_0 \models^* \Pi$ .

**7 THREAD-MODULAR SEMANTICS**

Our final semantics is a *thread-modular* semantics that provides the foundation for our verification methodology, as it avoids explicitly reasoning about all interleavings of an unbounded number of threads. Instead, it analyzes one thread at a time in a cooperative fashion, using the synchronization specification to model possible behaviors of other threads at yield points.

When analyzing some thread  $t$ , the thread-modular semantics maintains a state  $\Theta = (s \cdot \sigma) \cdot H \cdot C \cdot p$  consisting of the thread state  $s \cdot \sigma$  for  $t$ , the heap  $H$ , the CasSet  $C$ , and the phase  $p$  of that thread. The relation  $\Theta \models_t \Theta'$  performs an arbitrary step possible in state  $\Theta$ . This relation models steps of  $t$  precisely by delegating to the instrumented semantics via rule [TM STEP] or [TM STEP WRONG]. If  $s = \mathcal{E}[\text{yield}]$ , then rule [TM YIELD] models possible behaviors of other threads under the given synchronization specification. In particular, the relation  $\text{Yield}(t, H, H')$  captures heap mutations that threads other than  $t$  may perform in  $H$ . A variable  $x$  can only change in  $H'$  if some thread  $u \neq t$  has permission to modify it in  $H$ , and a lock  $l$  is held by  $t$  in  $H'$  iff it was held by  $t$  in  $H$ . Note that, at each yield, [TM YIELD] can fire multiple times before [TM STEP] transitions to a non-yielding state, thus modeling non-deterministic scheduling.

The following simulation mapping  $\Pi|t$  maps the instrumented state  $\Pi$  to a corresponded thread-modular state  $\Theta$  by projecting away threads other than  $t$ :

$$(T \cdot H \cdot C \cdot P)|t = T(t) \cdot H \cdot \{ (t, \_, \_) \in C \} \cdot P(t)$$

Given  $\Pi_0 = T_0 \cdot H_0 \cdot C_0 \cdot P_0$ , running  $\Pi_0|t$  under  $\models_t$  simulates (over-approximates) the behavior of thread  $t$  under  $\Rightarrow$  and so detects if  $t$  would go wrong.

**Theorem 4** (Simulation). Suppose  $\Pi_0 \Rightarrow^* \Pi$  where thread  $t$  has gone wrong in  $\Pi$ . Then  $\Pi_0|t$  goes wrong under  $\models_t$ .

We now state and prove our central correctness result relating the behavior of the original program  $\Sigma_0 = T_0 \cdot H_0$  and the thread-modular program  $\Pi_0|t$ , where  $\Pi_0 = T_0 \cdot H_0 \cdot C_0 \cdot P_0$ .

**Theorem 5** (Correctness). Suppose that for all  $t$ ,  $\Pi_0|t$  does not go wrong under  $\models_t$ . Then  $T_0 \cdot H_0$  does not go wrong under  $\rightarrow$  and is P/C-equivalent.

PROOF. By Theorem 4,  $\Pi_0$  does not go wrong under  $\Rightarrow$ . By Theorem 3(1),  $\Pi_0$  does not go wrong under  $\Rightarrow$ . By Corollary 1,  $\Sigma_0$  does not go wrong under  $\rightarrow$ .

Next, consider any standard, preemptive run  $T_0 \cdot H_0 \rightarrow^* T \cdot H$  where  $T \cdot H$  is yielding. By Theorem 1,  $T_0 \cdot H_0 \cdot C_0 \cdot P_0 \Rightarrow^* T \cdot H \cdot \emptyset \cdot P$  for some  $C_0$  and  $P$ . By Theorem 3(2),  $T_0 \cdot H_0 \cdot C_0 \cdot P_0 \Rightarrow^* T \cdot H \cdot \emptyset \cdot P$ . By Theorem 2,  $T_0 \cdot H_0 \mapsto^* T \cdot H$ .

□

## 8 ANCHOR VERIFIER

We have implemented the ANCHOR verifier based on these ideas. The input language for ANCHOR is a subset of Java extended with specifications. ANCHOR does not yet support some Java features, such as inheritance and subtyping, but is sufficient for writing many concurrent algorithms. ANCHOR also includes a compiler to generate executable Java code directly from ANCHOR source code. That compiler utilizes the standard Java concurrency library [Lea 2019] to implement locks and cas.

Given a target program, ANCHOR verifies that no assertions fail; that the synchronization specification is valid, stable, and respected by the code; and that the code is race-free and P/C equivalent. If the code contains method specifications, those specifications are also verified. To check these properties, ANCHOR generates a Boogie program embodying the necessary validity/stability checks and the execution of each public method under the thread-modular semantics. That program is checked with the Boogie verifier [Barnett et al. 2005], and any errors are mapped back to the ANCHOR source code and reported along with details extracted from Boogie’s counter-examples, as shown in Section 2.

ANCHOR verifies each public method modularly but handles all embedded method calls via inlining, which simplifies our formal development and implementation when compared to existing techniques such as Calvin-R [Freund and Qadeer 2004], Armada [Lorch et al. 2020], and CIVL [Hawblitzel et al. 2015a]. The specification burden of using ANCHOR is also lower than it would otherwise be, and since concurrent components are typically relatively small, we do not expect this to become a limiting factor.

**Thread-local Analysis.** ANCHOR uses a simple strategy to identify thread-local objects. A newly-allocated object is thread-local until a reference to it is stored in another object, at which point it is considered shared. Thus, shared objects never refer to thread-local data. The same applies to arrays. Also, ANCHOR assumes the receiver and all objects passed as parameters to public methods are shared. However, the receiver of a call to public constructor is considered to be local as we expect clients to call those methods only on newly-allocated thread-local objects. One area for future work is to integrate a more robust analysis for ownership [Clarke et al. 1998].

**Modeling Field Updates by Other Threads.** ANCHOR includes an additional annotation to aid in modeling state changes at yields. The thread-modular semantics models the effect of a yield as zero or more heap updates via the *Yield* relation. That relation, in turn, is defined in terms of each memory location’s write access permission. Given the difficulty of computing the transitive closure of *Yield*, we instead over-approximate it by characterizing all possible changes to each location  $x.f$  in one of two ways.

The first (default) approximation is that if the current thread has right-mover read access to  $x.f$  at the yield, then the value of  $x.f$  does not change. If the current thread does not have right-mover read access,  $x.f$  may have any value after the yield. This rule subsumes all possible writes permissible by the synchronization specification, and it is reflexively and transitively closed (since our validity/stability requirements ensure other threads cannot modify  $x.f$  or take away the current thread’s right-mover permission).

This rule works for the vast majority of examples we studied, but it may admit changes to  $x.f$  that are not actually feasible if the possible updates to  $x.f$  performed by other threads are restricted in some way. For example, consider again `AtomicInt` from Figure 2 and a client of that class:

```

class AtomicInt {
  noABA volatile int n  moves_as isRead() ? N
                        : (newValue == this.n + 1) ? N : E
                        yields_as newValue >= this.n;

  ensures this.n == old(this.n) + 1;
  public int inc() { ... }
}
...
public void incTwice(AtomicInt counter) {
  int first = counter.inc();
  yield;
  int second = counter.inc();
  assert second > first;
}

```

Ignoring the `yields_as` annotation for the moment, ANCHOR would be unable to prove that the assertion `assert second > first` in `incTwice` always succeeds even though it does. Specifically, since the current thread does not have right-mover read access to `counter.n` at the `yield`, ANCHOR must assume `counter.n` could have any value after the `yield`.

This motivates our introduction of `yields_as` annotations to approximate heap updates. These annotations explicitly relate a field's post-`yield` value to its pre-`yield` value. For our `AtomicInt` class, we include a `yields_as` annotation guaranteeing the value of `n` may only increase at a `yield`. ANCHOR verifies that `yields_as` annotations subsume all writes permissible by the synchronization specification and are reflexively/transitively closed.

The related `noABA` annotation further restricts how a field may be changed. It ensures that the field exhibits ABA freedom, namely that that the field is never changed from a value  $A$  to  $B$  and then back to  $A$  again. ANCHOR verifies a field's `noABA` annotation using that `yields_as` annotation. For example, the `yields_as` annotation on `n` above indicates that if `n` is currently  $A$  and another thread updates it to a new and distinct value  $B$ , it must be that  $B > A$ . No thread could change `n` back to  $A$  without violating the field's `yields_as` specification since  $A \not\geq B$ .

**Post Phase Termination and Termination Metrics.** Our correctness argument requires that any reducible code sequence reaching its commit point must terminate. As such, ANCHOR verifies that any thread entering the `POST` phase of a reducible block reaches a `yield` point, and it rejects any program that, when in the `POST` phase, may fail at run time (e.g., due to a null pointer error), block indefinitely (e.g., due to an `acquire`), or loop indefinitely. To prove loops terminate, the programmer may supply a termination metric, as in, e.g., Dafny [?], via a `decreases` annotation that provides a non-negative integer expression that decreases in value on each loop iteration. (Standard loop invariants are also supported.)

**Object Invariants.** ANCHOR also supports object invariants. For example, to express that `Nodes` in a linked list must be ordered by their `items`, we can add the following invariant to our `Node` class from Figure 3.

```
invariant this.next != null ==> this.item <= this.next.item;
```

```

class LockBasedStack {
    modifies this;
    ensures this.head.next == old(this.head) && this.head.item == item;
    public int push(int item) { ... }

    modifies this;
    ensures old(this.head) != null;
    ensures $result == old(this.head.item) && this.head == old(this.head.next);
    public int pop() { ... }
}

```

Fig. 8. ANCHOR method specifications for LockBasedStack.

ANCHOR assumes all object invariants hold at the start of each public method and immediately after each yield operation, and it verifies that the invariants hold at the end of each public method and immediately before each yield operation.

**Method Specifications.** ANCHOR additionally supports specifications for public methods using via an approach inspired by earlier work on Calvin-R [Freund and Qadeer 2004] and CIVL [Hawblitzel et al. 2015a]. Space limitations prevent a full discussion of ANCHOR’s method specifications, but we illustrate the core ideas on several small examples.

A public method containing no yields always has atomic behavior. That behavior can be specified with standard requires, modifies, and ensures annotations, as illustrated in Figure 8 for the `Stack.push()` method from Figure 3, and ANCHOR verifies that the method body conforms to that specification.

A public method containing yields may also exhibit atomic behavior if it never executes more than one yield-free code region with visible side effects. The `pop` method for `LockBasedStack` has this property, since all but that last yield-free region in any execution of that method is side-effect free. This atomic behavior is captured by `pop()`’s specification in Figure 8. The special variable `$result` refers to the method’s return value, and terms of the form `old(e)`, such as `old(this.head)`, refer to the value of *e* at the beginning of the yield-free region captured by the specification. Note that `old(this.head)` may have a different value than it had at the start of the method call if interference occurs at the documented yield point. `LockFreeStack`’s method satisfies the *exact same* specifications as `LockBasedStack`’s, despite using optimistic concurrency control instead of locks.

The behavior of a public method with non-atomic behavior can be specified via a sequence of blocks containing modifies and ensures clauses. For example, the `incTwice` method above can be specified as:

```

{ modifies counter; ensures counter.n == old(counter.n) + 1; }
yield;
{ modifies counter; ensures counter.n == old(counter.n) + 1; }

```

We include the `yield` keyword in the specification to reinforce that interference may occur at those intermediate points, and that the state for those points may be exposed to other threads.

The `add` method for a sorted linked list implemented with hand-over-hand locking is similarly non-atomic and be specified in ANCHOR as a sequence of three atomic blocks that refer to an additional specification variable `ptr`. The first initializes `ptr` to the head of the list; the second (which may be iterated any number of times) moves `ptr` one node further down the list, performing the appropriate synchronization, until the insertion point is found; and the third inserts a new node at that location. One area for future work is to extend ANCHOR with data abstraction or a layering

Program	Synchronization Idiom	Size (LOC)	Sync. Specs	Yields	requires/ Invariants	ANCHOR Time (s)
<b>Stacks (w/ push, pop, and init)</b>						
Coarse	Lock-based (as in Figure 3)	31	3	0	0	3.20
Lock-free	CAS-based (as in Figure 3) [Treiber 1986]	43	3	2	0	3.48
<b>Linked Lists (w/ add, remove, contains, and init)</b>						
Coarse	One lock for all nodes	100	4	0	26	4.24
Fine	Hand-over-hand locking [Bayer and Schkolnick 1977]	115	4	3	22	3.62
Optimistic	Fine, with lock-free search + validation [Herlihy and Shavit 2008]	157	4	14	26	4.60
Lazy	Optimistic, with lock-free contains [Heller et al. 2005]	113	4	11	18	4.68
Lock-Free	CAS-based [Harris 2001; Michael 2002]	192	4	14	26	21.46
<b>Queues (w/ enqueue, dequeue, and init)</b>						
Coarse	One lock for all nodes	45	2	0	6	4.79
Lock-Free	CAS-based [Michael and Scott 1996]	74	2	8	4	5.55
Bounded	Separate locks for enq/deq, bounded size [Lea 2019; Michael and Scott 1996]	137	2	6	16	35.49
<b>HashSets (w/ add, remove, contains, and init)</b>						
Coarse	One lock for all buckets	190	3	0	28	14.68
Striped	array of locks for buckets [Lea 2019]	232	3	3	39	62.09
<b>FastTrack</b>	[Wilcox et al. 2018]	264	6	2	22	21.89

Table 1. Concurrency examples verified by ANCHOR.

mechanism, as in CIVL [Hawblitzel et al. 2015a], to hide yields in a method that only affect the concrete internal representation of a data structure but not the public abstraction of that structure.

## 9 EVALUATION

We evaluated ANCHOR on a variety of concurrent collection classes and the FASTTRACK dynamic data race detection algorithm [Flanagan and Freund 2010; Wilcox et al. 2018].

**Collection Classes.** We begin by verifying synchronization specifications and P/C equivalence on concurrent collection implementations. We adopted the following methodology in our work:

- (1) Write the synchronization specification and verify validity and stability.
- (2) Implement the code and verify it in a single-threaded setting via an ANCHOR command-line option for assuming no heap changes occur during yields.
- (3) Verify the code in a multi-threaded setting, in which the heap may change at yields.

We found the first two steps quite valuable, enabling us to first debug synchronization specifications without writing any code and then identify and fix as many programming/reduction errors as possible before reasoning about concurrent heap changes.

Table 1 lists the number of non-empty, non-comment lines of code in each component, as well as counts of: fields with synchronization specifications, yield annotations, and requires clauses and loop/object invariants. The table also includes ANCHOR verification time (computed as the average of 10 runs on a MacOS 10.15 computer with 3.2 GHz Intel Core i7 processor and 64GB of memory).

Our collection classes are adaptations of Java implementations presented in *The Art of Multi-processor Programming* [Herlihy and Shavit 2008]. (Table 1 refers to the origins of the techniques employed in the more sophisticated versions.) We include the lock-based and lock-free [Treiber 1986] stack implementations from Figure 3 as well as five linked list implementations that store integers in increasing order with no duplicates. Most of the requires clauses and invariants needed



to verify those lists are related to ordering rather than concurrency and would be needed even if verifying a sequential implementation.

The Coarse List protects all linked list nodes with a single lock, and the Fine List protects each node with its own lock. The latter utilizes hand-over-hand locking to support concurrent traversals. The yields indicate that other threads may change the list during traversals.

Optimistic and Lazy Lists adopt optimistic concurrency control mechanisms in which initial traversals performed without locking are followed by a validation step to ensure the absence of conflicts. The Lazy variant also supports a lock-free contains operations. The Lock-Free list foregoes locks altogether in favor of CAS operations. As one would expect, the three optimistic cases require more yield operations and result in proof obligations that are more difficult to dispatch, as evidenced by the higher ANCHOR run times.

The Coarse and Lock-Free Queues follow the same pattern in the number of yields required and the verification time. The Bounded Queue uses separate enqLock and deqLock locks for adding and removing items, enabling those operations to run in parallel. This Bounded Queue has a maximum capacity and a current size field, which requires a sophisticated synchronization specification. That field is essentially write-guarded by this, but it can only be incremented when the enqLock is held and size is smaller than capacity. Similarly, it can only be decremented when the deqLock is held and size is greater than 0.

```

int size moves_as isRead()
    ? write_guarded_by this
    : (holds(this.enqLock) && newValue==this.size+1 && this.size < this.capacity) ||
      holds(this.deqLock) && newValue==this.size-1 && 0 < this.size) ? write_guarded_by this
      : E
yields_as (0 <= this.size && this.size <= this.capacity)
==> ((0 <= newValue && newValue <= this.capacity) &&
      (holds(this.enqLock) ==> newValue <= this.size) &&
      (holds(this.deqLock) ==> newValue >= this.size));

```

This specification necessitates a yields\_as annotation to capture how size may change at a yield: if the current value is in the expected range 0..capacity, then it remains in that range. Also, if enqLock is held, size can only get smaller (due to concurrent dequeue operations), and vice-versa for deqLock. ANCHOR time is high due, we believe, to the need to solve verification conditions involving modular arithmetic. Time is also highly variable for this particular program due to the randomized nature of the underlying SMT solver.

Another sophisticated synchronization discipline readily captured by ANCHOR is the table array maintained by the Striped HashSet. That HashSet uses the objects stored in its locks array to guard the linked lists stored in the table array. More specifically, table[i] is guarded by locks[i % NUM], where NUM is the length of the locks array. A resizing operation replaces the table with a larger one when a certain usage threshold is reached. To ensure that resizing happens atomically with respect to other concurrent operations, the table field can be read when any lock is held but can only be modified when *all* locks are held:

```

List[moves_as guarded_by this.locks[index % NUM]] table
moves_as isRead() ? (exists int i :: 0 <= i && i < NUM && holds(this.locks[i])) ? B : E
: (forall int i :: 0 <= i && i < NUM ==> holds(this.locks[i])) ? B : E;

```

**FASTTRACK Dynamic Data Race Detector.** As an additional case study, we re-implemented the core FASTTRACK dynamic data race detection algorithm in ANCHOR. We chose this algorithm because it is a complex, self-contained concurrency component that has been precisely specified and previously verified [Wilcox et al. 2018] in the CIVL verifier [Hawblitzel et al. 2015a]. The algorithm



uses a variety of synchronization idioms in its six main entry points to ensure lock-free handling of the most common cases, including a mix of immutable, thread-local, read-only, lock-protected, write-protected, and volatile data, as well as synchronization mechanisms that change over time.

Despite having a sophisticated synchronization discipline, the algorithm itself is straightforward and was originally described in roughly 120 lines of Java-like pseudo-code. Our ANCHOR implementation is about 220 lines, with the additional lines due to syntactic differences, the inclusion of constructors absent in the original, and field and method duplication necessitated by the lack of inheritance. Verifying P/C equivalence required adding about 50 lines of synchronization specifications and other ANCHOR annotations. ANCHOR allowed for the precise and concise specification of all synchronization idioms used in the code. We refer the reader to the Supplementary Appendix for our FASTTRACK implementation and synchronization specification.

Earlier work used CIVL to verify that the FASTTRACK algorithm correctly implements a complete, formal specification of the FASTTRACK analysis rules. However, that correctness guarantee comes at a cost. The core algorithm requires about 250 lines of code in CIVL, but the CIVL specification consists of an additional roughly 530 additional lines [Flanagan et al. 2017]. In other words, the specification was roughly twice the size of the code. Those specifications are quite involved and reflect a significant amount of time and effort to develop.

To capture similar functional correctness guarantees for our ANCHOR version required adding an additional 100 lines of specification (primarily method specifications and loop invariants) to the 50 lines used for verifying P/C equivalence, making the total specification be 150 lines on top of the original 220 lines of code. In this case, the specification was only about 70% the size of the code but expressed the same key correctness requirements as the larger CIVL version.

One reason for this difference is ANCHOR's concise synchronization specifications, and its ability to characterize the possible effects of thread interference at yield points using these specifications. More verbose mechanisms are needed to do that in CIVL. One downside of ANCHOR's higher-level approach to synchronization specifications is that it generates more complex verification conditions that lead to longer Boogie verification times (presently about 2.5 minutes vs. 15 seconds for the CIVL version). However, we have yet not conducted performance tuning. We expect optimizing the generated VCs and introducing specialized triggers for quantified formulas to improve performance.

We also note that CIVL employs a lower-level programming language suitable for verification but not for execution or ease of use. In contrast, ANCHOR can compile input programs directly into Java, meaning that the code that's executed is exactly the code that is verified.

## 10 CONCLUSION

Reduction is an effective technique for concurrent program verification. Reduction proofs are fundamentally about movers that specify how heap operations commute over steps of other threads. This paper extends movers to play a primary role in synchronization specification, in addition to their traditional role in reduction-based verification.

In ANCHOR, conditional movers are the basis of both the programmer's conceptual model of correctness and the verifier's SMT-based reasoning, and are also used to communicate from the programmer to the verifier (via synchronization specifications) as well as from the verifier to the programmer (via error messages).

This approach appears to work well in practice. Conditional mover synchronization specifications are expressive, concise, and relatively intuitive. They enable a modular methodology for interleaved development and verification (Section 9), and they have enabled verification of several rather sophisticated concurrent algorithms with moderate effort.

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## A GENERIC REDUCTION THEOREM

We start by presenting a generic reduction theorem that extends Theorem 1 of [Flanagan and Qadeer 2003]. The key extension is that we now consider two operations to commute even if swapping them could introduce new errors (but never hide old errors), as any errors from a preemptive execution will still also be present in the corresponding cooperative execution obtained via repeated swapping.

Given a set of states  $State$ , with error states  $E \subseteq State$ , and transition relations  $\rightarrow_i, \rightarrow_j \subseteq State \times State$ , we say that  $\rightarrow_i$  *commutes with*  $\rightarrow_j$  *with respect to*  $E$  if whenever  $s_1 \rightarrow_i s_2 \rightarrow_j s_3$  then either:

- (1)  $\exists e \in E. s_1 \rightarrow_j e$ , or
- (2)  $\exists s_4 \in State, e \in E. s_1 \rightarrow_j s_4 \rightarrow_i e$ , or
- (3)  $\exists s_4 \in State. s_1 \rightarrow_j s_4 \rightarrow_i s_3$ .

Thus, swapping  $\rightarrow_i$  and  $\rightarrow_j$  transitions either does not affect the final state  $s_3$  or introduces a new error state  $e$ .

For  $S \subseteq State$ , we define

$$S/\rightarrow_i = (\rightarrow_i) \cap (S \times State)$$

$$\rightarrow_i \setminus S = (\rightarrow_i) \cap (State \times S)$$

**Theorem 6** (General Reduction). For all  $i$ , let  $R_i, L_i$ , and  $E_i$  be sets of states and  $\rightarrow_i$  be a transition relation. Suppose, for all  $i$ ,

- (1)  $R_i, L_i$ , and  $E_i$  are pairwise disjoint.
- (2)  $(L_i/\rightarrow_i \setminus R_i)$  is false.

and for all  $j \neq i$ ,

- (3)  $\rightarrow_i$  and  $\rightarrow_j$  are disjoint.
- (4)  $(\rightarrow_i \setminus R_i)$  commutes with  $\rightarrow_j$  with respect to  $E$ .
- (5)  $\rightarrow_j$  commutes with  $(L_i/\rightarrow_i)$  with respect to  $E$ .
- (6) if  $p \rightarrow_i q$ , then  $R_j(p) \Leftrightarrow R_j(q), L_j(p) \Leftrightarrow L_j(q), E_j(p) \Leftrightarrow E_j(q)$ .
- (7)  $\forall q \in L_i. q \rightarrow_i^* q' \in N_i$ , i.e.,  $q$  is non-blocking.

Let

$$N_i = \neg(R_i \vee L_i)$$

$$N = \forall i. N_i$$

$$E = \exists i. E_i$$

$$\rightarrow = \exists i. \rightarrow_i$$

$$\rightarrow = \exists i. (\forall j \neq i. N_j)/\rightarrow_i$$

If  $p \in N$  with  $p \not\rightarrow^* E$ , then

- (1)  $p \not\rightarrow^* E$ , and
- (2) if  $p \rightarrow^* q \in N$  then  $p \rightarrow^* q$ .

The proof of this theorem follows the structure of the proof of Theorem 1 in [Flanagan and Qadeer 2003], extended to permit the reduced trace to go wrong more often than the original.

## B PROOFS FOR SECTION 6

We now leverage the generic reduction theorem to prove our central reduction argument for ANCHOR.

First, we prove the  $\Rightarrow$ -steps right-commute (or go wrong) in the PRE phase and left-commute (or go wrong) in the POST phase.

Proving this property requires a notion like strict stability from Definition 5.2. That notion of stability is satisfied by many synchronization specifications. However, strict stability is sometimes overly restrictive. For example, it prohibits interleaved writes from increasing the access permissions of a thread. For maximal expressiveness, we instead derive a more relaxed notion of stability from the conditions necessary to prove the following commuting lemma for all pairs of possible execution steps.

**Definition B.1** (Stability). *Specification  $R, W$  is stable if for all  $l, k, t, H, v, w$ , and  $u$  where  $u \neq t$ :*

A.1	$W_l(t, H, v) \sqsubseteq R \wedge W_k(u, H[l := v], w) \sqsubseteq E \Rightarrow W_k(u, H, w) \in \{W_k(u, H[l := v], w), E\}$
A.2	$W_l(t, H, v) \neq E \wedge W_k(u, H[l := v], w) \not\sqsubseteq L \Rightarrow W_k(u, H, w) \not\sqsubseteq L$
A.3	$k \neq l \wedge W_l(t, H, v) \neq E \wedge W_k(u, H[l := v], w) \sqsubseteq L \Rightarrow W_k(u, H, w) \in \{W_k(u, H[l := v], w), E\}$
C	$W_l(t, H, v) \sqsubseteq E \wedge W_k(u, H, w) \sqsubseteq L \Rightarrow W_l(t, H[k := w], v) \in \{W_l(t, H, v), E\}$
D	$W_l(t, H, v) \sqsubseteq R \wedge W_k(u, H[l := v], w) \sqsubseteq N \Rightarrow W_l(t, H[k := w], v) \in \{W_l(t, H, v), E\}$
E	$W_l(t, H, v) \sqsubseteq N \wedge W_k(u, H[l := v], w) \sqsubseteq L \Rightarrow W_l(t, H[k := w], v) \in \{W_l(t, H, v), E\}$
F	$R_l(t, H) \sqsubseteq R \wedge W_k(u, H, w) \sqsubseteq N \Rightarrow R_l(t, H[k := w]) \in \{R_l(t, H), E\}$
H	$R_l(t, H, v) \sqsubseteq E \wedge W_k(u, H, w) \sqsubseteq L \Rightarrow R_l(t, H[k := w]) \in \{R_l(t, H), E\}$
I	$k \neq l \wedge R_l(t, H) \sqsubseteq N \wedge W_k(u, H, w) \sqsubseteq N \Rightarrow R_l(t, H[k := w]) \in \{R_l(t, H), E\}$
J	$W_l(t, H, v) \sqsubseteq R \wedge R_k(u, H) \sqsubseteq E \Rightarrow R_k(u, H) \in \{R_k(u, H[l := v]), E\}$
K	$W_l(t, H, v) \sqsubseteq N \wedge R_k(u, H[l := v]) \not\sqsubseteq L \Rightarrow R_k(u, H) \in \{R_k(u, H[l := v]), E\}$
L	$W_l(t, H, v) \sqsubseteq N \wedge R_k(u, H[l := v]) \not\sqsubseteq L \Rightarrow R_k(u, H) \not\sqsubseteq L$
M	$W_l(t, H, v) \sqsubseteq N \wedge W_k(u, H, w_1) \sqsubseteq E \Rightarrow W_k(u, H[k := w_1], w_2) \in \{W_k(u, H[l := v][k := w_1], w_2), E\}$
N	$W_l(t, H, v_1) \sqsubseteq E \wedge W_k(u, H, w) \sqsubseteq L \Rightarrow W_l(t, H[k := w][l := v_1], v_2) \in \{W_l(t, H[l := v_1], v_2), E\}$

(Shaded terms are trivially true but included for symmetry among the rules.)

**Lemma 1** (Commuting). Suppose  $R, W$  is a valid and stable synchronization discipline,  $u \neq t$ , and

$$\Pi_1 \Rightarrow_t \Pi_2 \Rightarrow_u \Pi_3$$

where  $\Pi_2 = T_2 \cdot H_2 \cdot C_2 \cdot P_2$ , and  $P_2(t) = \text{PRE}$  or  $P_2(u) = \text{POST}$ . Then:

- (1)  $\exists \Pi_4. \Pi_1 \Rightarrow_u \Pi_4 \Rightarrow_t \Pi_3$ , or
- (2)  $\exists \Pi_4, \Pi_5. \Pi_1 \Rightarrow_u \Pi_4 \Rightarrow_t \Pi_5$  and  $t$  is wrong in  $\Pi_5$ , or
- (3)  $\exists \Pi_4. \Pi_1 \Rightarrow_u \Pi_4$  and  $u$  is wrong in  $\Pi_4$ .

Next, we define the predicates  $\mathbb{R}_i, \mathbb{L}_i, \mathbb{E}_i, \mathbb{N}_i, \mathbb{N} \subseteq \Pi$  over an instrumented state  $\Pi = T \cdot P \cdot H$ :

$$\begin{aligned}
 \mathbb{R}_i(\Pi) &= P[i] = \text{PRE} \wedge \neg \mathbb{N}_i(\Pi) \\
 \mathbb{L}_i(\Pi) &= P[i] = \text{POST} \wedge \neg \mathbb{N}_i(\Pi) \\
 \mathbb{E}_i(\Pi) &= \text{thread } i \text{ is wrong in } \Pi \\
 \mathbb{N}_i(\Pi) &= \text{thread } i \text{ is yielding in } \Pi \\
 \mathbb{N}(\Pi) &= \forall i. \mathbb{N}_i(\Pi)
 \end{aligned}$$

These predicates characterize whether thread  $i$  is in the pre-commit, or right-mover, part of a reducible code sequence ( $\mathbb{R}_i$ ); in the post-commit, or left-mover, part ( $\mathbb{L}_i$ ); gone wrong ( $\mathbb{E}_i$ ); or is yielding ( $\mathbb{N}_i$ ).

We can now formalize the *nonblocking* requirement that any transaction that has passed its commit point must be able to terminate, i.e. if  $\Pi_0 \Rightarrow^* \Pi'$  and  $\mathbb{L}_i(\Pi')$  then  $\Pi' \Rightarrow_i^* \Pi''$  such that  $\mathbb{N}_i(\Pi'')$ .

**Restatement of Theorem 3** (Reduction). If  $\Pi = T_0 \cdot H_0 \cdot C_0 \cdot P_0$  and  $\Pi_0$  does not go wrong under  $\Rightarrow$ , then:

- (1)  $\Pi_0$  does not go wrong under  $\Rightarrow$ .
- (2) If  $\Pi_0 \Rightarrow^* \Pi$  where  $\Pi$  is yielding, then  $\Pi_0 \models^* \Pi$ .

PROOF. By Theorem 6, where the preconditions of that theorem are satisfied as follows. For all  $i, j \in \text{Tid}$  where  $i \neq j$ :

- (1)  $\mathbb{R}_i$ ,  $\mathbb{L}_i$ , and  $\mathbb{E}_i$  are pairwise disjoint by construction.
- (2)  $\mathbb{L}_i / \Rightarrow_i \setminus \mathbb{R}_i$  is false.  $\mathbb{L}_i$  says that  $P(i) = \text{POST}$  and  $T(i)$  is not yielding.  $\mathbb{R}_i$  says that  $P(i) = \text{PRE}$ . However, the only transition of  $P(i)$  from  $\text{POST}$  to  $\text{PRE}$  is for yield.
- (3)  $\Rightarrow_i$  and  $\Rightarrow_j$  are disjoint.
- (4)  $\Rightarrow_i / \mathbb{R}_i$  commutes with  $\Rightarrow_j$  with respect to  $E_i$ . By Lemma 1.
- (5)  $\Rightarrow_j$  commutes with  $\mathbb{L}_i \setminus \Rightarrow_i$  with respect to  $E_i$ . By Lemma 1.
- (6)  $\Rightarrow_i$  does not change the phase or statements of other threads.
- (7) By the non-blocking assumption.

□

## C VERIFIEDFT IMPLEMENTATION IN ANCHOR

The following is the ANCHOR implementation of the core FASTTRACK algorithm, as outlined in [Wilcox et al. 2018]. It includes the specification of the synchronization discipline, and ANCHOR verifies that this code is P/C equivalent.

```

/*
  An Anchor implementation of the VerifiedFT-v2 algorithm from

  VerifiedFT: A Verified, High-Performance Precise Dynamic Race Detector
  James R. Wilcox, Cormac Flanagan, Stephen N. Freund
  PPOPP, 2018

  We refer the reader to that paper for a full discussion of the
  synchronization and algorithm.

  Notes:

  * In the original, inheritance was used to create three specialized
    versions of VectorClocks for ThreadState, VarState, LockState. In
    Anchor, we needed to duplicate the VectorClock code in each of the
    three classes since there is no inheritance.

  * Unlike the original, we include initializers for each of the
    three main classes.

  * We use array abbreviations in Anchor, which were not included in
    the paper, eg:

    array T = int[moves_as ...]

    This introduces an array type abbreviation that can be used
    later, as in

    [T] v = new [T](10);

  * In array specs, the array object is referred to as "athis", and the
    enclosing object is "this".

  * We encode an ecoch tid@c as (tid + c * 256). That is, the lower 8
    bits of an int is the tid and the upper 24 is the clock. We
    assume no more than 255 threads will be used and that overflow
    does not occur. We use the constant -1 to represent the SHARED
    special value.
*/

// Some macros to avoid repeated low-level expressions:
#define EPOCH_TID(x) (x % 256)
#define EPOCH_CLOCK(x) (x / 256)
#define EPOCH_LEQ(x,y) x <= y
#define INC(x) (x + 256)

```



```

1422 #define VC_GET(vc, i) ((i < vc.length) ? vc[i] : (i))
1423 #define MAX(x,y) ((x) > (y) ? (x) : (y))
1424
1425 class Object { }
1426
1427 //
1428
1429 class VarState {
1430
1431     // NOTES:
1432     // * SHARED is -1.
1433     // * We omitted thread-local accesses from the specs in the body of the paper
1434     //   for simplicity, but include them here in order to verify
1435     //   the VarState constructor.
1436
1437     array VC_VarState =
1438         int[moves_as isLocal(athis) ? B
1439             : (this.read != -1) ? guarded_by this
1440               : isRead() ? (holds(this) || tid == index ? B:E)
1441               : (holds(this) && tid == index ? B:E)]
1442
1443     volatile int read moves_as isLocal(this) ? B
1444         : (this.read != -1) ? write_guarded_by this
1445           : (isRead() ? R : E);
1446
1447     volatile int write moves_as isLocal(this) ? B : write_guarded_by this;
1448
1449     volatile [VC_VarState] vc moves_as isLocal(this) ? B
1450         : (this.read != -1) ? guarded_by this
1451           : write_guarded_by this;
1452
1453     invariant isShared(this) ==> this.vc != null;
1454
1455     public VarState() {
1456         this.read = 0;
1457         this.write = 0;
1458         this.vc = new [VC_VarState](0);
1459     }
1460
1461     int get(int i) {
1462         [VC_VarState] vc = this.vc;
1463         return (i < vc.length) ? vc[i] : i;
1464     }
1465
1466     void ensureCapacity(int n) {
1467         if (n > this.vc.length) {
1468             [VC_VarState] newVC = new [VC_VarState](n);
1469
1470             for (int i = 0; i < n; i = i + 1) {
1471                 newVC[i] = this.get(i);
1472             }
1473         }
1474     }

```

```

1471         this.vc = newVC;
1472     }
1473 }
1474
1475 void set(int index, int value) {
1476     this.ensureCapacity(index + 1);
1477     this.vc[index] = value;
1478 }
1479
1480 int size() {
1481     return this.vc.length;
1482 }
1483
1484 bool leq(ThreadState st) {
1485     int stSize = st.size();
1486     int thisSize = this.size();
1487     int n = MAX(thisSize, stSize);
1488     int i = 0;
1489     while (i < n) {
1490         if (this.get(i) > st.get(i)) {
1491             return false;
1492         }
1493         i = i + 1;
1494     }
1495     return true;
1496 }
1497
1498 //
1499
1500 class LockState {
1501     array VC_LockState = int[moves_as guarded_by this.target]
1502
1503     Object target moves_as isLocal(this) ? B : readonly;
1504
1505     [VC_LockState] vc moves_as isLocal(this) ? B : guarded_by this.target;
1506
1507     invariant isShared(this.target);
1508     invariant isShared(this) ==> this.vc != null;
1509
1510     requires target != null;
1511     public LockState(Object target) {
1512         this.target = target;
1513         this.vc = new [VC_LockState](0);
1514     }
1515
1516     int get(int i) {
1517         [VC_LockState] vc = this.vc;
1518         return (i < vc.length) ? vc[i] : i;
1519     }
1520
1521     void ensureCapacity(int n) {

```

```

1520     [VC_LockState] vc = this.vc;
1521
1522     if (n > vc.length) {
1523         [VC_LockState] newVC = new [VC_LockState](n);
1524         for (int i = 0; i < n; i = i + 1) {
1525             newVC[i] = this.get(i);
1526         }
1527         this.vc = newVC;
1528     }
1529
1530     void set(int index, int value) {
1531         this.ensureCapacity(index + 1);
1532         this.vc[index] = value;
1533     }
1534
1535     int size() {
1536         return this.vc.length;
1537     }
1538
1539     void copy(ThreadState st) {
1540         [VC_LockState] oldVCPtr = this.vc;
1541
1542         this.ensureCapacity(st.size());
1543         for (int j = 0; j < this.size(); j = j + 1) {
1544             int x = st.get(j);
1545             this.vc[j] = x;
1546         }
1547     }
1548
1549     //////////
1550     class ThreadState {
1551
1552         array VC_ThreadState = int[moves_as isLocal(this) ? B
1553                                     : this.stopped ? (isRead() ? B : E)
1554                                     : (tid == this.t ? B:E)]
1555
1556         volatile bool stopped
1557             moves_as isLocal(this) ? B
1558                 : isRead() ? (tid == this.t ? B
1559                               : (this.stopped ? R : N))
1560                 : (tid == this.t && !this.stopped && newValue ? N : E);
1561
1562         Tid t moves_as isLocal(this) ? B : readonly;
1563
1564         invariant 0 <= this.t && this.t < 256;
1565
1566         volatile [VC_ThreadState] vc
1567             moves_as isLocal(this) ? B
1568                 : this.stopped ? isRead() ? B : E

```

```

1569                                     : (tid == this.t ? B : E);
1570
1571 invariant isShared(this.vc) && this.vc != null;
1572
1573
1574 int get(int i) {
1575     [VC_ThreadState[this]] vc = this.vc;
1576     return (i < vc.length) ? vc[i] : i;
1577 }
1578
1579 void set(int index, int value) {
1580     this.ensureCapacity(index + 1);
1581     this.vc[index] = value;
1582 }
1583
1584 void ensureCapacity(int n) {
1585     [VC_ThreadState] vc = this.vc;
1586
1587     if (n > vc.length) {
1588         [VC_ThreadState] newVC = new [VC_ThreadState](n);
1589
1590         for (int i = 0; i < n; i = i + 1) {
1591             newVC[i] = this.get(i);
1592         }
1593         this.vc = newVC;
1594     }
1595 }
1596
1597 int size() {
1598     return this.vc.length;
1599 }
1600
1601 void joinThread(ThreadState st) {
1602     for (int i = 0; i < st.size(); i = i + 1) {
1603         int thisI = this.get(i);
1604         int stI = st.get(i);
1605         this.set(i, MAX(thisI, stI));
1606     }
1607 }
1608
1609 void inc(int t) {
1610     this.set(t, INC(this.get(t)));
1611 }
1612
1613 requires tid == this.t;
1614 requires !this.stopped;
1615 public bool write(VarState sx) {
1616     int e = this.get(this.t);
1617     int w = sx.write;
1618     if (w == e) { return true; }
1619     yield;

```

```

1618     synchronized(sx) {
1619         w = sx.write;
1620         int ww = this.get(EPOCH_TID(w));
1621         if (w > ww) { return false; }
1622         int r = sx.read;
1623         if (r != -1) {
1624             int rr = this.get(EPOCH_TID(r));
1625             if (r > rr) { return false; }
1626             sx.write = e;
1627         } else {
1628             if (!sx.leq(this)) {
1629                 return false;
1630             }
1631             sx.write = e;
1632         }
1633         return true;
1634     }
1635
1636     requires tid == this.t;
1637     requires !this. stopped;
1638     public bool read(VarState sx) {
1639         int t = this.t;
1640         int e = this.get(t);
1641
1642         int r;
1643         r = sx.read;
1644         if (r == e || r == -1 && sx.get(t) == e) { return true; }
1645         yield;
1646         synchronized(sx) {
1647             int w = sx.write;
1648             int ww = this.get(EPOCH_TID(w));
1649             if (w > ww) { return false; }
1650             r = sx.read;
1651             if (r != -1) {
1652                 int rr = this.get(EPOCH_TID(r));
1653                 if (r <= rr) {
1654                     sx.read = e;
1655                 } else {
1656                     sx.set(EPOCH_TID(r), r);
1657                     sx.set(t, e);
1658                     sx.read = -1;
1659                     return true;
1660                 }
1661             } else {
1662                 sx.set(t, e);
1663             }
1664         }
1665         return true;
1666     }

```

```

1667     requires tid == this.t;
1668     requires !this.stopped;
1669     requires holds(sm.target);
1670     public void acq(LockState sm) {
1671         [VC_ThreadState] oldThisVc = this.vc;
1672         for (int j = 0; j < sm.size(); j = j + 1)
1673         {
1674             int thisJ = this.get(j);
1675             int smJ = sm.get(j);
1676             this.set(j, MAX(thisJ, smJ));
1677         }
1678     }
1679
1680     requires tid ==this.t;
1681     requires !this.stopped;
1682     requires holds(sm.target);
1683     modifies sm, sm.vc;
1684     public void rel(LockState sm) {
1685         sm.copy(this);
1686     }
1687
1688
1689     requires 0 <= t && t < 256;
1690     requires t != 0 ==> forker != null && tid == forker.t;
1691     public ThreadState(int t, ThreadState forker) {
1692         this.t = t;
1693         this.stopped = false;
1694
1695         if (t != 0) {
1696             int fSize = forker.size();
1697             int n = MAX(t + 1, fSize);
1698             [VC_ThreadState] vc = new[VC_ThreadState] (n);
1699             for (int i = 0; i < n; i = i + 1) {
1700                 vc[i] = i == t ? INC(forker.get(i)) : forker.get(i);
1701             }
1702             this.vc = vc;
1703         } else {
1704             [VC_ThreadState] vc = new[VC_ThreadState](1);
1705             vc[0] = 256;
1706             this.vc = vc;
1707         }
1708     }
1709
1710     requires tid == this.t;
1711     requires !this.stopped;
1712     requires this.t != uTid;
1713     requires uTid > 0 && uTid < 256;
1714     public ThreadState fork(int uTid) {
1715         // We create the new ThreadState object here so that we

```

```
1716     // have threadlocal access to it.
1717     ThreadState u = new ThreadState(uTid, this);
1718     this.inc(this.t);
1719     return u;
1720 }
1721
1722
1723 requires tid == this.t;
1724 requires !this.stopped;
1725 requires u.stopped;
1726 public void join(ThreadState u) {
1727     [VC_ThreadState] oldVCPtr = this.vc;
1728     int n = MAX(u.size(), this.size());
1729
1730     for (int i = 0; i < n; i = i + 1) {
1731         int uI = u.get(i);
1732         int thisI = this.get(i);
1733         int x = MAX(uI, thisI);
1734         this.set(i, x);
1735     }
1736     this.inc(this.t);
1737 }
1738
1739 }
1740
1741
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