CV for Sin Sai Weng, Terry 冼世榮

Associate Professor

Academic Qualifications

Ph.D. in Electrical and Electronics Engineering, Faculty of Science and Technology, University of Macau, China (2008)

M.Sc. in Electrical and Electronics Engineering, Faculty of Science and Technology, University of Macau, China (2003)

B.Sc. in Electrical and Electronics Engineering, Faculty of Science and Technology, University of Macau, China (2001)

Professional Experience

Associate Head, Dept. of ECE, FST, University of Macau (2016 Nov – present)

Associate Professor, Dept. of ECE, FST, University of Macau (2015 – present)

Assistant Professor, Dept. of ECE, FST, University of Macau (2009 – 2015)

Academic Coordinator, State-Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau (2014 – Present)

Coordinator, Data Conversion and Signal Processing (DCSP) Research Line, State-Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau (2007 – Present)

Co-Coordinator, Integrated Power Research Line, State-Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau (2007 – Present)

Post-Doctoral Fellow, Analog and Mixed-Signal VLSI Laboratory, Dept. of EEE, FST, University of Macau (2008 –2009)

Senior Research Assistant, Analog and Mixed-Signal VLSI Laboratory, Dept. of EEE, FST, University of Macau (2007 –2008)

Teaching Experience

B.Sc. Courses

1. Analog Integrated Circuit Design (ELEC371)
2. Signals and Systems (ECEB210/ELEC261)
3. System Design (ELEC437) / Design Project I (ECEB410)
4. Project (ELEC402) / Design Project II (ECEB420)

M.Sc. Courses

1. Advanced Topics in Analog and Mixed-Signal Integrated Circuits (IMSE022/ELCE722)
2. Microelectronic Circuit Design (IMSE004)
3. Microelectronic for Telecommunication and Signal Processing (IMSE011/ELCE711)
4. Introduction to Research (IMSE001/ELCE701)
5. Thesis (ELCE799)

Ph.D Courses

1. Advanced Topics in Electrical and Computer Engineering (ELCE818)
2. Microelectronics in Signal Processing and Communications (ELCE808)

Research

Research Interests

- High-Performance Data Converters
  - Pipelined, SAR, Flash, Binary Search, etc…
  - Oversampling Data Converters
- Power Management Integrate Circuits
- Analog and Mixed-Signal Integrated Circuits
- Low Voltage Switched-Capacitor Circuits
- Integrated Analog Front-Ends

Thesis Co-Supervision

Ph.D Theses

1.	**Jan 2015 – Present**	**Qi Liang**, *CMOS Continuous-Time MASH Sigma-Delta Modulators*
2.	**Sep 2014 – Present**	**Dongyang Jiang**, *Advanced Techniques for CMOS Sigma-Delta Modulators*
3.	**Sep 2014 – Present**	**Mingqiang Guo**, *Advanced Techniques for CMOS Pipelined Data Converters*
4.	**Sep 2014 – Present**	**Shasha Liu**, *Advanced Techniques for CMOS Pipelined Data Converters*
5.	**Sep 2013 – Present**	**Biao Wang**, *Incremental Oversampling Sigma-Delta*

Converters

6. **Sep 2012 – Present** **Xing Dezhi,** *Advanced Techniques in Analog to Digital Converters*
7. **Sep 2012 – Present** **Jianwei Liu,** *Time-to-Digital Converter*
8. **Sep 2010 – Present** **Feng Da,** *Hybrid Continuous- and Discrete-Time Sigma-Delta Modulator*
9. **Sep 2009 – Jan 2017** **Arshad Hussain,** *The Design of Passive Sigma-Delta ADC*
10. **Sep 2009 – Sep 2016** **Zhong Jianyu,** *Design of High-Speed, Power-efficient SAR-Type ADCs*
11. **Sep 2011 – Jul 2015** **Chi-Hang Chan,** *Design Techniques and Considerations in Low to Moderate to Low Resolution Power efficient GHz Range ADCs*
12. **Sep 2005 – Apr 2012** **U-Fat Chio, Design Techniques for Low-Power High-Speed Analog-to-Digital Converters using Binary-Search and Subranging Schemes**

Master Theses

1. **Sep 2016 – Present** *Cui Song, Digital Calibration Techniques for CMOS Pipelined Converters*
2. **Sep 2016 – Present** *Hanyu Wang, Digital Calibration Techniques for CMOS Pipelined Converters*
3. **Sep 2014 – Present** *Jixuan Li, Power Efficient Techniques for Battery Management System*
4. **Sep 2014 – Present** *Hubert Liang, Low Power Sigma-Delta Modulator*
5. **Sep 2013 – Present** *Jiaji Mao, Low Power Pipelined Analog-to-Digital Converter*
6. **Sep 2012 – May 2017** *Qin Weiwei, Measurement Techniques for High-Performance Data Converters*
7. **Sep 2012 – May 2017** *Yan Rongshen, On the Study of Advanced CMOS Operational Amplifiers*
8. **Sep 2012 – Dec 2016** *Li Wei, On the Study of Mixed Signal Interface Circuit for Inertial Navigation System*

9. **Sep 2012 – Dec 2016** *Ren Yuan, On the study of High DR Multi-Channel Stage-Shared Hybrid Front-End for Integrated Power Electronics Controller*

10. **Sep 2010 – Oct 2013** *Yun Du, High-Performance Continuous-Time Sigma-Delta Modulator*

11. **Sep 2006 – Mar 2015** **Yuan Fei**, *A 10b Pipelined ADC with Nonlinear Digital Background Calibration & 2.5b/stage Opamp Sharing Architecture*

12. **Sep 2010 – Jul 2013** **Wenlan Wu**, *Monotonic Multi-Switching Method for Ultra-Low-Voltage Energy Efficient SAR ADCs*

13. **Sep 2006 – Jul 2013** **Cheok-Teng Lei**, *Applying the Novel High Speed Robust Level Converter to a 12-bit Successive Approximation Analog-to-Digital Converters with Dual Supply Domain*

14. **Sep 2009 – Feb 2013** **Cai Chenyan**, *Low Power High Efficiency Excess-Loop-Delay Compensation Techniques in Continuous-Time Delta-Sigma Modulators*

15. **Sep 2009 – Jun 2012** **Jiang Yang**, *On the Study of Clock-Jitter Insensitive Circuit Techniques in Continuous-Time Sigma-Delta Modulators*

16. **Sep 2010 – May 2012** **Peng Zhang**, *时间交织型模数转换器时钟偏差校准技术研究(Joint-Supervision with Tsinghua University)*

17. **Sep 2010 – May 2012** **Zhijie Chen**, *应用于生物医学领域的ΣΔ调制器低功耗研究 (Joint-Supervision with Tsinghua University)*

18. **Sep 2009 – May 2012** **Rui Wang**, *基于数字校准的流水线逐次逼近模数转换器的芯片实现 (Joint-Supervision with Tsinghua University)*

19. **Sep 2009 – Dec 2011** **Guohe Yin**, *满足生物医学低功耗需求的模数转换器设计技术研究 (Joint-Supervision with Tsinghua University)*

20. **Sep 2009 – Jul 2011** **Chi-Hang Chan**, *A Study on Comparator and Offset*

Calibration Techniques in High Speed Nyquist ADCs

21. **Sep 2009 – Jul 2011** **Si-Seng Wong,** *Design of Analog-to-Digital Converters with Binary Search Algorithm and Digital Calibration Techniques*

22. **Sep 2008 – Aug 2010** **Li Ding,** *Comprehensive Digital Calibration Techniques For High Resolution ADCs*

23. **Sep 2007 – Aug 2010** **Kim-Fai Wong,** *Speed Enhancement Techniques for Comparator-Based Switched-Capacitor Circuits*

Bachelor Theses **(15 Projects, 27 B.Sc students)**

1. **Sep 2016 – Present** **Leong Hoi Chon, Lam Sao Son,** *High Performance Pipelined Analog-to-Digital Converter*

2. **Sep 2016 – Present** **Chu Meng Lok,** *Low quiescent current power management*

3. **Jul 2015 – Jun 2016** **Wang Linxuan, Mao Xinwei, Cui Song,** *Bandwidth mismatch calibration techniques for wideband time-interleaved pipelined analog-to-digital converters*

4. **Jul 2013 – Jun 2014** **Jiang Dongyang, Liang Junhao,** *A 107 dB DR, 106dB SNDR Sigma-Delta ADC Using a Charge-Pump Integrator for Audio Application*

5. **Jul 2013 – Jun 2014** **Li Ji Xuan, Zeng Wen Liang,** *Power Efficient and Fast Charger Techniques Applied for Battery Management System*

6. **Jul 2012 – Jun 2013** **Fong Tek Kei,** *A 103dB Dynamic Range, 106dB SNDR Sigma-Delta ADC for Audio Applications*

7. **Jul 2012 – Jun 2013** **Bai Ziwen,** *A Micropower Management System for Photovoltaic Cells with Maximum Output Power Control*

8. **Jul 2011 – Jun 2012** **Zhou Tianxiang,** *A Multibit Dual-Feedback CT Sigma Delta Modulator with Lowpass Signal Transfer Function*

9. **Jul 2011 – Jun 2012** **Cheng Xiaojing, Ding Shixuan,** *Wideband Time-Interleaved Pipelined ADC using LMS Timing-Skew Calibration Engine for a 4G LTE Smartphone*

10. **Jul 2010 – Jun 2011** **Yan Pengyu, Chen Zhiyuan,** *A 13-bit 64 MS/s Digital Enhanced Pipelined ADC for 4G LTE Application*

11. **Jul 2009 – Jun 2010** **Du Yun, He Tao,** *A 65nm CMOS High-Speed Low-Power Continuous-Time Sigma-Delta Modulator with VCO-Based Quantizer for WiMAX Application*

12. **Jul 2008 – Jun 2009** **Jiang Yang, Yu Xiaofeng, Cai Chenyan,** *A 65nm CMOS High-Speed Low-Power Continuous-Time Sigma-Delta Modulator For 3G WCDMA Receivers*

13. **Jul 2008 – Jun 2009** **Fan Wa Pan, Chio Chan Keong,** *A 1-V 12-bit 200-MS/s Pipelined ADC with Digital Signal-Dependant Dithering Calibration for HDTV Video Analog Frond-End*

14. **Jul 2007 – Jun 2008** **Chon-Hei Lei**, *Background Digital Calibration for Full HD(High-Definition) Video Analog Front-End*

15. **Jul 2007 – Jun 2008** **Sio Chan** *and* **Li Ding,** *Low-Power High-Speed Comparator-Based Pipeline ADC for Portable Wireless Devices*

16. **Jul 2007 – Jun 2008** **Wai-Hou Chan and Li Xie**, *A 10-bit 60-MS/s Asynchronous Charge-Sharing SAR ADC in 90-nm CMOS for Mobile TV Applications*

17. **Jul 2007 – Jun 2008** **Yin-Sheng Zhao and Seng-Cheong Chao,** *Comparator-Based Multi-mode Sigma Delta Modulator for 3G Analog Front-End*

18. **Jul 2007 – Jun 2008** **Po-Lap Chan and Ka-Cheong Lao,** *Study of Low Drop-Out Regulators for Power Management in Portable Devices*

Funded Research Projects

- **Principal Investigator**, "Mismatch- and Supply-Noise-Tolerant Design for Wideband Nyquist Analog-to-Digital Conversion Integrated Circuits," Multi-Year Research Grant, funded by Research Committee of University, 2018 – 2020.
- **Member**, "Research on mm-size Extremely Power-Constrained Implantable ECG System on Chip Design," Jointly-funded by Macau Science and Technology Development Fund & National Science Foundation Committee, China (FDCT-NSFC), 2017 – 2019.
- **Principal Investigator**, "High-Performance Wideband Data Conversion Interfaces for an Evolving Informative World," funded by Macau Science and Technology Development Fund & Match-Fund from RC, UM, 2014 – 2016.

- **Co-Principal Investigator**, "ASIANS – Advances on Sensor Inertial Aided Navigation Systems," Multi-Year Research Grant, funded by Research Committee of University, 2012 – 2015.
- **Principal Investigator**, "Support in Establishment of State Key Laboratory of Analog and Mixed-Signal VLSI (Data Conversion and Signal Processing Research Line)," funded by Macau Science and Technology Development Fund, 2011 – 2013.
- **Principal Investigator**, "Research and Development of Comprehensive Data Conversion Platforms in Nanometer CMOS Technology," funded by Macau Science and Technology Development Fund, 2010 – 2012.
- **Principal Investigator**, "Research and Development of Comprehensive Data Conversion Platforms in Nanometer CMOS Technology," Match-Fund, funded by Research Committee of University, 2010 – 2012.
- **Co-Principal Investigator**, "Integrated generalized PWM controller for DC-AC inverter," funded by Macau Science and Technology Development Fund, 2010 – 2012.
- **Co-Principal Investigator**, "Integrated generalized PWM controller for DC-AC inverter," Match-Fund, funded by Research Committee of University, 2010 – 2012.
- **Co-Principal Investigator**, "High-Speed, High-Resolution, Low-Power Analog-to-Digital Conversion System with Emerging Scaled CMOS Technology," funded by Macau Science and Technology Development Fund, 2007 – 2009.
- **Co-Principal Investigator**, "High-Speed, High-Resolution, Low-Power Analog-to-Digital Conversion System with Emerging Scaled CMOS Technology," Match-Fund, funded by Research Committee of University, 2007 – 2009.

Industrial Engineering Projects

- Advanced IC project developed in the area of high-performance Analog-to-Digital Converter, in collaboration with Hisilicon-Huawei, China.
- Advanced engineering project developed in the area of high-performance Analog-to-Digital Converter, in collaboration with Synopsys-Chipidea.

Professional Services - External

2016	**Publication Chair,** The IEEE Asian South Pacific Design Automation Conference (ASPDAC)
2015	**Track Chair,** The IEEE TENCON Conference
2013 - Present	**Technical Program Committee Member,** The IEEE Asian Solid-State Circuits Conference (A-SSCC)
2013 - Present	**Student Design Contest Committee Member,** The IEEE Asian Solid-State Circuits Conference (A-SSCC)
2015	**Review Track Chair,** The IEEE TENCON Conference
2015	**Technical Program Committee Member,** The IEEE VLSI-SoC Conference
2015	**Technical Program Committee Member,** The IEEE International Wireless Symposium Conference
2015	**Technical Program Committee Member,** The IEEE ASICON Conference
2011 - 2012	**Technical Program Committee Member,** The IEEE Radio Frequency Integration Technology Conference (RFIT)
2012	**Ph.D Defense Examination Committee Member (External),** The New University of Lisbon, Lisboa, Portugal
2011	**Technical Program Committee Member,** The IEEE Sensors 2011 Conference
2009 - Present	**Secretary,** IEEE Solid-State Circuit Society (SSCS) Macau Chapter.
2009 - Present	**Treasurer/Secretary,** IEEE Macau CAS/COM Joint Chapter.
2009	**Review Committee Member (RCM),** The 2009 Asia Pacific Conference on Postgraduate Research in Microelectronics & Electronics (PrimeAsia)
Dec 2008	**Special-Session Co-Chair & Local Organization Member,** IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), 2008, Macau, China.
Jul 2008	**Referee Committee,** 2008 Macau's High-School Student Funny Science Competition, Macau, China
Jul 2006	**Technical Session Chair,** the Regional Inter-University Postgraduate Electrical and Electronic Engineering Conference (RIUPEEEC), 2006, Macau, China

Dec 2004	**Financial Committee Co-Chair & Technical Session Co-Chair**, 2004 IEEE/IEEJ (7th) International Analog VLSI Workshop, Macau, China

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Professional Services - Internal

2012 Sept - Present	**Chair, Program Revision Committee,** ECE, FST, University of Macau
2012 - Present	**Member, Department Executive Committee** ECE, FST, University of Macau
2012 Sept – 2013 Aug	**Member, Program Accreditation Committee,** ECE, FST, University of Macau
Sep 2007 – Present	**Coordinator**, **Data Conversion and Signal Processing (DCSP) Research Line**, State-Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau
Sep 2007 – Present	**Co-Coordinator**, **Integrated Power Research Line**, State-Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau
2011 – 2012 Aug	**Member of Board of Examiner, ECE, FST, University of Macau**
2010 - Present	**PhD Thesis Proposal Assessment Committee Member, FST, University of Macau**
2010 - Present	**PhD Qualifying Examination Committee Member, FST, University of Macau**
2009 - 2010	**Member of Establishment Task Force, State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau**
2009 - 2011	**Mentor, FST, University of Macau**
2009 - Present	**Member of Academic Council, FST, University of Macau.**

Professional Review Services

- Journal
  - IEEE Journal of Solid-State Circuits
  - IEEE Transactions on Circuits and Systems I – Regular Papers
  - IEEE Transactions on Circuits and Systems II – Express Briefs
  - IEEE Transactions on VLSI Systems

- IEEE Transactions on Instrumentation and Measurement
- Journal of Circuits, Systems and Computers
- International Journal of Circuit Theory and Applications

▪ Conferences

- IEEE International Symposium on Circuits and Systems (ISCAS)
- IEEE Biomedical Circuits and Systems Conference (BIOCAS)
- IEEE Conference on Postgraduate Research in Microelectronics & Electronics (PRIME)
- IEEE Conference on Asia-Pacific Conference on Postgraduate Research in Microelectronics & Electronics (PrimeAsia)

Honors and Awards

2016 **Co-recipient of Third Class, Macau Scientific and Technological Invention Award 澳門科學技術發明獎三等獎**

2014 **Co-recipient of Second Class, Macau Scientific and Technological Invention Award 澳門科學技術發明獎二等獎**

2012 **Co-recipient of Second Class, Macau Scientific and Technological Invention Award 澳門科學技術發明獎二等獎**

2012 **Co-recipient of Macau Scientific and Technological Special Award 澳門科學技術特別獎勵**

2011 **(First-time in Macau) Co-recipient of Second Class, State Scientific and Technological Progress Award (澳門首獲)國家科學技術進步獎二等獎**

Nov 2008 **Chipidea Microelectronics Prize – Postgraduate Level,** for the outstanding academic and research achievement in Microelectronics. (organized by University of Macau)

Jul 2006 **Paper with Certificate of Merit**, *Regional Inter-University Post-graduate Electrical and Electronic Engineering Conference – IEEE RIUPEEEC'2006.*

May 2005 **Student Paper Contest Award,** *International Symposium on Circuits and Systems (ISCAS'2005)*:

Student Honors and Awards under Advisory

Oct 2016 1 students win **2016 Postgraduate Science and Technology Research and Development Award (FDCT)**

Oct 2014 2 students win **2016 Postgraduate Science and Technology Research and Development Award (FDCT)**

Nov 2012 4 students win **2012 Postgraduate Science and Technology Research and Development Award (FDCT)**

Jun 2012 ***2012 Best Master Thesis Award in Tsinghua University***

By Guohe Yin, *满足生物医学低功耗需求的模数转换器设计技术研究 (Joint-Supervision with Tsinghua University)*

Jun 2012 **Travel Grant Award, 2012 IEEE Symposium on VLSI Circuits, Hawaii**

Paper: Chi-Hang Chan, Yan Zhu, Sai-Weng Sin, Seng-Pan U, and R. P. Martins, "A 3.8mW 8b 1GS/s 2b/cycle Interleaving SAR ADC with Compact DAC Structure"

Nov 2011 **Student Design Contest Award, IEEE 2011 Asian Solid-State Circuits Conference (A-SSCC)**

Paper: Yan Zhu, Chi-Hang Chan, Sai-Weng Sin, Seng-Pan U, R.P.Martins, Franco Maloberti, "A 35 fJ 10b 160 MS/s Pipelined-SAR ADC with Decoupled Flip-Around MDAC and Self-Embedded Offset Cancellation"

Feb 2011 **Silk Road Paper Award, IEEE 2011 Internal Solid-State Circuits Conference (ISSCC)**

Paper: He-Gong Wei, Chi-Hang Chan, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, R. P. Martins and F. Maloberti, "A 0.024mm2 8-bit 400 MS/s SAR ADC with 2-bit per Cycle and Resistive DAC in 65 nm CMOS"

Jun 2012 **2nd Runner-up** for the Final Year Project Supervised: Zhao Tianxiang, "A Multibit Dual-Feedback CT Sigma Delta Modulator with Lowpass Signal Transfer Function," ***2012 IEEE Project Competition, Macau***

Nov 2009 **Third Prize** for the Final Year Project Supervised: Jiang Yang, Yu Xiaofeng, Cai Chenyan, "A 65nm CMOS High-Speed Low-Power Continuous-Time Sigma-Delta Modulator For 3G WCDMA Receivers," *"Challenge Cup" National Intervarsity Science and Technology Competition, China*

Sep 2009 **Bronze Leaf Certificate, 2009 IEEE PrimeAsia Conference**

U-Fat Chio, Hou-Lon Choi, Chi-Hang Chan, Si-Seng Wong, Sai-Weng Sin, Seng-Pan U, R. P. Martins, "Comparator-Based Successive Folding ADC," *IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (PrimeAsia)*, pp. 117-120, Nov. 2009.

Sep 2009 **Champion** for the Final Year Project Supervised: Jiang Yang, Yu Xiaofeng, Cai Chenyan, "A 65nm CMOS High-Speed Low-Power Continuous-Time Sigma-Delta Modulator For 3G WCDMA Receivers," *2009 IEEE Project Competitions, Macau*

Sep 2008 **Champion** for the Final Year Project Supervised: Li Ding, Sio Chan, "A Pseudo-Differential Comparator-Based Pipelined ADC," *2008 IEEE Project Competitions, Macau*

Sep 2008 **1st Runner-Up** for the Final Year Project Supervised: *Lei Chon Hei*, "A Pseudo-Differential Comparator-Based Pipelined ADC," *2008 IEEE Project Competitions, Macau*

Jun 2008 **1st Runner-up – Undergraduate Section** for the Final Year Project Supervised: Li Ding, Sio Chan, "A Pseudo-Differential Comparator-Based Pipelined ADC with Common Mode Feedforward Technique," *IET Young Members Exhibition and Conference 2008*, **organized by Young members Section, IET(HK), Hong Kong, China**

Invited Talks

1. "Design Techniques for Nanometer Data Converters," University of Porto, Porto, Portugal, Jun. 2016.
2. "Energy Efficient SAR-Type ADCs, Part II – Practical Design Case Study," Tutorial Speaker, International Symposium on Integrated Circuits (ISIC), Singapore, Dec. 2014.
3. "Design Techniques for Nanometer Data Converters," Invited Speaker, CMOSET 2014 Dec. Grenoble, France, Jul 2014.

4. "Macao Chip by Macao People" - Sharing Session on the First State Scientific and Technological Progress Award for Macao **澳門人，澳門"芯" – 澳門首獲國家科學技術進步獎成果分享會,** Feb. 2012.
5. "Research and Future Perspective of Data Converters Research", **Academic Committee Meeting**, State-Key Laboratory of Analog and Mixed-Signal VLSI, Mar. 2012.
6. "Design Techniques for Nanometer Data Converters**," Institute of Superior Technico (IST)**, Lisboa, Portugal, Mar. 2012.
7. "Design Techniques for Nanometer Data Converters," **The New University of Lisbon, Lisboa, Portugal**, Mar. 2012.
8. "High-Speed, High-Resolution, Low-Power Analog-to-Digital Conversion System with Emerging Scaled CMOS Technology", **FDCT Project Presentation**, Macau Science and Technology Development Fund, Nov. 2011.
9. "Design Techniques for Nanometer Data Converters," **Hong Kong University of Science and Technology**, Hong Kong, Dec. 2010.
10. "Macau Microelectronics Development – Histories and Prospects" **University of Macau**, Macau, Oct. 2009 and Nov 2010.
11. "Introduction to the Research in Data Conversion and Signal Processing Research Line at University of Macau," **Tsinghua University**, Shenzhen, Nov 2009.
12. "Introduction to the Research in Data Conversion and Signal Processing Research Line at University of Macau," **Fudan University**, Shanghai, May 2009.

Scientific Publications

Book

1. Sai-Weng Sin, Seng-Pan U, and R.P.Martins, "Generalized Low-Voltage Circuit Techniques for Very High-Speed Time-Interleaved Analog-to-Digital Converters, *Analog Circuits and Signal Processing, Springer,* Oct. 2010.

   Printed version: (ISBN: 978-90-481-9709-5)

   e-Book: (ISBN: 978-90-481-9710-1)

   Link: http://www.springer.com/engineering/electronics/book/978-90-481-9709-5

Patents

1. Sai-Weng Sin, Li Ding, Yan Zhu, He-Gong Wei, Chi-Hang Chan, U-Fat Chio, Seng-Pan U, R.P.Martins, F.Maloberti, "Time-Interleaved Pipelined-SAR Analog to Digital Converter with Low Power Consumption," *US Patent,* No. 8,427,355, from 23rd Apr, 2013.

2. Sai-Weng Sin, Li Ding, Yan Zhu, He-Gong Wei, Chi-Hang Chan, U-Fat Chio, Seng-Pan U, R.P.Martins, F.Maloberti, "Analog to Digital Converter Circuit(類比至數位轉換器電路)," *Taiwan Patent, No. 201242261,* Mar 2014.

3. Yan Zhu, Chi-Hang Chan, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, R.P. Martins and Franco Maloberti, "N-Bits Successive Approximation Register Analog-to-Digital Converter Circuit," *US Patent* No: 8,344,931, from 1th Jan, 2013.

4. He-Gong Wei, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, R.P.Martins, "Delay Generator," *US patent, No. US8,411,259 B2,* May 2013.

5. U-Fat Chio, He-Gong Wei, Yan Zhu, Sai-Weng Sin, Seng-Pan U, R. P. Martins and Franco Maloberti, "Analog-to-Digital Converting System (類比數位轉換系統)," *Taiwan Patent Application No: 100103984,* 2011.

6. He-Gong Wei, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, R.P.Martins, "Delay Generator (延遲產生器)," *Taiwan Patent, No. 201246793,* Mar 2014.

7. U-Fat Chio, He-Gong Wei, Yan Zhu, Sai-Weng Sin, Seng-Pan U, R. P. Martins and Franco Maloberti, "Cascade Analog to Digital Converting System," *US Patent*, No. 8,466,823 B2, 2nd Aug, 2012.

8. Chi-Hang Chan, Yan Zhu, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, R. P. Martins " Comparator and Calibration Thereof," *US Patent*, No. 13/675311, Jul 2014.

Journal Papers

IEEE Journal of Solid-State Circuits (JSSC)

1. Chi-Hang Chan, Yan Zhu, Sai-Weng Sin, Seng-Pan U, Rui Paulo Martins, " A 6 b 5 GS/s 4 Interleaved 3 b/Cycle SAR ADC ", ***IEEE Journal of Solid-State Circuit***s. vol. 51, Issue 2, pp. 365-377, Feb 2016. [SCI, EI]

2. Chi-Hang Chan, Yan Zhu, Sai-Weng Sin, Seng-Pan U, Rui Paulo Martins, Franco Maloberti, "A 5-Bit 1.25-GS/s 4x-Capacitive-Folding Flash ADC in 65-nm CMOS", ***IEEE Journal of Solid-State Circuit***s. vol. 48, Issue 9, pp. 2154-2169, Sept 2013. [SCI, EI]
[Ranked 12th Top Aceess paper in IEEE Journal of Solid-State Circuits in Aug 2013 with it Early Access Version]

3. Si-Seng Wong, U-Fat Chio, Yan Zhu, Sai-Weng Sin, Seng-Pan U, Rui Paulo Martins, "A 2.3 mW 10-bit 170 MS/s Two-Step Binary-Search Assisted Time-Interleaved SAR ADC***",*** *in press in* ***IEEE Journal of Solid-State Circuits.*** vol. 48, Issue 8, pp. 1783-1794, Aug 2013. [SCI, EI]
[Ranked 3rd Top Aceess paper in IEEE Journal of Solid-State Circuits in Jul 2013 with it Early Access Version]

[Ranked 95th Top Aceess paper in the whole IEEE Xplore datebase in Jul 2013 with it Early Access Version]

4. He-Gong Wei, Chi-Hang Chan, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, Rui Paulo Martins, Franco Maloberti, "A 8-bit 400MS/s 2-bit per cycle SAR ADC with Resistive DAC", ***IEEE Journal of Solid-State Circuits***, vol. 47, Issue 11, pp. 2763-2772, Nov 2012. [SCI, EI] **[Ranked 78th Top Aceess paper in the whole IEEE Xplore datebase in Nov 2012]**

5. Yan Zhu, Chi-Hang Chan, Sai-Weng Sin, Seng-Pan U, R. P. Martins, Franco Maloberti, "A 50fJ 10b 160 MS/s Pipelined-SAR ADC with Decoupled Flip-Around MDAC and Self-Embedded Offset Cancellation**",** ***IEEE Journal of Solid-State Circuits***, vol. 47, Issue 11, pp. 2614 – 2626, Nov 2012. [SCI, EI] **[Ranked 43th Top Aceess paper in the whole IEEE Xplore datebase in Nov 2012]**

6. Yan Zhu, Chi-Hang Chan, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, R.P. Martins and Franco Maloberti, " A 10-bit 100-MS/s Reference-Free SAR ADC in 90nm CMOS," ***in IEEE Journal of Solid-State Circuits,*** vol. 45, no. 6, pp. 1111 – 1121, Jun 2010. [SCI, EI]

IEEE Transactions on Circuits and Systems I - Regular Papers (TCAS-I)

7. Liang Qi, Sai-Weng Sin, Seng-Pan U, Franco Maloberti, Rui Paulo Martins, "A 4.2mW 77.1dB-SNDR 5MHz-BW DT 2-1 MASH ΔΣ Modulator with Multirate Opamp Sharing ", in press in ***IEEE Transactions on Circuits and Systems I - Regular Papers***, 2017. [SCI, EI]

8. Jianyu Zhong, Yan Zhu, Chi-Hang Chan, Sai-Weng Sin, Seng-Pan U, and R.P.Martins, "A 12b 180MS/s 0.068mm2 with Full-Calibration-Integrated Pipelined-SAR ADC," in press in ***IEEE Transactions on Circuits and Systems I - Regular Papers,*** 2017. [SCI, EI]

9. Chi-Hang Chan, Yan Zhu, Sai-Weng Sin, Seng-Pan U, R.P.Martins, Franco Maloberti, "A 7.8-mW 5-b 5-GS/s Dual-Edges-Triggered Time-Based Flash ADC," in press in ***IEEE Transactions on Circuits and Systems I - Regular Papers,*** 2017. [SCI, EI]

10. Jianyu Zhong, Yan Zhu, Sai-Weng Sin, Seng-Pan U, and R.P.Martins, "Thermal and Reference Noise Analysis of Time-Interleaving SAR and Partial-Interleaving Pipelined-SAR ADCs," in ***IEEE Transactions on Circuits and Systems I - Regular Papers,*** vol. 62, no. 9, pp. 2196-2206, Sep 2015. [SCI, EI]

11. Sai-Weng Sin, Seng-Pan U, and R.P.Martins, "Generalized Circuit Techniques for Low-Voltage High-Speed Reset- and Switched-Opamps," in ***IEEE Transactions on Circuits and Systems I - Regular Papers,*** vol. 55, no. 8, pp. 2188-2201, Sep 2008. [SCI, EI]

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