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Date Submitted: 2017-10-31 23:09:15
Confirmation Number: 761384
Template: NSERC_Researcher

Dr. Seok-Bum Ko

Correspondence language: English
Sex: Male

Contact Information

The primary information is denoted by (*)

Address

Primary Affiliation (*)

57 Campus Drive
Saskatoon Saskatchewan S7N 5A9
Canada

Telephone

Work (*) 306-9665456

Email

Work (*) seokbum.ko@usask.ca

NSERC CRSNG

Canadian Common CV commun canadien

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Dr. Seok-Bum Ko

Language Skills

Language	Read	Write	Speak	Understand	Peer Review
English	Yes	Yes	Yes	Yes	Yes
French	No	No	No	No	No

Degrees

- 2002/8 — Doctorate, Electrical and Computer Engineering, University of Rhode Island
  Supervisors: Dr. Jien-Chung Lo, 1998/9 - 2002/8
- 1993/2 — Master's Thesis, Computer Engineering, Chonbuk National University
  Supervisors: Dr. Yong-Chon Kim, 1991/3 - 1993/2
- 1991/2 — Bachelor's, Computer Engineering, Chonbuk National University
  Supervisors: , 1987/3 - 1991/2

Recognitions

2017/9
STIC (Science, Technology, Innovation and Collaboration) Project Award Finalist
Saskatoon Regional Economic Development Authority
Prize / Award
This award recognizes an innovative product or service that has significantly impacted its sector. The results will be announced on Nov. 8, 2017. I've been nominated for my development of licence plate recognition technology.

2016/12
Intel Hardware Accelerator Research Program (HARP)
Intel
Prize / Award
An Intel Xeon+FPGA system (Broadwell + Arria10) will be made available to 30 research centers/universities worldwide including my research team via one of two centralized cluster installations in the US and in Germany.

2015/6 - 2016/7
Invited Professor
Hanyang University, Korea
Honor
From 2015 to 2016, I was invited to teach computer architecture course for undergrad/ graduate students and help faculties' research for three weeks every summer.

2012/6 - 2014/7
Invited Professor
Inner Mongolia Agricultural University, China
Honor
From 2012 to 2014, I was invited to teach computer architecture course for undergrad/ graduate students and help faculties' research for two weeks every summer.

2012/1	Nominee of SES Educator of the Year Award Saskatoon Engineering Society Prize / Award This award is given to recognize the outstanding work in engineering education and to encourage outstanding education by others.
2011/3	Best Paper Award IEEE Prize / Award IEEE International Workshop on Multimedia Signal Processing & Transmission

User Profile

Research Specialization Keywords: Application specific processor, Approximate computing, Computer arithmetic, Computer engineering, Embedded system

Employment

2015/6	Professor Computer Engineering, Hanyang University Part-time, Adjunct Tenure Status: Non Tenure Track
2014/7	Professor and Graduate Chair ECE, University of Saskatchewan Full-time, Professor Tenure Status: Tenure
2010/9	Professor Kinesiology, The University of Regina Part-time, Adjunct Tenure Status: Non Tenure Track
2017/1 - 2017/6	Visiting Professor ECE, Seoul National University Part-time, Visiting Professorship, Professor Tenure Status: Non Tenure Track
2008/7 - 2014/6	Associate Professor ECE, University of Saskatchewan Full-time, Associate Professor Tenure Status: Tenure
2002/9 - 2008/6	Assistant Professor ECE, University of Saskatchewan Full-time, Assistant Professor Tenure Status: Tenure Track
1993/3 - 1998/8	Researcher R&D, Korea Telecom Research and Development Center

Research Funding History

Awarded [n=5]

2017/4 - 2021/12 Co-investigator	Developing Processor-Memory-Storage Integrated Architecture for Low Power, High Performance Big Data Servers, Grant

Funding Sources:
Ministry of Trade, Industry and Energy, Korea
Total Funding - 4,700,000
Portion of Funding Received - 233,000
Funding Competitive?: Yes

2017/10 - 2018/4
Principal Applicant

Pre-study funding @ Aimday Imaging 2017, Grant

Funding Sources:
Innovation Saskatchewan/Canadian Light Source
Total Funding - 1,000
Portion of Funding Received - 1,000
Funding Competitive?: Yes

2012/4 - 2018/3
Principal Investigator

A Study on Decimal Floating-point Arithmetic Unit through Fused Multiply-Add Architecture, Grant

Funding Sources:
Natural Sciences and Engineering Research Council of Canada (NSERC)
DG
Total Funding - 90,000
Portion of Funding Received - 90,000
Funding Competitive?: Yes

2015/1 - 2017/12
Co-investigator

Development of an automated fungal detection system using MEMS-based spore sensor, Grant

Funding Sources:
Agriculture Development Fund
Total Funding - 200,000
Portion of Funding Received - 40,000
Funding Competitive?: Yes

2017/3 - 2017/11
Principal Investigator

Next generation residential kitchen fire prevention system, Grant

Funding Sources:
Natural Sciences and Engineering Research Council of Canada (NSERC)
EG
Total Funding - 25,000
Portion of Funding Received - 25,000
Funding Competitive?: Yes

Completed [n=11]

2010/1 - 2015/1
Co-investigator

Embedded Systems Canada (emSYSCAN), Grant

Funding Sources:
Canadian Microelectronics Corporation
Total Funding - 48,000,000
Portion of Funding Received - 192,000
Funding Competitive?: Yes

2012/1 - 2014/1
Co-investigator

Biological Sensor Technology for Safety and Security, Grant

Funding Sources:
Natural Sciences and Engineering Research Council of Canada (NSERC)
CRD
Total Funding - 174,000
Portion of Funding Received - 58,000
Funding Competitive?: Yes

2013/4 - 2013/9
Co-applicant

Novel Scalable Methodology for Designing Network on Chip, Scholarship

Funding Sources:
Canadian Commonwealth Exchange Program
Total Funding - 10,000
Portion of Funding Received - 0
Funding Competitive?: Yes

2010/9 - 2013/8
Co-applicant

Hardware implementations of scalable and unified ECC, Scholarship

Funding Sources:
Natural Sciences and Engineering Research Council of Canada (NSERC)
CGS D
Total Funding - 105,000
Portion of Funding Received - 0
Funding Competitive?: Yes

2012/9 - 2013/2
Co-applicant

Bandwidth-Aware Routing and Admission Control for Reliable Video Streaming over MANETs, Scholarship

Funding Sources:
Canadian Commonwealth Exchange Program
Total Funding - 10,000
Portion of Funding Received - 0
Funding Competitive?: Yes

2012/1 - 2012/9
Principal Investigator

FPGA-based Image Processing System using Network on Chip, Grant

Funding Sources:
Natural Sciences and Engineering Research Council of Canada (NSERC)
EG
Total Funding - 25,000
Portion of Funding Received - 25,000
Funding Competitive?: Yes

2007/3 - 2012/4
Principal Investigator

Efficient Implementation of Decimal Floating Point Arithmetic Unit, Grant

Funding Sources:
Natural Sciences and Engineering Research Council of Canada (NSERC)
DG
Total Funding - 75,000
Portion of Funding Received - 75,000
Funding Competitive?: Yes

2011/1 - 2011/9
Principal Investigator

Study of Low Power IEEE754 Compliant Arithmetic Adder for Scientific Applications, Grant

Funding Sources:
Natural Sciences and Engineering Research Council of Canada (NSERC)
EG
Total Funding - 25,000
Portion of Funding Received - 25,000
Funding Competitive?: Yes

2008/10 - 2011/9
Co-investigator

Near-Falls and Falls Detection System, Grant

Funding Sources:
Natural Sciences and Engineering Research Council of Canada (NSERC)
SPG
Total Funding - 416,294
Portion of Funding Received - 52,036
Funding Competitive?: Yes

2010/9 - 2011/2
Co-applicant

Efficient Design of Network on Chip, Scholarship

Funding Sources:
Canadian Commonwealth Exchange Program
Total Funding - 10,000
Portion of Funding Received - 0
Funding Competitive?: Yes

2010/3 - 2011/2
Co-investigator

Validity, Feasibility and Utility Testing of a Near-Falls and Falls Detection System (NF-FDS) Device for Older Adults, Grant

Funding Sources:
Royal University Hospital Foundation (Saskatoon, SK)
Total Funding - 25,000
Portion of Funding Received - 6,250
Funding Competitive?: Yes

Student/Postdoctoral Supervision

Bachelor's [n=9]

2017/5 - 2017/8
Principal Supervisor

T. Yan (Completed) , Chinese University of Hong Kong
Thesis/Project Title: Deep learning
Present Position: BSc student

2017/5 - 2017/8
Principal Supervisor

Z. Xiao (Completed) , Chinese University of Hong Kong
Thesis/Project Title: Deep learning
Present Position: BSc student

2017/5 - 2017/8
Principal Supervisor

W. Huang (Completed) , Chinese University of Hong Kong
Thesis/Project Title: Deep learning
Present Position: BSc student

2015/5 - 2015/8
Principal Supervisor

X. Liu (Completed) , City University of Hong Kong
Thesis/Project Title: Eye blood vessel extraction
Present Position: BSc student

2013/5 - 2013/8
Principal Supervisor

T. Zhang (Completed) , City University of Hong Kong
Thesis/Project Title: Graphics processing unit study
Present Position: n/a

2012/5 - 2012/8
Principal Supervisor

Y. Li (Completed) , City University of Hong Kong
Thesis/Project Title: Flower identification apps
Present Position: n/a

2011/5 - 2011/8
Principal Supervisor

Y. Wang (Completed) , City University of Hong Kong
Thesis/Project Title: Software verificationprogram for decimal floating point arithmetic
Present Position: n/a

2010/9 - 2011/8
Principal Supervisor

G. Dong (Completed) , University of Saskatchewan
Thesis/Project Title: Internal medicine resident's app for iPAD
Present Position: n/a

2010/9 - 2011/8
Principal Supervisor

P. Piao (Completed) , University of Saskatchewan
Thesis/Project Title: Internal medicine resident's app for iPAD
Present Position: architect, Cognitive Systems Corp

Master's non-Thesis [n=1]

2012/9 - 2014/8	S. Sami (Completed) , University of Saskatchewan
Principal Supervisor	Thesis/Project Title: Oil and gas leak detection
	Present Position: Engineering designer, Telecon Design

Master's Thesis [n=13]

2016/7 - 2018/6	Y. Wang (In Progress) , University of Saskatchewan
Principal Supervisor	Student Degree Expected Date: 2018/6
	Thesis/Project Title: TBA
	Present Position: MSc student
2016/6 - 2016/8	K. Ma, City University of Hong Kong
Principal Supervisor	Thesis/Project Title: Pattern Recognition
	Present Position: n/a
2015/9 - 2017/8	Z. Jiang (Completed) , University of Saskatchewan
Co-Supervisor	Thesis/Project Title: Retinal blood vessel segmentation: methods and implementations
	Present Position: Programmer, Axon Development Co
2015/9 - 2017/8	J. Yepez (Completed) , University of Saskatchewan
Principal Supervisor	Thesis/Project Title: Improved License Pate Localization Algorithm Based on Morphological Operations
	Present Position: PhD student, Univ. of Saskatchewan
2014/5 - 2014/8	H. Lui, City University of Hong Kong
Principal Supervisor	Thesis/Project Title: ECC implementation
	Present Position: n/a
2014/5 - 2015/12	H. Zhang (Completed) , University of Saskatchewan
Principal Supervisor	Thesis/Project Title: Single-Precision and Double-Precision Merged Floating-Point Multiplication and Addition Units on FPGA
	Present Position: PhD student, Univ. of Saskatchewan
2014/5 - 2014/8	V. Zhang, City University of Hong Kong
Principal Supervisor	Thesis/Project Title: network security
	Present Position: n/a
2013/9 - 2015/8	S. An (Completed) , University of Saskatchewan
Principal Supervisor	Thesis/Project Title: A Highly Accurate and Robust Retinal Vessel Segmentation Algorithm
	Present Position: Ecmictics Biotech Inc, Firmware engineer
2013/5 - 2013/8	H. Zhang, City University of Hong Kong
Principal Supervisor	Thesis/Project Title: GPU implementation
	Present Position: PhD student, Univ. of Saskatchewan
2012/5 - 2012/8	J. Chu, City University of Hong Kong
Principal Supervisor	Thesis/Project Title: Smartphone app development
	Present Position: n/a
2010/9 - 2012/8	Z. Wang (Completed) , University of Saskatchewan
Principal Supervisor	Thesis/Project Title: Design and Implementation of a Radix-100 Division Unit
	Present Position: Intermediate verification engineer, Huawei Canada
2010/9 - 2012/8	X. Jin (Completed) , University of Saskatchewan
Co-Supervisor	Thesis/Project Title: Improving GPU SIMD Control Flow Efficiency via Hybrid Warp Size Mechanism
	Present Position: PhD student, University of Saskatchewan

2010/9 - 2012/8 Co-Supervisor	A. Mostafa (Completed) , University of Saskatchewan Thesis/Project Title: Design and implementation of an efficient image compressor for wireless capsule endoscopy Present Position: PhD student, Univ. of Connecticut

Doctorate [n=11]

2017/10 - 2017/11 Principal Supervisor	MD BELAYET ALI (In Progress) , Iwate University, Japan Thesis/Project Title: Approximate computing Present Position: Visiting PhD student
2017/9 - 2020/8 Principal Supervisor	J. Yepez (In Progress) , University of Saskatchewan Thesis/Project Title: Deep learning based pattern recognition Present Position: PhD student, Univ. of Saskatchewan
2016/1 - 2019/8 Principal Supervisor	H. Zhang (In Progress) , University of Saskatchewan Student Degree Expected Date: 2019/8 Thesis/Project Title: Computer Arithmetic Present Position: PhD student, Univ. of Saskatchewan
2015/5 - 2019/4 Principal Supervisor	S. Venkatachalam (In Progress) , University of Saskatchewan Student Degree Expected Date: 2019/4 Thesis/Project Title: Approximate computing Present Position: PhD student, Univ. of Saskatchewan
2013/4 - 2013/9 Principal Supervisor	M. Bohra, Malaviya National Institute of Technology, Jaipur Thesis/Project Title: Network on Chip Present Position: Associate Professor, JIET Jodhpur, India
2012/9 - 2013/2 Principal Supervisor	C. Doot, Malaviya National Institute of Technology, Jaipur Thesis/Project Title: Computer Network Present Position: Research Associate, University of Padua, Italy
2011/9 - 2015/8 Principal Supervisor	A. Kaivani (Completed) , University of Saskatchewan Thesis/Project Title: High-Speed Co-processors Based on Redundant Number Systems Present Position: Senior product development engineer, Microsemi
2010/9 - 2011/2 Principal Supervisor	S. Kathirvel, National Institute of Technology, Tiruchirappalli Thesis/Project Title: Network on Chip Present Position: Associate Professor, VIT University, India
2010/9 - 2015/1 Principal Supervisor	C. Loi (Completed) , University of Saskatchewan Thesis/Project Title: Hardware Implementations of Scalable and Unified Elliptic Curve Cryptosystem Present Position: digital designer, SED systems
2009/9 - 2013/8 Principal Supervisor	L. Han (Completed) , University of Saskatchewan Thesis/Project Title: Decimal Floating-point Fused Multiply Add with Redundant Number Systems Present Position: Senior ASIC engineer, Marvell Semiconductor
2006/9 - 2011/1 Principal Supervisor	D. Chen (Completed) , University of Saskatchewan Thesis/Project Title: Algorithms and Architectures for Decimal Transcendental Function Computation Present Position: Senior member of technical staff, Altera, part of Intel

Research Associate [n=1]

2009/9 - 2011/8	Y. Choi, University of Saskatchewan
Co-Supervisor	Thesis/Project Title: Biomedical engineering (Cardiovascular study)
	Present Position: n/a

Organizational Review Activities

2011/10 - 2011/10	Member, University of Toronto NSERC site visit to Univ. of Toronto for evaluation of proposed NSERC/Altera Industrial Research Chair

Committee Memberships

2015/1	Committee Member, Graduate chairs and research committee, University of Saskatchewan research and outreach activities
2013/1	Committee Member, College of Reviewer, MITACS
2013/1	Committee Member, Program Committee, ICECCS
2013/1	Committee Member, Program Committee, VDAT
2012/6	Committee Member, VLSI Systems and its Application (VSA), IEEE Technical committee of Circuit and System Society, IEEE
2012/1	Chair, Development system coordinator, CFI emSYSCAN, CMC University of Saskatchewan representative of CFI emSYSCAN project
2017/10 - 2020/8	Committee Member, University Council, University of Saskatchewan
2013/1 - 2014/12	Chair, computer engineering program, University of Saskatchewan Accreditation committee, Canadian Engineering Accreditation Board
2013/1 - 2013/7	Committee Member, Program Committee, CCECE2013

Other Memberships

2011/1	Chair, Association of Korean Canadian Scientists and Engineers Lead National Math/Science Competition for Grades 4-11
2007/1	Board member, Association of Korean Canadian Scientists and Engineers
2005/1	Professional Engineer, APEGS
2004/1	Senior member, IEEE
2012/1 - 2014/12	President, Saskatoon Korean Association

Presentations

1. A. Kaivani*. (2016). Floating-Point Butterfly Architecture Based on Binary Signed-Digit Representation.
   International symposiums on circuits and systems, Montreal, Canada
   Invited?: Yes, Keynote?: No

2. C. Loi*. (2016). Scalable Elliptic Curve Cryptosystem FPGA Processor for NIST Prime Curves. International symposium on circuits and systems, Montreal, Canada
Invited?: Yes, Keynote?: No

3. (2015). Current trends in computer engineering. Distinguished guest lecture series, Seoul, Korea, Republic of
Invited?: Yes, Keynote?: No

4. (2014). What is SCG?. Distinguished guest lecturer series, Daejon, Korea, Republic of
Invited?: Yes, Keynote?: No

5. C. Loi*. (2014). FPGA Implementation of Low Latency Scalable Elliptic Curve Cryptosystem Processor in GF(2^m). IEEE Int'l Symp. on Circuits and Systems, Melbourne, Australia
Invited?: No, Keynote?: No

6. A. Kaivani*. (2014). High-Speed FFT Processors Based on Redundant Number Systems. IEEE Int'l Symp. on Circuits and Systems, Melbourne, Australia
Invited?: No, Keynote?: No

7. A. Kaivani*. (2013). Decimal Signed Digit Addition Using Stored Transfer Encoding. IEEE Canadian Conference on Electrical and Computer Engineering,, Regina, Canada
Invited?: No, Keynote?: No

8. C. Loi*. (2013). High Performance Scalable Elliptic Curve Cryptosystem Processor in GF(2^m). IEEE Int'l Symp. on Circuits and Systems, Beijing, China
Invited?: No, Keynote?: No

9. C. Vennila*, Suresh. K, R. Rathor, G. Lakshminarayanan. (2013). Dynamic Partial Reconfigurable Adaptive Transceiver for OFDM based Cognitive Radio. IEEE Canadian Conference on Electrical and Computer Engineering, Regina, Canada
Invited?: No, Keynote?: No

10. K. Swaminathan*, G. Lakshminarayanan, F. Lang, M. Fahmi. (2013). Design of a Low Power Network Interface for Network on Chip. IEEE Canadian Conference on Electrical and Computer Engineering, Regina, Canada
Invited?: No, Keynote?: No

11. (2012). Efficient hardware implementation of compute-intensive applications. Samsung distinguished guest lecturer series, Seoul, Korea, Republic of
Invited?: Yes, Keynote?: No

12. Z. Wang*, L. Han*. (2012). Design and Implementation of a Radix-100 Division Unit. IEEE Int'l Symp. on Circuits and Systems, Seoul, Korea, Republic of
Invited?: No, Keynote?: No

13. A. Kaivani*, L. Chen. (2012). High-Frequency Sequential Decimal Multipliers. IEEE Int'l Symp. on Circuits and Systems, Seoul, Korea, Republic of
Invited?: No, Keynote?: No

14. C. Vennila*, K. Palaniappan, K. Krishna, G.Lakshminarayanan. (2012). Dynamic partial reconfigurable FFT/IFFT pruning for OFDM based Cognitive radio. IEEE Int'l Symp. on Circuits and Systems, Seoul, Korea, Republic of
Invited?: No, Keynote?: No

15. A. Mostafa*, K. Wahid. (2012). A Low-Power Subsample-Based Image Compression Algorithm for Capsule Endoscopy. IEEE Int'l Symp. on Circuits and Systems, Seoul, Korea, Republic of
Invited?: No, Keynote?: No

16. V. Arasu*, G. Lakshminarayanan. (2011). High Speed Reconfigurable Viterbi Decoder for Wireless Standards. Int'l Workshop on Multimedia Signal Processing & Transmission, Jeonju, Korea, Republic of
Invited?: No, Keynote?: No

17. A. Dinh, Y. Choi*. (2011). A heart rate sensor based on seismocardiography for vital sign monitoring systems. IEEE Canadian Conference on Electrical and Computer Engineering, Niagara Falls, Canada
Invited?: No, Keynote?: No

18. A. Mostafa*, K. Wahid. (2011). An efficient YUV-based image compression algorithm for wireless capsule endoscopy. IEEE Canadian Conference on Electrical and Computer Engineering, Niagara Falls, Canada
Invited?: No, Keynote?: No

Broadcast Interviews

2017/07/10 - 2017/07/10	Impacts of our developed car license plate recognition program, CBC morning, CBC Saskatoon

Text Interviews

2017/06/28	Young Innovators: Student improves licence plate recognition technology, Saskatoon Starphoenix

Publications

Journal Articles

1. R. Marshal, G. Lakshminarayanan and S. Ko. (2017). Novel QCA Blocks for Digital Signal Processing and Storage. IEEE Transactions on VLSI.
Submitted
Refereed?: Yes

2. B. Suganthi, C. Vennila* and S. Ko. (2017). A Novel Link Reliable Routing Protocol for Video Content Delivery over Internet. Int'l Journal of Electronics and Communications.
Submitted
Refereed?: Yes

3. Z. Jiang*, H. Zhang*, Y. Wang* and S. Ko. (2017). Retinal blood vessel segmentation using fully convolutional network with transfer learning. Elsevier Computerized Medical Imaging and Graphics.
Submitted
Refereed?: Yes

4. R. Marshal, G. Lakshminarayanan and S. Ko. (2017). A Novel NAND/NOR Gate for QCA Circuit Design. IEEE Transactions on CAS II.
Submitted
Refereed?: Yes

5. H. Zhang*, D. Chen* and S. Ko. (2017). High Performance and Energy Efficient Floating-point Multiplier on FPGA. IET Circuits, Devices & Systems.
Submitted
Refereed?: Yes

6. S. Venkatachalam* and S. Ko. (2017). Design of Power and Area Efficient Approximate Multipliers. IEEE Transactions on VLSI. 25(5): 1782-1786.
Published
Refereed?: Yes

7. S. Venkatachalam* and S. Ko. (2017). Approximate sum of products designs based on distributed arithmetic. IEEE Transactions on VLSI.
Revision Requested
Refereed?: Yes

8. H. Zhang*, D. Chen* and S. Ko. (2017). Area and power efficient iterative single-precision and double-precision merged floating-point multiplier on FPGA. IET Computers and Digital Techniques.
Accepted
Refereed?: Yes

9. H. Zhang*, D. Chen* and S. Ko. (2017). Energy efficient multiple-precision Fused multiply-add with low-precision accumulation for deep learning applications. IEEE Transactions on Computers.
Submitted
Refereed?: Yes

10. H. Zhang*, D. Chen* and S. Ko. (2017). High performance and energy efficient single/double-precision merged floating-point adder on FPGA. IET Computers and Digital Techniques.
Accepted
Refereed?: Yes

11. Z. Jiang*, J. Yepz*, S. An* and S. Ko. (2017). Fast, accurate and robust retinal vessel segmentation system. Elsevier Biocybernetics and Biomedical Engineering. 37(3): 412-421.
Published
Refereed?: Yes

12. J. Yepez* and S. Ko. (2017). Improved License Plate Localization Algorithm Based on Morphological Operations. IET Intelligent Transport Systems.
Submitted
Refereed?: Yes

13. A. Kaivani* and S. Ko. (2016). Floating-Point Butterfly Architecture Based on Binary Signed-Digit Representation. IEEE Transactions on Very Large Scale Integration Systems. 24(3): 1208-1211.
Published
Refereed?: Yes

14. C. Loi* and S. Ko. (2016). Parallelization of Scalable Elliptic Curve Cryptosystem Processors in GF(2^m). Elsevier Journal of Microprocessors and Microsystems. 45(Part A): 10-22.
Published
Refereed?: Yes

15. L. Han*, H. Zhang* and S. Ko. (2016). Decimal Floating-Point Fused Multiply-Add with Redundant Internal Encodings. IET Computers & Digital Techniques. 10(4): 147-156.
Published
Refereed?: Yes

16. S. Kathirvel*, R. Jangre and S. Ko. (2016). Design of a novel energy efficient topology for maximum magnitude generator. IET Computers and Digital Techniques. 10(3): 93-101.
Published
Refereed?: Yes

17. A. Kaivani* and S. Ko. (2015). Area efficient floating-point FFT butterfly architectures based on multi-operand adders. IET Electronics Letters. 51(12): 895-897.
Published
Refereed?: Yes

18. C. Lal*, V. Laxmi, M. Gaur, and S. Ko. (2015). Bandwidth-aware routing and admission control for efficient video streaming over MANETs. Springer Wireless Networks. 21(1): 95-114.
Published
Refereed?: Yes

19. L. Han*, H. Zhang* and S. Ko. (2015). Area and Power Efficient Decimal Carry Free Adder. IET Electronics Letters. 51(23): 1852-1854.
Published
Refereed?: Yes

20. M. Kumar*, M. S. Gaur, V. Laxmi, M. Daneshtalab, M. Zwolinski and S. Ko. (2015). A Novel Highly Adaptive Routing for Networks-on-Chip. IET Electronics Letters. 51(25): 2092-2094.
Published
Refereed?: Yes

21. C.Loi* and S. Ko. (2015). Scalable Elliptic Curve Cryptosystem FPGA Processor for NIST Prime Curves. IEEE Transactions on Very Large Scale Integration Systems. 23(11): 2753-2756.
Published
Refereed?: Yes

22. K. Swaminathan*, G. Lakshminarayanan, and S. Ko. (2014). Design and Verification of an Efficient WISHBONE-based Network Interface for Network on Chip. Elsevier International Journal on Computers and Electrical Engineering. 40(6): 1838-1857.
Published
Refereed?: Yes

23. X. Jin*, B. Daku, and S. Ko. (2014). Improved GPU SIMD Control Flow Efficiency via Hybrid Warp Size Mechanism. Elsevier Journal of Microprocessors and Microsystems. 38(7): 717-729.
Published
Refereed?: Yes

24. A. Kaivani* and S. Ko. (2014). Improved Design of High-Frequency Sequential Decimal Multipliers. IET Electronics Letters. 50(7): 558-560.
Published
Refereed?: Yes

25. A. Kaivani* and S. Ko. (2013). Decimal SRT Square Root: Algorithm and Architecture. Springer Circuits, Systems & Signal Processing (CSSP). 32(5): 2137-2150.
Published
Refereed?: Yes

26. Y. Choi*, Q. Zhang*, and S. Ko. (2013). Noninvasive cuffless blood pressure estimation using pulse transit time and Hilbert-Huang transform. Elsevier International Journal on Computers and Electrical Engineering. 39(1): 103-111.
Published
Refereed?: Yes

27. K. Swaminathan*, G. Lakshminarayanan, and S. Ko. (2013). High Speed Generic Network Interface for Network on Chip using Ping Pong Buffers. Journal of Low Power Electronics. 9(3): 322-331.
Published
Refereed?: Yes

28. C. Loi* and S. Ko. (2013). High Performance Scalable Elliptic Curve Cryptosystem Processor for Koblitz Curves. Elsevier Journal of Microprocessors and Microsystems. 37(4-5): 394-406.
Published
Refereed?: Yes

29. L. Han*, A. Kaivani*, and S. Ko. (2013). Area Efficient Sequential Decimal Fixed-point Multiplier. Springer Journal of Signal Processing Systems. 75(1): 39-46.
Published
Refereed?: Yes

30. C. Vennila*, A. Patel, G. Lakshminarayanan and S. Ko. (2013). Dynamic Partial Reconfigurable Viterbi Decoder for Wireless Standards. Elsevier International Journal on Computers and Electrical Engineering. 39(2): 164-174.
Published
Refereed?: Yes

31. L. Han* and S. Ko. (2013). High Speed Parallel Decimal Multiplication with Redundant Internal Encodings. IEEE Transactions on Computers. 62(5): 956-968.
Published
Refereed?: Yes

32. A. Kaivani* and S. Ko. (2013). Decimal Division Algorithms: The Issue of Partial Remainders. Springer Journal of Signal Processing Systems. 73(2): 181-188.
Published
Refereed?: Yes

33. D. Chen*, L. Han*, and S. Ko. (2012). Decimal floating-point antilogarithmic converter based on selection by rounding: algorithm and architecture. IET Computers & Digital Techniques. 6(5): 277-289.
Published
Refereed?: Yes

34. D. Chen* and S. Ko. (2012). A Dynamic Non-Uniform Segmentation Method for First-Order Polynomial Function Evaluation. Elsevier Journal of Microprocessors and Microsystems. 36(4): 324-332.
Published
Refereed?: Yes

35. D. Chen* and S. Ko. (2012). A Novel Decimal Logarithmic Converter based on First-Order Polynomial Approximation. Springer Circuits, Systems & Signal Processing. 31(3): 1179-1190.
Published
Refereed?: Yes

36. D. Chen*, L. Han*, Y. Choi* and S. Ko. (2012). Improved Design of Decimal Floating-Point Logarithmic Converter with Selection by Rounding. IEEE Transactions on Computers. 61(5): 607-621.
Published
Refereed?: Yes

37. V. Arasu*, G. Lakshminarayanan, and S. Ko. (2012). Dynamic Partial Reconfigurable FFT for OFDM based Communication Systems. Springer Circuits, Systems & Signal Processing. 31(3): 1049-1066.
Published
Refereed?: Yes

38. C. Loi* and S. Ko. (2011). Improvements on the Design and Implementation of DVB-S2 LDPC Decoders. Elsevier International Journal on Computers and Electrical Engineering. 37(6): 1137-1146.
Published
Refereed?: Yes

Conference Publications

1. H. Zhang*, H. Lee and S. Ko. (2018). Efficient Fixed/Floating-Point Merged Multiply-Accumulate Unit for Deep Learning Processors. International Symposium on Circuits And Systems (ISCAS),
Paper
Submitted
Refereed?: Yes, Invited?: No

2. P. Perez, J. T-Tello, J. Yepez* and S. Ko. (2018). Digital Image Processing from Two Simultaneous Sources on a Raspberry Pi Board for the Navigation of a Robot. International Symposium on Circuits And Systems (ISCAS),
Paper
Submitted
Refereed?: Yes, Invited?: No

3. A. Dinh, Y. Choi*, P. Neary, D. Mac Quarie, and S. Ko. (2018). Motion Artifact Noise Mitigation Techniques inSeismocardiography. International Symposium on Circuits And Systems (ISCAS),
   Paper
   Submitted
   Refereed?: Yes, Invited?: No
4. J. Yepez* and S. Ko. (2018). AnFPGA-based Closed-loop Approach of Angular Displacement for a Resolver-to-Digital-Converter. International Symposium on Circuits And Systems (ISCAS),
   Paper
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5. S. Venkatachalam*, H. Lee and S. Ko. (2018). Power Efficient Approximate Booth Multiplier. International Symposium on Circuits And Systems (ISCAS),
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6. X. Shi, J. Dai, X. Luo, J. Yepez* and S. Ko. (2016). Foreground-Background Separation Guided by Statistical Features of Surveillance Video. IEEE International Conference on Consumer Electronics Asia,
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7. C. Loi*and S. Ko. (2016). Scalable Elliptic Curve Cryptosystem FPGA Processor for NIST Prime Curves. International symposium on circuits and systems, Montreal, Canada
   Conference Date: 2016/5
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8. A. Kaivani* and S. Ko. (2016). Floating-Point Butterfly Architecture Based on Binary Signed-Digit Representation. International symposiums on circuits and systems, Montreal, Canada
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9. M. Kumar*, V. Laxmi, M. Gaur, M. Daneshtalab, P. Srivastava, S. Ko, M. Zwolinski. (2014). A novel non-minimal/minimal turn model for highly adaptive routing in 2D NoCs. IEEE/ACM Int'l Symp. on Networks-on-Chip, (184-185)
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10. C. Loi* and S. Ko. (2014). FPGA Implementation of Low Latency Scalable Elliptic Curve Cryptosystem Processor in GF(2^m). IEEE Int'l Symp. on Circuits and Systems, Melbourne, Australia (822-825)
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12. S. Nambiar*, S. Kathirvel, G.Narayanan, and S. Ko. (2014). QaMC - QoS Aware Multicast Router for NoC Fabric. CCECE, Toronto, Canada
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14. S. Kathirvel*, R. Jangre, S. Nambiar, G. Narayanan, and S. Ko. (2014). A Novel Hybrid Topology for NoC. CCECE, Toronto, Canada
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15. K. Swaminathan*, D. Thakyal, S. Nambiar, G. Lakshminarayanan, and S. Ko. (2014). Enhanced Noxim Simulator for performance evaluation of NoC Topologies. Recent Advances in Engineering and Computational Sciences, India
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19. A. Kaivani* and S. Ko. (2013). Decimal Signed Digit Addition Using Stored Transfer Encoding. IEEE Canadian Conference on Electrical and Computer Engineering, Regina, Canada
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22. K. Swaminathan*, G. Lakshminarayanan, F. Lang, M. Fahmi and S. Ko. (2013). Design of a Low Power Network Interface for Network on Chip. IEEE Canadian Conference on Electrical and Computer Engineering, Regina, Canada
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Conference Date: 2012/12
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25. X. Jin* and S. Ko. (2012). GPU-based Parallel Implementation of SAR Imaging. International Symposium on Electronic System Design, Kolkata, India (125-129)
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35. Z. Wang* and S. Ko. (2011). Improved Design of a Radix-100 Decimal Division. International Workshop on Multimedia Signal Processing & Transmission, Seoul, Korea, Republic of (130-133)
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37. L. Han*, D. Chen*, K. Wahid, and S. Ko. (2011). Nonspeculative Decimal Signed Digit Adder. IEEE Int'l Symp. on Circuits and Systems, Rio de Janeiro, Brazil (1053-1056)
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39. A. Dinh, Y. Choi*, and S. Ko. (2011). A Heart Rate Sensor based on Seismocardiography for Vital Sign Monitoring Systems. IEEE Canadian Conference on Electrical and Computer Engineering, Niagara Falls, Canada (665-668)
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40. A. Ralhan* and S. Ko. (2011). A Study on Machine Learning Algorithms for Fall Detection and Movement Classification. International Conference on Information Science and Applications, Jeju, Korea, Republic of (1-8)
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41. V. Arasu*, G. Lakshminarayanan, S. Ko. (2011). High Speed Reconfigurable Viterbi Decoder for Wireless Standards. Int'l Workshop on Multimedia Signal Processing & Transmission, Jeonju, Korea, Republic of (114-119)
Conference Date: 2011/3
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Intellectual Property

Patents

1. Decimal floating-point fused multiply-add architecture. United States. 2015/05/15.
Patent Status: Pending
Inventors: S. Ko and L. Han

2. 32-bit Decimal Floating-Point Logarithmic Converter. United States. 2015/04/16.
Patent Status: Pending
Inventors: S. Ko, D. Chen, Y. Zhang and Y. Choi

3. 32-bit Decimal Floating-Point Antilogarithmic Converter. United States. 2015/04/16.
Patent Status: Pending
Inventors: S. Ko, D. Chen, Y. Choi and Y. Zhang

4. Multiplexer and Demultiplexer for ATM Transfer Mode Cell in Multimedia Service Processing. Korea, Republic of. 0257557.
Patent Status: Granted/Issued
Year Issued: 2000
Inventors: S. Ko, J. Park, and J. Kwon

5. AAL1 Receiving Apparatus for CBR. Korea, Republic of. 0271521.
Patent Status: Granted/Issued
Year Issued: 2000
Inventors: S. Ko, J. Park, and H. Chong,

6. Fitting Device in ATM System. Korea, Republic of. 0257556.
Patent Status: Granted/Issued
Year Issued: 2000
Inventors: S. Ko, J. Park, and J. Kwon

7. AAL1 Transmitting Apparatus for CBR. Korea, Republic of. 0271522.
   Patent Status: Granted/Issued
   Year Issued: 2000
   Inventors: S. Ko, J. Park, and H. Chong

Licenses

1. AAL1 Receiver with SRTS Mode
   Granted
   Date Issued: 1997/1
   S. Ko, J. Kwon and H. Chong, SWReg. No. 97-01-26-0431, Korea, 1997. Language: VHDL. (The registered software shall be protected for 50 years. Its right includes official announcement, declaration of author name and intellectual property.)
2. ATM Cell Multiplexer and Demultiplexer for 155 Mbps ATM Adapter Card
   Granted
   Date Issued: 1997/1
   S. Ko, J. Park, J. Kwon and H. Chong, SWReg. No. 97-01-24-4737, Korea. Language:VHDL. (The registered software shall be protected for 50 years. Its right includes official announcement, declaration of author name and intellectual property.)
3. RAM Board Logic Software for Storing Multimedia Data
   Granted
   Date Issued: 1997/1
   S. Ko, J. Park and H. Chong, SWReg. No. 96-01-26-7599, Korea. Language: VHDL. (The registered software shall be protected for 50 years. Its right includes official announcement, declaration of author name and intellectual property.)
4. ATM Cell Multiplexer and Demultiplexer for 25.6 Mbps ATM Adapter Card
   Granted
   Date Issued: 1997/1
   S. Ko, J. Park, J. Kwon and H. Chong, SWReg. No. 97-01-24-4736, Korea. Language: VHDL. (The registered software shall be protected for50 years. Its right includes official announcement, declaration of author nameand intellectual property.)
5. AAL1 Transmitter with SRTS Mode
   Granted
   Date Issued: 1997/1
   S. Ko, J. Kwon and H. Chong, SWReg. No. 97-01-26-0430, Korea. Language:VHDL. (The registered software shall be protected for 50 years. Its right includes official announcement, declaration of author name and intellectual property.)