

	1.	Comprehensive Device Reliability and Oxide Traps Distribution Analysis by the Low Frequency Noise in Ultra-Thin Body SOI (UTBSOI) MOSFETS By: Lin, Cheng-Li; Soh, Chun-Hung; Yeh, Wen-Kuan; et al. Conference: IEEE 8th Nanotechnology Materials and Devices Conference (NMDC) Location: Natl Cheng Kung Univ, Tainan, TAIWAN Date: OCT 06-09, 2013 Sponsor(s): IEEE; IEEE NANO 2013 IEEE 8TH NANOTECHNOLOGY MATERIALS AND DEVICES CONFERENCE (NMDC) Book Series: IEEE Nanotechnology Materials and Devices Conference Pages: 1-4 Published: 2013							
	2.	Substrate noise-coupling characterization and efficient suppression in CMOS technology By: Yeh, WK; Chen, SM; Fang, YK	1	1	2	3	0	25	1.67
		IEEE TRANSACTIONS ON ELECTRON DEVICES Volume: 51 Issue: 5 Pages: 817-819 Published: MAY 2004							
	3.	Impacts of notched-gate structure on contact etch stop layer (CESL) stressed 90-nm nMOSFET							
		By: Lin, Chien-Ting; Fang, Yean-Kuen; Yeh, Wen-Kuan; et al. IEEE ELECTRON DEVICE LETTERS Volume: 28 Issue: 5 Pages: 376-378 Published: MAY 2007	0	3	0	2	0	21	1.75
	4.	Optimum halo structure for sub-0.1 mu m CMOSFETs							
		By: Yeh, WK; Chou, JW IEEE TRANSACTIONS ON ELECTRON DEVICES Volume: 48 Issue: 10 Pages: 2357-2362 Published: OCT 2001	0	0	2	0	0	20	1.11
	5.	Reliability Improvement of 28-nm High-k/Metal Gate-Last MOSFET Using Appropriate Oxygen Annealing							
		By: Yang, Yi-Lin; Zhang, Wenqi; Cheng, Chi-Yun; et al. IEEE ELECTRON DEVICE LETTERS Volume: 33 Issue: 8 Pages: 1183-1185 Published: AUG 2012	4	4	1	3	1	17	2.43
	6.	Effects of Fin Width on Device Performance and Reliability of Double- Gate n-Type FinFETs							
		By: Lin, Cheng-Li; Hsiao, Po-Hsiu; Yeh, Wen-Kuan; et al. IEEE TRANSACTIONS ON ELECTRON DEVICES Volume: 60 Issue: 11 Pages: 3639-3644 Published: NOV 2013	2	2	5	4	2	15	2.50
	7.	Relationship between wafer edge design and its ultimate mechanical strength	0	2	2	4	0	15	1.67
		By: Chen, Po-Ying; Tsai, Ming-Hsing; Yeh, Wen-Kuan; et al. MICROELECTRONIC ENGINEERING Volume: 87 Issue: 11 Pages: 2065-2070 Published: NOV 2010							
	8.	The Improvement of High-k/Metal Gate pMOSFET Performance and Reliability Using Optimized Si Cap/SiGe Channel Structure							
		By: Yeh, Wen-Kuan; Chen, Yu-Ting; Huang, Fon-Shan; et al. IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY Volume: 11 Issue: 1 Pages: 7-12 Published: MAR 2011	3	1	0	1	0	14	1.75
	9.	Voltage-controlled multiple-valued logic design using negative differential resistance devices							
		By: Gan, Kwang-Jow; Tsai, Cher-Shiung; Chen, Yan-Wun; et al. SOLID-STATE ELECTRONICS Volume: 54 Issue: 12 Pages: 1637-1640 Published: DEC 2010	1	0	2	3	3	13	1.44
	10.	Design and fabrication of deep submicron CMOS technology compatible suspended high-Q spiral inductors	1	0	0	0	0	13	0.87
		By: Hsieh, MC; Fang, YK; Chen, CH; et al.							

