Jia Di's Homepage

Quick Links:

Jia Di

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Education:

08/2000 – now **University of Central Florida** **Orlando, FL**

PH. D. CANDIDATE / Electrical Engineering **GPA: 4.0 / 4.0**
Research emphasis in low power / energy synchronous / asynchronous DSP circuit and system design, power / energy-aware circuit design, power / energy estimation and optimization.

09/1997 – 01/2000 **Tsinghua University** **Beijing, P. R. China**

M. S. / Electrical Engineering
Master Thesis: *Design and Implementation of 200MHz Digital Storage Oscilloscope*
Course and research projects emphasis in digital circuit and system design, digital signal processing.

09/1992 – 07/1997 **Tsinghua University** **Beijing, P. R. China**

B. S. / Electrical Engineering
Course emphasis in digital and analog circuits design, signal processing, and control theory.

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Professional and Working Experience:

08/2000 – now **University of Central Florida** **Orlando, FL**

Research Assistant

Low Power Digital Signal Processing Circuit and System Design and Analysis

- Develop new power optimization techniques for synchronous and asynchronous logic circuits, both in gate-level and system-level. These techniques include Zero Insertion, 2-Dimensional Pipeline Gating, and Software-hardware Co-optimization.
- Design low power digital VLSI circuits using HDL, Synopsys Design Compiler/Analyzer, and Synopsys VHDL Debugger. These circuits are used to implement and test the developed power optimization techniques.
- Develop algorithms to estimate power dissipation quickly and accurately for asynchronous logic in transistor and gate levels, tested by EPIC Powermill and Cadence IC Design Environment.
- Explore power reduction techniques developed in all levels.
- Develop a program to test power estimation algorithm using C. This program can read specific VHDL code and calculate switching power based on input probability.

09/1996 – 01/2000 **Tsinghua University** **Beijing, P. R. China**

Research Assistant

Designed Digital Storage Oscilloscope at 200MHz sampling frequency

- Designed all the digital circuits in the oscilloscope, including CPU system, sampling control system, wave display system, and printed circuit board routing.
- Programmed the CPU control program in C and Assembly language.
- Was team leader during the developing process.

04/1996 – 08/1997 **IBM China Research Laboratory** **Beijing, China**

Part-time Assistant Engineer in IBM Via-Voice software development group

- Utilized interpersonal and teamwork skills to organize 400 people from different occupations (including managers, doctors, reporters, writers, teachers, researchers, students) and record their voices.
- Recognized sample voices and translated them into text, a very detail-orientated task.

08/1996 **Tianji Science & Trade Co.** **Shenzhen, China**

Internship

Software development of the microprocessors of video CD player

- Rewrote and debugged more than 2000 lines of assembly code to implement software for main control chip of Video CD player (Motorola 68HC11) in 4 weeks.

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Publications:

Book Chapters --

[1.] Wanzhou Li, Jia Di, Chuanzhao Yu, and Dikan Zhang, *Principles and design of Digital Storage Oscilloscope*, Tsinghua Press, 2001 (Book Chapter).

Journal Papers --

[1.] Jia Di, J. S. Yuan and M. Hagedorn, "Input mapping for modeling energy dissipation of complex CMOS gates", accepted by IEE Proceeding on Circuits and Systems.

[2.] Jia Di, J. S. Yuan and M. Hagedorn, "Asynchronous circuits design for energy awareness", revised and resubmitted to IEE Proceeding on Circuits and Systems.

[3.] Jia Di, J. S. Yuan and M. Hagedorn, "Accurate Switching Activity Modeling of Multi-rail Speed-independent Circuits", submitted to IEE Proceeding on Circuits and Systems.

[4.] Jia Di, J. S. Yuan, "Energy-aware Bit-wise Completion Dual-rail Asynchronous Speed-independent Circuits Design", revised and resubmitted to IEEE Transaction on VLSI Systems.

Conference Papers --

[1.] Jia Di, J. S. Yuan, "Energy-aware Asynchronous Pipelined Multiplier Design", The First Northeast Workshop on Circuits And Systems (NEWCAS), Jun. 2003

[2.] Jia Di, J. S. Yuan, "Run-time Reconfigurable Power-aware Pipelined Signed Array Multiplier Design", International Symposium on Signals, Circuits and Systems, Jun. 2003

[3.] Jia Di, J. S. Yuan, "Power-aware Pipelined Multiplier Design Based on 2-Dimensional Pipeline Gating", 2003 Great Lake Symposium on VLSI, Apr. 2003.

[4.] Jia Di, J. S. Yuan, and R. Demara, "High Throughput Power-aware FIR Filter Design by Fine-grain Pipelining Multipliers and Adders", IEEE Computer Society Annual Symposium on VLSI, Feb. 2003.

[5.] Jia Di, J. S. Yuan and M. Hagedorn, "Switching Activity Modeling of Multi-rail Speed-independent Circuits — A Probabilistic Approach", IEEE 45th Midwest Symposium on Circuits and Systems, Aug. 2002.

[6.] Jia Di, J. S. Yuan and M. Hagedorn, "Energy-aware Multiplier Design in Multi-rail Encoding Logic", IEEE 45th Midwest Symposium on Circuits and Systems, Aug. 2002.

Technical Reports --

[1.] Jia Di, "Energy-aware Pipelined Asynchronous Parallel Adders Design and Analysis", to Chip Design and Reliability Lab, School of Electrical Engineering and Computer Science, University of Central Florida, 2002.

[2.] Jia Di, "SAMTAC — A Switching Activity Modeling Tool for Speed-independent Asynchronous Circuits", to Chip Design and Reliability Lab, School of Electrical Engineering and Computer Science, University of Central Florida, 2002.

[3.] Jia Di, "Energy Dissipation Simulation and Analysis of NCL Multiply-and-Accumulate Units", to Theseus Logic Inc., 2001.

[4.] Jia Di, "Energy Dissipation Comparison of Semi-static and Static NCL Gates", to Theseus Logic Inc., 2001.

[5.] Jia Di, "Modeling Energy Dissipation in NCL Threshold Gates", to Theseus Logic Inc., 2001.

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Skills:

Computer skills: Operating Systems: Windows, Sun Solaris
Hardware Description Language: **VHDL, Verilog**
Programming language: **C,** Assembly

IC design tools: **Synopsys Design Compiler/Analyzer**
Synopsys VHDL Debugger
Cadence IC Design Tools
Powermill

Language: Fluent in Chinese and English

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Awards:

2001 – 2002 Univ. of Central FL Orlando, FL
Research Assistantship Enhancement Award (Fall 01 and Spring 02)
Provost's Fellowship (Fall 00 and Spring 01)

1993 – 1999 Tsinghua University Beijing, China
Guanghua Excellent Student Scholarship of Tsinghua graduate students (1998)
Excellent Undergraduate Student Scholarship (1993, 1994, 1995, 1996)

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Activities:

IEEE Student Member since Oct. 2000

IEEE Computer Society Student Member since Oct. 2001

President of Student Association in department and Class Auto21 of Tsinghua University

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