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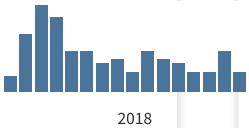
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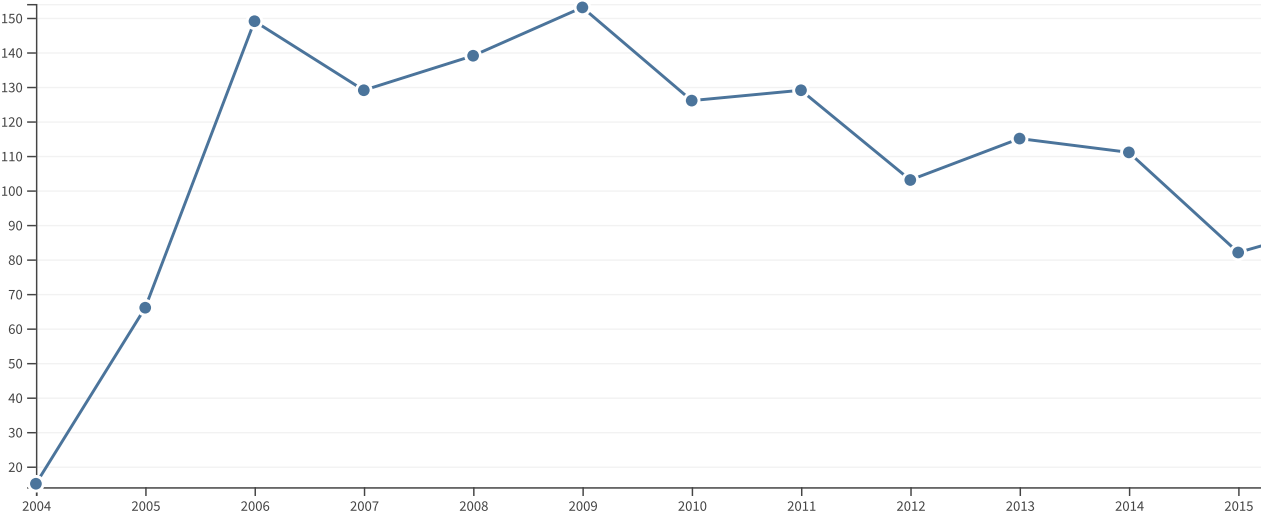
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2014	2015	2016	2017	2018	Total	Average Citations per Year
111	82	91	124	60	1592	106.13
9	6	11	14	5	131	11.91

<input type="checkbox"/>	1.	<b>Dipole model explaining high-k/metal gate field effect transistor threshold voltage tuning</b>	By: Kirsch, P. D.; Sivasubramani, P.; Huang, J.; et al. <a href="#">APPLIED PHYSICS LETTERS</a> Volume: 92 Issue: 9 Article Number: 092901 Published: MAR 3 2008							
<input type="checkbox"/>	2.	<b>The effect of interfacial layer properties on the performance of Hf-based gate stack devices</b>	By: Bersuker, G.; Park, C. S.; Barnett, J.; et al. <a href="#">JOURNAL OF APPLIED PHYSICS</a> Volume: 100 Issue: 9 Article Number: 094108 Published: NOV 1 2006	11	4	7	4	1	107	8.23
<input type="checkbox"/>	3.	<b>Mechanism of electron trapping and characteristics of traps in HfO(2) gate stacks</b>	By: Bersuker, Gennadi; Sim, J. H.; Park, Chang Seo; et al. Conference: 44th Annual IEEE International Reliability Physics Symposium Location: San Jose, CA Date: MAR 26-30, 2006 Sponsor(s): IEEE Electron Devices Soc; IEEE Reliabil Soc <a href="#">IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY</a> Volume: 7 Issue: 1 Pages: 138-145 Published: MAR 2007	15	3	7	11	3	84	7.00
<input type="checkbox"/>	4.	<b>Intrinsic characteristics of high-k devices and implications of fast transient charging effects (FTCE)</b>	By: Lee, BH; Young, CD; Choi, R; et al. Conference: 50th IEEE International Electron Devices Meeting Location: San Francisco, CA Date: DEC 13-15, 2004 Sponsor(s): IEEE Elect Devices Soc IEEE INTERNATIONAL ELECTRON DEVICES MEETING 2004, TECHNICAL DIGEST Pages: 859-862 Published: 2004	3	1	0	1	0	65	4.33
<input type="checkbox"/>	5.	<b>Interfacial layer-induced mobility degradation in high-k transistors</b>	By: Bersuker, G; Barnett, J; Moumen, N; et al. Conference: International Workshop on Dielectric Thin Films for Future ULSI Devices (IWDTF-4) Location: Tokyo, JAPAN Date: MAY 26-28, 2004 JAPANESE JOURNAL OF APPLIED PHYSICS PART 1-REGULAR PAPERS BRIEF COMMUNICATIONS & REVIEW PAPERS Volume: 43 Issue: 11B Pages: 7899-7902 Published: NOV 2004	2	3	1	0	0	63	4.20
<input type="checkbox"/>	6.	<b>High-k gate stacks for planar, scaled CMOS integrated circuits</b>	By: Huff, HR; Hou, A; Lim, C; et al. Conference: 1st International Symposium and Summer School on Nano and Giga Challenges in Microelectronics Research Location: MOSCOW, RUSSIA Date: SEP 10-13, 2002 Sponsor(s): Motorola Digital DNA Lab; Kurchatov Inst, Russian Res Ctr; Moscow State Univ; Int Sci & Technol Ctr; Elsevier; USAF, European Off Aerosp Res & Dev <a href="#">MICROELECTRONIC ENGINEERING</a> Volume: 69 Issue: 2-4 Pages: 152-167 Published: SEP 2003	2	3	0	1	0	57	3.56
<input type="checkbox"/>	7.	<b>Effect of pre-existing defects on reliability assessment of high-k gate dielectrics</b>	By: Bersuker, G; Sim, JH; Young, CD; et al. Conference: 15th European Symposium on the Reliability of Electron Devices, Failure P{hysics and Analysis Location: Swiss Fed Inst Technol, Zurich, SWITZERLAND Date: OCT 04-08, 2004 Sponsor(s): IEEE Electron Device Soc; IEEE Reliabil Soc <a href="#">MICROELECTRONICS RELIABILITY</a> Volume: 44 Issue: 9-11 Pages: 1509-1512 Published: SEP-NOV 2004	1	0	2	0	0	56	3.73
<input type="checkbox"/>	8.	<b>Electron trap generation in high-k gate stacks by constant voltage stress</b>	By: Young, Chadwin D.; Heh, Dawei; Nadkarni, Suvid V.; et al. Conference: IEEE International Integrated Reliability Workshop Location: S Lake Tahoe, CA Date: OCT 17-20, 2005 Sponsor(s): IEEE Elect Devices Soc; IEEE Reliabil Soc <a href="#">IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY</a> Volume: 6 Issue: 2 Pages: 123-131 Published: JUN 2006	2	0	1	2	0	53	4.08

7/9/2018

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9.

Effects of ALD HfO2 thickness on charge trapping and mobility

By: Sim, JH; Song, SC; Kirsch, PD; et al.  
Conference: 14th Biennial Conference on Insulating Films on Semiconductors  
Location: Univ Leuven, Dept Psychol, Leuven, BELGIUM Date: JUN 22-24, 2005  
Sponsor(s): IMEC; IEEE; Elect Devices Soc; ECS; Philips; ST; AIXTRON; Tokyo Elect; KEITHLEY  
MICROELECTRONIC ENGINEERING Volume: 80 Pages: 218-221 Published: JUN 2005

10.

Pulsed I-d-V-g Methodology and Its Application to Electron-Trapping Characterization and Defect Density Profiling

By: Young, Chadwin D.; Zhao, Yuegang; Heh, Dawei; et al.  
IEEE TRANSACTIONS ON ELECTRON DEVICES Volume: 56 Issue: 6 Pages: 1322-1329 Published: JUN 2009

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5	5	6	11	0	44	4.40

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