Dennis Sylvester

Professor

2417B EECS
Department of Electrical Engineering and Computer Science
1301 Beal Ave.
Ann Arbor, MI 48109-2122

dennis@eecs.umich.edu
(734) 615-8783 (office)
(734) 763-9324 (fax)
http://www.eecs.umich.edu/~dennis

Professional Experience

Professor, University of Michigan, Ann Arbor 2010 – present

Associate Professor 2005 – 2010

Assistant Professor 2000 – 2005

- Department of Electrical Engineering and Computer Science
- Director, Michigan Integrated Circuits Laboratory (MICL)

Visiting Professor, Nanyang Technological University, Singapore 2013 - present

Co-founder, CubeWorks, Inc. 2013

Co-founder, Ambiq Micro 2010

Visiting Associate Professor, National University of Singapore 2006 – 2007

- Department of Electrical and Computer Engineering

Senior R&D Engineer, Synopsys, Inc., Mountain View, CA 1999 – 2000

TCAD Engineer, Hewlett-Packard Laboratories, Palo Alto, CA 1996 - 1998

Education

University of California, Berkeley, Berkeley, California

Ph.D. Electrical Engineering, 1999

Dissertation: *Analytical Modeling and Characterization of Deep Submicron Interconnect*

M.S. Electrical Engineering, 1997

Thesis: *Interconnect Capacitance Characterization Using Charge-Based Capacitance Measurement (CBCM) Technique*

University of Michigan, Ann Arbor, Michigan

B.S. Electrical Engineering, 1995

Summa Cum Laude

Honors and Awards

- University of Michigan College of Engineering Innovation Excellence Award, joint with David Blaauw, 2014.
- ACM/IEEE Design Automation Conference 50th anniversary awards, DAC prolific author award (2nd most prolific author in DAC 5th decade), DAC collaborative award (for publishing at least 20 papers with Prof. David Blaauw), DAC most prolific author in a single year award (2004), and DAC prolific author award (more than 35 papers at DAC), 2013.
- University of Michigan Rackham Faculty Recognition Award, 2013.
- Top Contributing Authors, IEEE International Solid-State Circuits Conference, 60th anniversary celebration, named in top 10 authors in 2004-2013 timeframe.
- University of Michigan Electrical Engineering and Computer Science Department Outstanding Achievement Award, 2011.
- IEEE Fellow, 2011, "for contributions to energy-efficient integrated circuits"
- University of Michigan College of Engineering Ted Kennedy Family Team Excellence Award, 2009-2010
- Best Paper Award, *ACM/IEEE International Symposium on Low-Power Electronics and Design*, 2009
- University of Michigan College of Engineering Ted Kennedy Family Team Excellence Award, 2008-2009
- Best Paper Award, *IEEE International Symposium on Quality Electronic Design*, 2006
- Henry Russel Award, University of Michigan, given in recognition of distinguished scholarship and conspicuous ability as a teacher, 2006
- University of Michigan College of Engineering Vulcans Education Excellence Award, 2005-2006
- Semiconductor Research Corporation Inventor Recognition Award, 2005
- 1938E Award, U-M College of Engineering, given for outstanding teaching, counseling, and scholarly integrity, 2004
- IBM Faculty Award, IBM Austin Center for Advanced Studies, 2004
- Association for Computing Machinery (ACM) Special Interest Group on Design Automation (SIGDA) Outstanding New Faculty Award, 2003
- Ruth and Joel Spira Outstanding Teaching Award, U-M College of Engineering, 2003
- NSF Faculty Early Career Development (CAREER) Award, 2002
- David J. Sakrison Memorial Prize for best dissertation, UC-Berkeley EECS department, 2000
- Beatrice Winner Award, *IEEE International Solid-State Circuits Conference*, 2000
- Synopsys Special Recognition Award (for excellent performance and outstanding contribution to Synopsys Engineering), 2000
- Best Paper Award, Semiconductor Research Corporation Graduate Fellowship Program, 1999
- Outstanding Research Presentation Award, Semiconductor Research Corporation Technical Conference, 1998
- Best Student Paper Award, *IEEE International Semiconductor Device Research Symposium*, 1997
- Semiconductor Research Corporation Graduate Fellow, 1997 – 1999

Research Interests

- Low power integrated circuit design and design automation
- Variation-tolerant circuit design styles
- Near-threshold computing systems
- Millimeter-scale computing systems

Professional Activities and Service

- Advisory Board Member, DESIGN School, Kyoto University, 2013 – present
- External Advisory Committee Member, ATIC-SRC Center of Excellence on Energy-Efficient Electronic Systems, United Arab Emirates, 2014 – present
- Guest Editor, special issue on Circuits and Systems for Energy-Autonomous Microsystems, *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2013.
- Associate Editor, *IEEE Transactions on Computer-Aided Design*, 2006 – 2011
- Executive Committee member, *ACM/IEEE Design Automation Conference*, 2008 – 2009
- Tutorials Chair, *ACM/IEEE Design Automation Conference*, 2009
- Steering Committee member, *ACM/IEEE International Symposium on Physical Design*, 2006 – 2008
- Co-organizer, *ACM Workshop on Test Structure Design for Variability Characterization (TSD)*, 2008.
- Associate Editor, *IEEE Transactions on VLSI Systems*, 2003 – 2007
- Planning Committee member, Semiconductor Research Corporation Interconnect Forum, Santa Cruz, CA, 2006
- General Chair, *ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems* (TAU), 2005
- Panel moderator
  - "Crystal ball on low power: limiting trends and strategic solutions," *ACM/IEEE Design Automation Conference*, 2011
  - "Who is responsible for design for manufacturability issues in the era of nanotechnologies?", *ACM/IEEE Asia-South Pacific Design Automation Conference*, 2005
- Technical Program Committee co-Chair, *ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems* (TAU), 2004
- Tutorials Chair, *IEEE International Symposium on Quality Electronic Design* (ISQED), 2004
- Guest co-Editor, *IEEE Transactions on VLSI Systems*, special issue on System-Level Interconnect Prediction, October 2004
- General Chair, *ACM/IEEE International Workshop on System-Level Interconnect Prediction* (SLIP), 2003
- Co-organizer, panel on low-power design automation tools, *ACM/IEEE Design Automation Conference* (DAC), 2003
- Co-organizer and co-chair, special session on nanoscale CMOS, *ACM/IEEE Design Automation Conference*, 2002
- Member, U.S. Design Technology Working Group (TWG) for the International Technology Roadmap for Semiconductors (ITRS), 2001–2003

- Technical Program Committee Chair, *ACM/IEEE International Workshop on System-Level Interconnect Prediction* (SLIP), 2001 (co-chair), 2002
- Technical Program Committee member:
  - *IEEE International Solid-State Circuits Conference (ISSCC)*, 2015 – present
  - *IEEE Symposium on VLSI Circuits*, 2014 – present
  - *ACM/IEEE Design Automation Conference* (DAC), 2003–2006, sub-committee chair 2004–2006
  - *IEEE International Workshop on Design for Manufacturability and Yield* (DFM&Y), 2006
  - *ACM/IEEE International Symposium on Low-Power Electronics Design* (ISLPED), 2004–2005
  - *ACM/IEEE Asia-South Pacific Design Automation Conference* (ASP-DAC), 2005
  - *IEEE International Symposium on Quality Electronic Design* (ISQED), 2002–2003, chair of sub-committee on device, interconnect, and circuit-level modeling and analysis (2003)
  - *ACM/IEEE International Conference on Computer-Aided Design* (ICCAD), 2000–2002
  - *IEEE International Conference on Computer Design* (ICCD), 2001–2003, 2006 (Logic and Circuits Track co-chair)
  - *ACM/IEEE International Workshop on Timing Issues in Digital Systems* (TAU), 2002, 2006
  - *ACM/IEEE International Workshop on System-Level Interconnect Prediction* (SLIP), 2000, 2004–2006
  - *IEEE International Symposium on Circuits and Systems* (ISCAS), 2002–2003
  - *SPIE Design and Process Integration for Microelectronic Manufacturing Conference*, 2005–2008
  - *IEEE International Conference on VLSI and System-on-Chip*, 2010
- Executive committee member, Fabless Semiconductor Association, 2000
- Proposal reviewer for:
  - National Science Foundation
  - Portugal Foundation for Science and Technology (FCT)
  - University of California MICRO program
  - Netherlands Organization for Scientific Research
- Reviewer for:
  - *IEEE Transactions on Computer-Aided Design, IEEE Transactions on VLSI Systems, IEEE Journal of Solid-State Circuits, IEEE Transactions on Electron Devices, IEEE Transactions on Computers, IEEE Design & Test of Computers, IEEE Transactions on Circuits and Systems, Proceedings of the IEEE*
  - *ACM Transactions on Design Automation of Electronic Systems*
  - *Elsevier Integration: The VLSI Journal*

University Service

- ECE executive committee member, 2014 – 2016
- ECE faculty search committee member, 2012 – 2013
- ECE: EE program PhD recruiting coordinator, 2011 – 2013
- ECE graduate admissions committee member, 2009 – 2013
- CSE chair search advisory committee member (ECE representative), 2010 – 2011

- ECE: EE undergraduate program advisor, 2010 – 2011
- ECE financial aid strategy team member, 2009
- ECE executive committee member, 2007 – 2009
- ECE faculty search committee member, 2007 – 2009
- CSE chair search advisory committee member (ECE representative), 2007 – 2008
- VLSI graduate advisor (concurrently a member of EE graduate committee), 2000 – 2010
- Computer Engineering Center task force member, 2006
- ECE faculty search sub-committee chair (VLSI), 2004 – 2005
- EECS strategic planning sub-committee on department structure and faculty environment, 2005
- Eta Kappa Nu (HKN) faculty advisor, 2003 – 2006
- EECS building renovation committee member, 2003 – 2006
- ECE faculty search sub-committee member (RF circuits/MEMS), 2002–2003
- Departmental Computing Organization (DCO) review committee member, 2002
- Organizer, EECS Department VLSI seminar series (renamed the Micron Technology Foundation VLSI Seminar Series), 2001 – 2006
- Marshal, Spring 2002 Commencement Exercises
- Computer Engineering degree program committee member, 2001
- HKN Scholarship faculty reviewer, 2000, 2006
- Promotion and tenure, and/or reappointment casebook committee member or chair, 2005, 2006, 2008, 2009, 2010 (chair), 2011 (chair), 2012, 2014 (chair)

Teaching

Courses Taught:

- EECS 312, Digital Integrated Circuits
- EECS 427, VLSI Design I
- EECS 523, Digital Integrated Circuit Technology
- EECS 627, VLSI Design II
- EECS 628, Advanced High Performance VLSI Design

Courses Developed or Significantly Revised:

- EECS 312, Digital Integrated Circuits (Developed)
- EECS 427, VLSI Design I (Revised, Fall 2003)
- EECS 628, Advanced High Performance VLSI Design (Co-developed)

Consulting

- STMicroelectronics, Geneva, Switzerland, [Technology Council Member, 2006 – present]
- Tela Innovations, Campbell, CA [Technical Advisory Board member, 2009 – 2011]
- Sequence Design, Inc., Santa Clara, CA [Technical Advisory Board member, 2003 – 2009]
- Blaze DFM, Inc., Sunnyvale, CA [Technical Advisory Board member, 2004 – 2008]

- Cadence Design Systems, San Jose, CA
- Intel Corporation, Santa Clara, CA and Haifa, Israel
- Rader, Fishman, and Grauer PLLC, Bloomfield Hills, MI
- King Abdullah University of Science and Technology, Saudi Arabia
- NEC Research Labs, Princeton, NJ

Grants and Contracts

- Microelectronics Advanced Research Corporation (MARCO) and Defense Advanced Research Projects Agency (DARPA), "Circuits for spin-based devices," through the Center for Spintronic Materials, Interfaces and Novel Architectures (C-SPIN), 1/15/13 – 10/31/17, $766,400.
- Defense Advanced Projects Research Agency (DARPA), "Energy efficient 3D near-threshold computing systems for future embedded applications," 10/19/12 – 3/18/14, lead PI: Trevor Mudge, $1,528,161.
- Advanced Micro Devices, gift funding to support research in CMOS aging, $50,000, 2012.
- US Air Force, "Sub-1mm electronics for actuating, controlling, and linking programmable matter," 3/15/12 – 12/30/12, lead PI: David Wentzloff, $60,000.
- Defense Science and Technology Laboratory, "Dstl Sensor Development Kits," 8/1/12 – 2/28/13, co-PI with David Blaauw, $160,000.
- Advanced Energy Consortium, "An autonomous microsystem test-bed for extreme environments," 6/1/12 – 12/31/13, co-PI with Yogesh Gianchandani (lead), David Blaauw, $475,000.
- Semiconductor Research Corporation, "Shortstop: Fast power supply boosting for energy-efficient high-performance processors," 8/1/12 – 7/31/15, co-PI with David Blaauw, $360,000.
- National Science Foundation, "Minimally invasive error detection/correction for runtime margin elimination," 7/1/12 – 6/30/15, co-PI with David Blaauw, $450,000.
- University of Michigan Comprehensive Cancer Center, "Implantable biosensors for the tumor microenvironment," 12/1/11 – 11/30/12, $40,000.
- National Science Foundation, "Integrating Circuits, Sensing, and Software to Realize the Cubic-mm Computing Class," 08/15/11 – 07/31/16, lead PI: David Wentzloff, $2,533,000.
- Office of Naval Research, "Cognitive Ultra-low Power Sensor System (CUPSS)," STTR with Intelligent Automation, Inc., 09/01/11 – 03/31/14, $195,000 (Phase I + Option + Phase II).
- National Science Foundation, "Collaborative Research: Variability Aware Software for Efficient Computing with Nanoscale Devices ," 09/01/2010 – 08/31/2015, co-PI under Director Rajesh Gupta, UCSD, $10,000,000.
- Office of Naval Research, "A Hierarchical Wireless System for Distributed Strain Monitoring in Naval Structures," SBIR with Civionics, LLC, 05/10/2010 – 11/09/2010, $33,250.
- King Abdullah University of Science and Technology Saudi Arabia, "Toward efficient nanoelectronic systems for biomedical sensing," lead PI: Yogesh Gianchandani, 05/01/2010 – 04/30/2012, $680,000.
- Intel Corporation, "A confidence-driven model for predictable computing in future technologies," PI: Zhengya Zhang, co-PIs: Dennis Sylvester, David Blaauw, $249,000 (gift), 2010-2011.
- Google, gift to support research in energy-efficient memory and processor architectures, joint with Professor Thomas Wenisch, David Blaauw, and Trevor Mudge, $100,000, 2009.

- National Science Foundation, "Reclaiming Moore's Law through Ultra Energy Efficient Computing," 08/01/2009 – 07/31/2014, co-PI with David Blaauw (lead PI, U-Michigan), Trevor Mudge (U-Michigan), Chaitali Chakrabarti (Arizona St.), and David Harris (Harvey Mudd), $2,778,507.
- Microelectronics Advanced Research Corporation (MARCO) and Defense Advanced Research Projects Agency (DARPA), "Resiliency for ultra-low power platforms," through the Gigascale Systems Research Center (GSRC), 11/01/09 – 10/31/12, $315,250.
- Medical Innovation Center Innovation Grant, University of Michigan, "Brain Pressure Sensor – Wireless," co-PI with Dr. Lynda Yang and Mr. Alex Kim, $10,000, 2009.
- National Institute of Standards and Technology, "Cyber-enabled wireless monitoring systems for the protection of deteriorating national infrastructure systems," 02/01/2009 – 01/31/2014, $19,162,000.
- Army Research Laboratory, "COM-BAT: Center for Objective Microelectronics and Biomimetic Advanced Technology," Kamal Sarabandi (Director), Dennis Sylvester (Processing team leader), 04/01/08 – 03/31/13, $10,000,000.
- National Science Foundation, "An Engineering Research Center in Wireless Integrated Microsystems," Kensall D. Wise (Director), Dennis Sylvester (Micropower Circuits thrust leader, 02/01/05 – present), total thrust budget $417,000 (direct costs) in 2007-2008.
- National Science Foundation, "Probabilistic wearout in nanoscale CMOS: analysis, monitoring, and optimization," co-PI with David Blaauw, U-Michigan, 09/01/08 – 08/31/11, $300,000.
- Defense Advanced Research Projects Agency (DARPA), "Strained Si/SiGe/Ge HEterojunction Tunneling Transistor (HETT) Technology with Steep Subthreshold Slope for Extremely Low Power Electronics," (IBM lead organization), 01/01/08 – 12/31/09, $444,000 (UM share).
- Semiconductor Technology Academic Research Center (Japan), "Low-cost body biasing and reliability-aware CAD," 01/01/08 – 12/31/08, $180,000.
- Semiconductor Technology Academic Research Center (Japan), "Soft-edge flip-flops for timing yield and parametric yield budgeting across functional units," 09/01/06 – 08/31/07, $180,000.
- Microelectronics Advanced Research Corporation (MARCO) and Defense Advanced Research Projects Agency (DARPA), "ElastIC: An Adaptive Self-Healing Architecture for Unpredictable Silicon," 09/01/06 – 10/31/09, $378,000
- National Science Foundation, "Formal Design Techniques for Adaptive Circuit Fabrics," co-PI with Michael Orshansky, U-Texas, Austin, 09/01/06 – 08/31/09, $464,440
- Semiconductor Research Corporation, "A Design Optimization Framework for Process Variation Tolerance," co-PI with David Blaauw, U-Michigan, 09/01/06 – 12/31/09, $390,000
- Semiconductor Research Corporation, "CAD Solutions for Parametric Yield Optimization," co-PI with David Blaauw, U-Michigan, 09/01/05 – 08/31/08, $360,000
- Semiconductor Technology Academic Research Center (Japan), "Runtime leakage analysis and statistical static timing analysis enhancements," 09/01/05 – 08/31/06, $180,000.
- National Science Foundation and Semiconductor Research Corporation, "Communication Fabrics for the Globally Asynchronous Network-on-Chip Era," co-PI with Michael Flynn, U-Michigan, 9/01/04 – 08/31/07, $489,500
- Microelectronics Advanced Research Corporation (MARCO) and Defense Advanced Research Projects Agency (DARPA), "System-Level Living Roadmap," 09/01/03 – 08/31/06, $592,000
- National Science Foundation, "CAREER: Improving Technology-EDA Integration through Interconnect Design Tools for Nanometer Design," 01/01/02 – 12/31/08, $375,000

- National Science Foundation, "ITR: Methodologies for Robust Design of Information Systems under Multiple Sources of Uncertainty," co-PI with David Blaauw, U-Michigan, Sachin Sapatnekar, U-Minnesota, and Sarma Vrudhula, U-Arizona, 09/01/02 – 08/31/08, $1,800,000
- Semiconductor Research Corporation, "Analysis and Reduction of Simultaneous Gate-Oxide Tunneling and Subthreshold Leakage Current," co-PI with David Blaauw, U-Michigan, 07/01/03 – 06/30/06, $360,000
- Semiconductor Research Corporation, "Algorithmic and Circuit-level Approaches to Leveraging Multi-Vth processes," co-PI with Kurt Keutzer, UC-Berkeley, 07/01/01 – 04/30/05, $490,000
- Semiconductor Research Corporation, "Layout Techniques for Cost-driven Control of Lithography-induced Variability," co-PI with Andrew B. Kahng of UC-San Diego, 07/01/01 – 01/31/05, $420,000
- Defense Advanced Research Projects Agency (DARPA), "Complex Signal Processing Application Specific Integrated Circuit Designs," lead PI: Richard Brown, University of Michigan, subcontract of BAE Systems, 09/18/01 – 03/15/03, $225,000
- Microelectronics Advanced Research Corporation (MARCO) and Defense Advanced Research Projects Agency (DARPA), "GSRC Technology Extrapolation (GTX) Engine," 01/01/01 – 08/31/03, $285,000
- IBM Corporation, Austin Center for Advanced Studies, "Joint Statistical Optimization of Static Power Consumption and Performance," Faculty Award (gift), $40,000, 2004.
- Intel Corporation, "VLSI Design Curriculum," co-PI with Richard Brown, David Blaauw, and Michael Flynn, 09/01/03 – 08/31/04, $202,173.
- Intel Circuits Research Laboratory, gift to support research in the areas of global signaling and multi-Vdd circuit design, $120,000, 2003–2005.
- Intel Corporation, "Current Source Cell Models with Variability," $20,000, 2005.
- Intel Corporation, "An Alternative Framework for Statistical Optimization Based on Variation Space Sampling, including Current Source Models," $10,000, 2006.
- NEC USA, gift to support research in the area of noise-aware timing analysis, $38,000, 2001.
- Mentor Graphics Corporation, gift to support research in the area of design for manufacturability, $100,000, 2002–2005.
- Sun Microsystems Academic Equipment Grant, to support research in the area of multi-Vth and multi-Vdd circuit design, 2 Sun Blade 1000 workstations, $51,000, 2002.
- Intel Corporation, equipment donation to support research in global signaling and multi-Vdd circuit design, $19,645, 2003.
- Intel Corporation, equipment donation to support research in current source modeling and statistical optimization, $5,959, 2006.
- Intel Corporation, equipment donation to support the development of a showcase circuit design graduate student office space, $66,878, 2009.
- Intel Corporation, cash donations to support the Michigan Integrated Circuits Laboratory, $50,000, 2009, 2011.
- U-M College of Engineering, to support the creation of a VLSI seminar series, 09/01/01 – 04/30/03, $11,500 (supplemented with $3,500 of support from Solid-State Electronics Laboratory)
- Micron Technology Foundation, to support the VLSI seminar series, 09/01/03 – 04/30/06, $15,700

Selected Invited Talks and Tutorials

- IEEE Solid-State Circuits Society, UAE chapter, "Ultra-low power IC design 101," April 2014.
- Keynote speaker, "How to Design Nanowatt Microsystems," *IEEE International Conference on Electronics, Circuits, and Systems*, Abu Dhabi, UAE, December 2013.
- Kyoto University, "Ultra low power system design challenges and solutions," June 2013.
- Broadcom low-power forum speaker, "Energy efficient circuit design: research overview at University of Michigan," April 2013.
- *IEEE International Solid-State Circuits Conference (ISSCC)*, "An Energy-Centric Design Approach to Achieve Nanowatt Microsystems," Sunday night panelist, February 2013.
- Electrons to Electronics Symposium celebrating 65th birthday of Chenming Hu, "Towards Nanowatt Computing," Berkeley, CA, December 2012.
- Stanford University, "Millimeter-Scale Computing," December 2012.
- National University of Singapore, Electrical and Computer Engineering Department Seminar, "Enabling Millimeter-Scale Computing," August 2012.
- Rice University ECE Colloquium, "Millimeter-Scale Computing," November 2011.
- IEEE Central Texas Section Seminar, "Enabling Millimeter-Scale Computing," September 2011.
- *IEEE International Solid-State Circuits Conference (ISSCC)*, "Ultra-low power design for WSN," Sunday night panelist, February 2011.
- IEEE Circuits and Systems Forum on Emerging and Selected Topics (CAS-FEST), Variation-Aware Design for Nanoscale VLSI, "Mitigating variability in near-threshold computing," Athens, Greece, December 2010.
- National Science Foundation Workshop on Interdisciplinary Challenges Beyond the Scaling Limits of Moore's Law, "Enabling Ubiquitous Computing with Ultra-Low Power Integrated Circuits," Arlington, VA, August 2010.
- Columbia University, "Enabling Ubiquitous Computing with Ultra-Low Power Integrated Circuits," Dean's Distinguished Lecture, April 2010.
- University of Illinois, "Circuit design advances for ultra-low power sensing platforms," ECE Colloquium, April 2010.
- Michigan State University, "Low voltage circuits to enable widespread sensing applications," East Lansing, MI, October 2009.
- University of Texas VLSI seminar series, "Circuit design advances for wireless sensing applications," Austin, TX, September 2009.
- Panelist, "Steep slope or slippery slope," *IEEE Device Research Conference*, State College, PA, June 2009.
- *IEEE International Solid-State Circuits Conference (ISSCC)*, "Device sizing for variability in energy constrained systems," Low-voltage design forum speaker and panelist, February 2009.
- Electronic Design Systems Fair, System Design Forum, invited speaker, "Coping with variability in nanoscale CMOS: analyze, sense, correct, exploit," Yokohama, Japan, January 2009.
- IBM Design Automation Professional Interest Community Seminar, "Extending nanoscale CMOS: analyze, sense, correct, and exploit," Austin, TX, August 2008.
- Invited lecturer, EPFL summer school on Nanoelectronic Circuits and Tools, "Pushing nanoscale CMOS: Design-related challenges," and "Extending nanoscale CMOS: analyze, sense, correct, and exploit," Lausanne, Switzerland, July 2008.
- University of Waterloo, "Low-voltage circuit design for widespread sensing applications," July 2008.

- UCLA Departmental Seminar Series in Electrical Engineering, "Energy-driven circuit design for ubiquitous sensing applications," March 2008.
- Panelist, "Scaling the power wall," *IEEE International Symposium on System-on-Chip*, Tampere, Finland, November 2007.
- IBM Experts Workshop on Low Voltage CMOS, "Highly parallel adaptive systems for low voltage operation," Yorktown Heights, NY, November 2007.
- ST Microelectronics, "Low power circuit design research at the University of Michigan," Crolles, France, November 2006.
- Panelist, "How deep is it in here? Will variation-aware analysis be the savior for the nanometer era?", *ACM/IEEE Design Automation Conference*, July 2006.
- Intel Physical Verification and Physical Design (PVPD) research seminar, "Directions in low-power CAD," Haifa, Israel, July 2006.
- University of Utah, "IC design at ultra-low supply voltages," February 2006.
- Georgia Tech Electrical and Computer Engineering Departmental Seminar, "IC design at a crossroads: Enabling low-power and robust computing in nanometer CMOS," November 2005
- International Conference on Computer-Aided Design, half-day tutorial co-presenter, "Gate characterization and modeling for 90nm and below," November 2005.
- Cadence Design Systems Distinguished Speaker Series, "IC design at a crossroads: Enabling low-power and robust computing in nanometer CMOS," October 2005.
- Panelist, Manufacturing for Design meets Design for Manufacturing Forum, Semiconductor Research Corporation, October 2005.
- Northwestern University Seminar Series in Computational Sciences, "New approaches to parametric yield estimation and dual-Vth assignment," October 2005.
- Invited lecturer, Mead Engineering short course, "Circuit design challenges in nanometer-scale CMOS," Lausanne, Switzerland, July 2005.
- Semiconductor Research Corporation e-Workshop, "Multiple supply and threshold voltage design: guidelines, algorithms, and circuit solutions," March 2005.
- Austin Center for Advanced Studies Annual Conference, "Parametric yield estimation considering power/performance correlation," February 2005.
- Asia-South Pacific Design Automation Conference, full-day tutorial co-presenter, "Power-aware design for performance," January 2005.
- International Symposium on Microarchitecture, full-day tutorial co-presenter, "Low-power robust computing," December 2004.
- Sequence Design NanoCool Low-power Design Initiative Seminar Keynote, "New approaches to total power reduction including runtime leakage," San Jose, CA, August 2004.
- Intel VLSI curriculum development two-day workshop, presenter, Hangzhou, China, and Penang, Malaysia, July 2004.
- Design Automation Conference, full-day tutorial co-presenter, "Getting Your 'Cool ASIC' Up to Speed: Practical Techniques and Tools to Achieve Custom-like Performance in a Power-Aware Design Flow," June 2004.
- Synopsys technology offsite, "EDA and Design Challenges with 45nm Devices," Half Moon Bay, CA, May 2004.
- *IEEE Annual Workshop on Interconnections within High-Speed Digital Systems*, "Modeling and characterization of chip-level metal interconnects," Santa Fe, NM, May 2004.

- Panelist, "Buffering and Agony: What does the Future Hold?" *ACM/IEEE International Symposium on Physical Design*, Phoenix, AZ, April 2004.
- University of California, Berkeley, Distinguished Lecture Series, "IC Design at a Crossroads: Enabling Low-Power and Robust Computing in Nanometer CMOS," April 2004.
- University of Texas, Austin VLSI seminar series, "New Approaches to Total Power Reduction Including Runtime Leakage," March 2004.
- IBM Austin Research Laboratories and T.J. Watson Research Center, "Multi-Vdd/Vth Design Space and Early Algorithmic Results," Austin, TX and Yorktown Heights, NY, August 2003.
- Advanced Micro Devices, "Minimum Cost of Correction and Related Design for Value Topics," Sunnyvale, CA, July 2003.
- Panelist, "Judgment Day for Power Management," *IEEE VLSI Symposium on Circuits*, joint panel with *IEEE VLSI Symposium on Technology*, Kyoto, Japan, June 2003.
- Fujitsu Laboratories, "Multi-Vdd/Vth Design and Interconnect Tuning Strategies," Tokyo, Japan, June 2003.
- Mentor Graphics, "Towards Performance-driven Reduction of the Cost of RET-based Lithography Control," Wilsonville, OR, May 2003.
- Cypress Semiconductor, "Low-power Design for Global Interconnects and Dual-Supply Systems," San Jose, CA, March 2003.
- Panelist, 2002 International Technology Roadmap for Semiconductors conference, "Challenges and opportunities for a low-power roadmap in consistence with ITRS CMOS scaling," San Francisco, CA, July 2002.
- IEEE Solid-State Circuits Society Kansai Chapter technical seminar, "High Performance Design in Nanometer Technologies," Kyoto, Japan, May 2002.
- Hitachi Central Research Laboratories, "High Performance Design in Nanometer Technologies," Tokyo, Japan, May 2002.
- Sequence Design NanoCool Low-power Design Initiative Seminar Keynote, "Power-driven Challenges in Nanometer Design," Ottawa, Canada, May 2002.
- Intel Physical Design Symposium, "Global Signaling Strategies for Nanometer CMOS," Santa Clara, CA, April 2002.
- University of California, Berkeley Electronics System Design (ESD) Seminar, "Global Signaling Strategies for Nanometer CMOS," April 2002.
- International Conference on Computer-Aided Design, full-day tutorial co-presenter, "Electrical Integrity Design and Verification for Digital and Mixed-Signal Systems-on-a-chip," November 2001.
- NEC Computers and Communications Research Labs (CCRL), "Approaches to Noise-Aware Static Timing Analysis," Princeton, NJ, December 2000.
- International Conference on Computer-Aided Design, full-day tutorial co-presenter, "Interconnect-centric Design and Analysis for Electrical Integrity in Systems-on-a-chip," November 2000.
- University of California, Berkeley Solid-State Technology and Device Seminar, "Insights on Deep Submicron Design: An EDA Perspective," January 2000.
- Fabless Semiconductor Association Modeling Workshop, "The Role of Interconnect in System-Level Performance: Delay, Power, Noise," invited tutorial, San Jose, CA, May 1999
- IEEE Electron Devices Society Summer Symposium, "Interconnect Scaling: Signal Integrity and Performance in Future High-Speed CMOS Designs," Santa Clara, CA, June 1998

Patents

Patents Issued

1. Dennis Sylvester and Himanshu Kaul, "Transition-aware signaling," US patent 6,870,402, March 22, 2005.
2. Dennis Sylvester, Himanshu Kaul, and David Blaauw, "Actively shielded signal wires," US patent 6,919,619, July 19, 2005.
3. Trevor Mudge, Todd Austin, David Blaauw, Dennis Sylvester, and Krisztian Flautner, "Memory system having fast and slow data reading mechanisms," US patent 6,944,067, September 13, 2005.
4. Todd Austin, David Blaauw, Trevor Mudge, Dennis Sylvester, and Krisztian Flautner, "Memory system having fast and slow data reading mechanisms," US patent 7,072,229, July 4, 2006.
5. Andrew B. Kahng, Puneet Gupta, Dennis Sylvester, and Jie Yang, "Method for correcting a mask layout," US patent 7,149,999, December 12, 2006.
6. Andrew B. Kahng, Puneet Gupta, Dennis Sylvester, and Jie Yang, "Method for correcting a mask layout," US patent 7,614,032, November 3, 2009.
7. Gregory Chen, Dennis Sylvester, and David Blaauw, "Integrated circuit memory access mechanisms," US patent 7,864,562, January 4, 2011.
8. Andrew B. Kahng, Puneet Gupta, Dennis Sylvester, and Jie Yang, "Tool for modifying mask design layout," US patent 8,103,981, January 24, 2012.
9. Yoonmyung Lee, Michael Wieckowski, David Blaauw, and Dennis Sylvester, "Memory cell structure, a memory device employing such a memory cell structure, and an integrated circuit having such a memory device," US patent 8,107,290, January 31, 2012.
10. Sudhir Satpathy, David Blaauw, Trevor Mudge, Dennis Sylvester, and Ron Dreslinski, "Crossbar circuitry and method of operation of such crossbar circuitry," US patent 8,108,585, January 31, 2012.
11. Sudhir Satpathy, David Blaauw, Trevor Mudge, and Dennis Sylvester, "Crossbar circuitry and method of operation of such crossbar circuitry," US patent 8,230,152, July 24, 2012.
12. Sudhir Satpathy, David Blaauw, Trevor Mudge, and Dennis Sylvester, "Crossbar circuitry for applying a pre-selection prior to arbitration between transmission requests and method of operation of such crossbar circuitry," US patent 8,255,610, August 28, 2012.
13. Matthew Fojtik, Dennis Sylvester, David Blaauw, David Fick, "Stalling synchronization circuits in response to a late data signal," US patent 8,276,014, September 25, 2012.
14. Ronald Dreslinski, Greg Chen, Trevor Mudge, David Blaauw, Dennis Sylvester, "Cache memory system for a data processing apparatus," US patent 8,335,122, December 18, 2012.
15. David Fick, Ronald Dreslinski, Trevor Mudge, David Blaauw, and Dennis Sylvester, "Vertical interconnect patterns in multi-layer integrated circuits," US patent 8,381,155, February 19, 2013.
16. David Blaauw, Dennis Sylvester, David Fick, Stuart Biles, Michael Wieckowski, Scott Hanson, Gregory Chen, "Operating parameter control of an apparatus for processing data," US patent 8,407,025, March 26, 2013.
17. Greg Chen, Dennis Sylvester, and David Blaauw, "Integrated circuit memory power supply," US patent 8,526,261, September 3, 2013.
18. Sudhir Satpathy, David Blaauw, Trevor Mudge, Dennis Sylvester, "Crossbar circuitry for applying an adaptive priority scheme and method of operation of such crossbar circuitry," US patent 8,549,207, October 1, 2013.
19. Mingoo Seok, Dennis Sylvester, David Blaauw, Scott Hanson, and Gregory Chen, "Reference voltage generator having a two transistor design," US patent 8,564,275, October 22, 2013.
20. Sudhir Satpathy, David Blaauw, Dennis Sylvester, "Apparatus and method for transferring a data signal propagated along a bidirectional communication path within a data processing apparatus," US patent 8,713,232, April 29, 2014.

Students

Ph.D. committees chaired:

Name	**Project Area**	**Graduation/Status**
Kanak Agarwal	On-chip interconnect modeling	2004 (IBM)
Himanshu Kaul	Global signaling strategies for nanometer VLSI	2004 (Intel)
Ashish Srivastava	Statistical CAD tools for low power	2005 (Synopsys)
Sarvesh Kulkarni	Multi-voltage CAD and design	2006 (Intel)
Matt Guthaus	On-chip clock network optimization (co-chair)	2006 (UC-Santa Cruz)
Harmander Singh	Robust low-power design techniques	2006 (Intel)
Youngmin Kim	Exploiting design-process interactions	2007 (UNIST-Korea)
Saumil Shah	Parametric yield optimization tools	2007 (Synopsys)
Jie Yang	Design for manufacturability	2007 (Apple)
Eric Karl	Dynamic reliability management (co-chair)	2008 (Intel)
Yu-Shiang Lin	Ultra-low energy communication/computation	2008 (IBM)
Scott Hanson	Circuits for cubic millimeter computing	2008 (Ambiq Micro)
Jae-Sun Seo	Circuits for fast on-chip global signaling	2009 (Arizona St Univ)
Vineeth Veetil	Fast Monte Carlo-based statistical CAD	2010 (Applovin Corp)
Mingoo Seok	Extreme power-constrained IC design	2010 (Columbia)
Greg Chen	Millimeter-scale sensing systems	2011 (Intel)
Vivek Joshi	Variability-driven CAD	2011 (GLOBALFOUNDRIES)
Daeyeon Kim	Robust low-voltage memories	2012 (Intel)
Eric Marsman	Low power microcontrollers (co-chair)	2012 (Isocline)
Dave Fick	3D energy efficient computing (co-chair)	2012 (Isocline)
Matthew Fojtik	Adaptive error-correcting circuit design	2013 (Nvidia)
M. Hassan Ghaed	Wireless communication in implantable devices	2013 (Analog Devices)
Dongsuk Jeon	Energy efficient signal processing for VLSI	Candidate (expected 09/14)
Gyouho Kim	CMOS imaging in sensor nodes (co-chair)	Candidate (expected 08/14)
Yen-Po Chen	Low power analog building blocks	Pre-candidate (expected 05/15)
Suyoung Bang	Power management at nW scale	Pre-candidate (expected 05/15)
Laura Freyman	Low power embedded non-volatile memory	Pre-candidate (expected 05/16)
Seok Hyeon Jeong	Ultra-low power timers	Pre-candidate (expected 05/16)
Sechang Oh	Capacitance-to-digital conversion	Pre-candidate (expected 05/16)
Kaiyuan Yang	Circuits for security applications	Pre-candidate (expected 05/17)
Myungjoon Choi	Low power mixed-signal building blocks	Pre-candidate (expected 05/17)
Qing Dong	TBD	Pre-candidate (expected 05/18)
Yiqun Zhang	TBD	Pre-candidate (expected 05/18)
Jingcheng Wang	TBD	Pre-candidate (expected 05/19)

M.S. students supervised:

Robert Bai	Level-converting flip-flops for dual-Vdd CMOS	2003 (UBS bank)
Tejasvi Kachru	Statistical timing analysis of sequential elements	2006 (AMD)
Michelle Chang	Fast CAD algorithms using multi-processing	2010 (Peak6)

Mahmood Barangi	Low-power analog/digital conversion	2011
Allan Wang	Fast voltage level conversion (co-chair)	2014

Ph.D. committees served on:

Hongtao Zhong	Multicore processing for single threaded apps	Candidate
Sujay Phadke	Heterogeneous memory design	Candidate
Inhee Lee	Power management circuits for sensor nodes	Candidate
Dongmin Yoon	Low power analog circuits for wireless sensing	Candidate
Puneet Gupta	Design-manufacturing interface	2006 (University of California, San Diego)
Bulusu Anand	DTMOS for scaled low-voltage circuits	2006 (External examiner, Indian Institute of Tech., Bombay)
Ahmed Youssef	Power management for microprocessors	2008 (External examiner, University of Waterloo)
Javid Jaffari	Statistical timing analysis	2010 (External examiner, University of Waterloo)
Do Anh Tuan	Low voltage SRAM	2010 (External examiner, Nanyang Technological University)
Dandan Chen	Receivers for optical communication systems	2011 (External examiner, Nanyang Technological University)
Xiang Yi	mm-wave CMOS PLLs	2013 (External examiner, Nanyang Technological University)
Stevan Vlaovic	x86 microarchitecture performance simulation	2002
Mikhail Smelyanskiy	Approaches to efficient software pipelining	2003
Koushik Das	Robust low-power circuits in PD-SOI	2003
Nam Sung Kim	Low-power cache architecture and design	2004
Conrad Zeisler	Energy recovering pipelines	2004
Saurabh Adya	Algorithms for VLSI layout design	2004
Rahul Rao	Low-power SOI VLSI design	2004
Erik Hallnor	Advanced cache architectures	2004
Aseem Agarwal	Statistical static timing analysis	2005
David Oehmke	Novel register file architectures	2005
Daniel Ernst	Virtual global communication	2005
Dongwoo Lee	Leakage current analysis and reduction	2005
R. Venkatasubramanium	Fault detection in wireless networks	2005
Alan Drake	Local resonant clocking for low-power	2005
Jay Sivagnaname	Pseudo-NMOS SOI circuit design	2005
Leyla Nazhandali	Architecture for sensor networks	2006
Allen Cheng	Application specific instruction sets	2006
Jia-Yi Chen	Low-power wireless transceivers	2006

Rajeev Rao	Uncertainty-aware CAD tools	2006
Sunghyun Park	High-speed analog/digital converters	2006
Maher Mneimneh	Microprocessor verification	2006
Michael Geiger	Region-based caching	2006
Rajiv Ravindran	Compiler-driven memory power optimization	2007
Yoonna Oh	Constructive logic and layout synthesis	2007
Bo Zhai	Ultra-low power processors and memories	2007
Mini Nanua	Circuit modeling for signal integrity	2007
Taeho Kgil	Energy efficient servers using 3D integration	2007
Robert Senger	Micropower ASIC design techniques	2007
Sanjay Pant	On-chip power distribution networks	2008
Junyoung Park	High-speed CMOS serial links	2008
Jeff Ringenberg	Benchmarking for future microarchitectures	2008
Mark Ferriss	Low-power transmitters for sensor networks	2008
Debbie Marr	Simultaneous multithreading microarchitectures	2008
Stephen Plaza	Hierarchical logic synthesis and verification	2008
Kaviraj Chopra	Statistical CAD: Analysis and optimization	2008
Yuan Lin	Software-defined radio	2008
Smita Krishnaswamy	Design and test of logic circuits under uncertainty	2008
Carlos Tokunaga	Circuit design for security applications	2008
Jaeyoung Kang	Successive-approximation ADCs	2008
Shidhartha Das	Variation-tolerant circuit design	2009
Ali Saidi	Full-system critical path analysis	2009
Shahrzad Naraghi	Analog/digital converters	2009
Jarrod Roy	Placement and routing in nanometer CMOS	2009
Ravi Gandikota	Crosstalk noise analysis in VLSI	2009
Lisa Hsu	Cache resource allocation in multiprocessors	2009
Chun Chieh Lee	Low-power analog/digital converters	2009
Brian Cline	Design for manufacturability	2010
David Papa	Physical synthesis tools	2010
Cheng Zhuo	CAD for reliability	2010
David Roberts	Fault-tolerant architectures	2010
Geoffrey Blake	Transactional memory	2011
Rach Liu	Integrated circuits for security	2011
Amir Hormati	Compilers for streaming applications	2011
Youngmin Park	Synthesizing analog/RF designs	2011
Prashant Singh	Reliability monitoring for nanoscale CMOS	2011
Ron Dreslinski	Low power microarchitecture	2011
Razi ul-Haque	Implantable microsystem design	2011
Dongjin Lee	Clock network optimization	2011
Wei-Hsiang Ma	Resonant clocking	2011

Sudhir Satpathy	High-performance crossbar interconnect	2012
Yoonmyung Lee	Ultra-low power circuits for mm^3 systems	2012
Biju Edamana	Control strategies for micro-robots	2012
Korey Sewell	Architectures for network processors	2012
Jonathan Brown	Receivers for wireless sensor nodes	2012
Jorge Pernillo	High-speed analog/digital converters	2012
Seunghyun Oh	Wireless body area networks	2013
Kuo-Ken Huang	Low power radios	2013
Bharan Giridhar	High performance circuits and SRAM	2014

Postdoctoral scholars supervised:

Dr. Mike Wieckowski	Low-voltage memory and voltage regulators	2007-2010
Dr. Scott Hanson	Ultra-low power microcontrollers	2009-2010
Dr. David Fick	Energy efficient VLSI design	2012 - present
Dr. M. Khayatzadeh	Error resilient circuits	2013 - present

Professional and Honor Societies

- Fellow, Institute of Electrical and Electronics Engineers (IEEE)
- Member, Association for Computing Machinery (ACM)
- Member, Eta Kappa Nu (HKN)

Publications

h-index = 57, total citations = 10613 (Google Scholar, May 2014)

Books and book chapters

1. A. Srivastava, D. Sylvester, and D. Blaauw, *Statistical Analysis and Optimization for VLSI: Timing and Power*, Springer Publishers, New York, 2005.
2. D. Lee, B. Zhai, D. Blaauw, and D. Sylvester, "Static leakage reduction through simultaneous Vt/Tox and state assignment," in *Ultra Low-Power Electronics and Design*, E. Macii, Ed. Kluwer Academic Publishers, Boston, 2004.
3. L. Stok, R. Puri, S. Bhattacharya, J. Cohn, D. Sylvester, A. Srivastava, and S.H. Kulkarni, "Pushing ASIC performance in a power envelope," in *Closing the Power Gap Between ASIC and Custom*, D. Chinnery and K. Keutzer, ed., Springer Publishers, New York, 2007.
4. S.H. Kulkarni, A. Srivastava, D. Sylvester, and D. Blaauw, "Power optimization techniques using multiple supply voltages," in *Closing the Power Gap Between ASIC and Custom*, D. Chinnery and K. Keutzer, ed., Springer Publishers, New York, 2007.

Journal publications

5. I. Kwon, S. Kim, D. Fick, M. Kim, Y-P. Chen, and D. Sylvester, "Razor-Lite: A lightweight register for error detection by observing virtual supply rails," accepted for publication in *IEEE Journal of Solid-State Circuits*.

6. S-H. Jeong, Z. Foo, Y. Lee, J-Y. Sim, D. Blaauw, and D. Sylvester, "A fully integrated 71nW CMOS temperature sensor for low power wireless sensor nodes," accepted for publication in *IEEE Journal of Solid-State Circuits*.
7. D. Jeon, M. Henry, Y. Kim, I. Lee, Z. Zhang, D. Blaauw, and D. Sylvester, "An energy efficient full-frame feature extraction accelerator with shift-latch FIFO in 28nm CMOS," accepted for publication in *IEEE Journal of Solid-State Circuits*.
8. Y-S. Park, D. Blaauw, D. Sylvester, and Z. Zhang, "Low-power high-throughput LDPC decoder using non-refresh embedded DRAM," accepted for publication in *IEEE Journal of Solid-State Circuits*.
9. Y. Lee, M. Seok, S. Hanson, D. Sylvester, and D. Blaauw, "Achieving ultra-low standby power with an efficient SCCMOS bias generator," accepted for publication in *IEEE Transactions on Circuits and Systems II*.
10. C-H. Chen, D. Blaauw, D. Sylvester, and Z. Zhang, "Design and evaluation of confidence-driven error-resilient systems," accepted for publication in *IEEE Transactions on VLSI Systems*.
11. M.H. Ghaed, G. Chen, R-ul. Haque, M. Wieckowski, Y. Kim, G. Kim, Y. Lee, I. Lee, D. Fick, D. Kim, M. Seok, K.D. Wise, D. Blaauw, and D. Sylvester, "Circuits for a cubic millimeter energy-autonomous wireless intraocular pressure monitor," *IEEE Transactions on Circuits and Systems I*, pp. 3152-3162, December 2013.
12. R.G. Dreslinski, D. Fick, B. Giridhar, G. Kim, S. Seo, M. Fojtik, S. Satpathy, Y. Lee, D. Kim, N. Liu, M. Wieckowski, G. Chen, D. Sylvester, D. Blaauw, and T. Mudge, "Centip3De: A many-core prototype exploring 3D integration and near-threshold computing," *Communications of the ACM*, pp. 97-104, November 2013.
13. Y. Lee, B. Giridhar, Z. Foo, D. Sylvester, and D. Blaauw, "A Sub-nW Multi-stage Temperature Compensated Timer for Ultra-Low-Power Sensor Nodes," *IEEE Journal of Solid-State Circuits*, pp. 2511-2521, October 2013.
14. N. Pinckney, R.G. Dreslinski, K. Sewell, D. Fick, T. Mudge, D. Sylvester, and D. Blaauw, "Limits of Parallelism and Boosting in Dim Silicon," *IEEE Micro*, pp. 30-37, Sept-Oct. 2013.
15. Y. Lee, D. Kim, J. Cai, I. Lauer, L. Chang, S.J. Koester, D. Blaauw, and D. Sylvester, "Low power circuit analysis and design based on heterojunction tunneling transistors (HETTs)," *IEEE Transactions on VLSI Systems*, pp. 1632-1643, Sept. 2013.
16. C. Zhuo, D. Sylvester, and D. Blaauw, "A statistical framework for post-fabrication oxide breakdown reliability prediction and management," *IEEE Transactions on Computer-Aided Design*, pp. 630-643, April 2013.
17. R. Dreslinski, D. Fick, B. Giridhar, G. Kim, S. Seo, M. Fojtik, S. Satpathy, Y. Lee, D. Kim, N. Liu, M. Wieckowski, G. Chen, D. Blaauw, D. Sylvester, T. Mudge, "Centip3De: A 64-Core, 3D Stacked, Near-Threshold System," *IEEE Micro*, pp. 8-16, March/April 2013.
18. M. Fojtik, D. Kim, G. Chen, Y-S. Lin, D. Fick, J. Park, M. Seok, M-T. Chen, Z. Foo, D. Blaauw, and D. Sylvester, "A millimeter-scale energy-autonomous sensor system with stacked battery and solar cells," *IEEE Journal of Solid-State Circuits*, pp. 801-813, March 2013.
19. Y. Lee, D. Yoon, Y. Kim, D. Blaauw, and D. Sylvester, "Circuit and system design guidelines for ultra-low power sensor nodes," *IPSJ Transactions on System LSI Design Methodology (T-SLDM)*, pp. 17-26, February 2013. **[invited paper]**
20. P. Gupta, Y. Agarwal, L. Dolecek, N. Dutt, R. Gupta, R. Kumar, S. Mitra, A. Nicolau, T. Simunic Rosing, M.B. Srivastava, S. Swanson, and D. Sylvester, "Underdesigned and opportunistic computing in presence of hardware variability," *IEEE Transactions on Computer-Aided Design*, pp. 8-23, January 2013 (**invited keynote article**).

21. M. Fojtik, D. Fick, Y. Kim, N. Pinckney, D. Harris, D. Blaauw, and D. Sylvester, "Bubble Razor: Eliminating timing margins in an ARM Cortex-M3 processor in 45nm CMOS using architecturally independent error detection and correction," *IEEE Journal of Solid-State Circuits*, pp. 66-81, January 2013.
22. D. Fick, R. Dreslinski, B. Giridhar, G. Kim, S. Seo, M. Fojtik, S. Satpathy, Y. Lee, D. Kim, N. Liu, M. Wieckowski, G. Chen, T. Mudge, D. Blaauw, and D. Sylvester, "Centip3De: A cluster-based NTC architecture with 64 ARM Cortex-M3 cores in 3D stacked 130nm CMOS," *IEEE Journal of Solid-State Circuits,* pp. 104-117, January 2013.
23. Y. Lee, G. Kim, S. Bang, Y. Kim, I. Lee, P. Dutta, D. Sylvester, and D. Blaauw, "A modular 1mm^3 Die-Stacked Sensing Platform with Low Power I^{2}C Inter-die Communication and Multi-Modal Energy Harvesting," *IEEE Journal of Solid-State Circuits,* pp. 229 - 243, January 2013.
24. D. Jeon, M. Seok, Z. Zhang, D. Blaauw, and D. Sylvester, "A design methodology for voltage overscaled ultra-low power systems," *IEEE Transactions on Circuits and Systems II*, pp. 952-956, December 2012.
25. M. Seok, G. Kim, D. Blaauw, and D. Sylvester, "A portable 2-transistor picowatt temperature-compensated voltage reference operating at 0.5V," *IEEE Journal of Solid-State Circuits*, pp. 2534-2545, October 2012.
26. P. Singh, E. Karl, D. Sylvester, and D. Blaauw, "Compact degradation sensors for monitoring NBTI and oxide degradation," *IEEE Transactions on VLSI Systems*, pp. 1645-1655, September 2012.
27. K. Sewell, R.G. Dreslinski, T. Manville, S. Satpathy, N. Pinckney, G. Blake, M. Cieslak, R. Das, T. Wenisch, D. Sylvester, D. Blaauw, and T. Mudge, "Swizzle-switch networks for many-core systems," *IEEE Journal on Emerging Topics in Circuits and Systems*, pp. 278-294, June 2012.
28. A. DeOrio, D. Fick, V. Bertacco, D. Sylvester, D. Blaauw, J. Hu, and G. Chen, "A reliable routing architecture and algorithm for NoCs," *IEEE Transactions on Computer-Aided Design*, pp. 726-739, May 2012.
29. M. Seok, S. Hanson, D. Blaauw, and D. Sylvester, "Sleep mode analysis and optimization with minimal-sized power gating switch for ultra-low Vdd operation," *IEEE Transactions on VLSI Systems*, pp. 605-615, April 2012.
30. D. Jeon, M. Seok, C. Chakrabarti, D. Blaauw, and D. Sylvester, "A super-pipelined energy efficient subthreshold 240MS/s FFT core in 65nm CMOS," *IEEE Journal on Solid-State Circuits*, pp. 23-34, January 2012.
31. J-S. Seo, D. Blaauw, and D. Sylvester, "Crosstalk-aware PWM-based on-chip links with self-calibration in 65nm CMOS," *IEEE Journal on Solid-State Circuits*, pp. 2041-2052, September 2011.
32. P. Singh, E. Karl, D. Sylvester, and D. Blaauw, "Dynamic NBTI management using a 45nm multi-degradation sensor," *IEEE Transactions on Circuits and Systems I*, pp. 2026-2037, September 2011.
33. C. Zhuo, K. Chopra, D. Sylvester, and D. Blaauw, "Process variation and temperature-aware full-chip oxide breakdown reliability analysis," *IEEE Transactions on Computer-Aided Design*, pp. 1321-1334, September 2011.
34. M. Seok, D. Blaauw, and D. Sylvester, "Robust clock network design methodology for ultra-low voltage operations," *IEEE Journal on Emerging Topics in Circuits and Systems*, pp. 120-130, June 2011. **[invited]**
35. V. Veetil, K. Chopra, D. Blaauw, and D. Sylvester, "Fast statistical static timing analysis using smart Monte Carlo techniques," *IEEE Transactions on Computer-Aided Design*, pp. 852-865, June 2011.

36. M. Seok, G. Chen, S. Hanson, M. Wieckowski, D. Blaauw, and D. Sylvester, "CAS-FEST 2010: Mitigating variability in near-threshold computing," *IEEE Journal on Emerging Topics in Circuits and Systems*, pp. 42-49, March 2011.
37. J-S. Seo, D. Sylvester, D. Blaauw, H. Kaul, and R. Krishnamurthy, "A robust edge encoding technique for energy-efficient multi-cycle interconnect," *IEEE Transactions on VLSI Systems*, pp. 264-273, February 2011.
38. G.K. Chen, S. Hanson, D. Blaauw, and D. Sylvester, "Circuit design advances for wireless sensing applications," *Proceedings of the IEEE*, pp. 1808-1827, December 2010. **[invited]**
39. G. Chen, D. Sylvester, D. Blaauw, and T. Mudge, "Yield-driven near-threshold SRAM design," *IEEE Transactions on VLSI Systems*, pp. 1590-1598, November 2010.
40. V. Joshi, B. Cline, D. Sylvester, D. Blaauw, and K. Agarwal, "Mechanical stress aware optimization for leakage power reduction," *IEEE Transactions on Computer-Aided Design*, pp. 722-736, May 2010.
41. S. Hanson, Z. Foo, D. Blaauw, and D. Sylvester, "A 0.5V sub-microwatt CMOS image sensor with pulse-width modulation read-out," *IEEE Journal of Solid-State Circuits*, pp. 759-767, April 2010.
42. R.G. Dreslinski, M. Wieckowski, D. Blaauw, D. Sylvester, and T. Mudge, "Near-threshold voltage scaling for energy optimal systems," *Proceedings of the IEEE*, pp. 253-266, February 2010. **[invited]**
43. R. Gandikota, K. Chopra, D. Blaauw, and D. Sylvester, "Victim alignment in crosstalk-aware timing analysis," *IEEE Transactions on Computer-Aided Design*, pp. 261-274, February 2010.
44. H. Singh, R.M. Rao, D. Sylvester, R. Brown, and K. Nowka, "Dynamically pulsed MTCMOS with bus encoding for total power and crosstalk minimization," *IEEE Transactions on VLSI Systems*, pp. 166-170, January 2010.
45. R.R. Rao, V. Joshi, D. Blaauw, and D. Sylvester, "Circuit optimization techniques to mitigate the effects of soft errors in combinational logic," *ACM Transactions on Design Automation of Electronic Systems*, pp. 5:1-5:27, December 2009.
46. P. Singh, C. Zhou, E. Karl, D. Blaauw, and D. Sylvester, "Sensor driven reliability and wearout management," *IEEE Design & Test of Computers*, pp. 40-49, Nov/Dec 2009. **[invited]**
47. B. Zhai, S. Pant, L. Nazhandali, S. Hanson, J. Olson, A. Reeves, M. Minuth, R. Helfand, T. Austin, D. Sylvester, and D. Blaauw, "Energy efficient subthreshold processor design," *IEEE Transactions on VLSI Systems*, pp. 1127-1137, August 2009. [top 25 downloaded manuscripts, TVLSI 2009]
48. Y. Kim, D. Petranovic, and D. Sylvester, "Simple and accurate models for capacitance increment due to metal fill insertion," *IEEE Transactions on VLSI Systems*, pp. 1166-1170, August 2009.
49. S. Hanson, M. Seok, Y-S. Lin, Z. Foo, D. Kim, Y. Lee, N. Liu, D. Sylvester, and D. Blaauw, "A low voltage processor for sensing applications with picowatt standby mode," *IEEE Journal of Solid-State Circuits*, pp. 1145-1155, April 2009.
50. Y-S. Lin, D. Sylvester, and D. Blaauw, "Alignment independent chip-to-chip communication for sensor applications using passive capacitive signaling," *IEEE Journal of Solid-State Circuits*, pp. 1156-1166, April 2009.
51. F. Albano, Y-S. Lin, D. Blaauw, D. Sylvester, K.D. Wise, and A.M. Sastry, "A fully integrated microbattery for an implantable microelectromechanical system," *Elsevier Journal of Power Sources*, 185 (2), pp.1524-1532, December 2008.
52. B. Zhai, S. Hanson, D. Blaauw, and D. Sylvester, "A variation-tolerant sub-200mV 6-T subthreshold SRAM," *IEEE Journal of Solid-State Circuits*, pp. 2338-2348, October 2008.
53. P. Singh, J-S. Seo, D. Blaauw, and D. Sylvester, "Self-timed regenerators for high-speed and low-power on-chip global interconnect," *IEEE Transactions on VLSI Systems*, pp. 673-677, June 2008.

54. D. Sylvester, K. Agarwal, and S. Shah, "Variability in nanometer CMOS: Impact, analysis, and minimization," *Integration, the VLSI Journal*, vol. 41, no. 3, pp. 319-339, May 2008. **[invited]**
55. S. Hanson, B. Zhai, M. Seok, B. Cline, K. Zhou, M. Singhal, M. Minuth, J. Olson, L. Nazhandali, T. Austin, D. Sylvester, and D. Blaauw, "Exploring variability and performance in a sub-200mV processor," *IEEE Journal of Solid-State Circuits*, pp. 881-891, April 2008.
56. E-H. Toh, G. H. Wang, L. Chan, D. Sylvester, C.-H. Heng, G. Samudra, and Y.-C. Yeo, "Device design and scalability of a double-gate tunneling field-effect transistor with silicon-germanium source," *Japanese Journal of Applied Physics*, vol. 47, no. 4, pp. 2593-2597, April 2008.
57. E. Karl, D. Blaauw, D. Sylvester, and T. Mudge, "Multi-mechanism reliability modeling and management in dynamic systems," *IEEE Transactions on VLSI Systems*, pp. 476-487, April 2008.
58. S.H. Kulkarni, D. Sylvester, and D. Blaauw, "Design time optimization of post-silicon tuned circuits using adaptive body bias," *IEEE Transactions on Computer-Aided Design*, pp. 481-494, March 2008.
59. A. Srivastava, K. Chopra, S. Shah, D. Sylvester, and D. Blaauw, "A novel approach to perform gate-level yield analysis and optimization considering correlated variations in power and performance," *IEEE Transactions on Computer-Aided Design*, pp. 272-285, February 2008.
60. S. Hanson, M. Seok, D. Sylvester, and D. Blaauw, "Nanometer device scaling in subthreshold logic and SRAM," *IEEE Transactions on Electron Devices*, pp. 175-185, January 2008.
61. J. Lin, E.-H. Toh, C. Shen, D. Sylvester, C-H. Heng, G. Samudra, and Y-C. Yeo, "Compact HSPICE model for IMOS device," *IET Electronics Letters*, vol. 44, no. 2, pp. 91-92, January 17 2008.
62. P. Gupta, A.B. Kahng, D. Sylvester, and J. Yang, "Performance-driven optical proximity correction for mask cost reduction," *SPIE Journal of Micro/Nanolithography, MEMS, and MOEMS (JM3)*, pp. 031005-1 – 031005-8, July-September 2007.
63. H. Singh, K. Agarwal, D. Sylvester, and K. Nowka, "Enhanced leakage reduction techniques using intermediate strength power gating," *IEEE Transactions on VLSI Systems*, pp. 1215-1224, November 2007. [top 25 downloaded manuscripts, TVLSI 2008]
64. P. Gupta, A.B. Kahng, Y. Kim, and D. Sylvester, "Self-compensating design for reduction of timing and leakage sensitivity to systematic pattern dependent variation," *IEEE Transactions on Computer-Aided Design*, pp. 1614-1624, September 2007.
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