Prof. Peide Peter Ye

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Journal Publications: >150
Total number of citation (without self-citation): >2400
H-index: 28

Prof. Peter Ye received his B. Sci. from Fudan University, Shanghai 1988, and Ph.D. from Max-Planck-Institute for Solid State Research, Stuttgart, Germany in 1996. He is currently a full professor in School of Electrical and Computer, Engineering, Purdue University, USA. His area of research includes Semiconductor physics and devices, Nano-structures and nano-fabrications, Quantum/spin-transport, Atomic layer deposition, High-k/III-V device integration, High-performance III-V MOSFETs, high-k/graphene integration, High-performance graphene FETs, Graphene spintronics.

Selected publications:

1. Fabrication of fully transparent nanowire transistors for transparent and flexible electronics By: Ju, Sanghyun; Facchetti, Antonio; Xuan, Yi; et al. NATURE NANOTECHNOLOGY Volume: 2 Issue: 6 Pages: 378-384 Published: JUN 2007
No. of Citation: 248

2. High-performance inversion-type enhancement-mode InGaAs MOSFET with maximum drain current exceeding 1 A/mm, By: Xuan, Y.; Wu, Y. Q.; Ye, P. D. IEEE ELECTRON DEVICE LETTERS Volume: 29 Issue: 4 Pages: 294-296 Published: APR 2008
No. of Citation: 184

3. GaN metal-oxide-semiconductor high-electron-mobility-transistor with atomic layer deposited Al2O3 as gate dielectric By: Ye, PD; Yang, B; Ng, KK; et al. APPLIED PHYSICS LETTERS Volume: 86 Issue: 6 Article Number: 063501 Published: FEB 7 2005
No. of Citation: 164

4. High performance submicron inversion-type enhancement-mode InGaAs MOSFETs with ALD Al(2)O(3), HfO(2), and HfAlO as gate dielectrics By: Xuan, Y.; Wu, Y. Q.; Shen, T.; et al. Book Group Author(s): IEEE Conference: IEEE International Electron Devices Meeting Location: Washington, DC Date: DEC 10-12, 2007 Sponsor(s): IEEE 2007 IEEE INTERNATIONAL ELECTRON DEVICES MEETING, VOLS 1 AND 2 Book Series: International Electron Devices Meeting Pages: 637-640 Published: 2007

No. of Citation: 125

5. Top-gated graphene field-effect-transistors formed by decomposition of SiC By: Wu, Y. Q.; Ye, P. D.; Capano, M. A.; et al. APPLIED PHYSICS LETTERS Volume: 92 Issue: 9 Article Number: 092102 Published: MAR 3 2008
No. of Citation: 118

6. Submicrometer inversion-type enhancement-mode InGaAs MOSFET with atomic-layer-deposited Al2O3 as gate dielectric By: Xuan, Y.; Wu, Y. Q.; Lin, H. C.; et al. IEEE ELECTRON DEVICE LETTERS Volume: 28 Issue: 11 Pages: 935-938 Published: NOV 2007,
No. of Citation: 112

7. Capacitance-voltage studies on enhancement-mode InGaAs metal-oxide-semiconductor field-effect transistor using atomic-layer-deposited Al2O3 gate dielectric By: Xuan, Y; Lin, HC; Ye, PD; et al. APPLIED PHYSICS LETTERS Volume: 88 Issue: 26 Article Number: 263518 Published: JUN 26 2006
No. of Citation: 100

8. Atomic-layer-deposited nanostructures for graphene-based nanoelectronics By: Xuan, Y.; Wu, Y. Q.; Shen, T.; et al. APPLIED PHYSICS LETTERS Volume: 92 Issue: 1 Article Number: 013101 Published: JAN 7 2008
No. of Citation: 80

9. Main determinants for III-V metal-oxide-semiconductor field-effect transistors (invited) By: Ye, Peide D. Conference: 54th AVS International Symposium and Exhibition Location: Seattle, WA Date: OCT 14-19, 2007 Sponsor(s): AVS JOURNAL OF VACUUM SCIENCE & TECHNOLOGY A Volume: 26 Issue: 4 Pages: 697-704 Published: JUL-AUG 2008
No. of Citation: 78

10. Channel Length Scaling of MoS2 MOSFETs By: Liu, Han; Neal, Adam T.; Ye, Peide D. ACS NANO Volume: 6 Issue: 10 Pages: 8563-8569 Published: OCT 2012
No. of Citation: 68