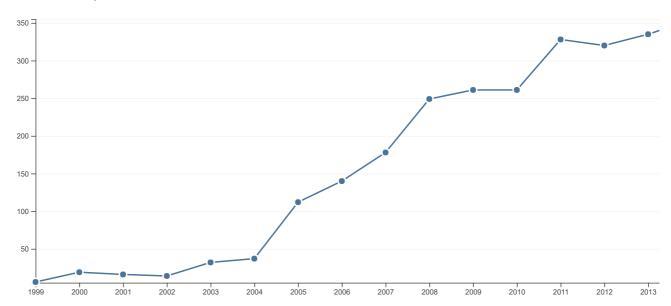


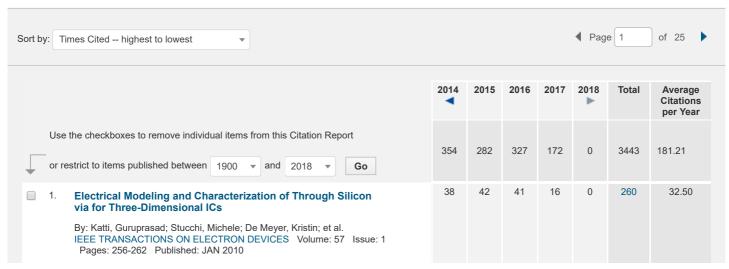


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	2.	Analysis of the parasitic S/D resistance in multiple-gate FETs								
		By: Dixit, A; Kottantharayil, A; Collaert, N; et al. IEEE TRANSACTIONS ON ELECTRON DEVICES Volume: 52 Issue: 6 Pages: 1132-1140 Published: JUN 2005	16	13	20	11	0	215	16.54	
	3.	VARIOT: A novel multilayer tunnel barrier concept, for low-voltage nonvolatile memory devices								
		By: Govoreanu, B; Blomme, P; Rosmeulen, M; et al. IEEE ELECTRON DEVICE LETTERS Volume: 24 Issue: 2 Pages: 99-101 Published: FEB 2003	11	5	3	2	0	136	9.07	
	4.	Influence of device engineering on the analog and RF performances of SOI MOSFETs								
		By: Kilchytska, V; Neve, A; Vancaillie, L; et al. IEEE TRANSACTIONS ON ELECTRON DEVICES Volume: 50 Issue: 3 Pages: 577-588 Published: MAR 2003	15	10	14	8	0	114	7.60	
	5.	Direct and Indirect Band-to-Band Tunneling in Germanium- Based TFETs								
		By: Kao, Kuo-Hsing; Verhulst, Anne S.; Vandenberghe, William G.; et al. IEEE TRANSACTIONS ON ELECTRON DEVICES Volume: 59 Issue: 2 Pages: 292-301 Published: FEB 2012	20	24	24	16	0	110	18.33	
	6.	Passivation of Ge(100)/GeO2/high-kappa gate stacks using thermal oxide treatments								
		By: Bellenger, F.; Houssa, M.; Delabie, A.; et al. JOURNAL OF THE ELECTROCHEMICAL SOCIETY Volume: 155 Issue: 2 Pages: G33-G38 Published: 2008	9	5	5	3	0	104	10.40	
- 7	7.	Record I-ON/I-OFF performance for 65nm Ge pMOSFET and novel Si passivation scheme for improved EOT scalability								
		By: Mitard, J.; De Jaeger, B.; Leys, F. E.; et al. Book Group Author(s): IEEE Conference: IEEE International Electron Devices Meeting Location: San Francisco, CA Date: DEC 15-17, 2008 Sponsor(s): IEEE Electron Devices Soc IEEE INTERNATIONAL ELECTRON DEVICES MEETING 2008, TECHNICAL DIGEST Book Series: International Electron Devices Meeting Pages: 873-+ Published: 2008	10	5	8	1	0	95	9.50	
= 8	8.	Impact of line-edge roughness on FinFET matching performance								
		By: Baravelli, Ernanuele; Dixit, Abhisek; Rooyackers, Rita; et al. IEEE TRANSACTIONS ON ELECTRON DEVICES Volume: 54 Issue: 9 Pages: 2466-2474 Published: SEP 2007	8	4	4	7	0	86	7.82	
	9.	FinFET analogue characterization from DC to 110 GHz By: Lederer, D; Kilchytska, V; Rudenko, T; et al.								
		Conference: 1st EUROSOI Workshop Location: Granada, SPAIN Date: JAN 19-21, 2005 Sponsor(s): EUROSOI SOLID-STATE ELECTRONICS Volume: 49 Issue: 9 Pages: 1488-1496 Published: SEP 2005	6	3	4	0	0	71	5.46	
	10.	Analysis of leakage currents and impact on off-state power consumption for CMOS technology in the 100-nm regime								
		By: Henson, WK; Yang, N; Kubicek, S; et al. IEEE TRANSACTIONS ON ELECTRON DEVICES Volume: 47 Issue: 7 Pages: 1393-1400 Published: JUL 2000	5	1	1	0	0	56	3.11	
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