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Publication

Journal Papers

1. C-M Chang and J-T Wu, "A 95-dBA DR Digital Audio Class-D Amplifier Using a Calibrated Digital-to-Pulse Converter," *IEEE Transactions on Circuits and Systems - I: Regular Papers,* Vol. 64, No. 5, pp. 1106-1117, May 2017. [PDF]
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5. Y Chai and J-T Wu, "A CMOS 5.37-mW 10-Bit 200-MS/s Dual-Path Pipelined ADC," *IEEE Journal of Solid-State Circuits,* Vol. 47, No. 12,, pp. 2905-2915, Dec. 2012. [PDF]
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11. C-W Fan and J-T Wu, "Jitter Measurement and Compensation for Analog-to-Digital Converters," *IEEE Transactions on Instrumentation and Measurement,* Vol. 58, No. 11, pp. 3874-3884, Nov. 2009. [PDF]
12. C-Y Wang and J-T Wu, "A Multiphase Timing-Skew Calibration Technique Using Zero-Crossing Detection," *IEEE Transactions on Circuits and Systems - I: Regular Papers,* Vol. 56, No. 6, pp. 1102-1114, June 2009. [PDF]
13. Z-M Lee, C-Y Wang, and J-T Wu, "A CMOS 15-bit 125-MS/s Time-Interleaved ADC With Digital Background Calibration," *IEEE Journal of Solid-State Circuits,* Vol. 42, No. 10, pp. 2149-2160, Oct. 2007. [PDF]
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1. C-M Chang and J-T Wu, "A Computationally-Efficient PWM Technique for Digital Class-D Amplifiers," *2016 IEEE International Symposium on Circuits and Systems,* pp. 1946-1949, May 2016. [PDF]
2. S-H Wu and J-T Wu, "Background Calibration of Integrator Leakage in Discrete-Time Delta-Sigma Modulators," *The 11th IEEE New Circuits and Systems Conference,* pp. 1-4, June 2013. [PDF]
3. C-L Chang and J-T Wu, "A 1-V 100-dB Dynamic Range 24.4-kHz Bandwidth Delta-Sigma Modulator," *2013 IEEE International Symposium on Circuits and Systems,* pp. 813-816, May 2013. [PDF]
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13. H-C Liu, Z-M Lee, and J-T Wu, "A 15-Bit 20MS/s CMOS Pipelined ADC with Digital Background Calibration," *2004 IEEE International Solid-State Circuits Conference,* pp. 454-455, Feb. 2004. [PDF]
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