




Yuan Taur

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Semiconductor device design expert who specializes in the structure and physics of transistors.

The computer revolution has been powered by unrelenting success at shrinking transistors, the most basic of microcircuit devices. Scientists now are attempting to engineer transistors with features sized between 10 and 100 nanometers. This nanoscale realm is the focus of Professor Taur's research. As dimensions shrink to a few atomic lengths or less, new fundamental physical challenges loom. When insulating layers become too thin, they can be penetrated by electrons practicing "quantum-mechanical tunneling." Unwanted standby power can be generated by electron thermal energy, which is another target of Taur's research. He is looking at how to stop leakage caused when electrons, powered only by ambient heat, hop barriers. Refrigeration or so-called low temperature CMOS is one solution, but a less costly approach that Taur is studying involves use of a double-gate structure to apply the controlling electric fields. Taur is also exploring the new physics of heat dissipation in the deepest of submicron designs. As size drops, the lattice structure of a semiconductor is less able to transfer heat, threatening the performance of high speed devices. Taur can shed light on most questions involving transistor physics, including conventional CMOS transistors, BiCMOS, SOI, or silicon on insulator, and related structural issues of today's state-of-the-art VLSI or Very Large Scale Integrated circuits.

Capsule Bio:

Yuan Taur came to UCSD's Jacobs School in 2001, after 20 years at IBM's T.J. Watson Research Center, where he was recipient of numerous invention and achievement awards. He is an IEEE fellow, Editor-in-Chief of IEEE Electron Device Letters, co-author of "Fundamentals of Modern VLSI Devices," and a holder of 13 U.S. patents. He received his Ph.D. in Physics in 1974 from UC Berkeley.

Selected Publications:

Google Scholar Publications

Web Page: <http://fleece.ucsd.edu/~taur/>