Short Biography of Pinaki Mazumder

Professor Pinaki Mazumder received his PhD in Electrical and Computer Engineering from the University of Illinois at Urbana-Champaign in 1988. Prior to that, he received his MS degree in Computer Science from University of Alberta in Canada, BS degree in Electrical Engineering from Indian Institute of Science at Bangalore, and BSc Physics Honors degree from Guwahati University in India. Currently, he is a Professor of Electrical Engineering and Computer Science at the University of Michigan where he has been teaching for the past 25 years. He spent 3 years at National Science Foundation serving as the lead Program Director of Emerging Models and Technologies Program in the CISE Directorate as well as leading the Quantum, Molecular and High Performance Simulation Program in the Engineering Directorate. He had worked for 6 years in industrial R&D laboratories which included AT&T Bell Laboratories in USA and Bharat Electronics Ltd. in India. Professor Mazumder spent his sabbatical at Stanford University, University of California at Berkeley, and NTT Center Research Laboratory in Japan. He has published over 260 technical papers and 4 books on various aspects of VLSI technology and systems. His research interest includes CMOS VLSI design, semiconductor memory systems, CAD tools and circuit designs for emerging technologies including quantum MOS, spintronics, plasmonics, and resonant tunneling devices.

Professor Mazumder's inventions in testable DRAM circuits, in-line accelerated testing procedures for high-density RAM chips, and testing of embedded ROM and SRAM through JEDEC boundary scan ports are widely used by memory and FPGA manufacturers. His research in biology-inspired VLSI layout synthesis, self-healing VLSI design and self-repairable memory compilers has made commercial impact. In revolutionary emerging technologies, Professor Mazumder has made sustained impact for the past 20 years by collaborating with multiple leading researchers in universities and companies. His research group has developed a Quantum SPICE simulator to design several innovative quantum tunneling based circuits that were fabricated by many US companies. Prof. Mazumder was a recipient of Digital's Incentives for Excellence Award, BF Goodrich National Collegiate Invention Award, and DARPA Research Excellence Award. Prof. Mazumder is an AAAS Fellow (2007) and an IEEE Fellow (1999) for his distinguished contributions to the field of VLSI.

PINAKI MAZUMDER[1]

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I. Visa Status

U.S. Citizen (from 1995); Permanent Resident (1989-1995).

II. Educational Qualification

Ph.D. in Computer Engineering	University of Illinois, Urbana-Champaign	1988
M. Sc. in Computer Science	University of Alberta, Edmonton, Canada	1985
B.S. in Electrical Engineering	Indian Institute of Science, Bangalore, India	1976

I also received a degree in B.Sc. Physics Honors securing the first rank in Gauhati University, India amongst estimated 100,000 students in all disciplines of liberal arts and basic sciences.

III. Work Experience

US Government (National Science Foundation):

2007-2008	Program Director for Emerging Models and Technologies Program (funding areas: Nanoelectronics, Quantum Computing, and Biologically Inspired Computing with an annual budget of $18 Million) in the Directorate for Computer and Information and Science and Engineering, National Science Foundation, Arlington, Virginia.
2009	Program Director in Electrical, Communications and Cyber Systems Division (funding areas: Quantum, Molecular and High Performance Computing, Adaptive Intelligent Systems, Electronic and Photonic Devices, and Major Research Instrumentation) of the Engineering Directorate at National Science Foundation.

Academic Teaching and Research:

1998- to date	Tenured Professor, Division of Computer Science and Engineering, Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, Michigan.
1996-1997	Research Fellow, Division of Electrical and Computer Engineering, Department of Electrical Engineering and Computer Science, University of California, Berkeley, California.
1996-1997	Visiting Associate Professor, Department of Computer Science and Engineering, Stanford University, Palo Alto, California.
1997 (Summer)	Visiting Professor, NTT Research Laboratories, Atsugi-shi, Japan.

[1] Fellow of AAAS, Fellow of IEEE, Member of Sigma Xi, and Member of Phi Kappa Phi

1992-1998	Tenured Associate Professor, Division of Computer Science and Engineering, Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, Michigan.
1987-1992	Assistant Professor, Division of Computer Science and Engineering, Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, Michigan.
1985-1987	Graduate Student Research Assistant, University of Illinois at Urbana-Champaign, Illinois.
1982-1984	Teaching Assistant at University of Alberta, Edmonton, Canada.
1974-1975	Undergraduate Research Assistant at Indian Institute of Science, Bangalore.

Industrial Research and Development:

1985, 1986 (Summer)	Member of Technical Staff, AT&T Bell Laboratories, Indian Hill, Chicago, Illinois.
1976-1982	Senior R&D Engineer, Bharat Electronics Ltd., Bangalore, India.

IV. Research Interest

Disruptive nanoarchitectures, modeling and simulation tools for nano-scale devices; Nanoscale CMOS VLSI system design issues; VLSI testing and fault-tolerance methodologies; and VLSI layout automation algorithms

V. Awards

- Fellow of American Association for the Advancement in Science (AAAS), 2007 for "distinguished contributions to the field of very large scale integrated (VLSI) systems". The honor of being elected a Fellow of AAAS is given to those whose "efforts on behalf of the advancement of science or its applications are scientifically or socially distinguished."
- Fellow of IEEE, 1999 for "contributions to the field of VLSI Design."
- IEEE Distinguished Lecturer
- Digital Equipment Corporation Faculty Award: Excellence in Research
- Departmental Research Excellence Award (1995), The University of Michigan
- BF Goodrich National Collegiate Invention Award
- DARPA Research Excellence Award for the work in Quantum MOS Project
- Best Undergraduate Student Medal
- IETE Best Student Paper Award, and IETE Best Paper Presentation Award
- NSF Research Initiation Award
- Bell Northern Research Laboratory Faculty Development Grant
- Commendation Letter from the Dean of College of Engineering, University of Michigan, for Excellence in Teaching
- Member, Sigma Xi
- Member, Phi Kappa Phi
- US Patent on Digital Logic Design Using Negative Differential Resistance Diodes and Field-Effect Transistors, US Patent No. 5903170, awarded on May 11, 1999.
- US Patent on High-speed, Compact, Edge-Triggered Flip-Flop Circuit Topologies Using NDR Diodes and FET's, US Patent No. 6,323,709, awarded on Nov. 21, 2001.
- US and International Patents on Method and Apparatus to Improve Noise Tolerance of Dynamic Circuits, US Patent No. 7,088,143, awarded on Aug. 8, 2006.
- Two US Patents are under review and one patent application is now being prepared for filing.

VI. Research Funding

1. National Science Foundation (RIA): $69,948; 1988 – 1991 (Single PI)
2. Bell Northern Research Laboratory: $20,900; 1988 – 1989 (Single PI)
3. National Science Foundation: $90,620; 1989 – 1990 (Single PI)
4. Digital Equipment Corporation: $180,000; 1989 – 1992 (Single PI)
5. Office of Naval Research: $420,000; 1988 - 1991, (Co-PI)
6. National Science Foundation: $125,000; 1991 – 1993 (Single PI)
7. Rackham Faculty Research Grant: $9,980; 1991 – 1993 (Single PI)
8. U.R.I. Program (US Army): $6,000,000 (total); $250,000 (my portion); 1988 - 1992
9. General Motors: $20,000; 1992 – 1992 (Single PI)
10. International Business Machines: $45,000 (student fellowship); 1990 – 1993
11. National Science Foundation: $47,000; 1992 – 1993 (Single PI)
12. Hewlett Packard: $81,400; 1993 – 1995 (Single PI)
13. Office of Vice President Research: $52,300; 1995 - 1996
14. Defense Advanced Research Projects Agency (DARPA): $825,000; 1993 -1997 (Co-PI)
15. National Science Foundation: $182,400; 1994 – 1998 (Single PI)
16. U.R.I. Program (US Army): $5,000,000; $200,000; 1993 - 1997
17. State of Michigan Display Technology Center: $2,000,000; My portion: $200,000; 1995 - 1998
18. Texas Instruments (subcontract of a DARPA project): $304,000; 1995 – 1998 (Single PI)
19. Army Research Office's MURI-95 (Co-PI with 7 others): $4,000,000; 1995-2000 + 1 year.
20. Army Research Office's MURI-96 (Co-PI with 13 others): $5,000,000; 1996-2001 + 1 year.
21. Defense Advanced Research Projects Agency: $750,000; June 1997- May 2000 (PI)
22. National Science Foundation: $300,000; 1998 – 2002 (Single PI)
23. Nippon Electric Company, Japan: $40,000; 1998 (Single PI)
24. National Science Foundation: $195,000; 1998 – 2002 (Single PI)
25. Hughes Research Laboratory (Office of Naval Research project); $270,000; 1998-2001 (Single PI)
26. NanoLogic Inc. $10,000; 1999-2000 (Single PI)
27. Air Force Office of Scientific Research: $5,000,000: 2001-2006 (Co-PI with 9 other investigators)
28. Office of Naval Research: $303,000: 2001-2002; (Single PI)
29. National Science Foundation: $210,000: 2001-2004 (Single PI)
30. Korean Government Nanoelectronics Research: $200,000: 2001-2002 (PI: Prof. G.I. Haddad).
31. Office of Naval Research: $820,000: 2002-2005 (PI)
32. Tera-Level Nanoelectronics Project, Korean Government: $170,000: 2003-2006; (Single PI)
33. National Science Foundation: $120,000: 2004-2007 (Single PI)
34. Air Force Office of Scientific Research, $480,000: 2006-2009 (Single PI)
35. National Science Foundation IPA Assignment Grant: $620,000; 2007-2009 (Single PI)
36. DARPA SyNAPSE Program on Brain Plasticity: $807,812; Co-PI: Hughes Research Laboratory
37. National Science Foundation, NIRT: **$1,000,000**: 2006-2012 (Co-PI).
38. SRC NRI Center (MIND): **~$200,000**: 2008-2011 (Single PI)
39. National Science Foundation: EAGER Grant, **$200,000**; 2009-2012. (Single PI)
40. National Science Foundation**: $400,281**; 2010-2014. (Single PI)
41. Army Research Office: **$580,000**; 2010-2013. (Single PI)
42. National Science Foundation: **$149,111**; 2011-2012. (Single PI)
43. Army Research Office, MURI: **$6,500,000**; 2010-2015. (Co-PI)
44. National Science Foundation: **$400,415**; 2011-2014. (Single PI)
45. National Science Foundation**: $1,750,000**; 2011-2015. (Co-PI)

46. Defense Advanced Research Projects Agency (DARPA): **$150,000;** 2011-2013 (Single PI)
47. Air Force Office of Scientific Research: **$449,772;** 2012-2015 (Single PI)
48. National Science Foundation: **$480,000**; 2012-2015 (Co-PI)

In the above list, the Active research grants are indicated in Bold (#37-#47).
Summary of Research Grants:

Individual portion of **active** grants = **$3,258,579 + $300,000** (gift grants).
Total individual portion of all grants awarded till to date = **$10,460,127** without the IPA grant
Total individual portion of all grants awarded = **$11, 080,127** with NSF IPA grant
Total of all active grants including portions of all collaborators = **$12,229,772**
Total of all grants awarded so far including portions of all collaborators > **$40,000,000**

Pending Proposals:

1. Expeditions for Computing: Foundation for Integrative Research on Storage Technologies, National Science Foundation, $10,000,000 (multiple universities). (PI)
2. STDP CMOS and Memristor-Based Neurodynamic Programming Design for Sensorimotor Neuromorphic Systems, National Science Foundation, $3,000,000 (with Duke Univ.). (PI)
3. Network for Computational Nanotechnology - NEEDS Node, National Science Foundation, $3,500,000. (with multiple universities) (Co-PI)
4. Nanoarchitectures for Adaptive Control and Intelligence Processing Chips, Office of Naval Research, $450,000 (PI).

VII. Consulting Activities

1. Served as ***Expert*** for the US National Science Foundation, Arlington, Virginia.
2. Served as a member of ***Technical Advisory Board*** for. Sequence Design Automation (Santa Clara, CA), Silicon Value Inc. (Jerusalem, Israel), and Tioga Technology (San Jose, CA).
3. Served as ***Advisor and Expert Witness*** in 5 lawsuits involving DRAM, SRAM, Flash, and FPGA.
4. Served as ***Consultant*** for several semiconductor companies in the areas of DRAM, SRAM, and Flash memories; radiation hardening and soft-error problems in SRAM, DRAM and FPGA's; JTAG testing of FPGA's; ultra-low-power CMOS circuits; nanoelectronic circuits and simulation tools.

VIII. Committees and Professional Activities

1. Member of Board of Editors, *Proceedings of the IEEE*
2. Associate Editor, *IEEE Transactions on VLSI Systems*, 1997-2000
3. Guest Editor, *IEEE Transactions on VLSI Systems* - A Special Issue on Impact of Emerging Technologies on VLSI Systems, December 1997
4. Guest Editor (with Prof. A. Seabaugh), *Proceedings of the IEEE* - A Special Issue on Nanoelectronic Devices and Circuits, June 1998
5. Guest Editor (with Prof. A. Benso and Prof. Y. Makris), *IEEE Transaction on Computer* – A Special Issue on Chips and Architectures for Emerging Technologies and Applications, June 2008

6. Guest Editor, *Journal of Electronic Testing - Theory and Application* - A Special Issue on Multi-megabit Memory Testing, April 1994
7. Guest Editor (with Prof. J.P. Hayes), *IEEE Design & Test Magazine* - A Special Issue on Memory Testing, 1993
8. Editorial Advisory Board, *The Arabian Journal for Science and Engineering*, King Fahd University of Petroleum and Minerals, Saudi Arabia.
9. Council of Editors, *International Society for Genetic and Evolutionary Computation* (ISGEC)
10. As lead NSF Program Director, organized the Emerging Models and Technology Workshop on Bio-Inspired Computing and Bio-Computing at Princeton University on July 24-25, 2008.
11. As lead NSF Program Director, organized the EMT Workshop on Nanoelectronics on October 29-30, 2007.
12. As lead NSF Program Director, held the EMT Workshop on Quantum Information Science and Engineering on September 10-11, 2007.
13. Member, University of Michigan Research Policies Committee of Senate Assembly, 2002-05.
14. Member, Electrical Engineering and Computer Science Curriculum Committee, 2002-03.
15. Member, Electrical Engineering and Computer Science DCO Committee, 2002-03.
16. Member, Computer Science and Engineering Graduate Curriculum Committee, 1988-89, 1998-00, 2002-06.
17. Counselor, Computer Engineering Undergraduate Students, 1990-95.
18. Member, Computer Science and Engineering Graduate Admission Committee, 1995-96.
19. Member, IEEE Standards Subcommittee for Semiconductor Memories, 1989-90.
20. Member, IEEE Test Technologies Committee
21. Member, IEEE VLSI Technical Committee
22. General Chair, 2007 High Performance Computing (HPC) for Nanotechnology
23. General Chair, 1999 IEEE Great Lakes VLSI Conference
24. Program Committee, 1992 Fault-Tolerant Computing Symposium Workshop
25. Program Committee, 1992 IEEE Defects and Fault Tolerance Workshop
26. Program Committee, 1993 IEEE Intl. Conference on Memory Testing
27. Program Committee, 1994 IEEE Intl. Conference on Memory Testing
28. Program Committee, 1994 IEEE Asian Testing Symposium
29. Program Committee, 2000 IEEE Great Lakes VLSI Conference
30. Serving on organizing committee for Department of Defense Nano Conference, 2009
31. Served regularly on NSF panels in Engineering and CISE Directorates
32. Proposals Reviewed for: US National Science Foundation, The Israel Science Foundation, Louisiana University Board of Regents, and US Army Research Office, New Jersey Center for Science and Technology, Saudi Arabia King Fahd University Research Foundation, and private venture capitalist firms.

IX. Professional Experience

Details of My Professional Accomplishments

***US Government at National Science Foundation* (3 years)**

In 2007 and 2008, I worked as the lead Program Director for Emerging Models and Technologies (EMT) program in the Division of Computing and Communication Foundations (having about $140 Million annual budget) of the Directorate for Computer and Information and Science and Engineering, National Science Foundation, Arlington, Virginia. My mandate was to manage research grants in Nanoelectronic Modeling and Systems, Quantum Computing, and Biologically Inspired Computing for which I had an operating annual budget of about $18 Million. Additionally, I participated in several NSF cross-cutting programs such as Cyber-Enabled Discovery

and Innovation (CDI), Expeditions in Computing, Major Research Instrumentation (MRI), Computing Research Infrastructure (CRI) and Cyber Physical Systems (CPS). In 2009, I worked as a Program Director in the Engineering Directorate where I managed research in three broad areas: Adaptive Intelligent Systems (Machine Learning), Quantum, Molecular and High-Performance Modeling, and Electronic and Photonic Devices. During these three years, I interacted with several program managers and administrators of NSF, DARPA, ARO, ONR, and AFOSR to help launch national-level major research initiatives. I consider that serving the US government for a stint of three years has provided me an exceptional opportunity to acquire a vast amount of knowledge in various fields of science and engineering, to network with numerous researchers around the nation, and to gain divergent administrative experience.

Teaching Experience **(24 years)**

Since 1988, I have been working as a professor at the Department of Electrical Engineering and Computer Science of the University of Michigan, Ann Arbor, Michigan.

Graduate courses developed and taught: 1) VLSI System Design, 2) Optimization and Synthesis of VLSI Layout, 3) Testing of Digital Circuits and Systems, 4) Advanced Computer Architectures, 5) Nanocircuits and Nanoarchitectures, and 6) Ultra-Low-Power Subthreshold CMOS Circuits.

Undergraduate courses upgraded and taught: 1) Introduction to Digital Logic Design (sophomore level), 2) Digital Integrated Circuit Design (junior level), and 3) VLSI System Design (senior level).

Industrial Experience **(6.5 years)**

After my baccalaureate degrees in Physics and Electrical Engineering, I worked for six years (1976-1982) as a Senior R&D Engineer at Bharat Electronics Ltd. (BEL) in its Integrated Circuits Division. I designed several bipolar and CMOS analog and digital integrated circuits for consumer electronic systems. I was associated with the following chip development projects: i) Raster-scan vertical deflection system microchip for TV display, ii) Sync processing and horizontal deflection system microchip for TV display, iii) Video and audio IF stage IC's for vestigial-AM and FM signal detection in TV receiver, iv) High-gain audio amplifier microchip for TV audio stage, v) Tape Recorder IC with automatic gain adjustments, vi) Hearing-aid IC, vii) Analog clock driver IC, and viii) LCD and AC Plasma display drive IC's. Several million commercial chips were fabricated based on these designs.

After finishing my MSc degree in Computer Science and while working towards my PhD degree in Electrical and Computer Engineering, I worked during the summers of 1985 and 1986 as a Member of Technical Staff at AT&T Bell Laboratories. I was one of the two engineers who started the Bell Laboratory *Cones/Spruce* project - a new behavioral synthesis and layout automation tool for rapid prototyping of digital circuits. The main contribution of this effort was to demonstrate how a restricted version of C language could be used to model digital hardware much before commercial hardware description language (HDL) software tools like Verilog and System C were designed.

X. List of Courses Taken During M.Sc. (in CS) and Ph.D. (in CE) Study

My BS degrees were in Physics Honors and Electrical Engineering, while my MSc and PhD degrees were in CS and CE, respectively. I took the following CS and CE courses while doing my MSc and PhD:

1) Analysis of Algorithms, 2) Artificial Intelligence, 3) Computer Networks, 4) Computer Architecture, 5) Software Engineering, 6) Local Area Networks, 7) Adaptive Systems, 8) VLSI Complexity Theory, 9) Switching Theory and Digital Logic Design, 10) Parallel Computer Architectures, 11) Minicomputer System Architecture, 12) VLSI Layout Automation and Circuit Simulation, 13) VLSI System Design, 14) AI Based CAD for VLSI, 15) Digital Testing and Fault Tolerance, and 16) Programming Languages.

M.Sc. Thesis Title: ***Networks and Embedding Aspects of Cellular Structures for On-Chip Parallel Processing in VLSI,*** *University of Alberta, Canada, 1985. Synopsis:* The thesis presented an asymptotic model to estimate the area, delay, and reliability performance metrics of multi-core parallel processing VLSI chips. Through a comparative theoretical analysis, the thesis demonstrated that two-dimensional meshes and torus class of interconnect topologies are superior for on-chip parallel processing to more powerful interconnection topologies such as perfect shuffle networks, cube connected cycles, and X-trees which perform slowly due to dilatation of wires when mapped onto VLSI chips. The thesis provides a few algorithmic models to bind the dilatations of wire lengths to retain the square shape of processor layouts. Finally, the thesis introduced novel cellular embedding layout methodologies for multi-core parallel processors by applying the chromatic plane ornamentation theory. This theoretically motivated research was performed almost 20 years before the commercial adoption of VLSI multi-core processors that are now dominating the microprocessor market. The research work resulted in 3 archival journal papers, 3 conference papers, and a section (on asymptotic modeling of VLSI interconnect networks) in a textbook, titled *Parallel Processing Architectures and VLSI Hardware*, Prentice Hall, 1989 by A. L. De CeGama.

NB: I also applied the theory of cellular embedding I developed in my MSc thesis to find planar and 3-D topologies that can be recursively decomposed to yield quad-tree and oct-tree data structures in spatial data query processing for computer vision, tomography, cartography, and gridded image processing.

Ph.D. Thesis Title: ***Testing and Fault-Tolerance Aspects of High-Density Random-Access Memory,*** *University of Illinois at Urbana-Champaign, 1988. Synopsis:* The thesis introduced the "line-mode plurality testing technique" for high-density DRAM and CAM chips. Based on this design-for-testability approach, fast parallel testing algorithms were developed for testing a broad class of parametric and pattern-sensitive faults. The resulting test procedures are significantly more efficient than previous approaches due to test length optimization by applying the chromatic plane ornamentation theory. In many embedded memory applications where neither the input address and read/write lines are externally controllable nor are the output lines directly observable, the proposed algorithms can be adapted for implementing deterministic built-in self-test (BIST) circuits by designing the read/write sequences through Hamiltonian tours on the hypercube graph. Also, the thesis presented an extensive amount of Markov modeling and probabilistic analysis in order to determine the lengths of randomly applied test patterns for various classes of functional faults in scattered and small embedded memories where the proposed deterministic BIST technique cannot be incorporated. Finally, the thesis addressed the improvement of storage reliability by two to three orders of magnitude by introducing a new on-chip error correcting (ECC) technique capable of correcting the double-bit errors due to alpha particles striking between the 3-D vertically integrated trench DRAM cells. The thesis also analyzed the limitations of popular types of double-bit ECC techniques like the Projective Geometry Code in VLSI applications. The research resulted in 6 archival journal papers, 6 conference papers, and several chapters in two books on semiconductor memories coauthored by me (see the Publications section).

NB: Even though when the thesis was written in 1987 the DRAM chip size was merely 256 Kilo bit and the proposed "line-mode plurality testing technique" was not necessary, the proposed method has been widely adopted by memory chip manufacturers in multi-Mega and Giga-bit DRAM chips in order to reduce the memory chip testing time by a significant margin (nearly a thousand times).

XI. Student Theses Supervised

Ph.D. Theses Completed

1. J. Yih, *"Built-In Self-Repair of Embedded Memory and Logic Arrays,"* 1990. Currently at IBM T. J. Watson Research Center, Yorktown, New York.
2. K. Shahookar, *"Genetic Algorithms for CAD Layout Problems,"* 1994. Currently at his start-up company.
3. H. Esbensen, *"Application of Genetic Algorithms for Cell Placement and Routing Problems,"* 1994. Currently at Avant! Fremont, California.
4. V. Ramachandran, *"Parallel Architectures for Multilayer Wire Routing Problems,"* 1994. Currently at Cadence Design Systems, San Jose, California.
5. S. Mohan, *"Design of Ultra-fast Digital Circuits using Quantum Electronic Devices,"* Dec. 1994. Currently at Xilinx Corporation, Campbell, California.
6. K. Chakraborty, *"Built-In Self-Repairable RAM Compiler Design,"* Mar. 1997. Currently at Agere Design, Murray Hills, New Jersey.
7. M. Bhattacharya, *"Simulation and Emulation of Digital Integrated Circuits Containing Resonant Tunneling Diodes,"* Oct 1999. Currently at Avant! Fremont, California.
8. S. Kulkarni, *"Quantum MOS Circuits and Systems,"* Oct 1999. Working in IDT, Atlanta, Georgia.
9. A. Gonzalez, *"Multiple-Valued Logic and High-Speed Digital Circuits Using Resonant Tunneling Diodes,"* June 2001. Currently at IDT, Atlanta, Georgia.
10. Li Ding, *"Dynamic Noise Analysis in Deep Sub-micron CMOS VLSI Systems,"* Feb. 2004. Currently at Synopsis, Sunnyvale, California.
11. Q. W. Xu, *"Accurate Interconnect Modeling for Efficient Transient Simulation in VLSI Chip Design,"* May 2006, currently at Cadence Design Systems.
12. B. Wang, *"Accelerated Chip-level Thermal Analysis Using Multilayer Green's Function,"* May 2008, currently at VmWare.
13. W. H. Lee, *"Applications of Nanoelectronic Technology to Image Processors, Velocity-Tuned Filters and Crossbar Memories"*, Dec 2008, currently at Intel.
14. K. Song, *"Applications of Surface Plasmon Polariton Plasmonic Devices,"* Aug. 2010, currently working as a Research Scientist, University of Michigan.
15. I. Ebong, *"Training Memristors for Reliable Computation,"* Dec. 2012, currently working as a Research Scientist, University of Michigan.

M.S. Theses/Projects Completed:

16. B. Brighton, *Pseudo-Random Testing for Embedded Memories*
17. K. Quasim, *Analog Circuit Testing*
18. J. Kapson, *Parallel CAD Architecture*

19. D. Berryman, *Parallel Processing for VLSI Routing*
20. M. Smith, *Self-Repairable Memory Array Using Digital Neural Circuit*
21. E. Chan, *RTD-based Multi-valued Circuit Design*
22. A. Arunachalam, *Fine-Grained Parallel Routing*
23. A. Gonzalez, *Multi-valued Adder Design Using CMOS and RTD*
24. A. Gupta, *Self-Repairable ROM Generator*
25. J. Xiong, *Quantum MOS Circuit Design*
26. G. Mittal, *Simultaneous Switching Noise Analysis in Embedded Memories*
27. V. Warraich, *Web-based Applets Design for Digital Logic*
28. M. Kumshikar, *Amorphous TFT-based Driver Logic Design for AMLCD Panel*
29. G. Shankar, *Amorphous TFT-based Operational Amplifier Design for AMLCD Panel*
30. V. Ramachandran, *Array Machine for VLSI Routing*
31. S. Mohan, *Parametric Testing for SRAM's Using GaAs High Electron Mobility Transistors*
32. S. Kulkarni, *CMOS and RTD-based Correlators Design*
33. K. Shahookar, *Genetic Algorithm for VLSI Placement*
34. H. Chan, *Macro-cell Placement Using Genetic Algorithm*
35. L. Ding, *Noises in Deep Sub-micron VLSI Chips*
36. Q. W. Xu, *VLSI Interconnect Modeling Using Differential Quadrature Method*
37. B. Wang, *3-Dimensional Full Chip Simulation by Transmission Line Matrix Method*
38. H. Zhang, *Ultra-fast RTD-based Circuit Design*
39. S.R. Li, *RTD-based Cellular Nonlinear Networks*
40. D. Shi, *Quantum Dot Based Image Processing*
41. M. Rajagopal, *Modeling of Resonant Tunneling Diodes*
42. W. Lee, *Image Processing Applications of Quantum Dots*
43. E. Ibong, *Subthreshold Low-power Operational Amplifier Design*
44. K. Song, *Plasmonics Applications in VLSI*
45. C. Ting, *Modeling of Ionic Current through Memristors*
46. Y. Yilmar, *Straintronics Pipelined Adder Design*
47. J. Qian, *Green Function based Thermal Modeling*
48. H. Liu, *Straintronics SRAM Design*

Number of Doctoral Students Currently Being Supervised: 8.

Names of Visiting Scientists (8):

Dr. Ueymura, NEC, Japan; Prof. Choi, Hanyang University, South Korea; Mr. H. Esbensen, Aarhus University, Denmark.; Dr. Q. W. Xu, China; UK; Dr. J. P. Sun, JT University, China and Prof. S. Duan, South East University, China; Mr. T. Glotzner, Germany; Mr. P. Kelly, Ulster University, Ireland.

XII. Publications

Books and Book Chapters

Books

1. P. Mazumder and K. Chakraborty, "Testing and Testable Design of Random-Access Memories", ***Kluwer Academic Publishers***, 1996 (428 pages).

2. P. Mazumder and E. Rudnick, "Genetic Algorithms for VLSI Layout and Test Automation", ***Prentice Hall***, 1999 (460 pages).

3. K. Chakraborty and P. Mazumder, "Fault Tolerance and Reliability Aspects of Random-Access Memories," ***Prentice Hall***, 2002. (440 pages).

4. P. Mazumder, "Introduction to Digital Systems", Video Book on DVD, produced at MGM Studio (Orlando, Florida), ***Laureate Education, Inc.,*** 2005.

5. P. Mazumder, "Models and Techniques for VLSI Routing", ***Springer Verlag***, (under preparation)

6. R. Rajasuman (Editor) and P. Mazumder (Editor), "Semiconductor Memories: Testing and Reliability", ***Computer Science Press***, May 1998.

7. R. J. Lomax (Editor) and P. Mazumder (Editor), "Great Lakes Symposium on VLSI, 1999", ***Computer Science Press***, March 1999.

8. P. Mazumder and K. Shahookar, "MathGuru Tutorial" for K-12 Education Software.

Book Chapters

9. K. Shahookar and P. Mazumder, "Standard Cell Placement and the Genetic Algorithm", Book chapter in "Advances in Computer-Aided Engineering Design, Vol. II", I. N. Hajj (editor), ***Jai Press***, Greenwich, Connecticut, 1990, pp. 159-234.

10. W. K. Fuchs, M. F. Chang, S. Y. Kuo, P. Mazumder and C. B. Stunkel, "The Impact of Parallel Architecture Granularity on Yield", Book chapter in "Designing for Yield," Moore, Strowjas and Maly (editors), ***Adam Hilger Publisher***, 1988.

11. P. Mazumder and J. H. Patel, "Parallel Testing of Parametric Faults in DRAM", in "Advanced Research in VLSI: Design and Applications of Very Large Scale Systems", Leighton and Allen (editors**),** ***MIT Press***, 1988. (Presented at the 5-th Massachusetts Institute of Technology Conference on VLSI).

12. P. Mazumder, "Design of a Fault-Tolerant DRAM with New On-Chip ECC", Book Chapter in "Defects and Fault Tolerance in VLSI Systems", I. Koren (editor), ***Plenum Press***, 1989.

13. H. Chan and P. Mazumder, "A Systolic Architecture for High-Speed Hyper-graph Partitioning Using a Genetic Algorithm", Book Chapter in "Progress in Evolutionary Computation", Vol. 956**,** ***Springer- Verlag***, Heildelberg, 1995, pp. 109-126.

Reviewed Journal Publications

Cataloging of Journal Publications

1. *Semiconductor Memory Systems* - Papers: 14, 15, 16, 17, 18, 19, 20, 21, 22, 28, 30, 36, 44, 81, 96
2. *Quantum Tunneling Circuits and CAD Tools* - Papers: 33, 35, 36, 37, 38, 39, 47, 48, 49, 53, 70, 97, 99, 100, 102, 103
3. *VLSI Circuit Optimization Techniques* - Papers: 74, 79, 80, 84
4. *Bio-Inspired Computing* - Papers: 57, 62, 64, 65, 69, 92, 93
5. *Reliable VLSI Systems Design* - Papers: 23, 24, 25, 26, 27, 28, 31, 34, 75, 77, 78
6. *Plasmonics and THz Bio-Sensing* - 86, 88, 89, 90, 91, 98, 101
7. *Quantum Physics and VLSI Synergies* - Papers: 40, 41, 42, 45, 50, 51, 76, 84, 85, 87, 92, 93, 94, 95, 99
8. *EM Theory and VLSI Synergies* - Papers: 71, 72, 73, 82, 83, 91, 98, 101
9. *Innovative VLSI Chip and System Design* - Papers: 29, 32, 46, 52, 54, 55, 56, 58, 59, 67, 97
10. *VLSI Complexity Issues* - Papers: 43, 60, 61, 63, 66, 68

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(Generally these conferences have acceptance ratio between 15% and 35% and they require rigorous review of full paper before the decision on a paper is made. The following papers are mostly 4 or more published pages in the proceedings).

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Workshop Presentations

1. P. Mazumder, "Neuromorphic Applications of Memristors," ***Memristor Symposium,*** University of California at Berkeley, Feb 2010. (See the oral presentation in YouTube at http://www.youtube.com/watch?v=h7cX_m5IKxk).

2. P. Mazumder,"Memristor Based Circuit Design," ***DARPA Defense Science Research Conference***, Santa Clara, May. 2009. **(Invited)**

3. P. Mazumder, "Beyond CMOS and Evolutionary Architectures," ***Memristor Symposium***, University of California at Berkeley, Nov. 2008. **(Invited)**

4. P. Mazumder, "Plasmonics for Digital Logic Design," ***SRC-NRI Meeting,*** South bend, August 2010.

5. P. Mazumder,"Quantum circuits and CAD tools design ," ***Proceedings on SRC Nanoelectronics Symposium*** , Aug. 2005. **(Invited)**

6. P. Mazumder, "Quantum Tunneling Based Nanoscale Memories," ***A-STAR Research Laboratories workshop***, Singapore, Oct. 2009.

7. P. Mazumder, "CAD Tools Design for Surface Plasmon Polariton Based Systems", ***AFOSR MURI Review***, November 2007, Boston.

8. P. Mazumder, "Q-MOS Circuit Design Techniques and Future Prospects of Q-MOS," ***SRC Nanoelectronic Workshop***, Dec. 1999. Raytheon-TI, Dallas, Apr. 1998. (**Invited**).

9. P. Mazumder, "Visual Computing by Mesoscopic and Nanoscale Systems," ***National Nanoelectronics Initiative Workshop***, Organized Jointly by NNCO, NSF, ONR, AFOSR and DARPA, February 2004. (**Invited**)

10. P. Mazumder, "Beyond Moore's Law and CMOS Technology", ***Technology Vision -- Mad Scientist Conference***, ***US Army,*** Norfolk, August 2008.

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13. P. Mazumder, "Quantum Dot Based Cellular Image Processing: Theory and design," ***IEEE Workshop on Cellular Nonlinear Networks***, July, Budapest, Hungary (**Invited**).

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21. P. Mazumder, "Ultra-fast Circuit Design with NDR Devices," ***Advanced Research Project Agency: Ultra Project***, Santa Fe, Oct. 1994.

22. P. Mazumder, "Built-in Self-repair using Electronic Neural Networks," ***Advanced Research Project Agency: Neural Network Project***, San Diego, Nov. 1994.

23. P. Mazumder, "Ultra-fast Circuit Design with NDR Devices***," Defense Advanced Research Project Agency***, Estes Park, Colorado, 1998.

24. P. Mazumder, "Q-MOS Circuit Design," ***Defense Advanced Research Project Agency***, Raytheon, Dallas, 1999.

25. P. Mazumder, "RTD Circuit Design***," Office of Naval Research***, Ann Arbor, 1998.

26. P. Mazumder, "Ultra-fast Circuit Design with NDR Devices," ***Defense Advanced Research Project Agency***, Santa Fe, Oct. 1997.

27. P. Mazumder, "Q-MOS Circuit Design," ***Defense Advanced Research Project Agency***, Raytheon-TI, Dallas, Apr. 1998.

28. W. Wang, J. P. Sun, N. Gu, and P. Mazumder, "Gate Current Simulation of High-k Stack Nanoscale MOSFETs," ***IEEE Computer Society Annual Symposium on VLSI,*** Brazil, 2007.

Technical Reports

29. P. Mazumder and J. H. Patel, "Parallel Testing of Pattern-Sensitive Faults in Random-Access Memory," *Technical Report CSG-56, Coordinated Science Laboratory,* Aug. 1986.

30. P. Mazumder, "Networks and Embedding Aspects of Hyper-cellular Structures for On-Chip Parallel Processing," *M. Sc. Thesis, Department of Computer Science, University of Alberta,* 1985.

31. P. Mazumder and J. H. Patel, "Testable RAM Design," *SRC Corporate Research,* 1986 Annual Report.

32. P. Mazumder, "Testing and Fault-Tolerant Aspects of High-Density VLSI Memory," *Ph.D. Thesis, Coordinated Science Laboratory,* Aug. 1987.

33. P. Mazumder "On-Chip Double-Error-Correction Coding Circuit for Three-Dimensional DRAM's," *CRL-TR-05-88, Technical Report, Department of Electrical Engineering and Computer Science, University of Michigan,* Ann Arbor, Apr. 1988.

34. A. Chakravarthy and P. Mazumder, "Gate Matrix Layout Techniques," *CSE-TR-12-90, Technical Report, Department of Electrical Engineering and Computer Science, University of Michigan,* Ann Arbor, 1990.

35. R. Venkateswaran and P. Mazumder, "Hexagonal Array Machine for Multi-Layer Wire Routing," *CSE-TR-52-90, Technical Report, Department of Electrical Engineering and Computer Science, University of Michigan,* Ann Arbor, 1990.

36. R. Venkateswaran and P. Mazumder, "On Restructuring of Hexagonal Arrays," *CSE-TR-72-90, Technical Report, Department of Electrical Engineering and Computer Science, University of Michigan,* Ann Arbor, 1990.

37. K. Shahookar and P. Mazumder, "VLSI Cell Placement Techniques," *CRL-TR-07-88, Technical Report, Department of Electrical Engineering and Computer Science, University of Michigan,* Ann Arbor, Aug. 1988.

38. P. Mazumder, "CPLA - A Software Tool That Automatically Generates "C"-Model for PLA's," *Bell Laboratories Technical Memorandum, 55612-1A-262,* Aug. 1985.

39. P. Mazumder, "Placement Algorithms for CONES," *Bell Laboratories Technical Memorandum, 55612-1F-210,* Aug. 1986.

40. P. Mazumder, "Automatic Integrated Circuit Synthesizer: Generates PLA Layout from Behavioral Description Written in C Language," *Bell Laboratories Technical Memorandum, 55612-1A-262,* Aug. 1985.

Publications in Industry (during 1976-1982)

Mixed Signal Analog and Digital VLSI Chip Design

Published over ***fifteen*** technical papers and application ideas while working at the Bharat Electronics Ltd. Topics included

- An Integrated Circuit Design for the Raster-Scan Vertical Deflection System.

- An Integrated Circuit Design for the Sync Processing Circuit
- Integrated Chip Set for Laser Range Finder in Military Applications
- An Integrated Circuit Design for High-Gain Pre-Amplifier with Automatic Level Controller
- A Integrated Circuit Design for Hearing-Aid Amplifier
- An Integrated Circuit Design for Quadrant Detection and Amplification of Frequency-Multiplexed Voice Signal
- A Large-Scale Integrated Circuit Design for Stepper-Motor-Driven Analog Clock Chip
- Study of Failure Modes in CMOS ICs During Handling
- Leakage-Current-Based Fault Characterization in a Non-planar Gas Discharge Display
- IC Design Considerations in Fabrication of Large Planar Plasma Display
- Application Notes on Analog and Digital Circuits

All these articles were published in ***BEL Application Notes*** and ***BEL Technical Report***.

XIII. Book Reviews

1. J.V. Oldfield, J.P. Gray, T.A. Kean, and R.C. Dorf, "Field-Programmable Gate Arrays for Implementation and Rapid Prototyping of Digital Systems", ***John Wiley and Sons, Inc***., New York.
2. J. Beetam, "Computer Architectures", ***Aksen Associates Inc. Publishers,*** California.
3. "The Science and Technology of Microelectronic Processing", ***Saunders College Publishing***, Pennsylvania.
4. D. Pradhan, "Fault-Tolerant System Design", ***Prentice Hall***, New Jersey.
5. Price, "Introduction to VLSI Design", ***Prentice Hall,*** New Jersey.
6. C.P. Ravi Kumar, "Computer-Aided Design for VLSI Systems", ***Kluwer Academic Publishers,*** Massachusetts.
7. Fu, "Neural Networks in Computer Intelligence", ***Prentice Hall,*** New Jersey.
8. P. Banerjee, "Parallel Algorithms for VLSI Computer-Aided Design Applications", ***Prentice Hall,*** New Jersey.
9. R. Karri, "Automatic Synthesis of Fault-tolerant VLSI Systems", ***Kluwer Academic Publishers,*** Massachusetts.
10. A. S. Sedra and K. C. Smith, "SPICE Simulation: Microelectronics Circuits", ***Prentice Hall.***
11. A. B. Marcovitz, "Introduction to Logic Design," ***McGraw Hill.***
12. N. Jha and S. Gupta, "Testing of Digital Systems," ***Cambridge Press.***

XIV. Technical Presentations (excluding conferences and workshops)

At Industries and National Laboratories

Formal Talks

1. Quantum electronic circuit design at ***Intel Corporation***, Santa Clara, California.
2. Quantum electronic circuit design at ***Samsung,*** Korea
3. Quantum electronic circuit design at ***Nippon Telegraph and Telephone***, Atsugi-shi, Japan.

4. Quantum electronic circuit design at ***Silicon Value***, Jerusalem, Israel.
5. Quantum electronic circuit design ***at Fraunhofer Institute***, Freiburg, Germany.
6. Quantum electronic circuit design at ***A-STAR Research Laboratories,*** Singapore
7. Quantum electronic circuit design at ***Hitachi Central Research Laboratories***, Kokubunji, Japan.
8. Quantum electronic circuit design at ***NEC Corporation***, Tsukuba, Ibaraki, Japan.
9. Quantum electronic circuit design at ***Fujitsu***, Morinosato-Wakamiya, Japan.
10. Quantum electronic circuit design at ***Texas Instruments***, Dallas, Texas.
11. Quantum electronic circuit design at ***Hughes Research Laboratories***, Los Angeles, California.
12. Memory testing at ***Nippon Telegraph and Telephone***, Atsugi-shi, Japan.
13. Memory testing at ***Digital Equipment Corporation***, Hudson, Massachusetts
14. Memory testing at ***Fujitsu***, Morinosato-Wakamiya, Japan.
15. Memory testing at ***Intel***, Santa Clara, California
16. Memory testing at ***Hitachi Central Research Laboratories***, Kokubunji, Japan.
17. Memory testing at ***AT&T Bell Laboratories***, Murray Hill, New Jersey.
18. Memory testing at ***Bell Northern Research Laboratories***, Ottawa, Canada
19. Embedded memory compilation at ***Synopsys,*** Palo Alto, California.
20. Embedded memory compilation at ***Neo-Magic Corporation***, Santa Clara, California.
21. Embedded memory compilation at ***Ambit Design Systems***, Santa Clara, California.
22. Memory testing at ***Micron Technology***, Boise, Idaho.
23. Memory testing at ***MCC***, Austin, Texas
24. Memory testing at ***Texas Instruments***, Bangalore, India.
25. Memory testing at ***AT&T Bell Laboratories***, Holmdel, New Jersey.
26. VLSI chip testing at ***ERIM Research Laboratory***, Ann Arbor, Michigan.
27. VLSI layout techniques at ***Nippon Telegraph and Telephone***, Atsugi-shi, Japan.
28. VLSI layout techniques at ***General Motors Research***, Warren, Michigan.
29. VLSI layout techniques at ***Bell Northern Research Laboratories***, Ann Arbor, Michigan.
30. VLSI layout techniques at ***Cypress Semiconductor***, Santa Clara, California
31. VLSI layout techniques at ***National Semiconductor***, Santa Clara, California
32. Built-in self-repairable IC design at ***Nippon Electric Company***, Princeton, New Jersey.
33. Built-in self-repairable IC design at ***Bell Communications Research***, Morris Town, New Jersey.
34. Built-in self-repairable IC design at ***Ford Motors Company***, Dearborn, Michigan.
35. Built-in self-repairable IC design at ***Nippon Telegraph and Telephone***, Atsugi-shi, Japan.
36. Research activities on circuit design at ***IBM Watson Research Center***, New York.
37. Research activities on circuit design at ***Hitachi Development Laboratories***, Mobarra, Japan.
38. Research activities on circuit design at ***David Sarnoff Research Center***, Princeton, New Jersey.
39. Research activities on circuit design at ***NEC Central Research*** Laboratories, Kanagawa, Japan.
40. Quantum electronic circuit design at ***Sun Microsystems,*** Sunnyvale, California
41. Dynamic noise analysis methodology for VLSI design at ***Sun Microsystems***, Mountainview, California
42. Dynamic noise analysis methodology for VLSI design at ***Sequent Design Automation***, San Jose, California
43. Quantum electronic circuit design at ***AMD,*** Sunnyvale, California
44. Memory testing at ***Texas Instruments***, Houston, Texas.
45. Embedded memory testing at ***Logic Vision***, San Jose, California.
46. VLSI layout techniques at ***Avant!,*** Fremont, California.
47. VLSI layout techniques at ***International Business Machine***, Fishkill, New York.

48. Memory testing at ***LSI Logic***, Milpitas, California.
49. VLSI chip layouts at ***Xilinx***, Inc., San Jose, California.
50. Built-in self-repairable design at ***Phillips Laboratories***, Kirtland, New Mexico.
51. Built-in self-repairable design at ***Altera Corporation,*** San Jose, California.

Formal Talks at Universities

52. Multilayer VLSI routing techniques at ***University of California***, Berkeley, California.
53. Memory testing at ***Stanford University***, Palo Alto, California.
54. Beyond CMOS technologies and evolutionary architectures at ***California Institute of Technology***, Pasadena.
55. Beyond CMOS technologies and evolutionary architectures at ***Columbia University***, New York.
56. Quantum electronic circuit design at ***University of Illinois***, Urbana-Champaign, Illinois.
57. Quantum electronic circuit design at ***University of California***, Berkeley, California.
58. Quantum electronic circuit design at ***Seoul National University***, Seoul, Korea.
59. Quantum electronic circuit design at ***Beijing University***, Beijing, China.
60. Quantum electronic circuit design at ***Gerhard-Mercater University***, Duisburg, Germany.
61. Quantum electronic circuit design at ***University of Santiago***, Spain
62. VLSI layout design at ***Princeton University***, Princeton, New Jersey.
63. Memory testing at ***Purdue University***, West Lafayette, Indiana.
64. Memory testing at ***University of Southern California***, Los Angeles, California.
65. Built-in self-repairable IC design at ***University of Iowa***, Iowa City, Iowa.
66. Memory testing at ***King Fahd University***, Saudi Arabia.
67. Quantum electronic circuit design at ***Nanjing University,*** Nanjing, China
68. Memory testing at ***Johns Hopkins University***, Baltimore, Maryland.
69. Quantum electronic circuit design at ***Ohio State University***, Columbus, Ohio
70. Memory testing at ***University of Minnesota***, Minneapolis, Minnesota.
71. Quantum electronic circuit design at ***University of Tokyo***, Tokyo, Japan.
72. Quantum electronic circuit design at ***Delft Technological University***, Delft, Netherlands.
73. Quantum electronic circuit design at ***King Fahd University***, Saudi Arabia.
74. Quantum electronic circuit design at ***Universidad de Las Palmas de Gran Canaries***, Spain.
75. Quantum electronic circuit design at ***South East University,*** Nanjing, China
76. Memory testing and repair algorithms at ***Indian Institute of Technology***, New Delhi, India.
77. Memory testing at ***Texas A&M University***, College Station, Texas.
78. Quantum electronic circuit design at ***Northwestern University***, Evanston, Illinois
79. Built-in self-repairable IC design at ***Wayne State University***, Detroit, Michigan.
80. VLSI layout design at ***Indian Institute of Science***, Bangalore, India.
81. Quantum electronic circuit design at ***Indian Statistical Institute,*** Calcutta (Kolkata), India.
82. Quantum electronic circuit design at ***Indian Institute of Technology***, Khragpore, India
83. Beyond Moore's Law CMOS Technology and Revolutionary Architectures, ***Asian Institute of Technology,*** Bangkok
84. IEEE Distinguished Lecture Beyond Moore's Law CMOS Technology and Revolutionary Architectures at ***Indian Institute of Technology***, Madras (Chennai), India.
85. IEEE Distinguished Lecture Beyond Moore's Law CMOS Technology and Revolutionary Architectures at ***University of Illinois***, Chicago.
86. IEEE Distinguished Lecture on Beyond Moore's Law CMOS Technology and Revolutionary Architectures ***at Indian Institute of Science,*** Bangalore, India.
87. IEEE Distinguished Lecture Beyond Moore's Law CMOS Technology and Revolutionary Architectures at ***Dhaka University***, Dhaka, Bangladesh.

88. IEEE Distinguished Lecture Beyond Moore's Law CMOS Technology and Revolutionary Architectures at ***Tata Institute of Fundamental Research***, Mumbai, India.
89. IEEE Distinguished Lecture Beyond Moore's Law CMOS Technology and Revolutionary Architectures at ***Indian Institute of Technology***, Bombay (Mumbai), India.
90. IEEE Distinguished Lecture Beyond Moore's Law CMOS Technology and Revolutionary Architectures at ***Jadavpur University***, Calcutta (Kolkata), India.
91. Quantum electronic circuit design at ***Nanyang Technological University***, Singapore

Formal Visits to University Laboratories

92. VLSI Design and Education Center, ***University of Tokyo***, Tokyo, Japan.
93. Nanoscale Science and Engineering Center, ***Harvard University***, Harvard, Massachusetts
94. Computer Engineering Research Center, ***University of Texas***, Austin, Texas.
95. Nanoelectronics Laboratory, ***University of Texas***, Dallas, Texas.
96. Testing Laboratory, ***Technical University of Budapest***, Budapest, Hungary.
97. ***Rice University***, Houston, Texas.
98. ***University of North Carolina***, Chapel Hill.
99. ***Virginia Commonwealth University***, Richmond, Virginia.
100. ***Duke University***, Durham, North Carolina
101. ***Oxford University***, Oxford, England.
102. ***Zheng Zhou Light Industry University,*** Zheng Zhou, China
103. ***Syracuse University,*** New York
104. ***University of Virginia,*** Charlottesville, Virginia
105. ***University of California Supercomputing Center, San Diego,*** California.

XV. Teaching Accomplishments

Received Letter of Commendation for Teaching from the Dean of College of Engineering.

Courses Taught and Developed

1. Winter 2003: EECS 270: Logic Design
   Evaluation: 4.02/5.0 (first item) and 3.77/5.0 (second item)
2. Fall 2002: EECS 579: Digital Testing
   Evaluation: 3.88/5.0 (first item) and 3.90/5.0 (second item)
3. Winter 2002: EECS 270: Digital Logic Design
   Evaluation: 4.25/5.0 (first item) and 4.33/5.0 (second item)
4. Winter 2001: EECS 270: Logic Design
   Evaluation: 4.02/5.0 (first item) and 4.32/5.0 (second item)
5. Fall 2000: EECS 270: Digital Logic Design
   Evaluation 3.74/5.0 (first item) and 4.17/5.0 (second item)
6. Fall 1999: EECS 427: VLSI Design
   Evaluation: 4.05/5.0 (first item) and 3.50/5.0 (second item)
7. Fall 1998: EECS 270: Logic Design
   Evaluation: 4.00/5.0 (first item) and 3.99/5.0 (second item)
8. Winter 1999: EECS 579: Digital Testing
   Evaluation: 3.42/5.0 (first item) 3.20/5.0 (second item)
9. Fall 1998: EECS 270: Digital Testing
   Evaluation: 4.00/5.0 (first item) and 3.99/5.0 (second item)
10. Winter 1998: Digital Logic
    Evaluation: 4.00 (first item) and 3.99 (second item)

11. Fall 1997: Taught EECS 427: VLSI Design
    Evaluation: 4.71 (first item) and 4.58 (second item)
12. Winter 1996: Taught EECS 527: Computer-Aided Design for VLSI Systems
    Evaluation: 4.50 (first item) and 4.10 (second item)
13. Fall 1995: Taught EECS 427: VLSI Design
    Evaluation: 4.55 (first item) and 3.94 (second item)
14. Winter 1995: Taught EECS 527: Computer-Aided Design for VLSI Systems
    Evaluation: 4.25 (first item) and 4.08 (second item)
15. Fall 1994: Taught EECS 427: VLSI Design
    Evaluation: 4.81 (first item) and 4.12 (second item)
16. Fall 1993: Taught EECS 427: VLSI Design
    Evaluation: 4.32 (first item) and 3.83 (second item)
17. Spring 1992: Taught EECS 270: Digital Logic Design
    Evaluation: 4.6 (first item) and 4.43 (second item)
18. Winter 1992: Taught EECS 527: Computer-Aided Design for VLSI Systems
    Evaluation: 4.00 (first item) and 4.25 (second item)
19. Fall 1991: Taught EECS 427: VLSI Design
    Evaluation: 4.13 (first item) and 3.88 (second item)
20. Spring 1991: Taught EECS 270: Digital Logic Design
    Evaluation: 4.54 (first item) and 4.71 (second item)
21. Winter 1991: Taught EECS 570: Advanced Computer Architecture
    Evaluation: 4.20 (first item) and 3.89 (second item)

Legend: 5.0 – Excellent, 4.0 – Very Good, 3.0 – Good, 2.0 – Fair, 1.0 – Poor.

XVII. Extracurricular Activities

I am an avid tennis player and have been playing the game for the past 30 years, whenever I am not injured. Some of my sports awards that perhaps I am more proud of than my professional achievements are listed below. Of course, I belong to the category of hackers who pay to play rather than get paid to play. So these awards are small consolations for my efforts in these games. Memorable moments in my tennis life: i) To be selected as a Line Umpire in an ATP tour (professional) tennis tournament, and to call “Foot fault” thrice in a quarter final match after giving warning to a pro player. ii) An abridged version of my article, entitled “Is Rafael Nadal an anomaly like Bjorn Borg?” was published in New York Times in 2011.

- **Tennis**: Between 1975 and 2002, won several prizes in Singles and Doubles Events (between 4.0 and 4.5 NTRP levels) in Ann Arbor City Open Tennis Tournament, Ypsilanti (Michigan) City Open Tennis Tournament, Bangalore City Tennis Tournament, Indian Institute of Science Tennis Tournament, Bharat Electronics Ltd. Tennis Tournament, Huron Valley Tennis Club Tournament, etc.

- **Badminton**: Represented Indian Institute of Science in Karnataka State University Tournament and won the tournament in 1975 primarily due to the presence of Pradeep Padukone who is the brother of World Badminton Champion Prakash Padukone. Also won 3 prizes in I.I.Sc. Intramural Tournaments.

- **Table Tennis**: Between 1974-1976, won 4 prizes in I.I.Sc. Intramural Tournaments.

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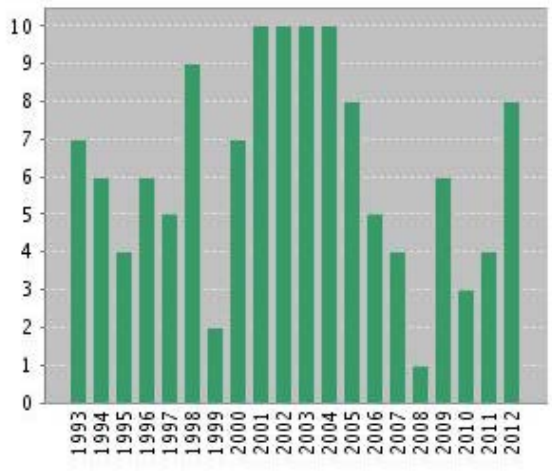

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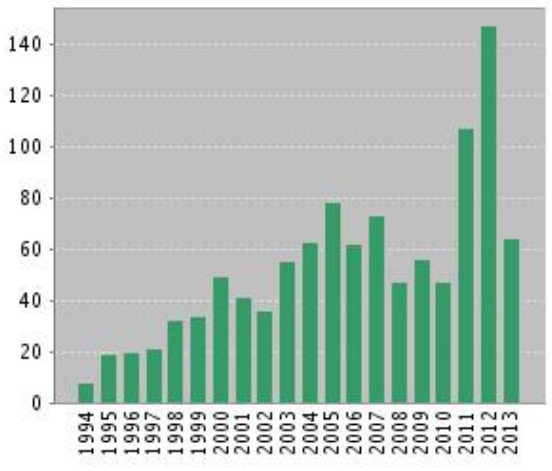

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	56	**47**	**107**	**147**	**64**	**1081**	**43.24**
1. Title: **Digital circuit applications of resonant tunneling devices** Author(s): Mazumder, P; Kulkarni, S; Bhattacharya, M; et al. Source: PROCEEDINGS OF THE IEEE Volume: **86** Issue: **4** Pages: **664-686** DOI: **10.1109/5.663544** Published: **APR 1998**	16	9	18	12	5	227	14.19
2. Title: **Nanoscale Memristor Device as Synapse in Neuromorphic Systems** Author(s): Jo, Sung Hyun; Chang, Ting; Ebong, Idongesit; et al.	0	8	57	95	46	206	51.50

	Source: NANO LETTERS Volume: **10** Issue: **4** Pages: **1297-1301** DOI: **10.1021/nl904092h** Published: **APR 2010**							
3.	Title: **Resonant tunneling diodes: Models and properties** Author(s): Sun, JP; Haddad, GI; Mazumder, P; et al. Source: PROCEEDINGS OF THE IEEE Volume: **86** Issue: **4** Pages: **641-661** Published: **APR 1998**	10	5	7	1	2	105	6.56
4.	Title: **A GENETIC APPROACH TO STANDARD CELL PLACEMENT USING META-GENETIC PARAMETER OPTIMIZATION** Author(s): SHAHOOKAR, K; MAZUMDER, P Source: IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS Volume: **9** Issue: **5** Pages: **500-511** DOI: **10.1109/43.55180** Published: **MAY 1990**	5	0	2	1	0	76	3.17
5.	Title: **VLSI CELL PLACEMENT TECHNIQUES** Author(s): SHAHOOKAR, K; MAZUMDER, P Source: COMPUTING SURVEYS Volume: **23** Issue: **2** Pages: **143-220** Published: **JUN 1991**	0	0	2	1	2	46	2.00
6.	Title: **DEVICE AND CIRCUIT SIMULATION OF QUANTUM ELECTRONIC DEVICES** Author(s): MOHAN, S; SUN, JP; MAZUMDER, P; et al. Source: IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS Volume: **14** Issue: **6** Pages: **653-662** DOI: **10.1109/43.387727** Published: **JUN 1995**	0	0	0	0	0	30	1.58
7.	Title: **Compact multiple-valued multiplexers using negative differential resistance devices** Author(s): Chan, HL; Mohan, S; Mazumder, P; et al. Source: IEEE JOURNAL OF SOLID-STATE CIRCUITS Volume: **31** Issue: **8** Pages: **1151-1156** DOI: **10.1109/4.508262** Published: **AUG 1996**	3	2	0	0	0	26	1.44
8.	Title: **CMOS implementation of a multiple-valued logic signed-digit full adder based on negative-differential-resistance devices** Author(s): Gonzalez, AF; Bhattacharya, M; Kulkarni, S; et al. Source: IEEE JOURNAL OF SOLID-STATE CIRCUITS Volume: **36** Issue: **6** Pages: **924-932** DOI: **10.1109/4.924855** Published: **JUN 2001**	2	2	1	1	0	22	1.69
9.	Title: **Multiple-valued signed-digit adder using negative differential-resistance devices** Author(s): Gonzalez, AF; Mazumder, P Source: IEEE TRANSACTIONS ON COMPUTERS Volume: **47** Issue: **9** Pages: **947-959** DOI: **10.1109/12.713314** Published: **SEP 1998**	2	1	1	1	0	20	1.25
10.	Title: **PARALLEL TESTING FOR PATTERN-SENSITIVE FAULTS IN SEMICONDUCTOR RANDOM-ACCESS MEMORIES** Author(s): MAZUMDER, P; PATEL, JK Source: IEEE TRANSACTIONS ON COMPUTERS Volume: **38** Issue: **3** Pages: **394-407** DOI: **10.1109/12.21126** Published: **MAR 1989**	0	0	0	0	0	20	0.80

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