CURRICULUM VITAE – Wai Tung NG

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a) Academic History

Education

Year	Degree	Discipline	Institution	Country
1990	Ph.D.	Electrical Engineering	University of Toronto	Canada
1985	M.A.Sc.	Electrical Engineering	University of Toronto	Canada
1983	B.A.Sc.	Electrical Engineering	University of Toronto	Canada

Teaching and Research Appointments

08/93 to Present **Professor (since 2008)**
Director, Toronto Nanofabrication Centre (2014-2015)
Associate Chair, Undergraduate Studies (2005-2011)
Associate Professor (98-08)
Assistant Professor (93-98)
Dept. of Electrical and Computer Engineering
Dept. of Material Science and Engineering (cross appointed)
University of Toronto, Toronto, Ontario, Canada M5S 3G4

Research Area: Microelectronic devices and circuit design for telecommunication and power management applications.

01/00 to 06/00 **Visiting Associate Professor**
Dept. of Electrical and Electronic Engineering
Hong Kong University of Science and Technology, Clearwater Bay, Kowloon, Hong Kong

Research Area: Semiconductor fabrication processes

09/99 to 12/99 **Visiting Associate Professor**
Dept. of Electrical and Electronic Engineering
University of Hong Kong, Pokfulam Road, Hong Kong

Research Area: Semiconductor fabrication processes

01/92 to 06/93 **Lecturer**
Dept. of Electrical and Electronic Engineering
University of Hong Kong, Pokfulam Road, Hong Kong

Research Area: Smart Power Semiconductor Devices for VLSI Applications, Low Voltage Analog Circuit Designs

07/90 to 12/91 **Member of Technical Staff**
Corporate Research Development & Engineering
Texas Instruments Incorporated
13536 N. Central Expwy, MS 944, Dallas TX 75243 U.S.A.

Research Area: Duties included design and development of MOS smart power integrated circuit devices suitable for VLSI applications.

Awards & Honours

2014	Taishan Scholar, Shangdong, China (泰山学者海外特聘专家−创新类) http://www.shandong.gov.cn/art/2014/12/10/art_275_962.html
2014	Yellow River Delta Scholar, Dongying City, Shangdong, China (东营第三批黄河三角洲学者）No. DYRC20140110 http://www.dongying.gov.cn/html/2013-10/13101512211764109.html
2011	FY20l1 JSPS Invitation Fellowship Program for Research in Japan (Short-Term), Jan 30 to Feb. 27, 2012. (Success rate = 25%)
2006	Best Student Paper O. Trescases, W.T. Ng, H. Nishio, M. Edo and T. Kawashima, "A Digitally Controlled DC-DC Converter Module with a Segmented Output Stage for Optimized Efficiency," *IEEE Int. Sym. on Power Semiconductor Devices and Integrated Circuits*, Tech Digest, ISPSD'06, Naples, Italy, pp. 373-376, June 4-9, 2006.
2005	Best Student Paper I.-S. M. Sun, W.T. Ng, K. Kanekiyo, T. Kobayashi, H. Mochizuki, M. Toita, Y. Furukawa, H. Imai, A. Ishikawa, S. Tamura, and K. Takasuka, "A Novel SOI Lateral Bipolar Transistor with 30GHz Fmax and 27V BVceo for RF Power Amplifier Application," *IEEE Int. Sym. on Power Semiconductor Devices and Integrated Circuits*, Tech Digest, ISPSD'05, Santa Barbara, pp. 99-102, May 22-26, 2005.
1999	Best Student Paper D. Gradinaru, W.T. Ng, and C.A.T. Salama, "High Voltage High Frequency Silicon Bipolar Transistors," *IEEE Int. Sym. on Power Semiconductor Devices and Integrated Circuits*, Tech Digest, Toronto, Canada, pp. 293-296, May 1999.
1993 to 1996	Honorary Lecturer in Electrical and Electronic Engineering, University of Hong Kong.
1987 to 1988	University of Toronto Open Doctoral Fellowship
1983 to 1987	Natural Sciences and Engineering Research Council of Canada, Postgraduate scholarship
1983	Wilson Medal for graduating with 1st rank in Electrical Engineering, University of Toronto
1981	Andrew Alexander Kinghorn Scholarship, University of Toronto
1980	Baptie Scholarship, University of Toronto
1979	Wallberg Admission Scholarship, University of Toronto Ontario Scholar

b) Scholarly and Professional Work

Refereed journal publications (published or accepted)

1. S. Xie, and W.T. Ng, "An all-digital self-calibrated delay-line based temperature sensor for VLSI thermal sensing and management," *Integration, the VLSI Journal*, Vol. 51, pp. 107-117, Sep. 2015. (Impact Factor 0.66)
2. X. Tang, W.T. Ng, and K.P. Pun, "A Resistor-based sub-1V CMOS Smart Temperature Sensor for VLSI Thermal Management," *IEEE Transactions on Very Large Scale Integration Systems*, Vol. 23, No. 9, pp. 1651-1660, Sep. 2015.
3. W. Du, X. Lyu, W.T. Ng, and X. Chen, "An Ultra-low Specific On-resistance LDMOST with Self-driven Split Gate", *IEEE Transactions on Electron Devices*, Vol. 62, No. 4, pp. 1230-1234, Apr. 2015. (Impact Factor 2.47)
4. L. Sun, B. Li, A.K.Y. Wong, W.T. Ng, and K.P. Pun, "A Charge Recycling SAR ADC with a LSB-Down Switching Scheme," *IEEE Transactions on Circuit and Systems I*, Vol. 62, No. 2, pp. 356-365, Feb. 2015. 5. L. Sun, C.T. Ko, M. Ho, W.T. Ng, K.N. Leung, C.S. Choy, K.P. Pun, "23 μW 8.9-effective number of bit 1.1 MS/s successive approximation register analog-to-digital converter with an energy-efficient digital-to-analog converter switching scheme," The Journal of Engineering, Aug. 2014, 6 pp.
6. S.A. Shen, S. Xie and W.T. Ng, "A power and area efficient 65 nm CMOS delay line ADC for on-chip voltage sensing," *Journal of Circuits, Systems and Computers (JCSC),* 7 pages, Vol. 22, No. 9, Oct. 2013. (Impact Factor 0.349)
7. J. Wang, A. Prodić, W.T. Ng, "Mixed-Signal-Controlled Flyback-Transformer-Based Buck Converter with Improved Dynamic Performance and Transient Energy Recycling," *IEEE Trans. Power Electronics*, Vol. 28, No. 2, pp. 970-984, 2013.
8. Xie Gang(谢 刚), Tang Cen(汤 岑), Wang Tao(汪 涛), Guo Qing(郭 清), Zhang Bo(张 波), Sheng Kuang(盛 况), and Wai Tung Ng "An AlGaN/GaN HEMT with Enhanced Breakdown and a Near-zero Breakdown Voltage Temperature Coefficient," *Chinese Physics B*, Vol. 22, No. 2 (2013) 026103, 2013.
9. G. Xie, E. Xu, J. Lee, N. Hashemi, B. Zhang, F.Y. Fu and W.T. Ng, "Breakdown Voltage Enhancement Technique for RF Based AlGaN/GaN HEMTs with a Source-connected Air-bridge Field Plate," *IEEE Electron Device Lett.,* Vol. 33, No. 5, pp. 670-672, 2012.
10. G. Xie (谢刚), E. Xu, N. Hashemi, B. Zhang (张波), F.Y. Fu and W.T. Ng, "An AlGaN/GaN HEMT with Reduced Surface Electric Field and Improved Breakdown Voltage," *Chinese Physics B*, Vol. 21, No. 8 (2012) 086105, 2012.
11. G. Xie, E. Xu, B. Zhang, W.T. Ng, "Study on Breakdown Failure Mechanism of Power AlGaNGaN HEMTs on a RF Compatible Process," *Microelectronics Reliability*, Vol. 52, No. 6, pp. 964-968, June 2012.
12. W.M. Tang, M.G. Helander, M.T. Greiner, Z.H. Lu and W.T. Ng, "Effects of Annealing Time on the Performance of OTFT on Glass with ZrO_2 as Gate Dielectric," *Active and Passive Electronic Components*, Volume 2012 (2012), Article ID 901076, 5 pages.
13. W.M. Tang, M.T. Greiner, Z.H. Lu, W.T. Ng and H.G. Nam, "Effects of UV-ozone treatment on radio-frequency magnetron sputtered ZnO thin films," *Thin Solid Films*, Vol. 520, pp. 569-573, July 2011.
14. W. M. Tang, M. T. Greiner, M. G. Helander, Z. H. Lu, and W.T. Ng, "Effects of interfacial oxide layers of the electrode metals on the electrical characteristics of organic thin-film

transistors with HfO_2 gate dielectric," *J. of Applied Physics*, Vol. 110, No. 4, 044108 (2011).

15. O. Trescases, A. Prodić, and W.T. Ng, "Digitally Controlled Current-Mode DC-DC Converter IC," *IEEE Trans. Circuits and Systems I*, Vol. 58, No. 1, pp. 219 – 231, 2011.
16. W. M. Tang, W. T. Ng, M. G. Helander, M. T. Greiner, Z. H. Lu, "UV ozone passivation of the metal/dielectric interface for HfO_2-based organic thin film transistors," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, Vol. 28, No. 6, pp. 1100 – 1103, 2010.
17. A. Yoo, Y. Onishi, H.P.E. Xu, W.T. Ng, "A Low-Voltage Lateral SJ-FINFET With Deep-Trench p-Drift Region," *IEEE Electron Device Lett.*, Vol. 30, No. 8, pp. 858-860, Aug. 2009.
18. H. Wang, H.P.E. Xu, W.T. Ng, "A Novel Orthogonal Gate EDMOS Transistor With Improved dv/dt Capability and Figure of Merit (FOM)," *IEEE Electron Device Lett.*, Vol. 29, No. 12, pp. 1386-1388, Dec. 2008.
19. H. Wang, H.P.E. Xu, W.T. Ng, "Observation and Utilization of Boron Segregation in Trench MOSFETs to improve Figure-of-Merit (FOM)," *IEEE Electron Device Lett.*, Vol. 29, No. 11, pp. 1239-1241, Nov. 2008.
20. O. Trescases, G. Wei, A. Prodic, and W.T. Ng, "Predictive Efficiency Optimization for DC-DC Converters with Digital Electronic Loads," *IEEE Trans. Power Electronics*, *IEEE Trans. Power Electronics*, Vol. 23, No. 4, pp. 1859-1869, July 2008.
21. G. Yip, J. Qiu, W.T. Ng, and Z.H. Lu, "Effect of Metal Contacts on the Electrical Characteristics of Al_2O_3 Dielectric Thin Films," *Appl. Phys. Lett.* **92**, 122911, Mar. 2008.
22. R. Azar, F. Udrea, W.T. Ng, F. Dawson, W. Findlay, and P. Waind, "The Current Sharing Optimization of Paralleled IGBTs in a Power Module Tile Using a PSpice Frequency Dependent Impedance Model," *IEEE Trans. Power Electronics*, Vol. 23, No. 1, pp. 206-217, Jan. 2008.
23. H.P.E. Xu, O.P. Trescases, I-S.M. Sun, D. Lee, W.T. Ng, K. Fukumoto, A. Ishikawa, Y. Furukawa, H. Imai, T. Naito, N. Sato, S. Tamura, K. Takasuka, and T. Kohno, "Design of a Rugged 60V VDMOS Transistor," *Circuits, Devices & Systems, IET*, Vol. 1, No. 5, pp. 327-331, October 2007.
24. O. Trescases, G. Wei, A. Prodic, W.T. Ng, "An EMI Reduction Technique for Digitally Controlled SMPS," *IEEE Trans. Power Electronics*, Vol. 22, No. 4, pp. 1560-1565, July 2007.
25. I-S. M. Sun, W. T. Ng, .K. Kanekiyo, T. Kobayashi, H. Mochizuki, M. Toita, H. Imai, A. Ishikawa, S. Tamura, and K. Takasuka, "Lateral High-Speed Bipolar Transistor on SOI for RF SoC Applications," *IEEE Trans. Electron Devices*, vol. 52, no. 7, pp. 1376-1383, July 2005.
26. R. Azar, F. Udrea, W.T. Ng, F. Dawson, W. Findlay, P. Waind, and G. Amaratunga, "The Current Sharing Optimisation of Paralleled IGBTs in a Power Module Tile Using a PSpice Frequency Dependent Impedance Model," *IEEE Trans. Industry Applications,* Vol. 40, No. 3, pp. 710-716, May/June 2004. (with Dynex Semiconductor, UK)
27. R. Azar, F. Udrea, W.T. Ng, F. Dawson, W. Findlay, P. Waind and G. Amaratunga, "Advanced Electrothermal Spice Modelling Of Large Power IGBTs," *IEE Proc.-Circuits Devices Syst.*, Vol. 151, No. 3, pp. 249-253, June 2004. (with Dynex Semiconductor, UK)

28. M. Lee, Z.H. Lu, W.T. Ng, D. Landheer, X. Wu, and S. Moisa, "Interfacial Growth in HfO_xN_y Gate Dielectrics Deposited Using $[(C_2H_5)_2N]_4Hf$ with O_2 and NO," *Applied Physics Letters*, Vol. 83, No. 13, pp. 2638-2640, Sep. 2003.
29. D. Cho, W.T. Ng, and J.K. Mills, "Multiple Simultaneous Specification (MSS) Control of a High Speed Linear Positioning System Driven by a Brushless DC Motor," *Trans. of ASME J. Dyn. Systems, Meas., and Control*, Vol. 123, pp. 296-299, Jun. 2001.
30. A. Khoueir, Z.H. Lu, W.T. Ng, & Y. Ma, "Ultrathin Oxynitride Formation by Low Energy Ion-Implantation," *Journal Vac. Sci. Tech. A*, Vol. 18, Issue 2, pp. 724-729, Mar. 2000.
31. J. Cai, J.K.O. Sin, P.K.T. Mok, W.T. Ng, and P.T. Lai, "A New Lateral Trench-Gate Conductivity Modulated Power Transistor," *IEEE Trans. Electron Devices*, Vol. 46, No. 8, pp. 1788 –1793, Aug. 1999.
32. C. Zhu, J.K.O. Sin, and W.T. Ng, "Characteristics of P-channel Polysilicon Conductivity Modulated Thin-Film Transistors," *IEEE Trans. Electron Devices*, Vol. 46, No. 7, pp. 1406 –1410, Jul. 1999.
33. J. Ranaweera, W.T. Ng, and C.A.T. Salama, "Simulation, fabrication and Characterization of a 3.3V Flash ZEEPROM Array Implemented in a 0.8µm CMOS Process," *Solid-St. Electron.*, Vol. 43, No. 2, pp. 263-273, Feb. 1999.
34. Z. Xu, P.T. Lai, and W.T. Ng, "AC Hot-Carrier-Induced Degradation in NMOSFETs with N2O-based Gate Dielectrics," *IEEE Electron Device Lett.* Vol. 18, No. 2, pp. 39-41, Feb. 1997.
35. Z. Xu, P.T. Lai, and W.T. Ng, "A Novel Technique of N2O-Treatment on NH_3-Nitrided Oxide as Gate Dielectric for nMOS Transistors," *IEEE Trans. Electron Devices*, Vol. 43, No. 11, pp. 1907-1913, Nov. 1996.
36. J. Ranaweera, I. Kalastirsky, E. Gulersen, W.T. Ng and C.A.T. Salama, "A Novel Programming Method for High Speed, Low Voltage Flash E^2PROM Cell," *Solid-St. Electron.*, Vol. 39, No. 7, pp. 981-989, Jul. 1996.
37. Z. Xu, P.T. Lai, and W.T. Ng, "Enhanced Off-State Leakage Currents in N-Channel MOSFET's with N_2O-Grown Gate Dielectric," *IEEE Electron Device Lett*. Vol. 16, No. 10, pp. 436-438, Oct. 1995.
38. Z. Xu, P.T. Lai, and W.T. Ng, "Mobility Improvement of n-MOSFET's with Nitrided Gate Oxide by Backsurface Ar^+ Bombardment," *IEEE Electron Device Lett.*, Vol. 16, No. 8, pp. 354-356, Aug. 1995.
39. W.T. Ng and C.A.T. Salama, "A CMOS Compatible HVIC Process with Complementary SINFETs," *IEEE Trans. Electron Devices*, Vol. 38, No. 8, pp. 1935-1942, Aug. 1991.
40. W.T. Ng, S. Liang and C.A.T. Salama, "SINFET Device Modeling," *Solid-St. Electron.*, Vol. 33, No. 12, pp. 1569-1579, Dec. 1990.
41. W.T. Ng, S. Liang and C.A.T. Salama, "Schottky Barrier Diode Characteristics under High Level Injection," *Solid-St. Electron.*, Vol. 33, No. 1, pp. 39-46, Jan. 1990.
42. W.T. Ng and C.A.T. Salama, "High Speed High-Resolution CMOS Voltage Comparator," *Electron. Lett.*, Vol. 22, No. 6, pp. 338-339, Jun. 1986.

Refereed conference publications (published or accepted)

43. J.X. Chen, A. Shorten, M. Sasaki, T. Kawashima, H. Nishio, W.T. Ng, "An Automatic IGBT Collector Current Sensing Technique via the Gate Node," PCIM Europe (Power conversion and Intelligent Motion), Nuremberg, Germany, May 10- 12, 2016.

44. W.M. Tang, M.G. Helander, J. Qiu, M.T. Greiner, Z.H. Lu and W.T. Ng, "Thermal Annealing Effect on Electrical Characteristics of CuPc Thin-Film Transistors on Glass with ZrO2 as Gate Dielectric," *IEEE International Conference on Electron Devices and Solid-State Circuits* (*EDSSC*), pp. 197-200, Singapore, Jun 1-4, 2015.
45. J.S. Yu, G. Jin, S.L. Cheng, and W.T. Ng, "An Integrated Tri-Mode DC-DC Converter with Segmented Power Devices and Power Transmission Gate," *IEEE International Conference on Electron Devices and Solid-State Circuits* (*EDSSC*), pp. 41-44, Singapore, Jun 1-4, 2015.
46. J.S. Yu, G. Jin, S.L. Cheng, and W.T. Ng, "Digital Dead-Time Control for an Integrated Tri-Mode Buck-Boost DC-DC Converter," *9th International Conference on Power Electronics – ECCE Asia* (*ICPE 2015-ECCE Asia*), pp. 1768-1771, Seoul, Korea, June 1 to 5, 2015.
47. S. Xie and W.T. Ng, "Digital Integrated Temperature Sensors for VLSI Thermal Management," *12th IEEE International Conference on Solid-State and Integrated Circuit Technology* (*ICSICT*), pp. 905-908, Guilin, China, Oct. 28 - 31, 2014.
48. S.L. Cheng, S. Yao, G. Jin and W.T. Ng, "Digital Controlled Dead-time for Tri-mode Buck-boost DC-DC Converter," *12th IEEE International Conference on Solid-State and Integrated Circuit Technology* (*ICSICT*), pp. 1580-1582, Guilin, China, Oct. 28 - 31, 2014.
49. A. Liu, H. Liu and W.T. Ng, "Validation of an Energy-Optimal Path Planning Algorithm through a Solar-Assisted Mini UAV," *10th International Conference on Intelligent Unmanned Systems* (*ICIUS*), Montreal, Canada, Sep. 29 - Oct. 1, 2014
50. J. Chen, A. Shorten and W.T. Ng, "IGBT Collector Current Sensing Using Gate Current", *International Seminar on Power Semiconductors* (*ISPS'14*), Prague, Czech Republic, Aug. 26-29, 2014.
51. G. Jin, W.T. Ng, "An Integrated Tri-Mode Non-Inverting Buck-Boost DC-DC Converter with Segmented Power Devices and Power Transmission Gate Structure," *26th International Symposium on Power Semiconductor Devices and ICs* (*ISPSD '14*), Waikoloa, Hawaii, USA, pp. 201-204, June 15-19, 2014.
52. J.S. Yu, W.J. Zhang, W.T. Ng, "A Segmented Output Stage H-Bridge IC with Tunable Gate Driver," *26th International Symposium on Power Semiconductor Devices and ICs* (*ISPSD '14*), Waikoloa, Hawaii, USA, pp. 205-208, June 15-19, 2014.
53. S. Xie and W.T. Ng, "Delay-Line Based Temperature Sensors and VLSI Thermal Management Demonstrated on a 60nm FPGA," *IEEE International Symposium on Circuits and Systems* (*ISCAS*), Melbourne, Australia, pp. 2571-2574, June 1-5, 2014.
54. W.M. Tang, M.G. Helander, M.T. Greiner, J. Qiu, Z.H. Lu, and W.T. Ng, "A Study on the Electrical Characteristics of Copper Phthalocyanine-based OTFTs with ZrTaO as Gate Dielectric," *IEEE International Conference on Electron Devices and Solid-State Circuits* (*EDSSC*), Hong Kong, China, Jun. 3-5, 2013.
55. Z. Ning, L. He, Z. Hu, G. Jin and W.T. Ng, "A Feedback-Voltage-Sensing Translator for Floating Buck DC-DC Converters," *IEEE International Conference on Electron Devices and Solid-State Circuits* (*EDSSC*), Hong Kong, China, Jun. 3-5, 2013.
56. M. Sasaki, H. Nishio, A. Shorten and W.T. Ng, "Current Balancing Control for Parallel Connected IGBTs Using Programmable Gate Driver Output Resistance," *25th International Symposium on Power Semiconductor Devices and ICs* (*ISPSD '13*), Kanazawa, Japan, pp. 65-68, May 26-30, 2013.

57. A. Shorten and W.T. Ng, "A Segmented Gate Driver IC for the Reduction of IGBT Collector Current Over-Shoot at Turn-on," *25th International Symposium on Power Semiconductor Devices and ICs* (*ISPSD '13*), Kanazawa, Japan, pp. 73-76, May 26-30, 2013.
58. S. Xie and W.T. Ng, "A Low Power All-digital Self-calibrated Temperature Sensor using 65nm FPGAs," *IEEE Int. Sym. on Circuits and Systems* (*ISCAS 2013*), Beijing, China, May 19-23, 2013.
59. M. Sasaki, H. Nishio, and W.T. Ng, "Dynamic Gate Resistance Control for Current Balancing in Parallel Connected IGBTs," *Applied Power Electronics Conference and Exposition (APEC 2013)*, Long Beach, CA, pp. 244 - 249, Mar. 17-21, 2013.
60. S.A. Shen, S. Xie, and W.T. Ng, "A Power and Area Efficient 65 nm CMOS Delay Line ADC for On-chip Voltage Sensing," *IEEE International Conference on Electron Devices and Solid-State Circuits* (*EDSSC*), 4 pages, Bangkok, Thailand, Dec. 3-5, 2012.
61. S. Xie and W.T. Ng, "Delay-line based Temperature Sensors for On-chip Thermal Management," *11th IEEE International Conference on Solid-State and Integrated Circuit Technology* (*ICSICT*), 4 pages, Xian, China, Oct. 29, 2012-Nov. 1, 2012.
62. G. Xie, E. Xu, J. Lee, N. Hashemi, F.Y. Fu, B. Zhang, and W.T. Ng, "Breakdown Voltage Enhancement Technique for RF Process Compatible Power AlGaN/GaN HEMTs," *24th International Symposium on Power Semiconductor Devices and ICs* (*ISPSD '12*), Bruges, Belgium, pp. 337- 340, June 3-7, 2012.
63. S. Xie and W.T. Ng, "A 0.02 nJ Self-calibrated 65nm CMOS Delay Line Temperature Sensor," *IEEE Int. Sym. on Circuits and Systems (ISCAS 2012)*, pp. 3126-3129, Seoul, Korea, 20-23 May 2012.
64. W.M. Tang, M.T. Greiner, M.G. Helander, Z.H. Lu and W.T. Ng, "Effects of Different Ar/O_2 Ratios on the Electrical Properties of CuPc-based TFTs with ZrO_2 Gate Dielectric," *IEEE International Conference on Electron Devices and Solid-State Circuits* (*EDSSC*), 2 pages, Tianjin, China, Nov. 17-18, 2011.
65. S. Xie and W.T. Ng, "A 65nm CMOS Low Power Delay Line Based Temperature Sensor," *IEEE International Conference on Electron Devices and Solid-State Circuits* (*EDSSC*), 2 pages, Tianjin, China, Nov. 17-18, 2011.
66. G. Xie, E. Xu, J. Lee, N. Hashemi, F.Y. Fu, B. Zhang, and W.T. Ng, "Breakdown Voltage Enhancement for Power AlGaN/GaN HEMTs with Air-bridge Field Plate," *IEEE International Conference on Electron Devices and Solid-State Circuits* (*EDSSC*), 2 pages, Tianjin, China, Nov. 17-18, 2011.
67. J. Wang, W.T. Ng, A. Prodic, "Flyback Transformer Based Transient Suppression Method for Digitally Controlled Buck Converters," *2011 IEEE Energy Conversion Congress and Exposition* (*ECCE 2011*), pp. 3354-3361, Phoenix, AZ, Sep. 17-22, 2011.
68. M.S. Zaman, P.K. Cao, O. Trescases, W.T. Ng, "H^2-optimal Thermal Management for Multi-Phase Current Mode Buck Converters," *2011 IEEE Energy Conversion Congress and Exposition* (*ECCE 2011*), pp. 4177-4182, Phoenix, AZ, Sep. 17-22, 2011.
69. Y. Zhao, W.T. Ng, "An Energy Conservation Based High-efficiency Dimmable Multi-channel LED Driver," *2011 IEEE Energy Conversion Congress and Exposition* (*ECCE 2011*), pp. 2576-2580, Phoenix, AZ, Sep. 17-22, 2011.
70. W.T. Ng, A. Shorten, "Efficiency Enhancement and EMI Suppression via Dynamically Adjustable Gate Driving Strength," *54th IEEE International Midwest Symposium on Circuits and Systems* (*IEEE MWSCAS 2011*), Seoul, Korea, Aug.7-10, 2011.

71. A. Shorten, A.A. Fomani, W.T. Ng, H. Nishio, and Y. Takahashi, "Reduction of Conducted Electromagnetic Interference in SMPS using Programmable Gate Driving Strength," *23rd International Symposium on Power Semiconductor Devices and ICs (ISPSD '11)*, pp. 364-367, San Diego, CA, May 23-26, 2011.
72. J. Wang, W.T. Ng, and O. Trescases, "Versatile Capabilities of Digitally Controlled Integrated DC-DC Converters," *IEEE Int. Sym. on Circuits and Systems (ISCAS 2011)*, pp. 293-296, Rio de Janeiro, Brazil, 15-18 May 2011.
73. P.K. Cao, W.T. Ng, O. Trescases, "Thermal Management for Multi-Phase Current Mode Buck Converters," *Applied Power Electronics Conference and Exposition (APEC 2011)*, Fort Worth, TX, pp. 1124 - 1129, Mar. 6-10, 2011.
74. W.M. Tang, M.G. Helander, M.T. Greiner, W.T. Ng, Z.H. Lu, "Electrode effects on the breakdown characteristics of high-k HfO_2 metal-insulator-metal capacitors," *IEEE International Conference on Electron Devices and Solid-State Circuits* (*EDSSC*), Hong Kong, China, Dec. 15-17, 2010.
75. A. Yoo, J.C.W. Ng, J.K.O. Sin, W.T. Ng, "High performance CMOS-compatible super-junction FINFETs for Sub-100V Applications," *IEEE International Electron Devices Meeting* (*IEDM*), pp. 20.7.1 - 20.7.4, San Francisco, CA, Dec. 6-8, 2010.
76. X. Gang, B. Zhang, F.Y. Fu, W.T. Ng, "GaN high electron mobility transistors with localized Mg doping and Drain Metal Extension," *10th IEEE International Conference on Solid-State and Integrated Circuit Technology* (ICSICT), pp. 1341 – 1343, Shanghai, China, Nov. 1- 4, 2010.
77. A. Akhavan Fomani, A. Shorten and W.T. Ng, "An Integrated Segmented Gate Driver with Adjustable Driving Capability," *2010 IEEE Energy Conversion Congress and Exposition*, pp. 2430 – 2433, Atlanta, Georgia, USA, September 12-16, 2010.
78. A. Yoo, and W.T. Ng, "Sub-200V Lateral SJ-FINFETs with Low On-Resistance," *International Seminar on Power Semiconductors (ISPS'10)*, Prague, Czech Republic, Aug. 31 - Sep. 3, 2010.
79. A. Akhavan Fomani, and W.T. Ng, "A Segmented Gate Driver with Adjustable Driving Capability for Efficiency Optimization," *International Power Electronics Conference* (IPEC-2010), pp. 1646 – 1650, Sapporo, Japan, Jun. 21 - 24, 2010.
80. J. Wang, K. Ng, T. Kawashima, M. Sasaki, H. Nishio, A. Prodić and W.T. Ng, "A Digitally Controlled Integrated DC-DC Converter with Transient Suppression," *22nd International Symposium on Power Semiconductor Devices and ICs (ISPSD '10)*, Hiroshima, Japan, pp. 277 - 280 , June 6-10, 2010.
81. G. Xie, B. Zhang, and W.T. Ng, "Breakdown Voltage Enhancement for GaN High Electron Mobility Transistors," *22nd International Symposium on Power Semiconductor Devices and ICs (ISPSD '10)*, pp. 237 – 240, Hiroshima, Japan, June 6-10, 2010.
82. Y. Zhao, A. Shorten, H. Nishio, and W.T. Ng, "An Integrated DC-DC Converter with One-Step Digital Dead-time Correction," *22nd International Symposium on Power Semiconductor Devices and ICs (ISPSD '10)*, pp. 57 – 60, Hiroshima, Japan, June 6-10, 2010.
83. N. Saniei, A. Tofangdarzade, and W.T. Ng, "Locking Time of Oscillators Under External Frequency Injection," *18th Iranian Conference on Electrical Engineering (ICEE)*, 2010 pp. 391-396, Isfahan, Iran, May 11-13, 2010.

84. Y. Zhao, A. Akhavan Fomani, and W.T. Ng, "One-Step Digital Dead-Time Correction for DC-DC Converters," *Applied Power Electronics Conference and Exposition, APEC 2010*, Palm Springs, CA, pp. 132 - 137, Feb. 21 - 25, 2010.
85. J. Wang, K. Ng, T. Kawashima, M. Sasaki, H. Nishio, A. Prodić and W.T. Ng, "Integrated DC-DC Converter with an Auxiliary Output Stage for Transient Suppression," *2009 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, Xi'an, China, Nov. 25-27, 2009.
86. W.M. Tang, M.G. Helander, M.T. Greiner, G. Dong, W.T. Ng and Z.H. Lu, "Enhanced Performance for OTFT on Glass with HfO_2 as Gate Dielectric by UV-Ozone Treatment," *2009 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, Xi'an, China, Nov. 25-27, 2009.
87. Y. Feng, G. Wei, W.T. Ng, and T. Sugimoto, "A 38W Digital Class D Audio Power Amplifier Output Stage with Integrated Protection Circuits," *21st International Symposium on Power Semiconductor Devices and ICs (ISPSD '09)*, pp. 53-56, Barcelona, Spain, June 14-17, 2009.
88. K. Ng, J. Wang, W.T. Ng, "A digitally controlled transient suppression method for integrated DC-DC converters," *2008 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, Hong Kong, China, Dec. 8-10, 2008.
89. A. Yoo, M. Chang, O. Trescases, and W.T. Ng, "Smart Power IC Design Methodology Based on a New Figure of Merit (FOM) in Standard CMOS," *8th International Seminar on Power Semiconductors (ISPS'08)*, Prague, Czech Republic, 27 -29 August, 2008.
90. O. Trescases, N. Rahman, A. Prodić, and W.T. Ng, "A 1V Buck Converter IC with Hybrid Current-Mode Control and a Charge-Pump DAC," *IEEE 39th Power Electronics Specialists Conference (PESC 2008)*, pp. 1122 – 1128, Rhodes, Greece, June 15-19, 2008.
91. A. Yoo, M. Chang, O. Trescases, and W.T. Ng, "High Performance Low-Voltage Power MOSFETs with Hybrid Waffle Layout Structure in 0.25µm Standard CMOS Process," *20th International Symposium on Power Semiconductor Devices and ICs (ISPSD '08)*, pp. 95-98, Orlando, Florida, May 18-22, 2008.
92. H. Wang, J. Wang, H.P.E. Xu, W.T. Ng, K. Fukumoto, A. Ishikawa, H. Imai, and K. Takasuka, "A 30V EDMOS with Orthogonal Gate Structure Based on a 0.18µm CMOS Technology," *20th International Symposium on Power Semiconductor Devices and ICs (ISPSD '08)*, pp. 20-23, Orlando, Florida, May 18-22, 2008.
93. Y. Onishi, H. Wang, H. P. Edward. Xu, and W.T. Ng, "SJ-FINFET: A New Low Voltage Lateral Superjunction MOSFET," *20th International Symposium on Power Semiconductor Devices and ICs (ISPSD '08)*, pp. 111-114, Orlando, Florida, May 18-22, 2008.
94. H. Wang, A. Yoo, H.P.E. Xu, W.T. Ng, K. Fukumoto, A. Ishikawa, H. Imai, K. Sakai, and K. Takasuka, "A Floating RESURF EDMOS with Enhanced Ruggedness and Safe Operating Area," *2007 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, pp. 279-282, Tainan, Taiwan, ROC, Dec. 19-21, 2007.
95. A. Yoo, M. Chang, O. Trescases, H. Wang, and W.T. Ng, "FOM (Figure of Merit) Analysis for Low Voltage Power MOSFETs in DC-DC Converter," *2007 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, pp. 1039-1042, Tainan, Taiwan, ROC, Dec. 19-21, 2007.
96. Q. Fung, A. A. Fomani, Y. Feng and W.T. Ng, "Design of a 2-GSample/s Track-and-Hold Amplifier implemented in a 60-GHz SiGe BiCMOS Process," *2007 IEEE International*

Conference on Electron Devices and Solid-State Circuits (EDSSC), pp. 937-940, Tainan, Taiwan, ROC, Dec. 19-21, 2007.

97. O. Trescases, A. Parayandeh, A. Prodic and W.T. Ng, "Sensorless Digital Peak Current Controller for Low-Power DC-DC SMPS Based on a Bi-Directional Delay Line," *38th IEEE Power Electronics Specialist Conference*, Orlando, Florida, June 17-21, 2007.
98. H. Wang, O Trescases., H.P.E. Xu, W.T. Ng, K. Fukumoto, A. Ishikawa, Y. Furukawa, H. Imai, T. Naito, N. Sato, K. Sakai, S. Tamura, and K. Takasuka, "A 70V UMOS Technology with Trenched LOCOS Process to Reduce C_{gs}," *Proc. IEEE International Symposium on Power Semiconductors and ICs* (*ISPSD*), pp. 181-184, Jeju Korea, May 28-30, 2007.
99. O. Trescases, G. Wei, W.T. Ng, H. Nishio, T. Sugimoto, and K. Takasuka, "A Digital Predictive On-Line Energy Optimization Scheme for DC-DC Converters," *Applied Power Electronics Conference and Exposition, APEC'07*, Anaheim, CA, pp. 557 - 562, Feb. 25 - Mar. 1, 2007.
100. H.P.E Xu, O.P. Trescases, I-S.M. Sun, D. Lee, W.T. Ng, K. Fukumoto, A. Ishikawa, Y. Furukawa, H. Imai, T. Naito, N. Sato, K. Sakai, S. Tamura, K. Takasuka, and T. Kohno, "Design of a Rugged 60V VDMOS Transistor," *Int. Seminar On Power Semiconductors, ISPS'06*, Prague, Czech Republic, Aug. 29 - Sep. 1, 2006.
101. O. Trescases, G. Wei, W.T. Ng, "A Low-Power DC-DC Converter with Digital Spread Spectrum for Reduced EMI," *37th IEEE Power Electronics Specialist Conference*, Jeju, Korea, June 18-22, 2006.
102. O. Trescases, W.T. Ng, H. Nishio, M. Edo and T. Kawashima, "A Digitally Controlled DC-DC Converter Module with a Segmented Output Stage for Optimized Efficiency," *18th International Symposium on Power Semiconductor Devices and Integrated Circuits* (*ISPSD '06*), pp. 373-376, Naples, Italy, June 4-9, 2006. (**Young Researcher Award**)
103. O. Trescases, Z. Lukic, W.T. Ng, A. Prodic, "Low Power Mixed-Signal Current-Mode DC-DC Converter Using a One-bit Delta Sigma DAC," *Applied Power Electronics Conference and Exposition, APEC '06*, Dallas, TX, pp. 700-704, March 19-23, 2006.
104. I-S. M. Sun; W.T. Ng; H. Mochizuki, K. Kanekiyo, T. Kobayashi, M. Toita, H. Imai, A. Ishikawa, S. Tamura, K. Takasuka, "A RF lateral BJT on SOI for Realization of RF SOI-BiCMOS Technology," Silicon Monolithic Integrated Circuits in RF Systems, SiRF2006. Digest pp. 50-53, Jan. 18-20, 2006.
105. I.-S. M. Sun, W.T. Ng, H. Mochizuki, K. Kanekiyo, T. Kobayashi, M. Toita, H. Imai, A. Ishikawa, S. Tamura, and K. Takasuka. "Novel ultra-low power RF lateral BJT on SOI-CMOS compatible substrate," *2005 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, Hong Kong, China, pp. 317-320, Dec. 19-21, 2005.
106. D. Lee, I-S. M. Sun and W.T. Ng, "RF Model of Lateral Bipolar Junction Transistor on Silicon-on-Insulator Substrate," *2005 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, Hong Kong, China, pp. 313-316, Dec. 19-21, 2005.
107. G. Wei, O. Trescases, W.T. Ng, "A Dynamic Voltage Scaling Controller for Maximum Energy Saving Across Full Range of Load Conditions," *2005 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, Hong Kong, China, pp. 371-374, Dec. 19-21, 2005.
108. O. Trescases, G. Wei, W.T. Ng, "A Segmented Digital Pulse Width Modulator with Self-Calibration for Low-Power SMPS," *2005 IEEE International Conference on Electron*

Devices and Solid-State Circuits (EDSSC), Hong Kong, China, pp. 367-370, Dec. 19-21, 2005.

109. I.-S. M. Sun, W.T. Ng, H. Mochizuki, K. Kanekiyo, T. Kobayashi, M. Toita, H. Imai, A. Ishikawa, S. Tamura, and K. Takasuka, "Novel Ultra-Low Power RF Lateral BJT on CMOS Compatible SOI Substrate," *2005 IEEE International SOI Conference*, Honolulu, Hawaii, pp. 123-125,Oct. 3-6, 2005.
110. D. Lee, W.T. Ng, "Beamforming System for 3G and 4G Wireless LAN Applications," *2005 European Conf. on Circuit Theory and Design, Proceedings*, pp. III/137 - III/140, vol. 3, Cork Ireland, Aug. 29 - Sep. 2, 2005.
111. D. Lee, W.T. Ng, "Beam Steering System for 3G and 4G Wireless LAN Applications," *The Second IASTED International Conference On Antennas, Radar, and Wave Propagation*, Banff, Canada, pp. 267-271, July 19-21 2005.
112. I.-S. M. Sun, W.T. Ng, K. Kanekiyo, T. Kobayashi, H. Mochizuki, M. Toita, Y. Furukawa, H. Imai, A. Ishikawa, S. Tamura, and K. Takasuka, "A Novel SOI Lateral Bipolar Transistor with 30GHz Fmax and 27V BVceo for RF Power Amplifier Application," *17th International Symposium on Power Semiconductor Devices and ICs*, 2005, Proceedings, ISPSD '05, pp. 99-102, May 22-26, 2005. (**Young Researcher Award**)
113. V.W.Y. Ma, E.H.P. Xu, W.T. Ng, Y. Hara, Y. Furukawa, K. Sakai, H. Imai, T. Naito, N. Sato, S. Tamura, K. Takasuka, T. Kohno, "Design and Optimization of a 40V, 0.35µm Versatile HV-CMOS Technology," *Int. Seminar On Power Semiconductors*, ISPS'04, Prague, Czech Republic, Aug. 31 - Sep. 3, 2004.
114. X. Wu, M. Couillard, M-S. Lee, J-H. Chen, G.A. Botton, D. Landheer, Z-H. Lu, W-T. Ng, T-S. Chao, "Spatially-resolved EELS and EDS Analysis of HfO_xN_y Gate Dielectrics Deposited by MOCVD using $[(C_2H_5)_2N]_4Hf$ with NO and O_2," *Microscopy & Microanalysis 2004*, pp. 606-607, Savannah, GA, August 1-5, 2004.
115. O. Trescases, and W.T. Ng "Variable Output, Soft-Switching DC/DC Converter for VLSI Dynamic Voltage Scaling Power Supply Applications," *IEEE Power Electronics Specialists Conference PESC04*, Aachen, Germany, pp. 4149-4155, June 20-25, 2004.
116. O. Trescases, W.T. Ng, and S. Chen, "Precision Gate Drive Timing in Zero-Voltage-Switching DC/DC converter with Integrated Dead-Time-Locked-Loops," *IEEE Int. Sym. on Power Semiconductor Devices and Integrated Circuits, Tech. Digest*, Kitakyushu, Japan, pp. 55-58, May 24-27, 2004.
117. M. Lee, D. Landheer, X. Wu, M. Couillard, Z.-H Lu, W-T. Ng, and G. Botton, "Nitrogen distribution in HfO_xN_y gate dielectrics deposited by MOCVD using $[(C_2H_5)_2N]_4Hf$ with NO and O_2," *2004 MRS Spring Meeting*, San Francisco, April 12-16, 2004.
118. S. Chen, O. Trescases and W.T. Ng, "Fast Dead-Time Locked Loops for a High-Efficiency Microprocessor-Load ZVS-QSW DC/DC Converter," *EDSSC'03, Tech. Digest*, Hong Kong, pp. 391-394, Dec. 16-18, 2003. (**Best Circuit Paper**)
119. I-S. M. Sun, H. E. Xu, R. Tam, W.T. Ng, H. Mochizuki, M. Toita, T. Kobayashi, Y. Furukawa, H. Imai, A. Ishikawa, N. Saito, Y. Ueda, Y. Ueshima, S. Tamura, K. Takasuka, T. Kohno, S. Soga, K. Sako, and H. Imai, "Delay Time Constant Analysis for f_τ Optimization in RF Si/SiGe Bipolar Devices," *EDSSC'03, Tech. Digest*, Hong Kong, pp. 323-326, Dec. 16-18, 2003.
120. V.W.Y. Ma, E.H.P. Xu, W.T. Ng, Y. Hara, Y. Furukawa, K. Sakai, H. Imai, T. Naito, S. Nobuyuki, S. Tamura, K. Takasuka, T. Kohno, "Integration of Complementary EDMOS in

a Standard 0.35µm CMOS Technology for 40V Applications," *EDSSC'03, Tech. Digest*, Hong Kong, pp. 301-304, Dec. 16-18, 2003.

121. H.P. Xu, V.W.Y. Ma, I.S.M. Sun, W.T. Ng and Y.C. Liang, "Superjunction LDMOS with Drift Region Charge-Balanced by Distributed Hexagon p-islands," *EDSSC'03, Tech. Digest*, Hong Kong, pp. 313-316, Dec. 16-18, 2003.
122. S. Chen and W.T. Ng, "High-Efficiency Operation of High-Frequency DC/DC Conversion for Next-Generation Microprocessors," *The 29th Annual Conference of the IEEE Industrial Electronics Society IECON '03, Tech. Dig. Vol. 1*, Roanoke, VA, pp. 30-35, Nov. 2-6, 2003.
123. R. Azar, F. Udrea, W.T. Ng, F. Dawson, W. Findlay, P. Waind, G. Amaratunga, "Advanced Electro-thermal SPICE Modelling of Large Power IGBTs," *IEEE Int. Sym. on Power Semiconductor Devices and Integrated Circuits, Tech. Digest*, Cambridge, UK , pp. 291-294, Apr. 14-17, 2003.
124. W.T. Ng, I-S.M. Sun, H.E. Xu*, H. Mochizuki, M. Toita, T. Kobayashi, H. Imai, A. Ishikawa, N. Saito, Y. Ueda, S. Tamura, K. Takasuka, Y. Furukawa, T. Kohno, S. Soga, K. Sako, H. Imai, Y. Ueshima, "SiGe HBTs for System on Chip Applications," *Int. Sym. New Paradigm VLSI Computing, Tech. Digest*, Sendai, Japan, pp. 109-112, Dec. 12-14, 2002.
125. R. Azar, F. Udrea, W.T. Ng, F. Dawson, P. Waind, B. Findley, M. De Silva, and G. Amaratunga, "Advanced SPICE Modelling of Large Power IGBT Modules," *IAS 2002 Annual Meeting*, Vol. 4, Pittsburgh, Pennsylvania, pp. 2433-2436, October 13-18, 2002.
126. I.S.M. Sun, W.T. Ng, P.K.T. Mok, H. Mochizuki, K. Shinomura, H. Imai, A. Ishikawa, N. Saito, K. Miyashita, S. Tamura, and K. Takasuka, "A CMOS Compatible RF Bipolar Transistor Technology," *2001 Asia-Pacific Workshop on Fundamental and Application of Advanced semiconductor Devices (AWAD), Tech. Dig.*, Cheju-Do, Korea, pp. 301-307, July 5-7, 2001.
127. E.C.K. Yu, J.K. Mills, and W.T. Ng, "On-Chip Monitoring for Smart Power Integrated Circuits," *ISIC-2001, Tech. Dig.*, Singapore, pp. 446-449, Sept. 4-5, 2001.
128. D.H.S. Tam, W.T. Ng, "A Novel Mixed-Mode Adaptive Equalization System for High-Speed 2-Level PAM Signals," *Int'l Sym. on Circuits and Systems (ISCAS-2000)*, Geneva Switzerland, paper no. IV-749, June, 2000.
129. A. Khoueir, Z.H. Lu, W.T. Ng, S.P. Tay, & P.T. Lai, "RTP Formed Oxynitride Via Direct Nitridation in N_2," *Proc. IEEE Hong Kong Electron Device Meeting*, Hong Kong, pp. 104-107, June 24, 2000.
130. A. Khoueir, Z.H. Lu, W.T. Ng, S. P. Tay, "Growth of ultrathin nitride on Si (100) by rapid thermal N2 treatment," *Electrochemical Society Conference on Rapid Thermal and other Short-time Processing Technology*, Toronto, pp. 223-226, May 14-18, 2000.
131. A. Khoueir, Z.H. Lu, W.T. Ng, P.T. Lai, "Ultrathin Oxynitride Formation by Low Energy Ion-implantation," *International Conference on VLSI and CAD (ICVC)*, Seoul, Korea, pp. 229 -232, Oct 26-17, 1999.
132. W.C. Chan, P.K.T. Mok, J.K.O. Sin and W.T. Ng, "Design of Monolithic RF Power Amplifier using Bulk BiCMOS Process," *42nd Midwest Symposium On Circuits and Systems, Tech. Digest*, Vol. 1, Las Cruces, NM, pp. 10-13, Aug. 8-11, 1999.
133. D. Gradinaru, W.T. Ng, and C.A.T. Salama, "High Voltage High Frequency Silicon Bipolar Transistors," *IEEE Int. Sym. on Power Semiconductor Devices and Integrated Circuits, Tech Digest*, Toronto, Canada, pp. 293-296, May 1999. (**Best Student Paper**)

134. J. Ranaweera, I. Kalastirsky, A. Dibu-Caiole, W.T. Ng and C.A.T. Salama, "Performance Limitations of a Flash E²PROM Cell, Programmed with Zener Induced Hot Electrons," *NVSM Workshop, Tech. Dig*., Monterey CA, February 9-12, 1997.
135. J. Cai, J.K.O. Sin, V.M.C. Poon, W.T. Ng, and P.T. Lai, "A Fast Switching Insulated-gate p-i-n Diode Controlled Thyristor Structure," *IEEE Int'l Conference on Semiconductor Electronics, Tech. Dig*., Malaysia, pp. 122-125, 1996.
136. Z. Xu, P.T. Lai, and W.T. Ng, "Charge Trapping Properties of N2O-Treated NH3-Nitrided Oxides Under High-Field Stress," *IEEE Region 10 Conference on Microelectronics and VLSI TENCON'95, Tech. Dig.*, Hong Kong, pp. 256-259, Nov. 6-10, 1995.
137. J. Cai, J.K.O. Sin, W.T. Ng, and P.T. Lai, "Latch-up Characteristics of a Trench-Gate Conductivity Modulated Power Transistor," *IEEE Region 10 Conference on Microelectronics and VLSI TENCON'95, Tech. Dig*., Hong Kong, pp. 424-427, Nov. 6-10, 1995.
138. Z. Xu, P.T. Lai, and W.T. Ng, "A Novel Techniques of N_2O-Treatment on NH_3-Nitrided Oxide for Fabricating Gate Oxide in n-MOSFETs," *International Conference on VLSI and CAD*, Seoul, Korea, 1995.
139. Z. Xu, P.T. Lai, and W.T. Ng, "Off-State Gate Leakage Current in N-Channel MOSFET's with Gate Dielectrics Prepared by Different Techniques," *Proc. IEEE Hong Kong Electron Device Meeting*, pp. 19-22, Jul. 1, 1995.
140. Z. Xu, P.T. Lai, and W.T. Ng, "Electrical Performance and Reliability of n-MOSFET's with Gate Dielectrics Fabricated by Different Techniques," *Proc. IEEE Hong Kong Electron Device Meeting*, Hong Kong, pp. 18-21, Jul. 18, 1994.
141. O.K. Kwon, T. Efland, S. Malhi, W. Bailey, W.T. Ng, and M. Torreno, "An Optimized RESURF Lateral Triple-Diffused MOS (LTDMOS) Device Module Compatible with Advanced Logic Processes," *IEDM Tech. Dig.*, pp. 237-240, 1992.
142. O.K. Kwon, T. Efland, W.T. Ng, S. Malhi, R. Todd and John K. Lee, "Optimized 60-V Lateral DMOS Devices for VLSI Power Applications," *Sym. on VLSI Technology, Tech. Digest*, , Oiso, Kanagawa Japan, pp. 115-116, May 28-30, 1991.
143. W.T. Ng and C.A.T. Salama, "CMOS Compatible Complementary SINFETs," *Proc. Sym. on High Voltage and Smart Power ICs*, Los Angeles, pp. 96-103, 1989.
144. W.T. Ng, C.A.T. Salama and J.K.O. Sin, "P-channel Schottky Injection Field Effect Transistors," *IEDM Tech. Dig*., pp. 770-773, 1987.

Other non-refereed publications

145. Joshua Chung, R. McKenzie and W.T. Ng, "A Comparison between GaN and Silicon Based Class D Audio Power Amplifiers with Pulse Density Modulation," *13th IEEE International Conference on Solid-State and Integrated Circuit Technology* (ICSICT-2016) Hangzhou, China, Oct. 25 - 28, 2016.
146. R. McKenzie and W.T. Ng, "Class D Audio Amplifiers - Comparison of Modulation Schemes using GaN and Silicon Output Stages," *2016 CMOS Emerging Technologies Workshop*, Montreal, PQ, Canada, May 25-27, 2016. (**Invited Paper**).
147. A. Shorten and W.T. Ng, "SPRUCE, an Embedded Compact Stack Machine for IGBT Power Modules," *IEEE International Symposium on Multiple-Valued Logic* (ISMVL 2016), May 18-20, 2016, Sapporo, Japan. (**Invited Paper**).

148. W.T. Ng, "Power Management and Gate Driver ICs for Future Power Semiconductor Devices," *SEMICON Korea* (*System LSI Forum*), Seoul, Korea, Jan 29, 2016. (**Invited Paper**)
149. W.T. Ng, "An Embedded Low Power RISC CPU for Power Management Applications," *2015 The International Workshop on Emerging Technologies of Microelectronics and Their Application to IoT Paradigm*, Honolulu, Hawaii, December 10-11, 2015. (**Invited Paper**)
150. W. T. Ng, "Power FINFET, a Novel Superjunction Lateral Power MOSFET," *2011 CMOS Emerging Technologies Workshop*, Whistler, BC, Canada, June 15-17, 2011. (**Invited Paper**)
151. W.T. Ng, and A. Yoo, "Advanced Lateral Power MOSFETs for Power Integrated Circuits," *10th International Conference on Solid-State and Integrated-Circuit Technology (ICSICT 2010)*, pp. 859 - 862 Shanghai, China, Nov. 1-4, 2010. (**Invited paper**)
152. W.T. Ng, J. Wang, O. Trescases, and A. Prodić, "Power Management for VLSIs — a Power Electronics Perspective," *The 4th International Symposium on Information Electronics Systems*, Sendai Excel Hotel Tokyu 3F, Sendai, Japan, July 7-8, 2010. (**Invited paper**) http://www.ecei.tohoku.ac.jp/gcoe/
153. W. T. Ng, J. Wang, Y. Zhao, A. Akhavan Fomani, "Circuit Techniques for High Performance Integrated DC-DC Converters," *2010 CMOS Emerging Technologies Workshop*, Whistler, BC, Canada, May 19-21, 2010. (**Invited Paper**)
154. W.T. Ng, J. Wang, K. Ng, A. Prodić, T. Kawashima, M. Sasaki, and H. Nishio, "Digitally Controlled Integrated DC-DC Converters with Fast Transient Response," *IEEE Int. Sym. Radio-Frequency Integration Technology (RFIT2009)*, Singapore, December 9-11, 2009. (**Invited paper**)
155. W.T. Ng, M. Chang, A. Yoo, J. Langer, T. Hedquist, H. Schweiss, "High speed CMOS output stage for integrated DC-DC converters," *9th International Conference on Solid-State and Integrated-Circuit Technology (ICSICT 2008)*, pp. 1909-1912, Beijing, China, Oct. 20-23, 2008. (**Invited paper**)
156. W.T. Ng, O. Trescases, and G. Wei, "Output Stages for Integrated DC-DC Converters and Power ICs," *2007 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, pp. 91-94, Tainan, Taiwan, ROC, Dec. 19-21, 2007. (**Invited paper**)
157. H. Wang, A. Yoo, H.P.E. Xu, W.T. Ng, K. Fukumoto, A. Ishikawa, H. Imai, K. Sakai, and K. Takasuka, "A Floating RESURF EDMOS with enhanced Safe Operating Area," *International Workshop on The Physics of Semiconductor Devices*, Mumbai, India, December 16-20, 2007. (**Invited paper**)
158. W.T. Ng, O. Trescases, and G. Wei, "Integrated Power Stages For Switched Mode Power Supplies," *Int. Sym. Power Electronics 2007*, Novi Sad, Republic of Serbia, Nov. 7-9, 2007. (**Invited paper**)
159. O. Trescases, G. Wei, A. Prodic, W. T. Ng, K. Takasuka, H. Nishio, "Power Management for Portable Audio Applications," *2007 CMOS Emerging Technologies Workshop*, Whistler, BC, Canada, July 11-13, 2007. (**Invited Paper**)
160. W.T. Ng, O. Trescases, G. Wei, "Integrated Switched Mode Power Supplies Using Digital Controllers," International Conference on Solid-State and Integrated Circuits Technology, Shanghai, China, October 24-26, 2006. (**Invited Paper**)

161. W.T. Ng, O. Trescases, "Integrated Digitally Controlled Switched Mode Power Supplies for Portable Applications," *2006 Emerging Technologies Workshop*, Banff, AB, Canada, July 19-21, 2006. (**Invited Paper**)
162. O. Trescases, and W.T. Ng, "Power Management for Modern VLSI Chips and Leakage Power Reduction Techniques," *International Conference on Solid-State and Integrated Circuits Technology*, Beijing, China, pp. 1412-1415, October 18-21, 2004. (**Invited Paper**)
163. O. Trescases, S. O'Loughlin, and W.T. Ng, "A Smart Motor Controller for E-bike Applications," *IEEE Canadian Review*, No. 43, pp. 16-19, Spring 2003. (**Invited paper**)
164. D. Prince, H. Xiao, and W.T. Ng, "A 100V, 3 Phase Gate Driver with integrated digital PWM Generation and Current Sampling," *PCIM Europe 2002*, Nuremberg, Germany, May 14-16, 2002.
165. I.S.M. Sun, W.T. Ng, P.K.T. Mok, H. Mochizuki, K. Shinomura, H. Imai, A. Ishikawa, N. Saito, K. Miyashita, S. Tamura, and K. Takasuka, "RF Bipolar Transistors in CMOS Compatible Technologies," *Proc. IEEE Hong Kong Electron Device Meeting,* Hong Kong, pp. 108-111, June 30, 2001. (Invited paper).

Short Courses

166. W.T. Ng, "Integrated Power Converters – Basic Concepts," *25th International Symposium on Power Semiconductor Devices and ICs* (*ISPSD '13*), Kanazawa, Japan, May 26-30, 2013. (Invited, Short Course)
167. W.T. Ng, "Energy Efficient Digital Class D Audio Power Amplifiers," *IEEE Singapore Solid-State Circuits Chapter*, Singapore, October 10-11, 2012. (Two Days Short Course)
168. W.T. Ng, "Smart Power ICs and Devices for Power Management Applications," *IEEE Singapore Solid-State Circuits Chapter*, Singapore, November 24-25, 2011. (Two Days Short Course)
169. W.T. Ng, "Integration of Low Power, High-Frequency Digitally Controlled SMPS—Power Management for Portable Applications," *Institute of Microelectronics (IME) and IEEE Singapore Solid-State Circuits Chapter*, Singapore, June 26-27, 2007. (Two Days Short Course)
170. A. Prodic, W.T. Ng, "IC Implementation of High-Frequency Digitally Controlled SMPS," *Applied Power Electronics Conference and Exposition, APEC'07 Prof. Education Seminars*, Anaheim, CA, Feb. 25, 2007.

Books

1. *Integrated Power Devices and TCAD Simulation*. Yue Fu, Zhanming Li, Wai Tung Ng, Johnny K.O. Sin, CRC Press, 2014.

   ISBN 978-1-4665-8383-2

Patents

1. *High Speed Orthogonal Gate EDMOS Device and Fabrication*. H. Wang, H.P.E. Xu, W.T. Ng, Jan. 22, 2013, U S Patent US 8,357,986 B2.

   This invention involve a unique orthogonal gate structure that can minimize the Miller capacitance (C_{GD}) in lateral power MOSFET, resulting in very high switching speed and low gate drive loss.

2. *Digitally Controlled Integrated DC-DC Converter With Transient Suppression*. W.T. Ng, J. Wang, K. Ng, H. Nishio, M. Sasaki, T. Kawashima, Dec. 8, 2011, US Patent US 8,441,242 B2.
3. *Distortion suppression circuit for digital class-D audio amplifier*. G. Wei and W.T. Ng, Aug. 17, 2010, Patent US7,777,562 B2.

   This invention provides a unique method of suppressing the harmonic distortion caused by non-ideal switching characteristics of the output stage in class D power amplifier. This work is particular useful for audio amplifiers with a long latency in their digital signal path.
4. *Circuit and method for reducing electromagnetic interference*. O. Trescases, W.T. Ng, March 11, 2008, US Patent 7,342,528 B2.

   This is a method to achieve variable frequency operation in a digitally controlled switch mode power supply for the purpose of reducing Electromagnetic Interference (EMI).
5. *Method of fabricating a fast programmable flash E^2PROM cell*. J. Ranaweera; I. Kalastirsky; E. Gulersen; W.T. Ng; and C.A.T. Salama, March 7, 2000, United States Patent 6,034,896

   This E^2PROM relies on zener and/or avalanche breakdown of the modified source and drain to substrate junctions to generate hot electrons for programming. Since the electric field generated is much larger than conventional designs, programming can be significantly faster and at reduced voltage levels.
6. *Windowed source and segmented backgate contact linear geometry source cell for power DMOS processes*. Efland; Taylor R. (Richardson, TX); Jones, III; Roy C. (Dallas, TX); Kwon; Oh-Kyong, (Seoul, Republic of Korea); Smayling; Michael C. (Missouri City, TX); Malhi; Satwinder (Garland, TX); Ng; Wai T. (Ontario, Canada), Aug. 12, 1997, United States Patent 5,656,517.
7. *Windowed and segmented linear geometry source cell for power DMOS processes*. Efland; Taylor R. (Richardson, TX); Jones, III; Roy C. (Dallas, TX); Kwon; Oh-Kyong, (Seoul, Republic of Korea); Smayling; Michael C. (Missouri City, TX); Malhi; Satwinder (Garland, TX); Ng; Wai T. (Ontario, Canada), Dec. 17, 1996, United States Patent 5,585,657.
8. *Lateral double diffused insulated gate field effect transistor and fabrication process*. Oh-Kyong (Plano, TX); Efland; Taylor R. (Richardson, TX); Malhi; Satwinder (Garland, TX); Ng; Wai T. (Thornhill, Canada), Nov. 26, 1996, United States Patent 5,578,514.
9. *Resurf lateral double diffused insulated gate field effect transistor*. Kwon; Oh-Kyong (Plano, TX); Efland; Taylor R. (Richardson, TX); Malhi; Satwinder (Garland, TX); Ng; Wai T. (Thornhill, CA), Apr. 11, 1995, United States Patent 5,406,110.
10. *Method of fabricating performance lateral double-diffused MOS transistor*. Malhi; Satwinder (Garland, TX); Ng; Wai T. (Plano, TX), Jan. 17, 1995, United States Patent 5,382,535.
11. *Method for forming a self-aligned lateral DMOS transistor*. Ng; Wai T. (Thornhill, CA), Kwon; Oh-Kyong (Seoul, Republic of Korea), Nov. 29, 1994, United States Patent 5,369,045.
12. *Lateral double diffused insulated gate field effect transistor fabrication process*. Kwon; Oh-Kyong (Plano, TX); Efland; Taylor R. (Richardson, TX); Malhi; Satwinder (Garland, TX); Ng; Wai T. (Thornhill, CA), Apr. 26, 1994, United States Patent 5,306,652.
13. *Performance lateral double-diffused MOS transistor*. Malhi; Satwinder (Garland, TX); Ng; Wai T. (Plano, TX), Apr. 19, 1994, United States Patent 5,304,827.

Current Research Direction

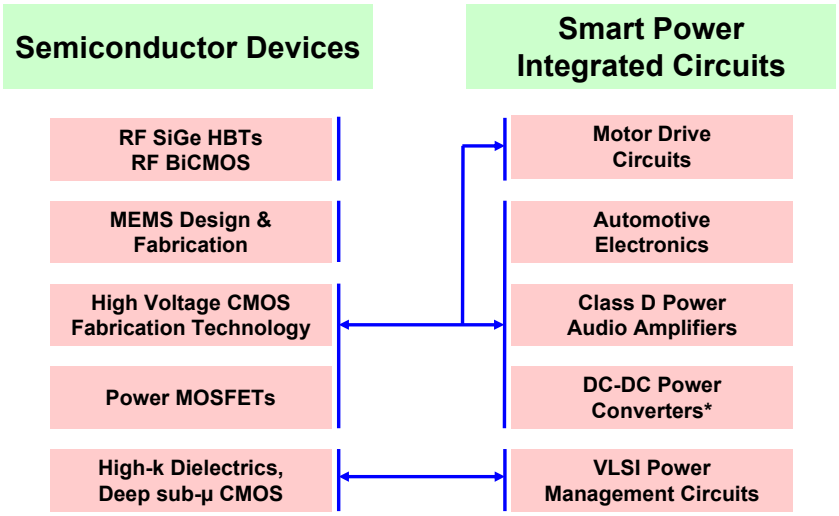
Our research group is currently working in a wide spectrum of areas, enabling the integration of power devices to form single chip systems. Our group has worked extensive in the development of CMOS compatible HV fabrication processes for automotive and consumer applications in the 40-100V range. We also has on-going collaboration with our industrial research partners to develop discrete and integrated power MOSFETs, silicon, GaN and SiGe based BiCMOS fabrication processes for smart power ICs and wireless applications, respectively.

In the past few years, we have also focused in the design and implementation of VLSI power management circuits. This includes the demonstration of integrated soft-switching topology with predictive dead-time control and a practical DVS (Dynamic Voltage Scaling) system in 2004. We are also working on the integrated DC-DC converters with digital control. We were able to demonstrate an integrated DC-DC converter with dynamically adjustable power transistor size for power conversion efficiency optimization at ISPSD'06 for the first time. This work allowed our group to win best student paper award for the 3rd time at this conference. We also have activities in integrated digital Class D power audio amplifiers with distortion suppression feedback to achieve highly competitive performance. Currently, we are working on Class D audio amplifiers with GaN power transistors for the output stage.

Given the fact that the nature of our work is mainly experimental based. This includes exploring the possibilities of adding new device modules such as RF power transistors and/or high voltage (HV) transistors to enhance the functional features of current CMOS/BiCMOS processes. It is very critical to collaborate with industrial partners. Our industrial collaborators are the key reasons that allow us to implement device and circuit ideas in non-standard CMOS fabrication processes with large die size.

Power and thermal management is currently an intensely pursued field. In addition to integrated digitally controlled DC-DC converters for portable power applications, we are also working on fully digital and synthesizable on-chip temperature sensors for monitoring the thermal profile of large VLSI dies. Another emerging area of importance is the development of GaN on Silicon power transistors. Power GaN HEMTs have the potential advantages of lower on-resistance, higher breakdown voltage, higher speed and higher operating temperature. Our group is currently working closely with an industrial sponsor to develop driving techniques to fully exploit the capabilities of these devices without introducing unwanted switching losses and electromagnetic interference.

The diagram below is a quick snap shot of the research activities in our group.



Administrative Experience

Significant portion of my administrative experience began in 2005 when I took office as the Associate Chair of Undergraduate Studies at the Department of Electrical and Computer Engineering, reporting directly to the chair of the department. We are a sizable department with approximately 1400 undergraduate students and 75 full time faculty members. My administrative responsibilities include the delivery of a nation leading flexible ECE curriculum (where students are can choose their courses for 3rd and 4th year), CEAB (Canadian Engineering Accreditation Board) accreditation, student affairs, academic curriculum and policies, teach assignment, the hiring of all stipend instructors and teaching assistance, management of our teaching laboratories, negotiation with other departments and Faculties on teaching resources. Frequent interactions with various administrative offices ranging from the Governing Council, Faculty Registrar to student clubs allowed me to become familiar with the operation of the University.

The Associate Chair position is a three years limited term appointment. In 2008, I was re-appointed with a 2nd three years term. This allowed me to continue with the smooth roll-out of our Undergraduate Program. Notability, our office has led the in-house development of an on-line academic credit tracking system that allows individual students to verify whether if they are meeting program and accreditation requirement based on their course selection.

The Associate Chair position has helped me to appreciate the importance of transparent administration, the enhancement of students' learning experience, alumni relationship, and teaching. In fact, my own personal teaching evaluation has steady improved during my term of office. I will continue to serve as the Associate Chair until 06/2011.

Since 2014, I am serving as the directory for the University of Toronto's Nanofabrication Centre (TNFC), an open access research facility for both domestic and international researchers. My duties include the supervision of five technical staff and one administrative staff to maintain the daily operation of three cleanrooms at the university. In addition, I am responsible for balancing the budget between user fees, university support, research grants, salaries, repair and maintenance.

My other notable administrative experience include volunteer service as the Vice Chair of the IEEE Toronto Section (2008-2011), past board of directors for Auto21 — a Networks Centres of Excellence in Canada (2006-2007), and long term member of organizing committees for various IEEE conferences such as EDSSC and ISPSD. In addition, serving on the Scientific Advisory Board for the VIRTUS IC Design Centre at NTU, Singapore gave me the opportunity to develop my ability to provide expert guidance and feedback to a large organization.

c) University Committees and Administrative Activities

Director, Toronto Nano-Fabrication Centre (01/14 to 06/15, 07/16 to present)

Administrative duties include the daily operation and infrastructure development of the Toronto Nano-Fabrication Centre, a University of Toronto open access research facility.

http://tnfc.utoronto.ca/

Director, ECE Undergraduate Curriculum Matters Committee (07/13 to 06/15)

Administrative duties include the constant review and delivery of the ECE undergraduate curriculum.

Vice Chair, APSC Faculty Curriculum Committee (07/13 to 06/15)

Administrative duties include the constant review, delivery of the undergraduate curriculum for the Engineering Faculty.

ECE Associate Chair, Undergraduate Studies (07/05 to 06/2011)

Administrative duties include all aspects on the delivery of the Electrical and Computer Engineering undergraduate program, monitoring and update departmental/faculty policies, management of teaching resources, and student affairs.

ECE Electronics Group Search Committee, Chair (09/01 to 08/02)
ECE Nano Engineering Search Committee, Chair (09/02 to 08/03)

I was the chair of the search committee for the Electronics Group and Nano Engineering in 01/02 and 02/03, respectively. The primary responsibility was to review all applications, organize meeting with the search committee, keep records of all applicants, coordinate with all applicants, arrange and host interviews with promising candidates.

IEEE Student Branch Counselor, U of T (09/97 to 08/08)

The responsibility of the counselor is to provide assistance and guidance to the IEEE Student Branch Executive Committee in organizing student events, career talks, membership drive and nomination for scholarships.

ECE Graduate Studies Committee (09/94 to 08/99)

The responsibility of this committee member is to co-ordinate the admission evaluation of applications for graduate studies with the department. In particular, I process all the applications submitted to the *Electronics Group*. It also involves frequent direct correspondence with potential graduate students, organizing recruiting functions, and the monitoring of admission decisions made by the group.

In addition, the committee is also involved in the planning of stream-lined graduate programs, Ph.D. qualifying exams, etc.

ECE Undergraduate Student-Staff Committee (09/94 to 04/99)

This committee works closely with undergraduate students in dealing with their academic and social concerns. Monthly meetings with student representatives provide the opportunity

for free dialog. This committee provides direct feedback from the students to the department toward curriculum planning and to individual professors on their teaching methods.

ECE Enabling Technology Committee (09/94 to 03/95)

This committee is a task force to identify the enabling technology that is relevant and critical for the growth of the department in the next 5 to 10 years. The members are required to survey the current status of leading edge technology and make recommendation to the department chair. This exercise is very important in road map planning for the ECE department.

d) Other Professional Activities

IEEE Electron Device Society, Technical Committee (2015/01 to present)

Area: Power Devices and ICs Committee

http://eds.ieee.org/technical-committees/eds-power-devices-a-ics-technical-committee.html

IEEE Electron Device Letters, Associate Editor (12/09 to present)

Area: Solid-State Power and High Voltage Devices

http://eds.ieee.org/edl/edl-editor-in-chief-and-editors.html

IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD) Technical Committee, Member (09/04 to present)

http://www.ecse.rpi.edu/conf/ispsd2005/
http://www.ispsd2006.it/
http://www.ispsd07.org/
http://www.ecse.rpi.edu/conf/ispsd08/
http://www.ispsd09.com/
http://www.ispsd2010.com/
http://www.ispsd2011.com/
http://www.ispsd2012.com/
http://www.ispsd2013.com/
http://www.ispsd.org/
http://www.ispsd2015.com/

ISPSD is recognized as the premier conference on smart Power Integrated Circuits. I was invited to participate as a technical program committee member after our paper presentation in ISPSD'04. The primary responsibility in the committee is paper selection.

In 2011, I am responsible for organizing the short courses.
http://www.ispsd2011.com/index-files/shortcourse.htm

In 2014, I am the publicity chair.
http://www.ispsd.org/#!/page_committee

In 2015, I am the Sponsorship/Exhibition Chair.
http://www.ispsd2015.com/about-ispsd-2015/committee/organizingcommittee/

IEEE Conference on Electron Devices and Solid-State Circuits, Committee

Hong Kong, Dec. 16-18, 2003
Hong Kong, Dec. 19-21, 2005
Tainan, Taiwan, ROC, Dec. 19-21, 2007
Hong Kong, Dec. 8-10 2008
Xian, China, Nov. 25-27, 2009
Hong Kong, Dec. 15-17, 2010
Tianjin, Nov. 17-18, 2011
Bangkok, Dec. 3-5, 2012
Hong Kong, Jun. 3-5, 2013
Hong Kong, August 3-5, 2016

The EDSSC'03 Conference is organized for celebrating the 10th Anniversary of IEEE EDS Hong Kong Chapter and the establishment of new EDS/SSCS joint Chapter in Hong Kong. It has evolved into a major conference in electron devices and solid-state circuits in the Far East. I have been an active supporter of this conference since its inception.

In 2003 and 2005, I served as the Vice Chair.

In 2007, I served as the International Advisory Committee Chairs.

In 2008, EDSSC was held in Hong Kong. I served as Technical Program Co-Chair

In 2009, EDSSC was held in Xian China. I served as the Publication Co-Chair

In 2010, EDSSC was held in Hong Kong. I served as Int. Advisory Committee Co-Chairs
In 2016, EDSSC will be held in Hong Kong. I am serving as the General Co-Chairs

VIRTUS IC Design Centre of Excellence, Nanyang Technological University (NTU) Singapore (2012 to 2014) http://www.virtus.eee.ntu.edu.sg/

Member of the Scientific Advisory Board, providing guidance and progress review on an annual basis.

University of Hong Kong, External Examiner for CE and EComE programs (2012 to 2014)

External examiner for the Computer Engineering and Electronic and Communications Engineering undergraduate programs

Professional Engineer Ontario, Examiner in Electronics Area (2005-present)

Setup and mark 07-Elec-A5, Electronics and 07-Elec-B5, Advanced Electronics exams, tow times per year.

CCECE 2011, General Chair

The 24th Canadian Conference on Electrical and Computer Engineering is the flagship event for IEEE Canada. In 2011, the IEEE Canada Central Region, along with the Toronto, Hamilton, Kingston, Kitchener/Waterloo, London, and Peterborough Sections, are hosting this important conference at Niagara Falls, ON. CCECE is Canada's premier networking forum for leading researchers in the board area of Electrical and Computer Engineering.

IEEE Toronto Section, Chair (01/2010 to 12/2011)

In charge of the operation and organization of the IEEE Toronto Section. Administrative duties include regular communication with executive committee members, event planning and budgetary issues.

IEEE Toronto Section, Vice Chair (01/2008 to 12/2009)

Assisting the chair (Dr. Alex Bot) in the operation and organization of the IEEE Toronto Section. Administrative duties include regular communication with executive committee members, event planning and budgetary issues.

IEEE Student Activity Chair, Toronto Section (08/2000 to 12/2007)

The responsibility of the student activity chair is to communicate among the various IEEE Student branches in the Toronto Section and the IEEE Toronto Section Committee, and to provide assistance and guidance in organizing student events, career talks, membership drive and nomination for scholarships. In addition, I was required to give talks at other universities and colleges in the Toronto area to promote IEEE studentship.

Board of Directors, Auto21 NCE (10/2006 to 09/2007) http://www.auto21.ca

I was elected to be the only academic member to serve on the board of directors in Auto21 NCE. My primary duty is to represent all the Canadian researchers and to monitor the operation of the network.

Program Advisory Committee for Electronics Engineering Technology (EET), Centennial College (09/2007 to present)

Program Advisory Committee for the Applied Degree in Software Development and Management, Centennial College (09/2001 to 05/2002)

Program Advisory Committee for Electronics Engineering Technology and Technician, Centennial College (09/2001 to 05/2002)

I was a committee member in the development of two brand new technical programs at Centennial College in 01/02. My duties included drafting the curriculum for these two programs, exchanging inputs from other committee members, solicit ideas from students and the industrial sectors. The structures of these two programs were finalized over a period of 8 months and are currently being offered at Centennial College.

International Meeting on “Multiple-Valued VLSI Processors for Intelligent Integrated Systems” — panel member (04/1997 to 04/1999)

This is a three years committee sponsored by Tohoku University, Dept. Computer & Mathematical Sciences, Sendai Japan and the Japanese government. Meetings are held annually, by invitation to the panel members, to discuss the research directions on Multiple-Valued VLSI technologies.

Member, IEEE (since 1990), Senior Member, IEEE (since 08/2004)

Member, Professional Engineer Ontario (since 1997)

Member, SAE (Society of Automotive Engineers) International (since 2008)

U.S. Federal Aviation Administration private pilot license (since 1991)

Qualify to fly single engine airplanes under VFR (visual flight rules) condition.

Member, Advanced Driving Instructor, Porsche Club of America (since 1997)