Prof. Judy L. Hoyt

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Education:

Ph. D. in Applied Physics, Stanford University, (1987)

B.S. in in Physics and Applied Mathematics, University of California, Berkeley, (1981)

Biography:

Judy L. Hoyt is a Professor in Electrical Engineering and Computer Science (EECS) at MIT. Dr. Hoyt received the B.S. degree in Physics and Applied Mathematics from the University of California, Berkeley in 1981, and the Ph.D. degree in Applied Physics from Stanford University in December, 1987. From 1988 through 1999 Dr. Hoyt was a Senior Research Scientist in Electrical Engineering at Stanford University. In January 2000, she joined the faculty at MIT in the Department of Electrical Engineering and Computer Science. She is presently serving as Associate Director within the Microsystems Technology Laboratories (MTL).

Publications:

Books

J.L. Hoyt, "Substitutional Carbon Incorporation and Electronic Characterization of Si1-yCy and SiGeC Grown by RTCVD," book chapter for volume edited by S. Pantelides and S. Zollner, Silicon-Germanium Carbon Alloys, Growth, Properties and Applications, (Taylor & Francis, NY, 2002), pp. 59–89.

Co-edited Conference Proceedings, Strained Layer Epitaxy Materials, Processing, and Device Applications, edt. E. Fitzgerald, J. Hoyt, K.-Y. Cheng and J. Bean, Symposium Proceedings, Vol 379, (Mat. Res. Soc., Pittsburgh, PA, 1995).

J.L. Hoyt, "Rapid Thermal Processing-based Epitaxy," book chapter in Rapid Thermal Processing: Science and Technology, edt. by R.B. Fair, (Academic Press, San Diego, CA, 1993), pp. 13-43. Articles

Articles

T. Yu, U. Radhakrishna, J.L. Hoyt, and D.A. Antoniadis, "Quantifying the Impact of Gate Efficiency on Switching Steepness of Quantum-Well Tunnel-FETs: Experiments, Modeling, and Design Guidelines," IEDM, Dec. 2015.

E. Polyzoeva, S.A. Hadi, A. Nayfeh, and J. L. Hoyt, "Reducing optical and resistive losses in graded silicon-germanium buffer layers for silicon based tandem cells using step-cell design," AIP Advances 5, 057161 (2015).

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Thompson, S. E., Sun, G., Choi, Y. S., & Nishida, T. (2006). Uniaxial-process-induced strained-Si: Extending the CMOS roadmap. *IEEE Transactions on Electron Devices*, *53*(5), 1010-1020.

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