PAUL D. FRANZON

B. BRIEF RESUME

1. Education

- Doctor of Philosophy, Electrical and Electronic Engineering 1989, University of Adelaide, Australia . Advisor: Kamran Eshraghian.
- Bachelor of Engineering with First Class Honours, Electrical and Electronic Engineering: 1984, University of Adelaide, Australia
- Bachelor of Science, Physics and Mathematics: 1983, University of Adelaide, Australia.

2. Professional Experience

- Assistant Professor, Associate Professor, Professor, and Distinguished Professor North Carolina State University, Department of Electrical and Computer Engineering, Raleigh, North Carolina, January 1989 – present
- Technical Director, Rambus (part time/consulting), 2009-11, Chapel Hill, NC.
- Cofounder, LightSpin Technologies Inc., 2001-. Vice-President of Engineering, 2001-2002, Raleigh NC.
- PhD Candidate, University of Adelaide, Department of Electrical and Electronic Engineering, Adelaide, South Australia, Australia, April 1987 - December 1988.
- Director and Co-Founder, Network Communications Pty. Ltd., Adelaide, South Australia, Australia, April 1987 - April 1989.
- Consultant, AT&T Bell Laboratories, Holmdel NJ, January 1986 - April 1987.
- PhD Candidate, University of Adelaide, Department of Electrical and Electronic Engineering, Adelaide, South Australia, Australia, August 1984-December 1985.
- Engineer, Defence Science and Technology Organization, Salisbury, South Australia, Australia, January 1984--July 1984
- Intern, Defense Science and Technology Organization, Salisbury, South Australia, Australia, December 1982--March 1983.
- Intern, Telecom Australia, Adelaide, South Australia, Australia, December 1981-March 1982.
- Infantry Soldier and Officer, (Ranks held: Private - Captain), Royal Australian Infantry Corps, Australian Army Reserve, December 1979 - December 1991.

3. Scholarly and Creative activities

Type	*Number*
Books	3
Solution Manuals	1
Edited Book chapter	15
Refereed Journal article	88

Conference Paper (refereed)	220
Patents granted	10

4. Membership in professional organizations

Fellow, Institute of Electrical and Electronic Engineers, 1984-
Member, IMAPS
Member, SPIE
Member, Association of Computing Machinery

5. Scholarly and professional honors

- NCSU Innovator of the Year Award, 2015
- College of Engineering Board of Governor's Award, 2014
- NRL Alan Berman Research Publication Award, 2008
- Babbage Award, Synopsys, 2008
- Fellow of the IEEE, 2006
- Alcoa Research Award, 2005
- ECE Graduate Teacher of the year award, 2007
- ECE Most Helpful Teacher of the year award, 2007
- ECE Teacher of the year award, 2006
- ECE Graduate Advisor of the year award, 2006
- Alumni Undergraduate Distinguished Professor, 2003-2005.
- Graduate teacher of the year, ECE department, 2005
- NSW Australia Expatriate Scientist Award, 2003
- Selected to the NCSU Academy of Outstanding Teachers, 2001
- First round prize winner, SRC copper challenge, 2000.
- Teacher of the Year Award, presented by the IEEE Student Branch, 1997
- National Science Foundation Young Investigator's Award, 1993.
- 13 prizes while a student at the University of Adelaide

6. Professional service on campus

- Member, STRAG 2003-2005
- Instructor, PE preparation course 1995-2000

7. Professional service off campus

- Consultant to DARPA, Thermal issues, 2012-
- Consultant to Paul Hastings, OMM, KL Gates, Samsung, Micron and SK Hynix, 2015-, Patent issues including IPR, (District of Delaware, CA N. 14-cv-01432-LPS-CJB and related cases)
- Consultant to LDKM and AVT, Patent issues, 2013- (New York Southern District, 1:11-cv-06604-CM, with 08908 and 00918)
- Consultant to Skiermont Puckett and Spherix, Patent issues including IPR, 2014-2015, (Texas Northern District, 3:13-cv-3494-M and 3496)

- Consultant to Haliburton, 2014
- Consultant to DARPA, Exascale Computing Study, 2007-9.
- Consultant to Rambus, Semiconductors, 2009-12
- Consultant to Techsearch, 2008.
- Consultant, NTU, 2004-9. ASIC Design.
- Consultant to Tessera, 2009. 3DIC advising.
- Consultant, Irvine Sensors, 2006. Secure chip design.
- Consultant, Cisco Systems, 2006, Signal Integrity.
- Consultant, Talon Logic, 2005. Secure system Design.
- Consultant to O'Malveny and Meyers, 2000-2002, Patent issues.
- Consultant to Venture 2000, 2000, Due Diligance.
- Consultant to CAPPS, 1999-2000, IP Development.
- Consultant to Sofrent, 1999-2000, IP Development.
- Consultant to Ericsson, 1997, Synthesis Methodology.
- Consultant to Cadence, 1996. Evaluated possible company acquisition.
- Consultant to Polychip, 1994 - 2000. Circuit Design.
- Consultant to Square-D, 1996. Interconnect Design.
- Consultant to Mentor Graphics, 1995, 1996. Technical advisory board.
- Consultant to Cadence Design Systems, 1992, 1996. Technical advisory board.
- Consultant to DCT, 1995-1996. ASIC Design.
- Consultant to Techsearch International, 1989-1991. Report Preparation.
- Consultant to BNR, HP, Sun. 1992-4. Interconnect Design.
- Consultant to MCNC, 1989. CAD

II. TEACHING AND MENTORING OF UNDERGRADUATE AND GRADUATE STUDENTS

A. TEACHING EFFECTIVENESS

1. Courses Taught

Course	When	Enrollment	Instructor effectiveness	Course excellence
ECE 464-001	S 15	19	4.3	4.3
ECE 520-001	S 15	119	4.3	4.3
ECE 520-601	S 15	11	4.8	5.0
ECE 520-603	S 15	3		
ECE 520-651	SuI 15	16	4.6	4.6
ECE 733-001	S 15	50	4.5	4.3
ECE 464-002	F 15	21	4.6	4.5
ECE 520-002	F 15	129	4.6	4.5
ECE 520-601	F 15	7	5.0	5.0
ECE 634-602 ASIC Design	F 2014	2		

ECE 520-601	S1 2014	9		
ECE 464-001	S 2014	10	4.5	4.5
ECE 520-001	S 2014	111	4.5	4.5
ECE 520-601	S 2014	9	4.5	4.5
ECE 733-001	S 2014	49	4.7	4.4
ECE 520-601	F 2013	2		
ECE 520-651 ASIC Design	SII '13	7	4.3	4.3
ECE 464-051 ASIC Design	SII '13	6	4.5	4.5
ASIC Design OOC	SII '13	635		
ECE 733 Digital Electronics	S 2013	62	4.5	4.3
ECE 520-001 ASIC Design	S 2013	136	4.6	4.5
ECE 464 ASIC Design	S 2013	(with above)	4.3	4.3
ECE 520-651 ASIC Design	Sum '12	18		
ECE 733 Digital Electronics	S 2012	52	4.2	4.2
ECE 520-601	S 2012	12	4.3	4.2
ECE 520-001 ASIC Design	S 2012	116	4.3	4.3
ECE 464 ASIC Design	S 2012	14	4.3	4.3
ECE 406 Des. Complex Systems	F 2011	58	4.6	4.6
ECE 520-651 ASIC Design	Sum '11	13	4.2	4.2
ECE 733 Digital Electronics	S 2011	18	4.5	4.5
ECE 520-601	S 2011	12	4.3	4.2
ECE 520-001 ASIC Design	S 2011	75	4.5	4.5
ECE 464 ASIC Design	S 2011	25	4.5	4.5
ECE 406 Des Complex Systems	F 2010	75	4.6	4.6
ECE 733 Digital Circuits 001	S 2010	36	4.3	4.2
ECE 733 Digital Circuits 601	S 2010	3	5.0	5.0
ECE 520 ASIC Design 001	S 2010	57	4.3	4.4
ECE 520 ASIC Design 601	S 2010	17	4.2	4.4
ECE 464 ASIC Design	S 2010	9	4.3	4.4
ECE 733 Digital Circuits 001	S 2009	57	4.6	4.5
ECE 733 Digital Circuits 601	S 2009	7	4.4	4.2
ECE 520 ASIC Design 001	S 2009	128	4.6	4.4
ECE 520 ASIC Design 601	S 2009	17	4.5	4.20
ECE 520 ASIC Design 620	S 2009	1		
ECE 464 ASIC Design	S 2009	16	4.6	4.4
ECE 733 Digital Circuits 001	S 2008	67	4.64	4.64
ECE 733 Digital Circuits 601	S 2008	2		
ECE 520 ASIC Design 001	S 2008	101	4.76	4.59
ECE 520 ASIC Design 601	S 2008	15	4.5	4.20
ECE 464 ASIC Design	S 2008	27	4.76	4.59

ECE 733	S 2007	58	4.64	4.46
ECE 520 ASIC Design 001	S 2007	129	4.75	4.68
ECE 520 ASIC Design 601	S 2007	6		
ECE 464 ASIC Design	S 2007	17	4.75	4.68
ECE 745 ASIC Verification	F 2006	20		4.6
ECE 733 Digital Circuits 001	S 2006	43	4.5	4.6
ECE 520 ASIC Design 001	S 2006	65		
ECE 520 ASIC Design 601	S 2006	8		
ECE 464 ASIC Design 001	S 2006	17	4.4	4.1
ECE 733 Digital Circuits 001	S 2005	30	4.5	4.6
ECE 733 Digital Circuits 601	S 2005	5		
ECE 520 ASIC Design 001	S 2005	44	4.6	4.3
ECE 520 ASIC Design 002	S 2005	34	4.6	4.5
ECE 520 ASIC Design 601	S 2005	2		
ECE 464 ASIC Design 001	S 2005	15	4.9	4.1
ECE 464 ASIC Design 002	S 2005	13	4.9	4.1
ECE 733 Digital circuits	S 2004	45	4.2 (4.1)	4.2 (3.9)
ECE 520 ASIC Design	S 2004	76	4.4 (4.1)	4.3 (3.9)
ECE 520 ASIC Design 601	S 2004	17		
ECE 464 ASIC Design	S 2004	69	4.5 (4.1)	4.0 (3.9)
ECE 733 Digital Circuits	S 2003	84	4.3 (4.0)	4.2 (3.8)
ECE 520 ASIC Design	S 2003	81	4.2 (4.0)	3.9 (3.8)
ECE 520 ASIC Design 601	S 2003	30		
ECE 464 ASIC Design	S 2003	63	3.9 (4.0)	3.5 (3.8)
ECE 406 Design Complex DS	F 2002	167	4.2 (4.1)	3.8 (3.9)
ECE 520 ASIC Design	S 2002	239	4.4 (4.1)	4.2 (3.9)
ECE 520 ASIC Design 601	S 2002			
ECE 464 ASIC Design	S 2002	39	4.1 (4.1)	3.6 (3.9)
ECE 406 Des. Complex Dig Sys	F 2000		4.7 (4.0)	4.5 (3.7)
ECE 704 Design For Test	F 2000		4.6 (4.0)	4 (3.8)
ECE 520 ASIC Design 001	S 2000		4.5 (4.1)	4.4 (3.9)
ECE 520 ASIC Design 002	S 2000		4.6 (4.1)	4.3 (3.9)
ECE 520 ASIC Design 601	S 2000			
ECE 492B ASIC Design	S 2000		4.5 (4.1)	4.3 (3.9)
ECE 342 Des. Complex Dig Sys	F 1999		4.4 (4.1)	4 (3.9)
ECE 520 ASIC Design 005	S 1999		4.6 (4.2)	4.5 (4.0)
ECE 520 ASIC Design 006	S 1999		4.5 (4.2)	4.3 (4.0)
ECE 342 Des. Complex Dig Sys	F 1998		4.3 (4.1)	4.1 (3.9)
ECE 520 ASIC Design	S 1998		4.6 (4.1)	4.4 (3.9)
ECE 492B ASIC Design	S 1998		4.7 (4.1)	4.8 (4.1)
ECE 342 Des. Complex Dig Sys	F 1997		4.6 (4.0)	4.4 (4.0)

ECE 520 ASIC Design	S 1997		4.7 (4.1)	4.7 (3.9)
ECE 492B ASIC Design	S 1997		4.7 (4.1)	4.4 (3.9)
AVERAGE				

- ECE 342 Design of Complex Digital Systems, Fall 1996, Overall Rating: 4.6/5.0.
- ECE 592B ASIC Design, Spring 1996, Overall Rating: 4.75/5.0. (With Dr. Liu.)
- ECE 492B ASIC Design, Spring 1996, Overall Rating: 4.00/5.0. (With Dr. Liu.)
- ECE 544, Design of Electronic Packaging and Interconnects, Spring 1999, Overall Rating : 4.60/5.0.
- ECE 520, Fundamentals of Logic Systems, Fall 1995, Overall Rating: 4.50/5.0.
- ECE 218, Computer Organization and Microprocessors, Both Sections, Spring, 1995: Section 001: 4.45/5.0; Section 002: 4.62/5.0.
- ECE 592V, VLSI Microprocessor Project, Spring 1995. (13 students but not rated).
- ECE 681/693A, Computer Engineering Seminar. Spring 1996 and Fall 1996.
- ECE 521 Computer Design and Technology, Fall 1994, Overall Rating: 4.24/5.0.
- ECE 691F, High Speed VLSI, Fall 1994, Overall Rating: 4.45/5.0.
- ECE 691P, Superscalar Processor Design, Spring 1994, Overall Rating: 4.67/5.0.
- ECE 591F, Design of Electronic Packaging and Interconnects, Spring 1994, Overall Rating: 4.60/5.0.

B. INSTRUCTIONAL DEVELOPMENT

1. NSF-funded CISE Infrastructure effort, “Experimental High Performance Computing and Communications Systems". (Total: $1,338,283 including $503,046 in matching.) Approximately $283,000 of this funding went towards outfitting the ECE Design Center.

2. CAD Tools. Modern design is done with sosphisticated Computer – Aided Design Tools, not with pencil and paper. I have spent considerable effort bringing such tools into the Unity environment, gaining the `corporate knowledge' about how to use these tools effectively and obtaining additional computers for use with these tools. *Students tell me that knowledge of these tools is highly regarded by potential employers. In fact one student stated that `Dr. Franzon teaches courses that gets jobs'. In addition , in 1999, we won the Cadence University Alliance Best Web site Awards.* Through my funded research efforts and Corporate Donations introduced the following Computer Aided Design Tools into the curricula:

- Cadence Design Systems. A complete suite of over 4 GB of executables that facilitate chip, board and system design, with a retail value of over $100,000,000. Cadence donates these tools because of the widespread recognition of our contributions to CAD. (i.e. It waives the $5,000 fee.)
- Synopsys. The industry leading chip (ASIC) synthesis tool,with a retail value of over $7,000,000.

- In 2008, NCSU won the "Babbage Award" from Sun and Synopsys, in recognition of our contributions towards lab infrastructure. The award comes in the form of $15,000 of computers.
- Mentor. We integrate some mentor graphics tools with the other tools above. The tools have a retail value of over $5,000,000. Mentor donates these tools because of the widespread recognition of our contributions to CAD.
- Mentor donates $30,000 annually to the University to assist in CAD infrastructure development.

As well as obtaining these tools, my group has spent considerable effort making these tools useful to us by writing integration scripts and generating `know-how'. Much of this `know-how' has been published on the Web and in our own lockers. Most of this learning was conducted driven by research needs and serves as an excellent example of the integration of research and teaching. This work is ongoing. For example, over 2000 organizations world-wide, use our "Physical Design Kit"..

3. ECE 745. ASIC Verification. I introduced this course in 2007, though it was taught by Meeta Yadav.

4. ECE 342, Design of Complex Digital System, Fall 1996:

- Completely redesigned and updated course to reflect modern design practices, and use of modern Hardware Description Languages and Design Tools.
- Completed a new laboratory course ECE 342L for use with this course.

5. ECE 520 ASIC Design (formerly `Fundamentals of Logic Systems'), Spring 1997:

- Based on my teaching of ECE592B in Spring 1995, this course has been completely updated to reflect modern design practices, modern tools, and emphasize an understanding of algorithms used in modern tools. (`ASIC' stands for `Application Specific Integrated Circuit'. For example the chips in a satellite dish receiver are ASICs. ASIC engineering is the fastest growing area of ECE today.)
- Once the course action forms are approved, this course will be taught concurrently with ECE 420 ASIC Design.

6. ECE 544, Design of Electronic Packaging and Interconnects, Spring 1995. New course emphasizing `transmission line effects' in electronic packages and how to design `deep sub-micron interconnect'. I receive tremendous demand from industry for graduates from this course.

7. ECE 691/693A, Computer Engineering Graduate Seminar

- Created new seminar course (with Dr. Tom Conte) for computer engineering students.
- Recruited and scheduled weekly speakers.

8. ECE CAD Lab. $75,000. Provost Office, 1995.

C. MENTORING ACTIVITIES

UNDERGRADUATE STUDENT SUPERVISION

1. 2012. Spring advisor to two undergraduates.
2. 2010. Summer REU supervisor to three Undergraduates
3. 2009. Summer REU supervisor to one Undergraduate.
4. 2009. Supervised Senior Design Team
5. 2008. Summer REU supervisor to two Undergraduates.
6. 2005 Andrew Pita, SRC Undergraduate Research Fellowship
7. 1999 Ecoh Oh, NSF Undergraduate Research Award
8. 1999 Ben Hughes, NSF Undergraduate Research Award
9. 1993- Numerous Senior Design projects

GRADUATE STUDENT SUPERVISION

GRADUATE COMMITTEES

Currently member of several PhD and MS committees.

GRADUATE COMMITTEES

For a list of graduate committees I chair, see below. I am on numerous committees as a member, but I do not track the numbers.

D. MASTER'S AND DOCTORAL THESES DIRECTED AND BEING DIRECTED

I am actively directing the theses of 20 Ph.D. students and 3 Master with thesis option (MST) students. I have graduated 50 Ph.D. students and 50 MST students.

Masters and Doctoral Theses under direction

Student Name	Degree [date]
Weiyi Qui	PhD [12/16]
Josh Schabel	PhD [12/16]
Weifu Li	PhD [12/16]
Sumon Dey	PhD [12/16]
David Winick	PhD [12/15]
Gary Charles	PhD [03/15]
Marcus Tshibangu	PhD [12/16]
Randy Widialaksono	PhD [05/16]
Zenquian Zhang	PhD [12/16]
Wenxu Zhao	PhD [05/16]
Jong Beom Park	PhD [08/16]

Luther Blackwood	MS to PhD [12/16]
Lee Baker	PhD [12/16]
Zhao Zhang	PhD [07/17]
Kirti Bhanushali	PhD [12/16]

Doctoral Theses Directed

1. Sarkar, Biplap, "Atomic Layer Deposition Techniques for Novel Memory Applications," August 2015. Cochair
2. Winick, David, "Electroactive Polymer Refreshable Braille Display, December 2015 (Posthumous).
3. Gary Charles, "Design, Model and Analysis of TSV-based On-Chip PDN Interconnects for 3-D Integrated Circuits. ", March 2015.
4. Zhao Yan, "S-Parameter Based Binary Multimode Interconnect Design Methodology and Implementation," December, 2014 .
5. W.S. Pitts, "High quality CMOS Integratable Varactors," March 2014.
6. Peter Gadfort, "Packaging and Integration of Three Dimensional Microsensors," December, 2013.
7. Evan Erickson, "Multi-Gbps Inductively Coupled Connectors," December, 2013.
8. Akalu Lentiro, "Low-Density, Ultra-Low Power and Smart Radio Frequency Telemetry Sensor," October, 2013.
9. Shivam Priyadarshi, "System and Gate Level Dynamic Electrothermal Simulation of Three Dimensional Integrated Circuits," June, 2013.
10. Eric Wyers, "Direct Search Calibration Algorithms for Digitally Reconfigurable Radio Frequency Integrated Circuits," March 2013.
11. Ojas Ashok BOpat, "A Generic Scalable Architecture For a Large Acoustic Model and Large Vocabularly Speech Recognition Accelerator," October, 2012.
12. Won Hao Choi, "System Level Power Prediction Methodology for Mobile 3-D Graphic Engines," May 2012.
13. Hsuan-Jung Su, "Continuous-Time Fractionally Spaced Equalization and Its Application in Capacitively Coupled Chip-To-Chip Interconnect," May, 2012.
14. Hsuan-Jung Su, "Continuous-Time Fractionally Spaced Equalizatoin and its Application to Capactively Coupled Chip-TO-Chip Interconnect", January 2012.
15. Matthew Hamlett, "A Novel Approach to IP Protection Using Automated Hardware Techniques to Secure a Design," March 2012.
16. Mustafa Berke Yelten, "Variability and Reliability in Nanoscale Circuits: Simulation, Desgin, Monitoring and Characterization," January, 2012.
17. Hoon Seok Kim, "Advanced Multi Mode Interconnect," December, 2011.
18. Xiangzhong Xue, "Electronic System Optimization Via Convex Programming," December, 2011.
19. Zhu
20. Zhu, A Surrogae Model-based Framework for Design and Macromodeling of Self-calibrated Analog Circuits," October, 2011.
21. Chanyoun Won, "Multimode Interconnect for High-Density Links: Implementation, Design Methodology and New Crosstalk Cencallation Scheme," July 2011

22. Thor Thorolfsson, “Three Dimensional Integration of Synthetic Aperture Radar Processors,” April 2011
23. Daniel Schinke, “Computing with Novel Floating Gate Devices,” April 2011
24. Yongjin Choi, “Design of Multimodel Signaling Transceiver for High-Density and High-Speed Links,” May 2010.
25. Eun Chu Julie Oh, Ph.D. Dissertation, “Design and Applications of Three-Dimensional Circuits”, December, 2009.
26. Karthik Chandrashekhar, Ph.D. Dissertation, “Inductively Coupled Connectors,” December, 2008
27. Dhruba Chandra, Ph.D. Dissertation, Speech Recognition CoProccessor, December, 2007.
28. Meeta Yadav, “Hardware Architecture of behavior Modeling Coprocessor for Network Intrusion Detection,” Ph.D. Dissertation, March, 2007.
29. Ullas Pazhayaveetil, “Hardware Implementation of a Low Power Speech Recognition System,” Ph.D. Dissertation, February, 2007.
30. Jian Xu, “AC Coupled Interconnect for Inter-Chip Communications,” Ph.D. Dissertation, December, 2006.
31. Ambrish Varma, “Improved behavioral modeling based on Input Output Buffer Information Specification,” Ph.D. Dissertation, NCSU, October, 2006.
32. Sachin Sonkusale, “Planar edge defined alternate layer process (PEDAL) – an unconventional technique for the fabrication of wafer scale sub-25 nm nanowires and nanowire template,” PhD, October, 2006.
33. Liang Zhang, “Driver Pre-emphasis Signaling for on-chip global interconnects,” Ph.D. Dissertation, September, 2006.
34. Monther Al Dwairi, “Hardware Efficient Pattern Matching Algorithms and Architectures for Fast Intrusion Detection,” Ph.D., November, 2006.
35. John Damiano, “Active body bias for low-power silicon-on-insulator design,” Ph.D., March 2006.
36. Neil DiSpigna, “Electronic Devices and Interface Strategies for Nanotechnology,” Ph.D., April 2006.
37. Christian Amsinck, “Molecular Electronic Memories,” Ph.D., March 2006.
38. Lei Luo, “Capacitively Coupled Chip to Chip Interconnect Design, Ph.D., December, 2005.
39. Leon Zhang, “Driver pre-emphasis signaling for on-chip global interconnects,” Ph.D., December, 2005.
40. Steve Lipa, “Phase Noise Analysis of Rotary Oscillators,” Ph.D. May 24, 2005
41. David Nackashi, Circuit and Integration Technologies for Molecular Electronics, Ph.D. 2004
42. Stephen Mick, AC Coupled Interconnect, Ph.D. 200
43. John Wilson, Linearly Tunable RF MEMS Capacitors Implemented Using an Integrated Removable Self-Masking Technique, Ph.D. 2004
44. Andrew Stanaski, Sensor Circuits for Flip Chip Debug, Ph.D. 2004
45. Pronita Mehrotra, High Performance Hardware Memory Algorithms, Ph.D. 2003
46. Bruce Duewer, MEMS Switch Fabric, Ph.D.
47. Toby Schaffer, Chip-package Codesign, Ph.D.
48. Mouna Nakkar, Dynamically Programmable Cache, Ph.D.

49. Mir Azam, Custom CMOS Design and Architecture for Low-Power High-Performance Circuits, PhD.
50. Debu Ghosh (co-chair), Synthesis of Benchmarking Expiriments, Ph.D.
51. Chris Harvatis, Performance Driven Partitioning for MCMs, PhD.
52. Slobodan Simovich, Computer-Aided Analysis of Interconnect,PhD.
53. Scott Washabaugh, Low energy FSM Design, PhD.
54. Sharad Mehrotra, Automated Synthesis of High Speed Digital Circuits and Package-Level Interconnect, PhD.
55. Todd Cook, Instruction Set Architecture Specification, PhD.
56. Robert Evans, Energy Consumption for Modeling and Optimization of SRAMs, PhD.

Masters Theses directed

1. Abhishek Bhattacharya, "Design and Power Optimization of a16 nm Dual Floating Gate FET Memory Array and Peripheral Circuits," Octover, 2013.
2. Joshua Schabel, "An Analysis of Subthreshold SRAM Bitcells for Operation in Low Power RF only Technologies," July 2013.
3. Vinod Kotipllai, "Impact of Process Variations on 16-nm Dual Floating Gate FET using TCAD simulations," December 2012.
4. Wenxu Zhao, "Headphone Deiver Design with Inductive Coupled Interconnection," November, 2012.
5. Shiney Gupta, "Multi-Storey Stacked Driver Topolo9gy for Reduced Swing and Low Power Bus Operation,", May 2012.
6. Pattabhiraman Ravindran, "Harvesting Thermal Energy to Power Agricultural Sensors," October, 2011.
7. Alex Leaonard, "Implementation of a System-on-Chip for self-healing of analog receiver components in a 65 nm CMOS process", May 2011
8. Seema Kumar, "Memory Diesgn for Sensor IC," May 2010.
9. Mihir Shiveshwarkar, "A Nanocrystal Floating Gate Flash Analog to Digital Converter," December, 2009.
10. Ojas Bapat. "Design of DDR2 Interface for Tezzaron TSC8200A Octupus Memory intended for Chip Stacking Applications," April 2009.
11. Peter Gadfort, "Low power driver for silicon carrier interconnects," April 2009.
12. Chintan Shah, "Inductively Coupled Interconnect for Chip to Chip Commmunication over Transmission Line," Feb 2009.
13. Kiran Gonsalves, "Memory Design for FFT Processor in 3DIC Technology," March, 2009.
14. Vinay Honnavara, "Cost optimization by method of allocating software component units to electronic control units for model-driven designs," October, 2008.
15. Wei Cao, "Design of temperature sensors for validation of aseptic food processing," Sept. 2008.
16. Akalu Lentiro, "Implemention of AC Coupled Interconnect Test Vehicle," May, 2008.

17. Vinayak Devasthali, “Application of body biasing and supply voltage scaling techniques for leakage reduction and performance improvement of CMOS Circuits,” December 2007.
18. Paul Fernando, “Adding scalability to IBIS using AMS Languages,” September 2007.
19. Vivek Jayadav, “Hardware-Software Codesign of a Large Vocabularly Speech Recognition System,” February, 2007.
20. Srivatsan Parthasarathy, “Interfacing AC Coupled Interconnect Design with Rocket I/O compatible FPGA Systems,” December 2006.
21. Janani Mukundan, “Instruction Cache Checkpoints Using Phase Tracking and Prediction,” June 2006.
22. Yasaswini Sudarsanam, “Implementatin of Double Precision Floating Point Arithmetic for Matrix Multiplication,” October 2006
23. Itisha Tyagi, “Design of array based row decoders and self-referencing sense amplifier for large scale resistance change style molecular memories,” June 2006.
24. Indraneel Kelkar, “Tradeoffs involved in the design of SRAMs,” December 2005.
25. Wallace Pitts, “Partially depleted silicon on insulator phase lock loop design,” January, 2006.
26. Janani Mukundan, “Instruction cache checkpoints using phase tracking and prediction,” December 2006.
27. Deepak Kumar, ”Design of fully integrated wireless CMOS MEMS device for intraocular pressure measurement,” March 2006.
28. Manav Shah, “Design of a self-test vehicle for AC Coupled Interconnect Technology,” May 2006.
29. Andrew Morgan, Design Flow based on Sensitivity Analysis for High Speed Digital Circuits, MS, 2004
30. Brian Phelp, Hardware Realization and Implementation Issues for the Sliding Window Packet Switch, MS, 2004
31. Ishdeep Sawhney, Hardware Forwarding for IPV6, MS, 2003
32. Kaustabh Bhate, MEMS Design for textiles sensor, MS
33. Praveen Prasad, Reconfigurable Computing for Network Security, MS
34. Patrick Lall, Verification of a Network Processor, MS
35. Ambrish Varma, SHOCC Design Tools, MS
36. Karthik Chandrasekhar, Hardware to support multicast in all-optical networks, M
37. V. Parameshawara (co-chair), Enhancement of NC Agricultural Automated Weather Network and Development of Advanced Communication, Data Acquisitions amd Dissemation System, MS.
38. Jeremy Palmer, Design and Analysis of a VLSI-MEMS-Based Diffractive Optical Beam Steering System, MS.
39. Som Chaudry, MEMS devices for laser radar, MS.
40. Srisai Rao, Design, place and route of an IDEA processor, MS.
41. Kevin Mock, IDEA Implementation, MS.
42. Sibi Kuruvilli, Synthesized SAND Issue Unit, MS
43. Tom Mills, Macromodelling of high speed digital drivers and receivers, MS.
44. Matreiya Sengupta, Managing Crosstalk in Interconnect Design, MS.
45. Andrew Stanaski, Optimizing Memory Design for Packagability, MS.

46. Jonathon Schaeffer, A 400 MHz CMOS Multiplier, MS.
47. Harsh Deshmane, MCM Extractor in Magic, MS.
48. Sha Ma, Circuits for Low Energy Computing, MS.
49. Shauki Elassaad, Placement tools for multi-chip modules, MS.
50. Alex Dalal, CAD tools for yield estimation, MS.

Committee Memberships: Do not track

III. SCHOLARSHIP IN THE REALMS OF FACULTY RESPONSIBILITY

A. PUBLICATIONS AND AWARDS

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Invited Research Presentations, Conferences

1. Franzon, P.D.; Rotenberg, E.; Tuck, J.; Davis, W.R.; Huiyang Zhou; Schabel, J.; Zhang, Z.; Park, J.; Dwiel, B.; Forbes, E.; Joonmoo Huh; Priyadarshi, S.; Lipa, S.; Thorolfsson, T., “Computing in 3D”, EDAPS 2014, Bangalore, India, Dec. 2014. (Invited presentation).
2. Franzon, P.D.; Rotenberg, E.; Tuck, J.; Davis, W.R.; Huiyang Zhou; Schabel, J.; Zhang, Z.; Park, J.; Dwiel, B.; Forbes, E.; Joonmoo Huh; Priyadarshi, S.; Lipa, S.; Thorolfsson, T., “Computing in 3D”, ICSJ 2014, Kyoto, Japan, Nov. 2014. (Invited presentation).
3. Franzon, P.D.; Rotenberg, E.; Tuck, J.; Davis, W.R.; Huiyang Zhou; Schabel, J.; Zhang, Z.; Park, J.; Dwiel, B.; Forbes, E.; Joonmoo Huh; Priyadarshi, S.; Lipa, S.; Thorolfsson, T., “Computing in 3D”, IME Workship 2014, Singapore, Aug. 2014. (Invited presentation).
4. Franzon, P.D.; Rotenberg, E.; Tuck, J.; Davis, W.R.; Huiyang Zhou; Schabel, J.; Zhang, Z.; Park, J.; Dwiel, B.; Forbes, E.; Joonmoo Huh; Priyadarshi, S.; Lipa, S.; Thorolfsson, T., “Computing in 3D”, SLIP 2014, San Francisco, CA< June. 2014. (Invited presentation).
5. Franzon, P.D.; Rotenberg, E.; Tuck, J.; Davis, W.R.; Huiyang Zhou; Schabel, J.; Zhang, Z.; Park, J.; Dwiel, B.; Forbes, E.; Joonmoo Huh; Priyadarshi, S.; **Lipa, S.;**

Thorolfsson, T., “Computing in 3D”, SPI 2014, Ghent, Belgium, May 2014. (Invited presentation).

6. Franzon, P.D “3D Design, Test and CAD”, SPI 2014, DesignCon, Santa Clara, CA, Jan. 2014. (Invited presentation).
7. P. Franzon, P. Gadfort, W. Zhou, “AC powered circuits,” S3S, San Francisco, California, Oct. 2014. (Invited presentation).
8. Franzon, P.D.; Rotenberg, E.; Tuck, J.; Davis, W.R.; Huiyang Zhou; Schabel, J.; Zhang, Z.; Park, J.; Dwiel, B.; Forbes, E.; Joonmoo Huh; Priyadarshi, S.; Lipa, S.; Thorolfsson, T., "Applications and design styles for 3DIC," *Electron Devices Meeting (IEDM), 2013 IEEE International* , vol., no., pp.29.4.1,29.4.4, 9-11 Dec. 2013 (invited paper)
9. Franzon, P.; Bar-Cohen, A., "Thermal requirements in future 3D processors," *3D Systems Integration Conference (3DIC), 2013 IEEE International* , vol., no., pp.1,6, 2-4 Oct. 2013 (Invited Paper)
10. Franzon, P.D., "MOOCs, OOCs, flips and hybrids: The new world of higher education," *Microelectronic Systems Education (MSE), 2013 IEEE International Conference on* , vol., no., pp.13,13, 2-3 June 2013 (Invited Paper)
11. Franzon, P.D.; Priyadarshi, S.; Lipa, S.; Davis, W.R.; Thorolfsson, T., "Exploring early design tradeoffs in 3DIC," *Circuits and Systems (ISCAS), 2013 IEEE International Symposium on* , vol., no., pp.545,549, 19-23 May 2013 (invited paper)
12. Keynote, “3D System Design: Present and Future,” IEEE 3DIC Test Workshop, Anaheim CA, Dec. 2012
13. Invited Paper, “3D Specific Systems”, NY packaging society, GE, Albany, NY, Oct. 2012.
14. Invited Paper, “Design of 3D Specific Systems,” D43D, Lausanne, Switzerland, July 2012.
15. Keynote, “Design of 3D Specific Systems: Prospectives and Interface Requirements,” IEEE NOC Conference, Copenhagen, Denmark, May 2012.
16. Keynote, “Design of 3D Specific Systems: Prospectives and Interface Requirements,” IEEE NOC Conference, Chipex, Tel Aviv, Isreal, May 2012.
17. Keynote, “Design of 3D Specific Systems,” DATE 3DIC Workshop, Dresden, Germany, March 2012.
18. Invited Paper, “Coordinating 3D Designs,” IEEE 3DIC Conference, Osaka Japan, January 2011.
19. Invited Paper, “3D Specific Design and Test” ATS 2011, New Delhi, India, Nov. 2011.
20. Invited Paper, “3D Specific Design,” IEEE SAMOS Conference, Samos, Greece, August 2011.
21. Keynote, “3D TSV Processes and Design Challenges,” ICMAT, Singapore, June 2011
22. “Computing with Novel Floating Gate Devices,” CMOS-ET, Whistler Canada, June 2011
23. Keynote “3DIC, Which Flavor for You?”, TIPPS, Chicago IL, June 2011
24. “Design of 3D Specific Systems,” NYU-AD 3DIC Workshop, April, 2011
25. “Design of 3D Specific Systems”, IMAPS 2010, Raleigh, NC, November, 2010
26. “Creating 3D Specific Systems,” DATE 2010, Dresden Germany, March, 2010.

27. “3D Design and Applications,” IEEE Litho 2009, June 2009.
28. “Creating 3D Specific Systems,” D43D, Grenoble France, June 2009.
29. “3DIC Design and CAD,” Austin Chapter Meeting on 3DIC, April 2009.
30. “Application and Design Exploration for 3D Integrated Circuits,” VLSI Multi-level Interconnect Conference, September 2008.
31. ”Memory rich applicatons for 3D integration,” in Proc SPIE 7268, Smart Structures, Devices and Systems IV, Dec. 2008.
32. “Green Electronics, Fact or Myth”, panel member, IEEE SOC Conference, September 2008.
33. “Application and Design Exploration for 3D Integrated Circuits,” VLSI Multi-level Interconnect Conference, September 2008.
34. “Design and CAD for 3D Integrated Circuits”, IEEE/ACM Design Automation Conference, June 2008.
35. “Keeping Chips Hot, Are IC Thermal Problems Hot Air”, panel member, IEEE/ACM Design Automation Conference, June 2008.
36. “Application and Design Exploration for 3D Integrated Circuits,” VLSI Multi-level Interconnect Conference, September 2007
37. “3DIC”, Materials Research Conference, Dec. 2007
38. **“**Molecular Computing,” 2nd IEEE International Workshop on advances in sensors and interfaces, June 2007.
39. “TCAM core design in 3D IC for low matchline capacitance and low power,” Proc. SPIE Smart Structures, Devices and Systems III, December, 2007.
40. “3-D Design,” Fall MRS Conference, December 2007.
41. “3-D Design,” RTI 3D Technologies Conference, November, 2007.
42. “Controlled nanowire fabrication by PEDAL process,” IEEE NanoNet ’06, Sept. 2006,
43. “An integrated self-masking technique for providing low-loss metallized RF MEMS devices in a polysilicon only MEMS process,” SPIE Euro Micro Conference, May 2005
44. “Simultaneous switching noise in IBIS models,” IEEE EMC, August 2004
45. “Nanoscale Circuits and Computing Systems,” ISCAS, May 2004
46. “Integration for Molecular Electronics,” FNANO, April 2004
47. “High Frequency, High Density Interconnect Using AC Coupling,” MRS Fall Meeting, December 2003
48. AC Coupled Interconnect for High-Density High-Bandwidth Packaging,” SPIE Australia Micro Conference, December 2003
49. “High Frequency, High Density Interconnect Using AC Coupling,” SSDM Japan, September, 2003
50. “Scalable Molecular Circuit Architectures,” Molecular Electronics Conference, Decemeber 2002
51. “4 Gbps AC Coupled Interconnection,” IEEE CICC, May 2002
52. “Design Automation and Design Challenges for Package/Systems,"Asia DAC, January 1999
53. “Integrated Package Design of a DES Processor,” IMAPS MCM Conference, Oquinqit Maine, August 1997.

54. "Computer Design Strategy for MCM-D/Flip-Chip Technology," IEEE ASIC, Sept. 1996.
55. "System Design Optimization With Multichip Module Technology," Brazil Microelectronics Conference, Aug. 1996.
56. "Optimal System Design with MultiChip Module Technology," Microelectronics 1995, June 1995.

Invited Research Presentations, Universities and Industry

1. "Computing in 3D", Google, Oct. 2014.
2. "Computing in 3D", Cirrus Logic, Aug. 2014.
3. "Computing in 3D", Sandia Labs, May 2014.
4. "3D Specific Design", Rambus, Sept. 2013
5. "3D Specific Design," University of Maryland, Dec. 2013
6. "3D Specific Design," Georgia Tech, May 2013.
7. "3D Specific Design", IBM, Jan. 2013.
8. "Connectivity in Future Systems," HP, October, 2012.
9. "3D Specific Design and CAD," IEEE CPMT Chapter, Portland OR, April 2012.
10. "Connectivity in Future Systems," IBM, March 2012.
11. "Sensors and System," IBM, April 2012.
12. "3D Specific Systems," Technicon, April 2012.
13. **"**3D Speicifc Design," Mentor Graphics, Nov. 2011.
14. "3D Specific Design", Ga. Tech, June 2011.
15. "3D Specific Desgn and CAD," IBM, January 2011.
16. "Creating 3D Specific Systems," CMOS ET Conference, May 2010.
17. "3DIC CAD," Synopsys, April 2010.
18. "Designing 3D Specific Systems," LSI Logic, March 2010.
19. "3DIC Design and CAD," IMEC, March 2010.
20. "Creating 3D Specific Systems", IBM, March 2010.
21. "Creating 3D Specific Systems," RTI 3D, December, 2009.
22. "3D Memory Systems," SRC Signapore, October 2009.
23. "3DIC Design and Applications," IMEC, June 2009.
24. "3DIC Technology Design and Applications," Tessera, April 2009.
25. "3DIC Technology Design and Applications," Ultratech, January 2009.
26. "3DIC Design and CAD," University of Adelaide, December, 2009.
27. "3DIC Design", Qualcomm, September 2008.
28. "AC Coupled Interconncect", DARPA Exascale Committee, August 2007.
29. "3DIC Design and CAD", TI, March 2008
30. "3DIC Design and CAD," IBM, April 2008
31. "AC Coupled Channels", IBM, April 2008
32. "AC Coupled Interconnect", HP, Sept. 2007
33. "3DIC", CEA-LETI, June, 2008
34. "Interconnect", McGill University, Canada, July 2007.
35. "AC Coupled Interconnect," Intel, AZ, March 2006.
36. "AC Coupled Interconnect", Rambus CA, December 2005
37. "AC Coupled Interconnect," IBM, NY, December 2005
38. "Equalization for on-chip interconnect," IBM, NY, December 2005.
39. "AC Coupled Interconnect," University of Adelaide, October, 2005.

40. “Molecular Electronics,” University of Sydney, October, 2005.
41. “AC Coupled Ineterconnect,” UFL, April 2005
42. “Molecular Computing,” UNCC, March 2005
43. “Nanoscale structures for Molecular Electronics,” HP Labs, December 2004
44. “AC Coupled Interconnect,” SRC Econfernce, Dec, 2004
45. “AC Coupled Interconnect,” Rambus CA, December 2004
46. “AC Coupled Interconnect,” Sun, CA, December 2004
47. “AC Coupled Interconnect,” IBM RTP, February 2005
48. “AC Coupled Interconenct,” Rambus NC, August 2004
49. “Emerging Memory Devices,” ITRS, Stresa Italy, April 2004
50. “Optical Networking,” ECU, Perth Australia, August 2003
51. “Molecular Electronics,” University of Adelaide, August 2003
52. “Molecular Electronics,” University of Sydney, August 2003
53. “AC Coupled Interconnect,” IBM TX, May 2003
54. “Scalable Molecular Circuit Architectures,” USC, April 2003
55. “Molecular Electronic Circuits,” KAIST, Korea, July 2002
56. “AC Coupled Interconnect,” IBM Research NY, April 2002
57. “AC Coupled Interconnect,” Intel AZ, Feb. 2002
58. “AC Coupled Interconnect,” Intel OR, Feb. Nov 2001
59. “Structures and CAD for Chip-Package Codesign,” TI TX, May 2000
60. “High Bandwidth On-Chip Interconnect,” TI Dallas TX, May 2000
61. “Heteregenous System Integration,” TI, Dallas TX, May 2000
62. “MEMS Application and Fabrication,” Ford Microlectronics, CO, Dec. 1998
63. “Chip Package Codesign,” Ga Tech, Oct, 1998
64. “Chip-Package Codesign,” SRC, NC, April 1997
65. “Chip-Package Codesign,” Intel, CA, Oct 1997
66. “Chip-Package Codesign,” DEC, MA, Dec 1997
67. “Optimal Computer Design with MCM-D/Flip Chip Technology,” Sun, CA, May 1996
68. “Signal Integrity Tools,” Sun, CA, May 1996

I have aslso given invited presentations at the following organizations: Stanford University, University of Adelaide, Silicon Graphics, Intel, Ross Technology, Cadence, Mentor Graphics, LSI Technology, Tandem Computer, IBM,Bell Northern Research, MCNC. Dates and exact titles unrecorded.

<u>Appointments or election to study sections and editorial boards.</u>

- **Associate Editor, IEEE Transactions on Advanced Pcakaging 1997-**
- Associate Editor, ACM Journal on Emerging Computing Technologies, 2004-2011
- Editorial Board, Journal of Microelectronics System Integration.
- Associate Editor, IEEE Transactions on VLSI Systems. 1997 – 2001

B. GRANTS AND CONTRACTS

Total Funding Summary.

60 Research grants and contracts, 1 equipment grant, 1 educational grant, 7 cash gifts, over $40 Million in research grants, and $500,000 in educational grants, and over $700,000 in gifts

EXTERNAL GRANT

1. **P. Franzon, "Planning Grant for I/UCRC for Advanced Electronics Through Machine Learning," NSF, 04/15/15 – 03/31/16, $11,499**

Planning grant for potential I/UCRC.

2. **P. Franzon, "Trusted Fabrication through 3D Integration," DARPA/ONR, 08/01/2015 – 07/31/2016**

Study on new techniques to effect trusted ICs.

3. **P. Franzon, "Cognitive Computing," Google, $41,000, 3/1/2015 – 2/28/2016.**

Investigate speedup potential of cognitively inspired algorithms.

4. **P. Franzon, "Hardware acceleration of sparse cognituve algorithms," DARPA/AFRL, $320,372, 12/01/14 – 6/30/16.**

Investigate speedup potential of new classes of cognitively inspried algorithms.

5. **P. Franzon, "SHF:Small AC Powered Digital Circuits," NSF, 08/01/14 – 07/31/17, $445,713, (PI).**

Design a new class of efficient RFID and backscatter BTLE chips.

6. **P. Franzon, A. Chakrabortty, "Faster than Real Time Simulation of Electromechanical Process of Large Scale Electrical Power Grid", $80,000, ABB, 12/15/14 – 12/14/15. (PI)**

Architect an accelerator to simulate power grids.

7. **P. Franzon, W. Davis, "Leveraging Commercial Flows for Heterogeneous Integration,", $1,505,643, DARPA, 5/16/2013 – 5/15/2016. (PI)**

Produce CAD flows for managing temperature and stress in Heterogeneous 3DIC chip stacks.

8. P.Franzon, E. Rotenberg, W. Davis, H. Zhou, J. Tuck, "3D-Enabled Customized Embedded Computer," $4.5M, DARPA, 9/14/2011 – 9/14/2016. (PI)

Architectect, design and implement a 3D CPU capable of low power computing.

9. P. Franzon W. Davis, E. Rotenberg, "Modular, Testable, Tightly Coupled 3D Implementation of a Heterogenous Processor", $1,200,000, Intel, 10/1/2011 – 9/30/2015. (PI)

Build novel architectural approaches to implementing 3D specific processors.

10. P. Franzon, Eric Rotenberg, "3D X86 Heterogeneous Core Stack," $55,000, Intel 11/12/2012 – 12/31/2013.

Investigate an X86 based CPU stack.

11. P. Franzon, NSF ASSIST ERC – portion to my projects, NSF, $150,000, 07/01/2011 – 12/31/2013.

System Thrust Leader for ASSIST ERC.

12. P. Franzon, V. Misra, and N.H. DiSpigna, "Computing via Monotlithic Three Dimensional Assemnbly of Novel Floating Gate Transistors," $839,740, NSF, 7/1/2011 – 6/30/2014 (PI)

We have developed the design for a new type of "unified" memory device, a Double Floating Gate FET (DGF FET). It can store two bits in each transistor, one in a volatile state, another in a non-volatile state. The purpose of this grant is to build sample devices and address practical issues related to implementation as a memory device.

13. P. Franzon, "Binary Multimode Interconnect for High Density Chip to Chip Communications," Intel, $300,000 7/1/2011 – 12/31/2014 (PI)

A new implementaiton method has been identified for a high-density, low-power, crostalk cancelling chip to chip communications scheme. This paper addresses demonstration of this method.

14. P. Franzon, W.Davis, "Thermal-System Codesign of a Mobile Application," Qualcomm, $150,000, 07/01/2011 – 12/31/2014. (PI)

Investigate pathfinding for 3D systems.

15. P. Franzon, “EAP actuators for a Braille Display,” PBI Inc., $30,000, 8/16/2012 – 12/31/2012.

Prototype a Braille cell based on EAPs.

16. **P**.Franzon, “Integrated 3D Packaging for Microscopic Systems,” MARCO, $321,000, 11/01/2009 – 1/31/2013. (PI)

Develop integrated packaging concepts and antenna for 1 mm and 1 cm scale systems.

17. P. Franzon, “Speech Recognition Acceleration,” Spansion, $123,761, 07/12/2010 – 05/15/2012.

Investigate hardware/software codesign for speech acceleration.

18. P. Franzon, N. DiSpigna, “Nanocrystal Computing,” NSF (CCF-0811582), $400,000 07/01/2008 – 06/30/2012. (PI)

Develop new devices, based on nanocrystal films, suited for digital applications. Explore those applications.

19. P. Franzon, “Algorithms and Structures for Self Healing Circuits,” $170,000, DARPA, 01/03/2012 – 12/31/2013. (PI)

Investigate CAD techniques for self-calibration of RF circuits

20. P. Franzon, “CAD Support for Tezzaron MPW,” DARPA as a subcontract through Tezzaron, $50,000, 7/1/2009 – 6/30/2010.

Support commercial tools as used in Tezzaron MPW run.

21. P. Franzon, M. Steer, T. Kelley, M. Chow, F. Wu, “Self Healing Circuits,” DARPA as a subcontract through Raytheon, $1,073,341, 4/1/2009 – 06/30/2013. (PI)

Investigate CAD techniques for self-calibration of RF circuits.

22. P. Franzon, M. Ozturk, “Reconfigurable RF Electronics,” AFRL, as a subcontract through Raytheon, $60,000, 5/1/2009 – 5/30/2010. (PI)

Design and model a new high-performance Varactor.

23. W.R. Davis, Paul D. Franzon, “Architectural Evaluator for Three Dimensional Integrated Circuits,” Semiconductor Research Corporation, $240,000, 7/1/2008 – 6/30/2012. (Co-PI).

Establish CAD tools to help architect 3D Circuits.

24. Paul D. Franzon, W.R. Davis, "CAD Support For the Third MIT-LL 3D-Integrated Circuit Run", $53,375, DARPA, 5/1/2008 – 12/31/2008. NCSU PI. Subcontract through MIT-LL. (PI)

Develop 3D PDK to support third fabrication run.

25. W.R. Davis, P.D. Franzon, "FreePDK: An Open-Source, Variation-Aware Design Kit", CMU as a subcontract to MARCO, $42,338, 9/1/2007 – 8/31/2009. CoPI.

This work will create an open-source, variation-aware 45nm PDK (Process Design Kit) for use in VLSI education and small-businesses. This kit will include the necessary layout design-rules and extraction command-decks to capture layout-dependent systematic variation and perform statistical circuit analysis. The kit will also include a standard-cell library and I/O-pad library with the necessary support files to enable full-chip place & route and verification for System on Chip designs. Test-chips designed with this PDK will be fabricated by an SRC member company, allowing validation of the design-rules so that the rules may be used in future multi-project runs and design contests

26. Paul D. Franzon, "Micromachined Braille Reader", US Department of Education, 11/01/2007 – 10/31/2010, $600,000. PI.

Investigate and build a "full screen" programmable Braille display using ElectroActive Polymers (EAPs).

27. Paul D. Franzon, "Computer Aided Design for Digital Trust", $110,000, DARPA, 1/1/2007 – 06/30/2009. NCSU PI, subcontract to Irvine Sensors Corporation.

Investigate methods to identify theft and modification of chip intellectual property.

28. Paul D. Franzon, "Multimode Interconnect," Semiconductor Research Corporation, 11/01/06 – 12/31/10, $300,000. PI.

With higher core clock speeds, and the trend to multi-core, the demands on chip I/O are increasing rapidly. The key question is how to increase both the density and speed of chip I/O without increasing packaging costs. At high speeds, crosstalk issues typically dictate inter-pair spacings of four times the wire width in PCBs, and rich use of power and ground shields in connectors. In this research, we will investigate coding and circuit techniques that enable a group of signals to travel down a wire bundle, and potentially connectors and cable assemblies, without crosstalk

29. Franzon, Kingon, Wilson, "System Technologies for Space Electronics," AFRL, 09/25/2006 – 6/30/2011, $1,287,807. PI.

Build interconnect technologies for Space Applications. Deploy a demonstrator in a satellite.

30. K.P. Sandeep, Paul D. Franzon, J. Simunovic, "Use of RFID Tags in Determining the Time-Temperature History Within a Product During Processing, Transportation, and Storage," CAPPS, $60,000, 11/01/06 – 12/31/07. and 5/1/06-4/30/10 Co-PI.

Improving food quality, enhancing food safety, and aiding process filing with the FDA are three important areas of interest to the food industry. Accurate determination of the time-temperature history at the critical point in a system (slowest heating point) is necessary to accomplish this. We would like to make use of the RFID technology to capture and transmit internal temperatures of food particulates while they are being pumped through the heating, holding, and cooling sections of a continuous flow food processing system.

31. K.P Sandeep, Paul D. Franzon, Josip Simunovic, "Development and Use of Sensors in Validating Aseptic Processing of Multiphase Foods," US. Dept. of Agriculture, 09/01/06 – 08/31/10. $278,936. Co-PI.

The overall objective of the current study is to develop a sensor that can be used to determine the location and internal temperature of food particles as they flow through the heating, holding, and cooling sections of an aseptic processing system.

32. Franzon, "System Technologies for Low-Power Spaceborne Electronics," AFRL, $1,287,807, 9/25/06 – 9/24/07, NCSU PI.

Demonstrate a complete AC Coupled first level packaging solution in both Bulk CMOS and SOI. Launch a space demonstration vehicle.

33. K.P. Sandeep, Paul Franzon, Josip Simunovic, "Development of a Micro-Electro-Mechanical-System-based (MEMS) temperature sensor to determine internal temperatures within multiphase food products", CAPPS, $54,422, 7/1/06-12/31/11.

In collaboration with Food Science, develop miniaturized sensors for monitoring internal conditions in Food Processing Equipment.

34. Franzon, "MoleFET Design and Fabrication," DARPA, $150,000, 5/11/06 – 11/10/08. (PI at NCSU, subcontract to UVA.)

Investigate molecular integration into FET structures for nanoflash and transistor applications.

35. Steer, Franzon, Davis, "Electromagnetic Modeling for 3D ICs," DARPA, $1,870,000, 7/5/04 – 3/31/10, (co-PI, subcontract through PTC).

Tools and Application Exploration for 3D ICs.

36. Franzon, "DNA Directed Circuit Assembly," NSF, $135,000 7/1/03 – 6/30/07. (PI at NCSU)

In collaboration with Duke University, determine circuit interconnect strategies using DNA scaffolds.

37. Franzon, "High Performance Computer Interconnect," NSF, $350,000, 9/01/2002 – 8/31/2008, (PI).

    We are determining new approaches to interconnect large systems at the system level. These approaches promise high density, low power and low cost.

38. Franzon, "AC Coupled Interconnect for Low-Power Space-Borne Electronics," Mission Research Corporation, $3,116,813, 05/16/03 – 09/30/06. (PI).

    Demonstrate a complete AC Coupled first level packaging solution in both Bulk CMOS and SOI. MCNC is a sub-contractor performing the solder bump and package fabrication investigation.

39. Steer, Franzon, Kingon, "Mixed Signal Interposer," $475,000, DARPA, 6/19/02 – 6/18/06. (co-PI, subcontract from Purdue University).

40. Franzon, "Hybrid Defense Mechanisms for Network Security," MDA, $30,000, 8/22/95 – 2/22/06 (PI at NCSU, subcontract from Irvine Sensors).

In collaboration with Irvine Sensors, implement new hardware algorithms for Intrusion Detection for high performance networks.

41. Franzon, "System Packaging for AC Coupled Interconnect," DARPA, $501,550, 7/1/04 – 9/30/09. (PI at NCSU, Subcontract from Irvine Sensors Corporation).

In collaboration with Irvine Sensors, design and build a 3D Module incorporating multiple FPGAs and memories, capable of high performance DSP.

42. Franzon, "Molecular Computing Technology," DARPA,$62,293, 8/1/04 – 7/31/05,(PI at NCSU, subctrontract from Rice University).

In collaboration with Rice University, build and demonstrate new technologies for Molecular Computing.

43. Franzon, "AC Coupled Interconnect Demonstration," SRC, 07/01/03 – 06/30/06, $300,000. (PI)

    Determine design rules for AC Coupled Interconnect Systems.

44. Franzon and Conte, "TRIPS SystemC/En-morph mode specification and Implementation", DARPA, 05/16/03-03/15/05, $275,000 (PI).

Investigate the implementation of programmable network processors using reconfigurable computing concepts. Aim at achieving configurable line rate (10 Gbps) solutions for network security, routing, and difserv.

45. Steer and Franzon, "Advanced Modeling of Mixed-Signal Systems" Agency: DARPA 08/01/01 to 07/31/04, $1,665,235. (co-PI). (See Steer's PA2 for description).

46. Steer, Kingon, and Franzon, Mixed-Signal Interposer Design and Fabrication (as subcontract to Purdue University), $1,070,000, 1 May 2002–30 April 2005., (co-PI). (See Steer's PA2 for description).

47. Franzon, "Molecular Interconnect Studies" Mission Research Corp. to DARPA 07/11/2001 to 07/10/05, $533,123 (PI).

    Work within a Naval Research Labs-lead team to develop solutions for build nanoscale molecular memories using viruses as an interconnect scaffold. Perform circuit studies, and characterization experiments.

48. Franzon, "Molecular Circuits II" DARPA, 03/21/01 - 03/31/05 $500,000 (PI).

    Work within the Rice-lead team to determine circuit architectures suited for molecular memories.

49. Franzon and Cangelleris, "Inductance Control for On-Chip Signal Integrity" NSF 08/01/00 to 07/31/05, $420,000 (PI).

    Determine practical techniques to reduce the impact of on-chip inductance on circuit performance and design time.

50. Franzon, Liu and Hughes, "SOI Deep Space Radio" NASA (sub thru A&T), 03/12/01 to 05/30/05, $771,080 (PI).

    Investigate novel circuit structures for use in an ultra-low power deep space VHF radio communications system.

51. Franzon and Liu, "AC Coupled Interconnect", SRC, 09/01/99 to 08/16/03 $321,166 (PI).

    Determine design rules and approaches for using capacitively and inductively coupled interconnect structures for between-chip communications.

52. Franzon, "Network Processor Design for Just in Time Optical Networking Protocols," ARDA, 10/01/01 to 03/28/03, $189,034 (PI).

Implement a network processor for a future optical backbone protocols using Just-In-Time (JIT) Optical Burst Switching concepts. Work with MCNC to get a small JIT network up and running. Develop new hardware algorithms for critical bottlenecks, particularly the Forwarding Engine.

53. P.D. Franzon, A. Kingon, E. Grant, “Planar Processed Robots", DARPA, 6/28/98 - 6/2/02, $1,274,527.

54. R. Hodges, et.al. and P. Franzon, “Applications of MEMS to textiles" National Textiles Foundation, 4/15/00 - 4/14/01, ECE share: $35,000.

55. P. Franzon, and W. Lui, “AC Coupled Interconnect,"10/1/99 - 9/30/02, Semiconductor Research Corporation, $321,166.

56. P. Franzon, “VLSI Approaches to Chip-Package Codesign," 1/1/00 - 6/30/00, Semiconductor Research Corporation Exploratory Grant, $25,000.

57. P. Franzon, “Molecular Circuits," 2/1/00 - 1/31/01, DARPA, $53,015.

58. P.D. Franzon, T. Conte, “SHOCC Demonstrator Study," 7/1/99 - 5/26/00, Northrop Grumman, $128,857.

59. P.D. Franzon, MEMS-based Diffractive Beam Steerer, STTR Phase 2 under sub-contract to NIPT from the USAF, Jan 1, 1998 -- June 30, 2000, ($170,000).

60. P. Franzon, W. Liu, M. Steer, Low-Power, High-Performance MEMS-based Switch Fabric, Oct. 1, 1996--Sept. 30, 1999, DARPA, ($1,047,658).

61. P. Franzon, T. Conte, W. Liu, Three Dimensional High Density Electronic Module Design and Manufacturing, Jan. 1, 1997--Dec 31., 1998, From MCMC under sub-contract from DARPA, ($257,285).

62. P. Franzon, MEMS-based Diffractive Beam Steerer, STTR under sub-contract to NIPT from the USAF, Sept. 14, 1996-- Sept. 13, 1997, ($35,000).

63. M. Steer, P. Russel, P. Franzon, “Experimental Determination of On-Chip nterconnect Capacitances", January 1, 1995 to October 31, 1995, warded by Sematech ($127,341).

64. G. Bilbro, P. Franzon, “Performance Driven System Design", awarded by Intel Corporation ($35,000 per year).

65. P. Franzon, G. Bilbro, M. Steer, “Methodology, Tools and Demonstration of MCM System Optimzition", November 1, 1993 to April 30, 1997,awarded by ARPA ($675,440).

66. P. Franzon, NSF Young Investigators Award, October 1993--March, 2000, ($285,000).

67. J. Bahler, J. Bowen, P. Franzon, “A Generic Architecture for Intelligent Networked Colocation in Concurrent Engineering" (with specific application to early system decision making vis electonic packaging), October 1, 1992 to March 31, 1996, awarded by NSF ($599,986).

68. P. Franzon, “P2E Transformation Engine for the Generation of Wiring Rules for Signal Integrity and Timing Management", May 1, 1992 to April 30, 1993, Cadence Design Systems ($35,009).

69. W. Alexander, P. Franzon, W. Liu, M. Steer, “Equipment for building and testing very high speed digital systems", awarded by NSF ($250,000).

70. P. Franzon, M. Steer, “Interconnect models for computer aided design of high speed, multichip modules and integrated circuits", 15 February, 1991 to 30 June, 1993, awarded by NSF ($273,466).

71. P. Franzon, A. Kelley, “New Approaches to Low Energy Computing", 28 February to 31 December, 1991, awarded by IBM ($29,994).

72. J. Bowen, J. Bahler, P. Franzon, “Design for Testability, Part II", 1 January, 1991 to 31 December, 1991, awarded by Integrated Manufacturing Systems Engineering Institute ($19,000).

73. H.T. Nagle, D. Van Den Bout, T. Miller, P. Franzon, “Design Center for Teaching Digital Design", 1 September, 1990 -- 31 August, 1993, awarded by NSF ($500,000).

74. P. Franzon, “Evaluation of CAD tools for teaching", MCNC, 1 January, 1991 -- 15 May, 1991, $4,500.

75. P. Franzon, “CAD Tools for MCMs", MCNC. ($24,008), 16 May 1989 -- 15 September 1990.

76. Principal Investigator, “CAD tools for yield modeling", MCNC. (\$8,694), 16 August 1989 -- 15 May 1990.

GIFTS IN CASH

1. P. Franzon, Google, Cognitive Computing, $41,000
2. P. Franzon, Mentor Graphics, Verification Tool flow, $180,000
3. P. Franzon, IBM, $95,000
4. P. Franzon, W. Davis, Cadence, Tool Flows, $25,000
5. P. Franzon, W. Liu, Analog Alliance, $142,263
6. P. Franzon, M. Steer, Cadence, Interconnect, $350,000
7. P. Franzon, W. Liu, Unrestricted Gift, Mitsubishi, VLSI Research, $93,899

8. P. Franzon, Unrestricted Gift, Motorola, $21,100
9. P. Franzon, SRC, Chip-package codesign, $25,000
10. P. Franzon, IEEE, $20,000

EDUCATIONAL GRANTS

1. H.T. Nagle, D. Van Den Bout, T. Miller, P. Franzon, “Design Center for Teaching Digital Design", 1 September, 1990 -- 31 August, 1993, awarded by NSF ($500,000).

UNSPONSORED REASEARCH

PENDING PROPOSALS

EXTERNAL EQUIPMENT

1. P. Franzon, T. Conte, W. Liu, C. Gloster, “Experimental High Performance Computing and Communications Systems", NSF CISE Infrastructure Award, July 1, 1997 -- June 30, 2003, ($1,338,283 including $503,046 in NCSU matching).

> Provide the research infrastructure for a variety of activities in the Computer Engineering group at NCSU-ECE.

INTERNAL GRANTS

1. Chancellors Innovation Fund Award, $50,000, 2013-14.
2. NCSU ECE CAD Lab, Provost Office, $75,000, 1995.

C. ORGANIZATION PARTICIPATION

- Center for Advanced Computation and Communications
- Electronics Research Laboratory, Co-Director
- Microelectronic Systems Laboratory, Director

IV. EXTENSION AND ENGATEMENT WITH CONSTITUENCIES OUTSIDE THE UNIVERSITY

A. ACCOMPLISHMENTS

- NCSU Education and Research Design Kit. This is a CAD tool (software) kit that enables researchers to design silicon chips using the MOSIS brokered foundries, and the popular Cadence And Mentor Design Tools. Originally introduced in 1994, we maintain this kit actively. Right now, there are over 2,000 active users, dominated by Universities, but also used by Industry.. I started and lead this activity. It has won several prizes from Cadence and the Cadence Users Group. With Rhett Davis, it recently expanded in a 45 nm PDK. Several tool tutorial were also recently added. More information can be found at www.ece.ncsu.edu/cadence

- NCSU Spice2Ibis Converter. This is a freeware software utility that allows the automatic macromodeling of chip input/output in the EIA IBIS standard. We have supported this converter since 1997. Version 3 was written last year. There are over 3,000 active users, mainly Industry. Together Michael Steer and I started and maintain this activity. More information can be found at www.ece.ncsu.edu/s2ibis

V. TECHNOLOGICAL AND MANAGERIAL INNOVATION

A. KNOWLEDGE/TECHNOLOGY TRANSFER

PATENTS FILED

Granted:

AT. NO.		Title
1	8,903,010	Methods, systems, and computer program products for low power multimode interconnect for lossy and tightly coupled multi-channel
2	8,804,394	Stacked memory with redundancy
5	8,208,578	Systems, methods, and computer readable media for fractional pre-emphasis of multi-mode interconnect
7	6,985,483	Methods and systems for fast packet forwarding
8	6,934,252	Methods and systems for fast binary network address lookups using parent node information stored in routing table entries
9	6,927,490	Buried solder bumps for AC-coupled microelectronic interconnects
10	6,885,090	Inductively coupled electrical connectors

Filed:

		Title
1	20140003549	METHODS, SYSTEMS, AND COMPUTER PROGRAM PRODUCTS FOR ASYMMETRIC MULTIMODE INTERCONNECT
2	20130314291	MILLIMETER SCALE THREE-DIMENSIONAL ANTENNA STRUCTURES AND METHODS FOR FABRICATING SAME
3	20130314102	DELAY FAULT TESTING FOR CHIP I/O
4	20130300498	METHODS, SYSTEMS, AND COMPUTER PROGRAM PRODUCTS FOR LOW POWER MULTIMODE INTERCONNECT FOR LOSSY AND TIGHTLY COUPLED MULTI-CHANNEL
5	20130279280	STACKED MEMORY DEVICE WITH REDUNDANT RESOURCES TO CORRECT DEFECTS
6	20130176763	STACKED MEMORY WITH REDUNDANCY
7	20130168674	Methods and Systems for Repairing Interior Device Layers in Three-Dimensional Integrated Circuits
8	20130069709	AC POWERED LOGIC CIRCUITS AND SYSTEMS INCLUDING SAME

11 20120175696 MULTILAYER FLOATING GATE FIELD-EFFECT TRANSISTOR (FET) DEVICES AND RELATED METHODS

12 20110310992 SYSTEMS, METHODS, AND COMPUTER READABLE MEDIA FOR FRACTIONAL PRE-EMPHASIS OF MULTI-MODE INTERCONNECT

14 20070297216 SELF-ASSEMBLY OF MOLECULAR DEVICES

16 20070128744 Self-assembly of molecules and nanotubes and/or nanowires in nanocell computing devices, and methods for programming same

17 20060022336 Microelectronic packages including solder bumps and AC-coupled interconnect elements

18 20050046037 Buried solder bumps for AC-coupled microelectronic interconnects

19 20040052251 Methods and systems for fast binary network address lookups using parent node information stored in routing table entries

20 20030100200 Buried solder bumps for AC-coupled microelectronic interconnects

21 20030091043 Methods and systems for fast packet forwarding

- P. Franzon, N. DeSpagna, C.J. Amsinc, D.P. Nackashi, "Achieving nanowire fanout with random alignment," provisional patent filed USPTO, 2003.
- J. Damiano, V. Misra, P. Franzon, "Multi-level Nano-Imprinting For Self-Alignment and Scalability", Provisional patent filed USPTO, 2003.

TECHNOLOGY TRANSFER

- <**Numerous submission – no longer tracked**>
- T. Conte and P. Franzon, "Networking Benchmark Kit", released 2004.
- P. Franzon. DLX RTL Design. This copyrighted microprocessor design has been released to several companies to help them evalaute their Computer Aided Design tools.
- P. Franzon. DES RTL Design. This copyright encryption design has been released to several companies to help them evalaute their Computer Aided Design tools.
- S. Lipa, A. Glaser, M. Steer, P. Franzon, Spice2Ibis software, available on the ERL Web Site.
- Y. Tekmen, S. Mehotra, P. Franzon, Signal Integrity Advisor software, available on the ERL Web Site.

B. DESCRIBE PROGRAM IMPACTS

VI. SERVICE TO UNIVERSITY AND PROFESSIONAL SOCIETIES

DEPARTMENT SERVICE

- Graduate Studies Committee, 1992-3, 2003-12
- **ECE Mission Committee, 2010-**
- **ECE Awards Committee, 2010-**
- Circuits Search Committee, 2001, 2002, 2003, 2004, 2005
- CPE Search Committee, 1995, 1996
- ECE Department Head Search Committee, 1995, 2002
- Obtained funding for and recruited, and directed NCSU IT infrastructure personnel, 1996-2001.

UNIVERSITY SERVICE

- **DELTA Advisory Committee, 2013-**
- Intellectual Property Committee, 2009-12
- STRAG committee member, 2003-2005
- COE Computing Committeee, 1994-1995

INTERNATIONAL PROFESSIONAL ACTIVITIES

- **Member, Board of Governors, IEEE CPMT, 2007-2009, 2010-2013.**
- **Chair, IEEE 3DIC Conference, 2009, 2013**
- **General Chair, IEEE CPCW, 2011.**
- Technical Program CoChair, NanoArch, 2009
- Chair, IEEE EPEP, 2007
- Co-chair, IEEE EPEP, 2006.
- **Associate Editor, IEEE Transactions on Advanced Packaging.**
- Associate Editor, ACM Journal on Emerging Computing Technologies**.**
- Program Committee Member, ChinaCOM, 2007-2008
- Program Committee Member, NanoArch, 2008-
- Program Committee Member, DesignCon, 2007-
- Program Committee Member, NanoNet, 2006-
- Program Committee Member, SPIE Microelectronics, MEMS, and Nanotechnology 2008
- **Program Committer Member, IEEE EPEP Workshop, ongoing**
- Program Committee Member, IEEE FDDP Workshop, ongoing
- Member, DARPA ISAT advisory committee on 3D ICs, 2003
- **Reviewer, Hong Kong Engineering Research Council.**
- **Reviewer, Australia Research Council**
- **Reviewer, Innovate Canada**
- **Reviewer, Singapore Science Foundation**
- **Reviewer, National Science Foundation**
- **Reviewer, Army Research Office**
- **Reviewer, US Department of Agriculture**

- **Reviewer for the journals: IEEE Transactions on Computer Aided Design, IEEE Transactions on Computers, IEEE Trans CPMT, IEEE Trans VLSI Systems, IEEE Journal of Solid State Circuits, IEEE Trans. Semiconductor Manfuacturing, Nature Materials, IEEE MTT, amongst others**
- Co-organizer, NSF Workshop on Molecular Computing, 2002
- Member, DARPA ISAT advisory committee on Molecular Computing, 2002.
- Co-Technical Chair, IEEE/IMAPS System Packaging Workshop, RTP, NC May 14-16, 2002.
- Chair, Design, Characterization, and Packaging for MEMS and Microelectronics II, SPIE Conference, Adelaide, Australia, Dec. 2001.
- General Chair, 1997 IEEE MultiChip Module Conference.
- Technical Program Chair, 1996 IEEE MultiChip Module Conference.
- Program Committee, 1996/1997 IEEE Innovative Systems In Silicon Conference.
- General Chair, 1997 IEEE MultiChip Module Conference.
- Technical Program Chair, 1996 IEEE MultiChip Module Conference.
- Co-Chair, 1993 SouthEastern Universities Undergraduate Design Conference.
- Co-Chair, 1997 IEEE Workshop on Clock Design.
- Program Committee, 1997, 1998 IEEE Int. Conference on Computer Design.
- Program Committee, 1997, 1998 ISIS.
- Tutorial Chair, 1994, 1995 IEEE MultiChip Module Conference.
- Education Committee Chair, IEEE CPMT Society, 1992-1995.
- Program Committee and Tutorial Chair, 1993-2000 IEEE Topical Meeting on
- Electrical Performance of Electronic Packaging.
- Program Committee, MICRO/MEMS'99.
- Program Committee, MICRO/MEMS'00.
- Program Committee, CPD-99, CPD-00.
- Program Committee, 1998 IPID.
- Program Committee, 1998 IMAPS MCM Conference.
- Reviewer, Design Automation Conference..
- Reviewer, Swiss National Science Foundation.