Biography

Sandip Kundu is a Professor of Electrical and Computer Engineering at the University of Massachusetts Amherst (2005-date). Currently, he is on leave from UMass, serving as a Program Director at the National Science Foundation.

Prior to joining UMass, he worked at the Intel Corporation (1997-2005) and at the Research Division of IBM Corporation (1988-1997).

He obtained his Ph.D in Electrical & Computer Engineering from University of Iowa (1988) and B.Tech (Hons.) in Electronics & Electrical Communication Engineering from the Indian Institute of Technology, Kharagpur (1984).

His research interests include Security of Mobile and Embedded devices, Computer Microarchitecture, VLSI Circuit Design and Testing, CAD algorithms, and Information and Coding Theory.

Prof. Kundu has won numerous awards including five best paper awards, Development Leadership Pioneer Award at Intel Corporation and Outstanding Technical Achievement award at IBM Corporation. He is a Fellow of the IEEE, invitational Fellow of the Japan Society for Promotion of Science (JSPS) and a Senior International Scientist of the Chinese Academy of Sciences. He has been a Distinguished Visitor of the IEEE Computer Society.

Currently he serves as an Associate Editor of the IEEE Transactions on Parallel and Distributed Systems. Previously, he has been an Associate Editor of the ACM Transactions on Design Automation of Electronic Systems, IEEE Transactions on Computers, and the IEEE Transactions on VLSI Systems.

Prof. Kundu has held visiting professor positions at the University of Freiburg in Germany, University of Montpellier in France, Kyushu Institute of Technology in Japan, Southampton University in UK, Chinese Academy of Sciences in Beijing, Tsinghua University in Beijing and the Federal University of Rio de Janeiro in Brazil.

Advanced VLSI Design and Test Laboratory

The Advanced VLSI Design and Test Group is involved in a number of projects covering a large spectrum of Microarchitecture, Security, VLSI Design and Test Research.

Computer Architecture: On a broad level, our research interests are in path finding for efficient, resilient, and reliable architectures for the *multicore era*. Today's designs are being shaped by the challenges of highly scaled technologies: stability and long-term reliability of devices, power dissipation limits that require dynamic adaptation of processor to computing needs. Our research in this area focuses on how to leverage the hardware and software abstraction layers of today's systems to tradeoff performance, power and reliability in multicores. Several of the low level details of hardware such as power, thermal, and faults are

tightly correlated to the hardware behavior, interactions within the system, and application behavior. The conventional approach to tackling such problems in hardware comes with additional costs and high design complexity. On the other hand, software based techniques are severely limited by observability and controllability into the hardware due to the strict abstraction layers of today's systems. We propose multiple alternatives for dynamic adaptation of hardware. One such approach is based on a middleware call *microvisor*. The hardware provides the knobs and controls to monitor the low level details at a fine granular level, whereas, the microvisor manages actions for the threads running on the cores. Insulating management from the traditional software (including the operating system) enables a scalable, flexible and secure system level solution and allows the microvisor to evolve freely. Other alternatives include, dedicated controller for dynamic thread monitoring and rescheduling for both symmetric and asymmetric chip multiprocessors. We are also working on the design and evaluation of a novel hybrid NoCarchitecture which utilizes separate network topologies for real time and best effort traffic so as to achieve higher QoS while simplifying arbitration.

Security: We have published a number of papers recently on Physically Unclonable Functions (PUF). Our current research focuses on PUF and True Random Number Generators (TRNG). PUF and TRNG circuits rely on underlying device characteristics to generate random response. However, they rely on different properties of underlying circuits. PUF circuits are used for chip authentication. Their responses must be *reliable* and *repeatable*, implying that PUF response should be invariant to environmental factors such as voltage and temperature disturbances, yet they must vary from one fabricated device to the other implying that they must rely on physical variations. However, the response of the PUF circuit must not be a simple linear transformation of the physical variations which makes them vulnerable to modeling attacks. If they rely on non-linear transformation of physical variations, such transformations must be sufficiently complex to withstand *modeling* attacks. Even the verifier needs to be able to withstand *cloning* attacks. It must not send the same sequence of challenges for authentication, as the correct responses may be memorized by an attacker and used subsequently. Our PUF circuits rely on exploiting lithographic distortions while we design these circuits to be insensitive to voltage and temperature to improve uniqueness while also improving their *reliability*. Our research in security is expanding to include various forms of attacks and countermeasures. We are also exploring how to use/secure NVRAM for crypto applications. Stay tuned for publications in this area soon.

VLSI CAD, Design Methodologies & Test: Our research in this area includes logic synthesis for emerging devices such as FinFETs, clocking and clock network design, 3D architectures, dynamic pattern generation for worst case power analysis, thermal simulation, lithography simulation, dual pattern lithography, optical proximity correction, lithographic error modeling, yield analysis, circuit reliability analysis, soft-error analysis, modeling of non-rectangular transistors and 3D devices. We have also explored suitability of GPGPUs for CAD algorithms. We have recently published a number of low-cost solutions for improving online error detection, diagnosis and repair that achieve nearly 100% coverage at about 15% energy overhead. We have a rich publication record in this area.

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- Technique for sorting high frequency integrated circuits (US Patent No. 5,796,751)
- System and method for testing internal nodes of an integrated circuit at any predetermined machine cycle (US Patent No. 5,793,777)
- CMOS transistor network to gate level model extractor for simulation, verification and test generation (US Patent No. 5,629,858)
- Adjustable weighted random test pattern generator for logic circuits (US Patent No. 5,297,151)
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Post-Doc:

- Hyunbean Yi (2007-2009), Assistant Professor, Hanban National Univeristy, Daejeon, Korea

PhD Students:

- Arunkumar Vijayakumar, 2016
- Sudarshan Srinivasan, 2016
- Rance Rodrigues, nVIDIA, 2013
- Kunal Ganeshpure, Mentor Graphics Corporation, 2011
- Aswin Sreedhar, Intel Corporation, 2010
- Alodeep Sanyal, Synopsys, 2010
- Omer Khan, University of Connecticut, Storrs, 2009

MS Students:

- Nithesh Kurella (2015), Samsung
- Bharath Phanibhushana (2013), Netronome
- Arunachalam Annamalai (2013), AMD
- Nishant Dhumane (2012), Broadcom Corporation
- Sudarshan Srinivasan (2012), continuing with PhD
- Lokesh Subramany (2011), Global Foundries

- Michael Buttrick (2011), Intel Corporation
- Shruti Vyas (2010), Intel Corporation
- Spandana Remarsu (2010), Intel Corporation
- Nagraj Kelageri (2009), Qualcomm
- Abhisek Pan (2009), continuing with PhD
- Rance Rodrigues (2009), continuing with PhD
- Aarti Choudhary (2008), Intel Corporation
- Kunal Ganeshpure (2007), continued to PhD
- Tariq Bashir Ahmed (2007), continued to PhD
- Aswin Sreedhar (2007), continued to PhD
- Ashesh Rastogi (2007), Intel Corporation
- Atchuthan S Perinkulam (2007), Vonage
- Tom Nielson (2006), BAE systems
- Joe Brackett (2006), BAE systems

PhD Students

- Vinay Patil, Hardware Security
- Mohammed Nazmul Islam, Hardware Security
- Brunno Goldstein, Visiting PhD student from Federal University of Rio de Janeiro, Neuromorphic Computing
- Leandro Santiago, Visiting PhD student from Federal University of Rio de Janeiro, Hardware assisted Malware Detection

MS Students

- Harikrishnan S Pillai, Quasiperiodic Oscillatory Machine for Neuromorphic Computing
- Pavithra Ramesh, Hardware Security