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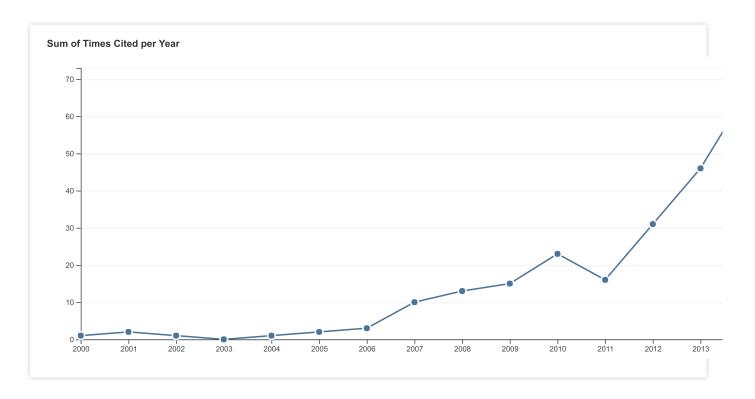




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2.	A 6.2-GFlops floating-point multiply-accumulator with conditional normalization							
	By: Vangal, Sriram R.; Hoskote, Yatin V.; Borkar, Nitin Y.; et al. IEEE JOURNAL OF SOLID-STATE CIRCUITS Volume: 41 Issue: 10 Pages: 2314-2323 Published: OCT 2006	4	1	1	0	0	25	1.92
3.	Modeling and Digital Predistortion of Class-D Outphasing RF Power Amplifiers							
	By: Landin, Per N.; Fritzin, Jonas; Van Moer, Wendy; et al. IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES Volume: 60 Issue: 6 Special Issue: SI Pages: 1907-1915 Part: 2 Published: JUN 2012	8	4	2	1	0	20	2.86
4.	A high density, low leakage, 5T SRAM for embedded caches							
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5.	Phase Predistortion of a Class-D Outphasing RF Amplifier in 90 nm CMOS							
	By: Fritzin, Jonas; Jung, Ylva; Landin, Per Niklas; et al. IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II-EXPRESS BRIEFS Volume: 58 Issue: 10 Pages: 642-646 Published: OCT 2011	4	2	2	1	0	18	2.25
6.	A Low-Power Digital DLL-Based Clock Generator in Open- Loop Mode							
	By: Mesgarzadeh, Behzad; Alvandpour, Atila Conference: 34th European Solid-State Circuits Conference Location: Edinburgh, SCOTLAND Date: SEP 15-19, 2008 Sponsor(s): Analog Devices; CamSemi; CSR; Dialog Semiconductor; JEMI; intersil; Natl Micoelectron Inst; Natl Semiconductor; Raytheon Syst Ltd; Scottish Enterprise; numonyx; Nanotechnol Electron; SMC; Memsstar Technol; NXP; Wolfson Microelectron; CHIPWORKS; IEEE; SSCS IEEE JOURNAL OF SOLID-STATE CIRCUITS Volume: 44 Issue: 7 Pages: 1907-1913 Published: JUL 2009	3	2	3	1	0	16	1.60
7.	1.56 GHz on-chip resonant clocking in 130nm CMOS							
	By: Hansson, Martin; Mesgarzadeh, Behzad; Alvandpour, Atila Book Group Author(s): IEEE Conference: IEEE Custom Integrated Circuits Conference Location: San Jose, CA Date: SEP 10-13, 2006 Sponsor(s): EEE; IEEE Solid State Circuits Soc; IEEE Elect Devices Soc PROCEEDINGS OF THE IEEE 2006 CUSTOM INTEGRATED CIRCUITS CONFERENCE Book Series: IEEE Custom Integrated Circuits Conference Pages: 241-244 Published: 2006	2	0	0	0	0	16	1.23
8.	Jitter characteristic in charge recovery resonant clock distribution	3	0	0	0	0	15	1.25

By: Mesgarzadeh, Behzad; Hansson, Martin; Alvandpour, Atila Conference: 32nd European Solid-State Circuits Conference Location: Montreux, SWITZERLAND Date: SEP 19-21, 2006 Sponsor(s): Ecole Polytech Fed Lausanne; IEEE; SSCS; Electron Devices Soc; ST; Marvell; Commune Montreux; Adv Silicon; CSEM; EM MICROELECTRONIC IEEE JOURNAL OF SOLID-STATE CIRCUITS Volume: 42 Issue: 7 Pages: 1618-1625 Published: JUL 2007 Comparative analysis of process variation impact on flip-flop power-performance By: Hansson, Martin; Alvandpour, Atila Book Group Author(s): IEEE 0 13 1.08 3 0 Conference: IEEE International Symposium on Circuits and Systems Location: New Orleans, LA Date: MAY 27-30, 2007 Sponsor(s): IEEE 2007 IEÈÉ INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS, VOLS 1-11 Book Series: IEEE International Symposium on Circuits and Systems Pages: 3744-3747 Published: 2007 **Utilizing Process Variations for Reference Generation in a** Flash ADC 2 1.20 3 0 12 By: Sundstrom, Timmy; Alvandpour, Atila IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II-EXPRESS BRIEFS Volume: 56 Issue: 5 Pages: 364-368 Published: MAY 2009 Select Page Save to Text File of 10 Sort by: Times Cited Date More Page 1 $97\ records$ matched your query of the 66,409,548 in the data limits you selected. © 2018 CLARIVATE ANALYTICS **TERMS OF USE** PRIVACY POLICY **FEEDBACK**