國立清華大學 電機工程學系

一〇四學年度第二學期

EE-5265 積體電路設計自動化

(VLSI Design Automation)

第二次作業（每人一組）

繳交日期：April 28, 2016 24:00PM 前（逾時不收）

請上 iLMS 上傳包含【原始碼及執行結果】的綜合 PDF file

(抄襲之作業將以零分計算)

◆ 題目: 平方根計算電路 **(The square root finder)** 之軟硬體設計

◆ 實習目的

To get familiarize with the modern front-end cell-based design flow.

◆ 實驗步驟與結果分析

Design a logic circuit that can *find the square root value of a given positive number, assuming that the give input number is less than* 1023.

(a) Implement a C-language program for this problem first. (Hint: You can try a successive approximation algorithm to approach to the final answer in stages iteratively.)
(b) Convert your software program into a synthesizable RTL code (in Verilog or VHDL).
(c) Verify the correctness of your RTL code by comparing its results with those from your C-code. You should try it out on at least 3 input numbers and find each of their square root values.
(d) Use a synthesis script to convert your RTL code into a gate-level netlist.
(e) Report the final gate count, the maximum operating speed (in MHz) and the estimated power dissipation in (mW) using *Design Compiler*.

◆ 繳交資料: **Mark each of the following documents clearly with a title, and then combined them into a single PDF file for submission to the iLMS system. On top of the combined PDF file should be a cover page with your** 系所，中英文姓名，學號等資訊**.**

(a) The source code of you **C-program**, and its **execution results for some inputs**.

(b) **Verilog Code**, and its **simulation results**. (Make sure the results are the same as those of your C-program)

(c) **Synthesized netlist**, and its **performance summary**.

◆ 延伸思考 **(無需繳交資料):** Can you apply your C-program to find cube root, or even $x^{(a/b)}$, where x is an input positive real number and a and b are both positive integers?