國立清華大學 電機工程學系

一〇四學年度第二學期

EE-5265 積體電路設計自動化

(VLSI Design Automation)

第三次作業（每人一組）

繳交日期：June 2, 2016 24:00PM 前（逾時不收）

請上 iLMS 上傳包含【原始碼及執行結果】的綜合 **PDF file**

(抄襲之作業將以零分計算)

◆ 題目: 平方根計算電路 **(The square root finder)** 之自動化佈局設計

◆ 實習目的

To get familiarize with the commercial back-end design flow, including the usage of a commercial Automatic Placement and Routing (APR) tool.

◆ 實驗步驟與結果分析

Perform back-end implementation for the circuit you have designed during homework #2.

(a) Use a commercial APR tool to generate the layout automatically.

(b) Perform post-layout simulation results (with back-annotation). Compare your results with those derived in the pre-layout simulation. Is post-layout faster or slower?

◆ 繳交資料: **Mark each of the following documents clearly with a title, and then combined them into a single PDF file for submission to iLMS system. On top of the combined PDF file should be a cover page with your** 系所，中英文姓名，學號等資訊**.**

(a) The overall **layout** of your design. Report your final layout size.

(c) **Post-layout simulation results**. Provide a waveform showing that your answer is correct for some input number.

(c) **Comparison table** of your pre-layout and post-layout performances of your design in terms of the maximum operating speed.

◆ 延伸思考 **(**無需繳交資料**):** Is there any way that you could do to reduce the layout size or improve the speed of your design?