

AN INTEGRATED CIRCUIT DESIGN FOR SILICON-NANOWIRE READ OUT CIRCUIT

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ABSTRACT

A read out circuit for poly-silicon nanowire field-effect transistor (SiNW FET) is proposed. The circuit use current variance of nanowire as small signal output. In other words, the readout circuit is designed to get correlation between measurement solution concentration variance and nanowire current variance.

Moreover, the circuit is able to regular the current of nanowire in a fixed value. This is referred to as constant current method in this article. With this method, the transconductance of nanowire is constant and make the output current variance purer. Moreover, a problem known as disparity is solved, which often happens by fabrication flaws or time degradation.

In summary,

1. INTRODUCTION

Poly-silicon nanowire(SiNW) is an interesting one-dimensional nano-structures because it can be directly integrated with IC. Many research of fabrication and electrical properties have been conducted [1]. Since it was first introduced to the biosensor field in 2001[2], it has become a promising candidate for ultra-sensitive, real-time and label-free sensor device. Although there has been some great advances on element structure design [3], the work of systems-level engineering is still insufficient. Mainly because a proper way of signal acquiring is still indefinite.

In this work, a read-out circuit for ion sensing SiNW based on constant current idea is proposed with some post-simulation results.

2. DESIGN DESCRIPTION

Conventionally, nanowire is treated as a simple resistor with resistance varies with ion concentration. Its read out circuits are targeted on current measurement [4] or resistance detecting [?]. However, these circuits give a mixed output result. Because nanowire is more like a MOSFET. Factors such as transconductance and short channel effect must be considered. In this work, nanowire is treated as a complete field-effect transistor(FET). The read out circuit is design for measuring the current variance with the element transconductance, drain-source voltage and even gate-source voltage fixed.

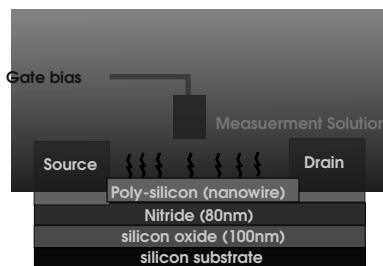


Fig. 1. The structure of SiNW element

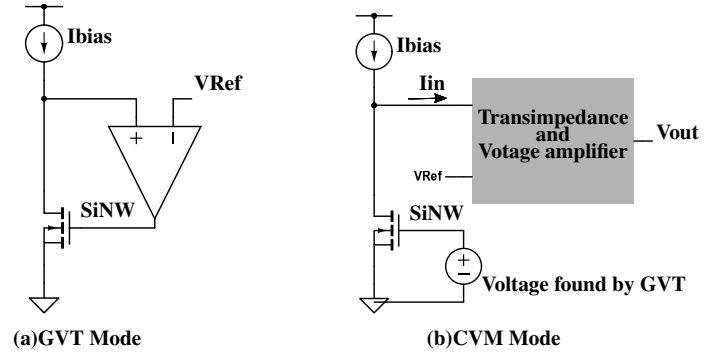


Fig. 2.

2.1. Constant Current

For a simple MOSFET, the transconductance(gm) is

$$\sqrt{2I_{DS}(\kappa\mu C_{ox} \frac{W}{L})} \quad (1)$$

in strong inversion region and

$$\frac{\kappa I_{DS}}{\phi_t} \quad (2)$$

in weak inversion region. ϕ_t is the thermal voltage. κ is the gate coupling coefficient that is 1 in strong inversion and approximately between 0.4 to 0.7 in weak inversion. The transconductance of MOSFET of a fixed size can be roughly determined by a constant drain-to-source current(I_{DS}). Furthermore, a problem known as disparity may be solved, which often happens by fabrication flaws or time degradation. Mismatched elements may still operate in a same transconductance by giving different bias current.

2.2. Architecture

The constant current structures such as source follower has been applied to several works of ion-sensitive field-effect transistor(ISFET) [5, 6], which is a relative of SiNW. A similar structure is presented here. The structure can switch between two modes: Gate-Source Voltage Tracing Mode (GVT) (showed in Fig. 2a) and Current Variance Measure Mode (CVM) (showed in Fig. 2b).

Operation in GVT is similar to Source follower. Except the negative feedback doesn't happen at source end but gate end through feedback loop circuits. This mode devotes to set up nanowire when reference ion solution is given.

CVM happens after suitable gate voltage is found in GVT. The feedback loop is removed and tested solution is given. The transconductance of nanowire changes which give rise to current variance signal. The signal will be amplified and converted into voltage by a series of transimpedance and voltage amplifier.

3. CIRCUIT IMPLEMENTATION

Fig. 3 shows the circuit schematic. GVT and CVM shared a common transimpedance, which is resistor implemented because linearity is necessary for operating under wide input current range (from 10nA to 1uA).

A controlling switch switch between integrated circuit and an external voltage source(V_b) that can memorized the voltage obtained by GVT. The switch is still operated manually. It will be designed to be automatically operated by finding a good switch time point in the future work.

At GVT SiNW gate control end, the open loop OP designed with narrow frequency response bandwidth ($\sim 20\text{Hz}$) has a use for low pass filter. It prevents noise disturbing. And most of all, it keeps the feedback loop stable when sometimes large gm of nanowire increases total loop gain.

For the output of CMS, an amplifier is designed with two amplification rate of 100 and 10. It is capacitor implemented for diminishing the offset voltage, which has maximal offset voltage of $0.2v$.

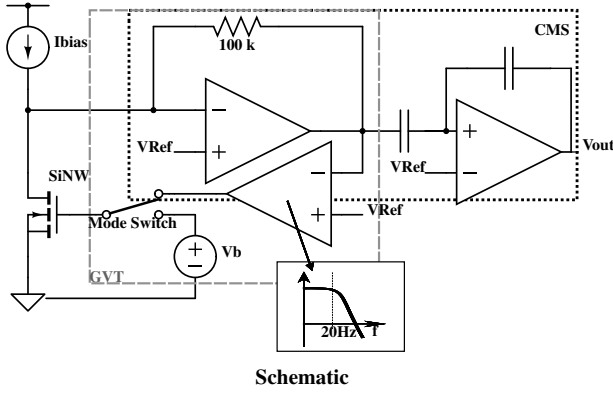


Fig. 3.

4. CONCLUSION

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