AN INTEGRATED CIRCUIT DESIGN FOR SILICON-NANOWIRE READ OUT CIRCUIT

Author(s) Name(s)

Department of Electrical Engineering, National Tsing Hua University

ABSTRACT

A read out circuit for poly-silicon nanowire field-effect transistor (SiNW FET) is proposed. The circuit uses current variance of nanowire as small signal output. In other words, the readout circuit is designed to find correlation between measurement solution concentration variance and nanowire current variance.

The circuit is able to regular the current of nanowire in a fixed value. This is referred to as constant current method in this article. With this method, the transconductance of nanowire is fixed. And the output current variance is correlate monotonically with solution concentration. Also, a problem known as disparity may be solved, which often happens by fabrication flaws or time degradation.

This article shows the design concept, circuit schematic, table of specification and some post-simulation results.

1. INTRODUCTION

Poly-silicon nanowire(SiNW) is an interesting one-dimensional nanostructures because it can be directly integrated with IC. Many research of fabrication and electrical properties have been conducted. Since it was first introduced to the biosensor field in 2001, it has become a promising candidate for ultra-sensitive, real-time and label-free sensor device. Although there has been some great advances on element structure design, the work of systems-level engineering is still insufficient. Mainly because a proper way of signal acquiring is still indefinite.

In this work, a read-out circuit for ion sensing SiNW based on constant current idea is proposed with some post-simulation results. All the design are based on the experiments before with nanowire elements from Yang's team (Fig. 1[1]). These experiments provide nanowire electrical properties and the design specification.

2. DESIGN DESCRIPTION

Conventionally, nanowire is treated as a simple resistor with resistance varies with ion concentration. Its read out circuits are targeted on current measurement or resistance detecting [2]. However, these circuits give a non-monotonic output result. Because nanowire is more like a MOSFET, and factors such as transconductance and short channel effect must be considered. In this work, nanowire is treated as a complete field-effect transistor(FET). The read out circuit is designed for measuring the current variance. And its element transconductance, drain-source voltage and even gate-source voltage are fixed.

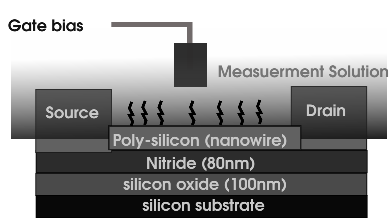

Fig. 1. Element Structure

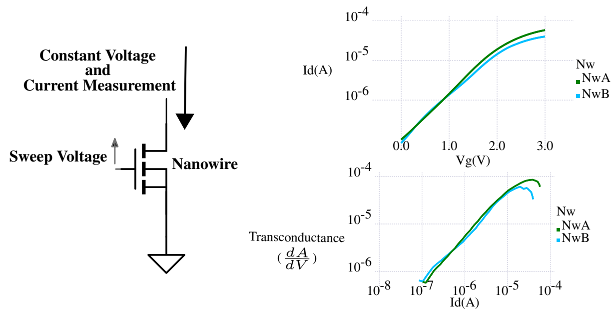

Fig. 2. Experiment for finding nanowire chracteristics. The structure is in the left side and the reults are in the right side. Transconductance is the derivative of $Id(vg)$

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2.1. Constant Current

For a simple MOSFET, its transconductance(Gm) is

$$\sqrt{2I_{DS}(\kappa\mu C_{ox}\frac{W}{L})} \tag{1}$$

in strong inversion region and

$$\frac{\kappa I_{DS}}{\phi_t} \tag{2}$$

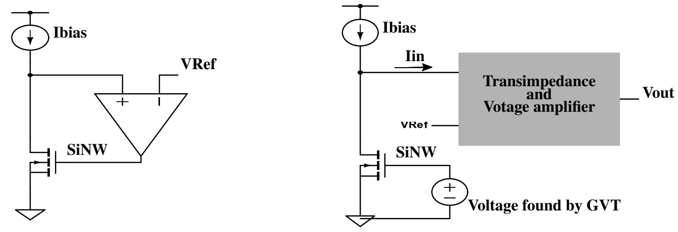
in weak inversion region. ϕ_t is the thermal voltage. κ is the gate coupling coefficient that is 1 in strong inversion and approximately between 0.4 to 0.7 in weak inversion. The transconductance of MOSFET of a fixed size can be roughly determined by a constant drain-to-source current(I_{DS}). Furthermore, a problem known as disparity which often caused by fabrication flaws or time degradation, may be solved because it is possible to force elements to operate in same transconductance by giving different bias currents.

2.2. Architecture

The constant current structures such as source follower has been applied to several works of ion-sensitive field-effect transistor(ISFET) [3], which is a relative of SiNW. A similar structure is presented here. The structure can switch between two modes: Gate-Source Voltage Tracing Mode (GVT) (Fig. 3(a)) and Current Variance Measuring Mode (CVM) (Fig. 3(b)).

Operation in GVT is similar to Source follower. Except the negative feedback doesnt happens at source but gate through feedback loop circuits. This mode devotes to set up nanowire in the beginning when the reference ion solution is given.

CVM is used after suitable gate voltage is found in GVT. In this mode, the feedback loop is removed and the tested solution is then given. The ions in the solution are attached to the surface of nanowire(gate of the FET) and the electrical field are changed. A variance of current will then appear and be converted to voltage output by a transimpedance.



(a)GVT Mode (b)CVM Mode

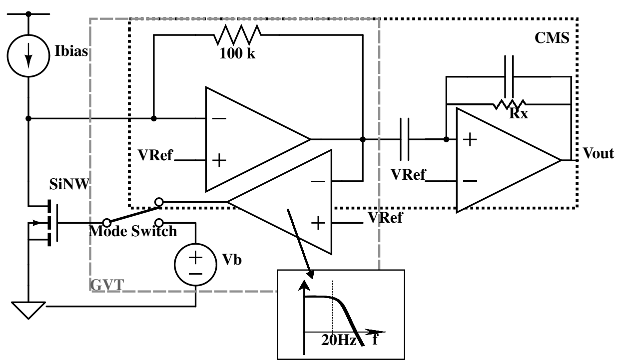
Fig. 3.

3. CIRCUIT IMPLEMENTATION

Fig. 4 shows the circuit schematic. GVT and CVM shared a common transimpedance, which is resistor-based because linearity is necessary for a wide input current range (from 10nA to 1uA). A controlling switch switches manually between integrated circuit and an external voltage source(Vb) that can memorize the voltage obtained by GVT.

At SiNW gate control terminal in the GVT block, the open loop OP with a narrow bandwidth ($<$ 20hz) has a use for low pass filter. It introduces only DC or low frequency signal into the feedback loop. Bsides, the low frequency dominant pole it creates can keeps the feedback loop stable for sometimes the large transconductance of nanowire increases total loop gain a lot.

For the output of CMS, an OP, 2 capacitor and a resistor compose a bandpass amplifier with two amplification rate, 100 and 10 respecificationtively. The pass band starts from point far below 1Hz and continue till about 1.4kHz. It is capacitor-based for diminishing the offset voltage, which has a maximal value of 0.2v. The resistor Rx is used for preventing a floating point on positive end of OP.



Schematic

Fig. 4.

4. SIMULATION RESULTS AND CONCLUSION

Fig 5 a-d shows the post-simulation results for operation under the CVM mode. A simple MOS with proper transconductances (Gm) is substituted for nanowire (By the experiment before, Gm should range from 200n to 20u). And a voltage signal is input to the gate of the MOS. Voltage of 20mV is used to emulate the ion effect when the measurement solution is added.

Maximal Signal Detection Speed(Hz)	1.4k
Maximal Input Reffered Noise(mV)	2.0
Power Consumption(mW)	0.25
SiNW transconductance Range	200n ~ 50u
SiNW Bias Current Range	100n ~ 10u

Table 1. Specification Summary

Fig. 5a shows that the total amplification rate is 6.45db (2.1) Gm: 200n. This rate increases with Gm in the same degree. The fastest signal that can be detected without attenuation is about 1.4kHz. Fig. 5b and 4c are the input-referred and output-referred noise response. The largest input referred noise should happen at Gm 200n when the total gain is smallest. The noise is small enough since its value is ten times smaller than the input signal (20mV).

Fig. 5d gives transient responses with an input signal rises in 1ms. It is to be observed that the output signal has a long settling time of about 1s. This is caused by the resistor Rx in Fig. 4. Its resistance (about 10G ohm in this work) makes the trade-off between low speed signal detection and fast responding time.

In summary, this design meets the specification propsed by the experiment before (Fig. 2) and is designed to give expected results with confidence. There are Two things can be improved in the future work. One is to make mode deciding automatic, which can be achieved by a output analysing circuit with digital structure asistance. The other is to find the bias current for each element also in an automatic way, which is mentioned in the end of the section 2.1 and can be achieved if one can find a way to detect the transconductance of individual nanowire.

5. REFERENCES

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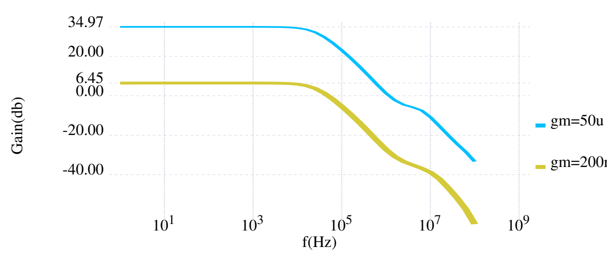
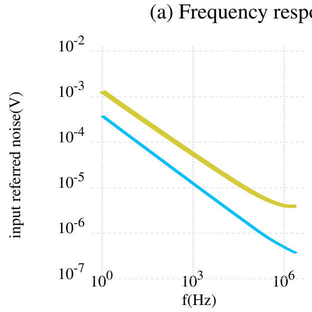
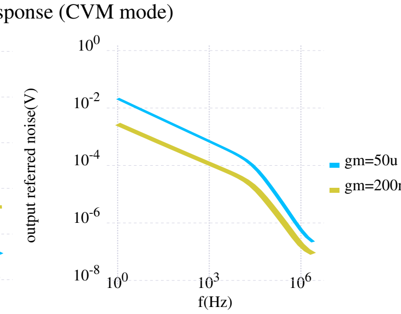


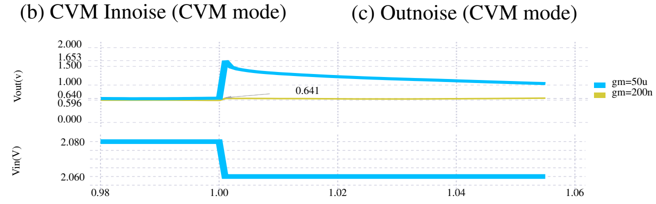
(a) Frequency response (CVM mode)



(b) CVM Innoise (CVM mode)



(c) Outnoise (CVM mode)



(d) Transient response(CVM Mode)

Fig. 5.