AN INTEGRATED CIRCUIT DESIGN FOR SILICON-NANOWIRE READ OUT CIRCUIT

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ABSTRACT

A read out circuit for poly-silicon nanowire field-effect transistor (SiNW FET) is proposed. The circuit use current variance of nanowire as small signal output. In other words, the readout circuit is designed to find correlation between measurement solution concentration variance and nanowire current variance.

The circuit is able to regular the current of nanowire in a fixed value. This is referred to as constant current method in this article. With this method, the transconductance of nanowire is fixed. And the output current variance is correlate monotonically with solution concentration. Also, a problem known as disparity may be solved, which often happens by fabrication flaws or time degradation.

This article shows the design concept, circuit schematic, table of spec and some post-simulation results.

1. INTRODUCTION

Poly-silicon nanowire(SiNW) is an interesting one-dimensional nanostructures because it can be directly integrated with IC. Many research of fabrication and electrical properties have been conducted [1]. Since it was first introduced to the biosensor field in 2001[2], it has become a promising candidate for ultra-sensitive, real-time and label-free sensor device. Although there has been some great advances on element structure design [3], the work of systems-level engineering is still insufficient. Mainly because a proper way of signal acquiring is still indefinite.

In this work, a read-out circuit for ion sensing SiNW based on constant current idea is proposed with some post-simulation results.

2. DESIGN DESCRIPTION

Conventionally, nanowire is treated as a simple resistor with resistance varies with ion concentration. Its read out circuits are targeted on current measurement [4] or resistance detecting [**?**]. However, these circuits give a non-monotonic output result. Because nanowire is more like a MOSFET, and factors such as transconductance and short channel effect must be considered. In this work, nanowire is treated as a complete field-effect

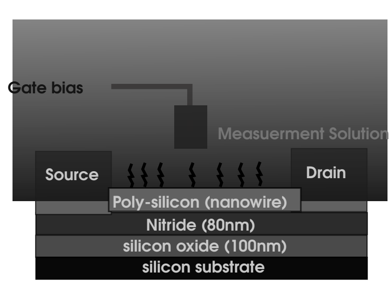


Fig. 1. The structure of SiNW element

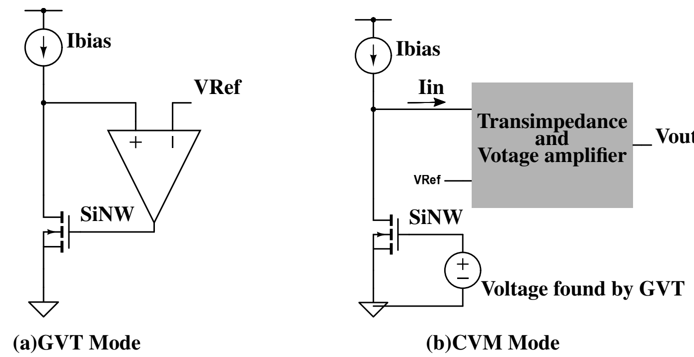


Fig. 2.

transistor(FET). The read out circuit is designed for measuring the current variance. And its element transconductance, drain-source voltage and even gate-source voltage are fixed.

2.1. Constant Current

For a simple MOSFET, the transconductance(gm) is

$$\sqrt{2I_{DS}(\kappa\mu C_{ox}\frac{W}{L})} \tag{1}$$

in strong inversion region and

$$\frac{\kappa I_{DS}}{\phi_t} \tag{2}$$

in weak inversion region. ϕ_t is the thermal voltage. κ is the gate coupling coefficient that is 1 in strong inversion and approximately between 0.4 to 0.7 in weak inversion. The transconductance of MOSFET of a fixed size can be roughly determined by a constant drain-to-source current(I_{DS}). Furthermore, a problem known as disparity which often caused by fabrication flaws or time degradation, may be solved because it is possible to force elements to operate in a same transconductance by giving different bias currents.

2.2. Architecture

The constant current structures such as source follower has been applied to several works of ion-sensitive field-effect transistor(ISFET) [5, 6], which is a relative of SiNW. A similar structure is presented here. The structure can switch between two modes: Gate-Source Voltage Tracing Mode (GVT) (Fig1(a)) and Current Variance Measuring Mode (CVM) (Fig1(b)).

Operation in GVT is similar to Source follower. Except the negative feedback doesnt happens at source end but gate *end through feedback loop circuits. This mode devotes to set up nanowire in the beginning when the reference ion solution is given.

CVM is used after suitable gate voltage is found in GVT. In this mode, the feedback loop is removed and the tested solution is then given. The ions in the solution are attached to the nanowire surface(gate-end of the FET) and the electrical field are changed. A variance of current will then appear and be converted to voltage output by a transimpedance.

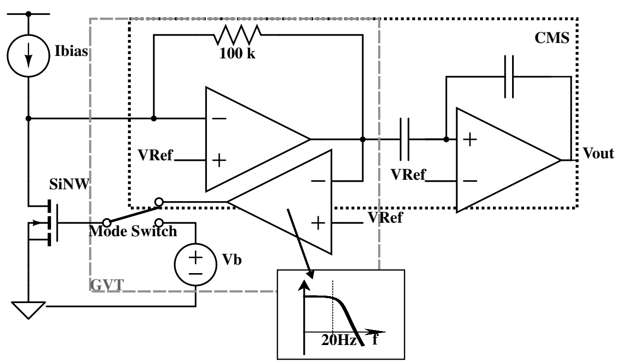
3. CIRCUIT IMPLEMENTATION

Fig. 3 shows the circuit schematic. GVT and CVM shared a common transimpedance, which is resistor-based because linearity is necessary for a wide input current range (from 10nA to 1uA). A controlling switch switches manually between integrated circuit and an external voltage source(Vb) that can memorize the voltage obtained by GVT.

At SiNW gate control end in the GVT block, the open loop OP with a narrow bandwidth (¡ 20hz) has a use for low pass filter. It prevents noise disturbing. And most of all, it keeps the feedback loop stable when sometimes large gm of nanowire increases total loop gain.

For the output of CMS, the amplifier has two amplification rate,100 and 10 respectively. It is capacitor-based for diminishing the offset voltage, which has a maximal value of 0.2v.

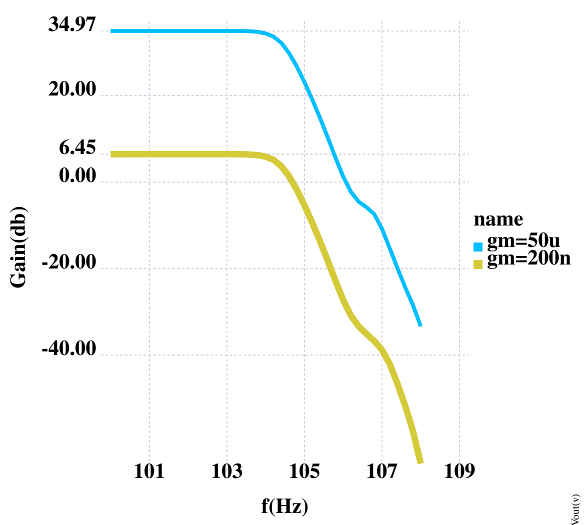
Fig 4 a-d shows some simulation results.



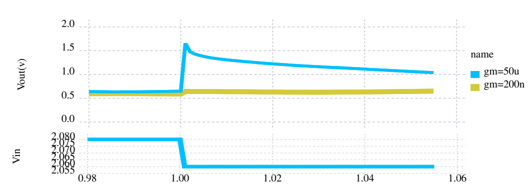
Schematic

Fig. 3.

4. CONCLUSION



(a)GVT Mode



(b)CVM Mode

Fig. 4.

5. REFERENCES

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