AN INTEGRATED CIRCUIT DESIGN FOR SILICON-NANOWIRE READ OUT CIRCUIT

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ABSTRACT

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1. INTRODUCTION

Among many kinds of one-dimensional nanostructure, the silicon nanowire(SiNW) has been highly interested in for the feasible integration with integrated circuitry. Many researches of fabrications and electrical properties have been done [1]. And since the first time it was introduced to the biosensor field in 2001[2], a promising candidate for ultra-sensitive, real-time and label-free sensor device it became.

While some great advances on element structure design were made[3], works of systems-level engineering is insufficient. Mainly because a proper way of signal acquiring is still indefinite. In this work, a read-out circuit for ion sensing SiNW based on constant current idea is proposed. Some post-simulation results are showed.

2. DESIGN DESCRIPTION

Conventionally, nanowire is treated as a simple resistor with resistance varies with ion concentration. The read out circuits are targeted on current measurement [4] or resistance detecting [5]. In this work, nanowire is treated as a complete field-effect transistor(FET) showed in Fig. 1. The read out circuit is design for measuring the current variance, which is interpreted into the transconductance of nanowire. For the reason that: the ion effects are simplified and hypothetically summed into the changes on transconductance.

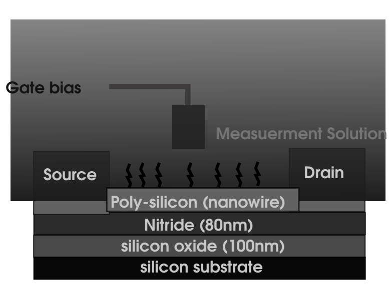


Fig. 1. The structure of SiNW element

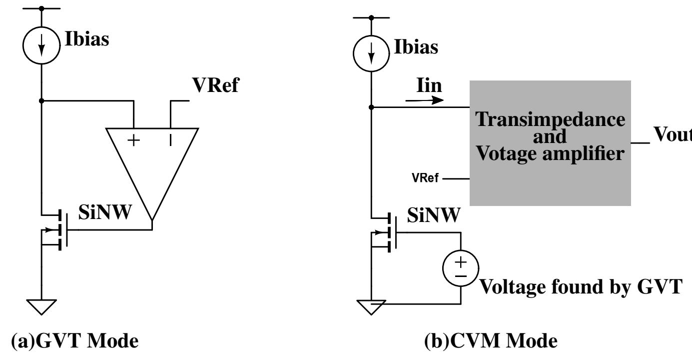


Fig. 2.

Since nanowire is analogous to the MOSFET, not only ions but intrinsic factors affect transconductance, which should be excluded. A constant current concept is adopted.

2.1. Constant Current

For a simple MOSFET, the transconductance(gm) is

$$\sqrt{2I_{Dsat}(\kappa\mu C_{ox}\frac{W}{L})} \quad (1)$$

in strong inversion region and

$$\frac{\kappa I_{Ds}}{\phi_t} \quad (2)$$

in weak inversion region. ϕ_t is thermal voltage. I_{Dsat} can be simplfied to I_{Ds} for a constant V_{Ds}. κ is the gate coupling coefficient that is 1 in strong inversion and approximately 0.4 to 0.7 in weak inversion. The equations show the transconductance of the MOSFET with fixed size can be roughly decided by giving constant drain-to-source current.

2.2. Architecture

The constant current structures such as source follower has been applied to several works of ion-sensitive field-effect transistor(ISFET) [6, 7], which is a relative of SiNW. A similar structure is presented here. The structure can switch between two modes: Gate-Source Voltage Tracing Mode (GVT) (showed in Fig. 2a) and Current Variance Measure Mode (CVM) (showed in Fig. 2b).

Operation in GVT is similar to Source follower. Except the negative feedback doesnt happens at source end but gate end through feedback loop circuits. This mode devotes to set up nanowire when reference ion solution is given.

CVM happens after suitable gate voltage is found in GVT. The feedback loop is removed and tested solution is given. The transconductance of nanowire changes which give rise to current varainace signal. The signal will be amplified and converted into voltage by a series of transimpedance and voltage amplifier.

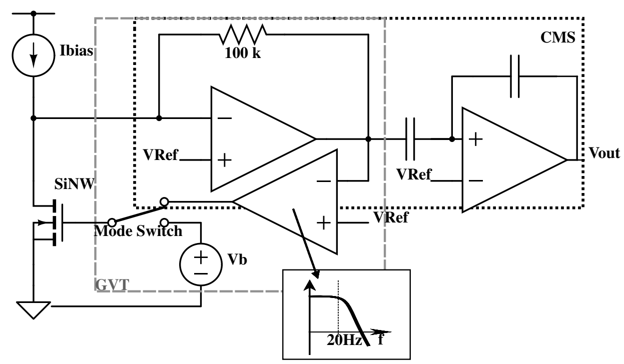
3. CIRCUIT IMPLEMENTATION

Fig. 3 shows the circuit schematic. GVT and CVM shared a common transimpedance, which is resistor implemented because linearity is necessary for operating under wide input current range (from 10nA to 1uA).

A controlling switch switch between integrated circuit and an external voltage source(Vb) that can memorized the voltage obtained by GVT. The switch is still operated manually. It will be designed to be automatically operated by finding a good switch time point in the future work.

At GVT SiNW gate control end, the open loop OP designed with narrow frequency response bandwidth (¡ 20hz) has a use for low pass filter. It prevents noise disturbing. And most of all, it keeps the feedback loop stable when sometimes large gm of nanowire increases total loop gain.

For the output of CMS, an amplifier is designed with two amplification rate of 100 and 10. It is capacitor implemented for diminishing the offset voltage, which has maximal offset voltage of 0.2v.



Schematic

Fig. 3.

4. CONCLUSION

Put your conclusion here.

5. REFERENCES

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