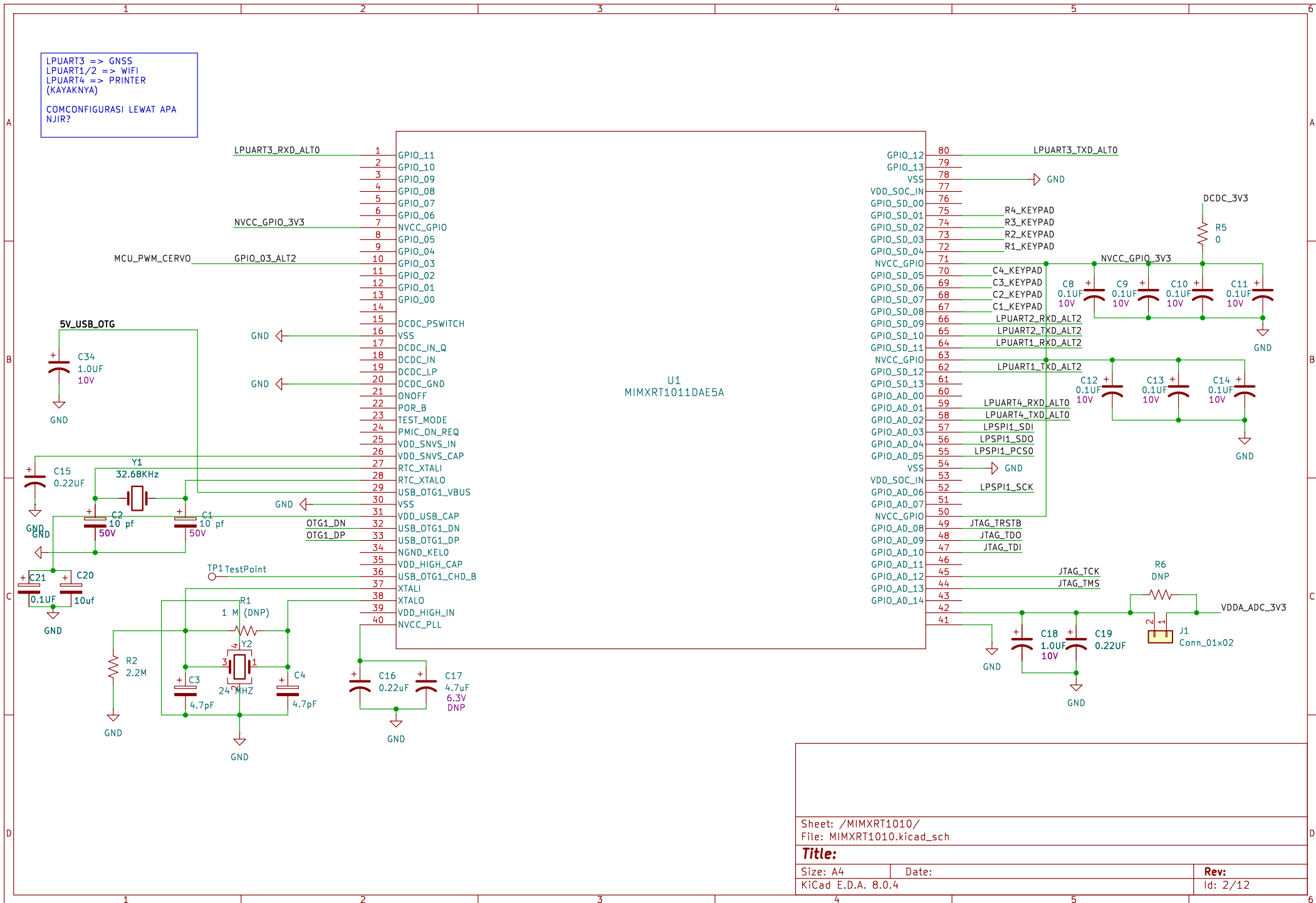
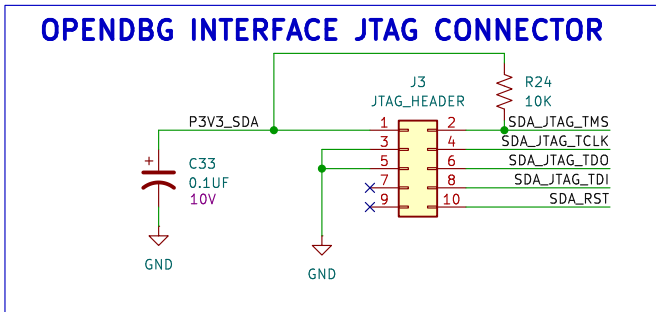
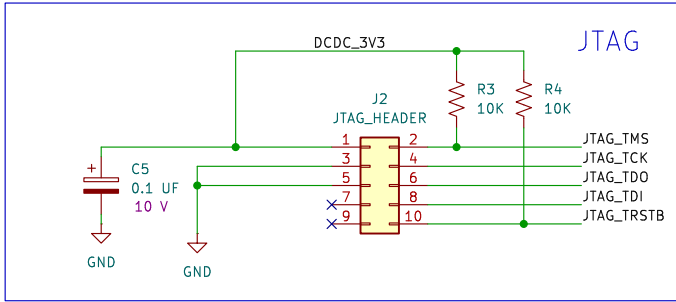


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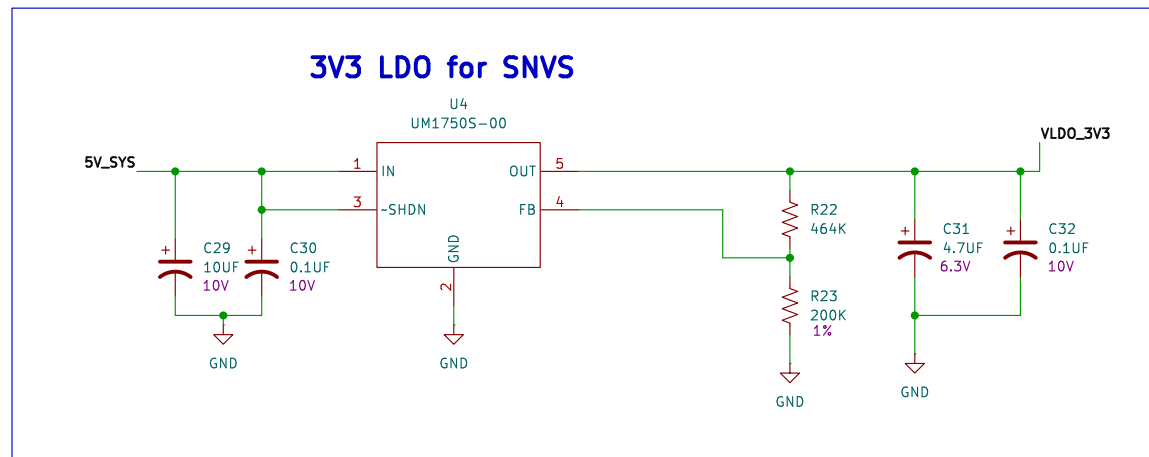
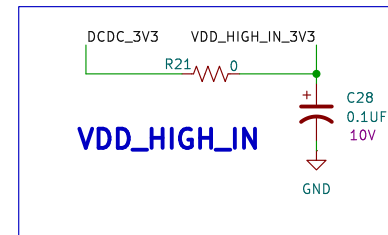
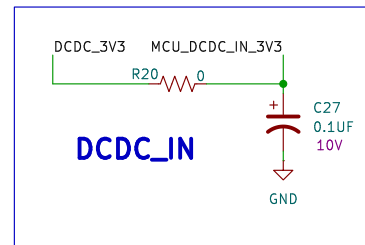
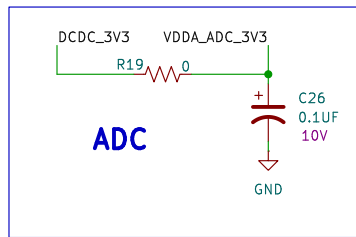
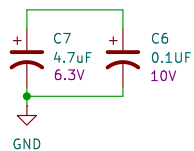
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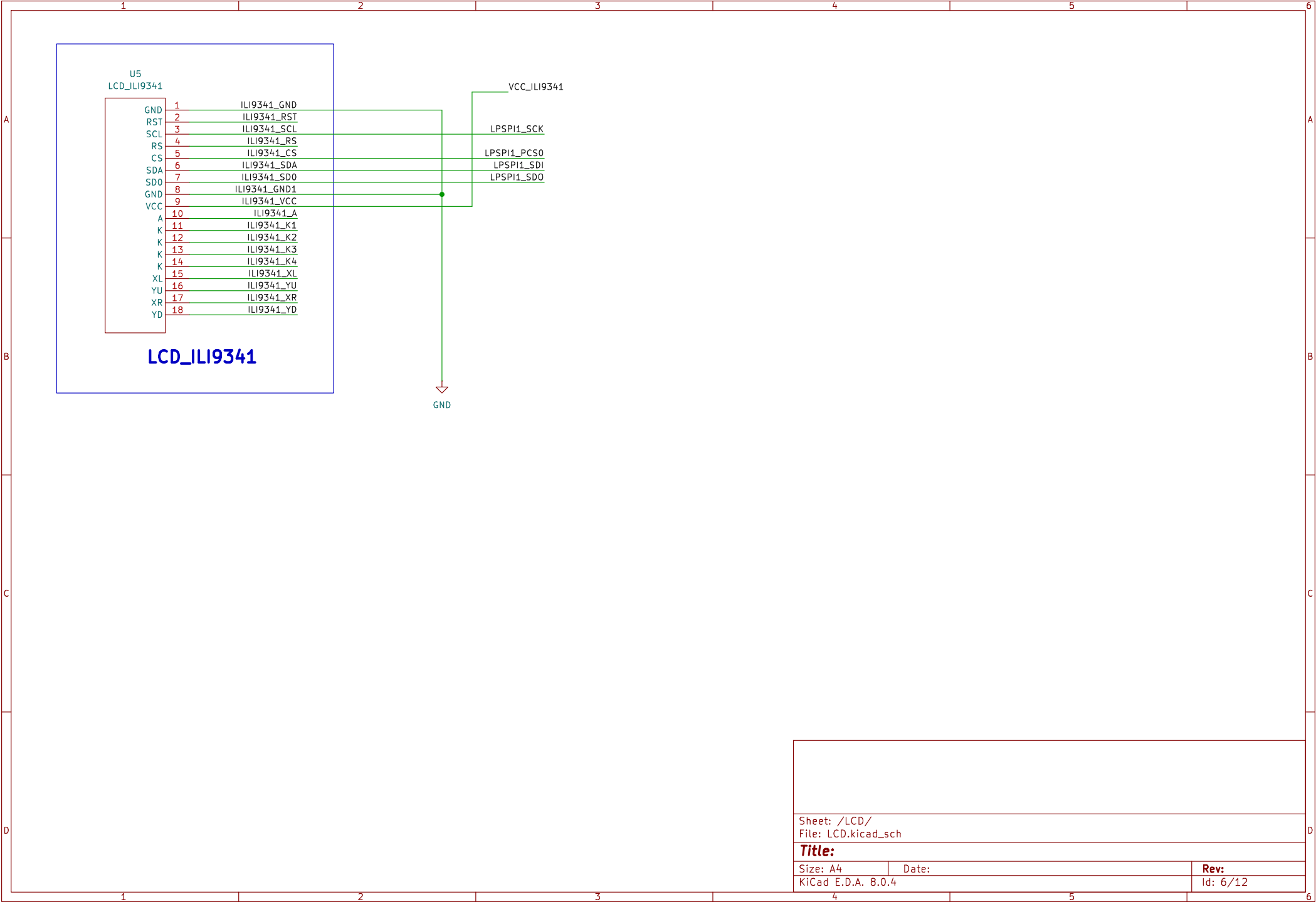
LPSPi Flash

The schematic diagram illustrates the LPSPi Flash circuit. The flash memory (U2, MX25L4006EM2R-12G) is connected to the LPSPi controller. The flash is connected to DCDC_3V3 via a 0.1uF capacitor (C22) and to GND via a 0.1uF capacitor (C23). The flash is also connected to the LPSPi controller via a 10k resistor (R9) and to the LPSPi controller via a 0.1uF capacitor (C22). The flash is connected to the LPSPi controller via a 0.1uF capacitor (C22). The flash is connected to the LPSPi controller via a 0.1uF capacitor (C22).

3v3 QSPI Flash

The diagram illustrates the electrical connections for a 3V3 QSPI Flash memory (U3: AT25SF128A-SHB-T). The circuit includes a DCDC_3V3 input, a resistor R15, two capacitors C25 and C24 (1.0UF 10V), a GND connection, a QSPI Flash chip U3 (AT25SF128A-SHB-T), and several signal lines: FlexSPL_D0_A, FlexSPL_CLK_A, FlexSPL_SS0, FlexSPL_D2_A, FlexSPL_D3_A, and FlexSPL_D1_A. The chip has pins for VCC, GND, SI/IO0, SCLK, ~CS, ~WP/IO2, and ~HOLD/IO3. The chip is connected to a 3V3 supply and ground, and its data lines are connected to the FlexSPL signals.

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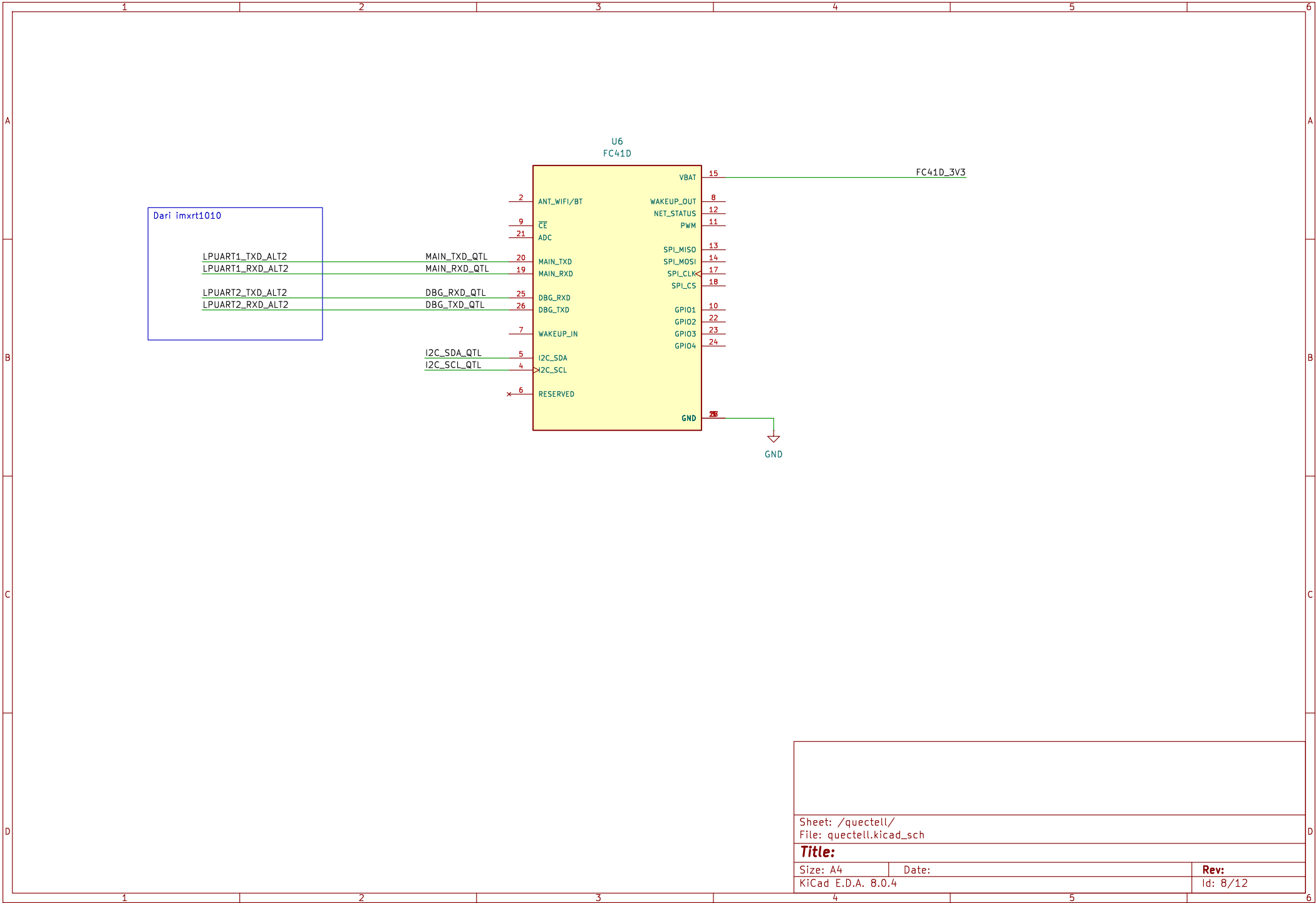
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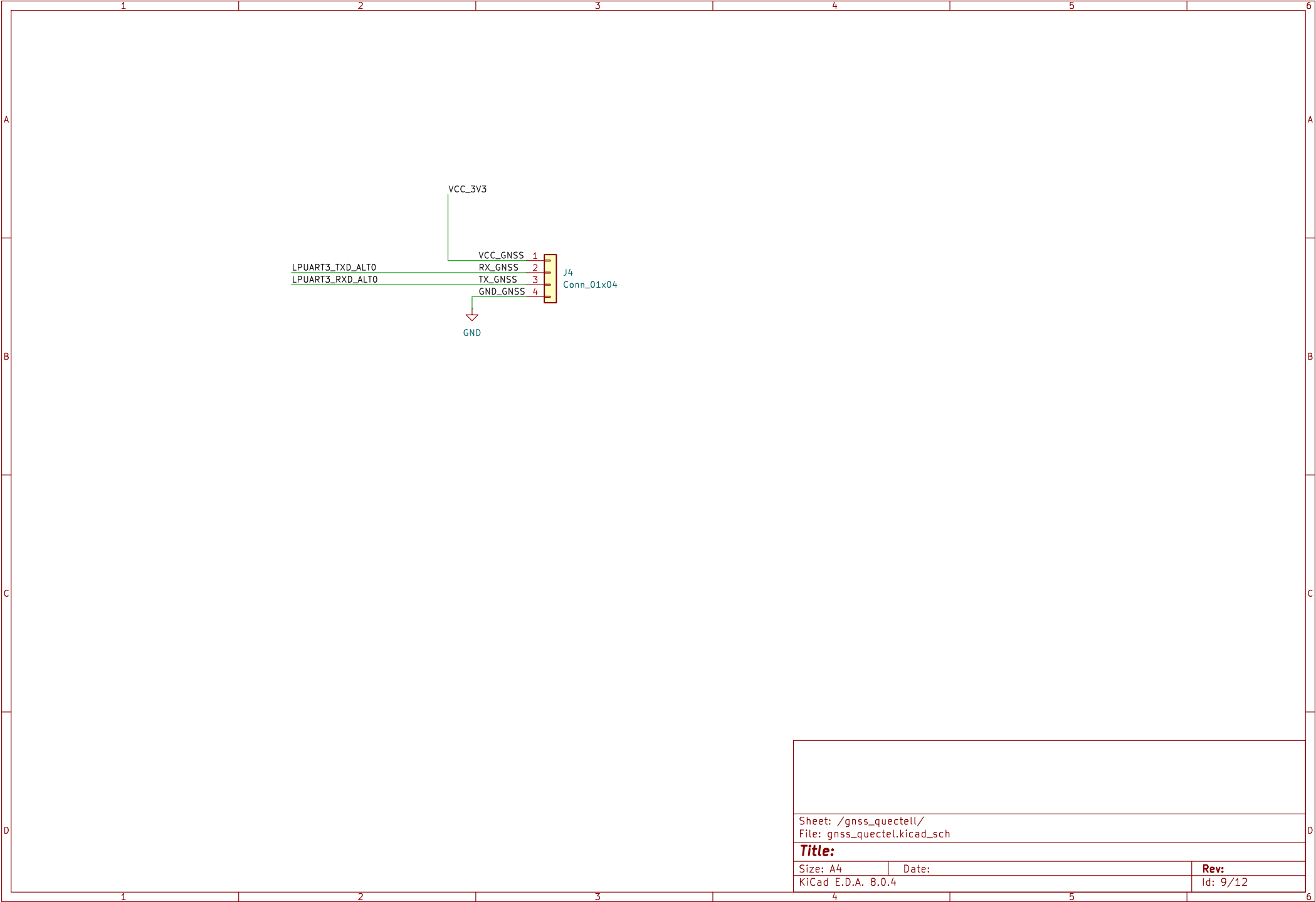
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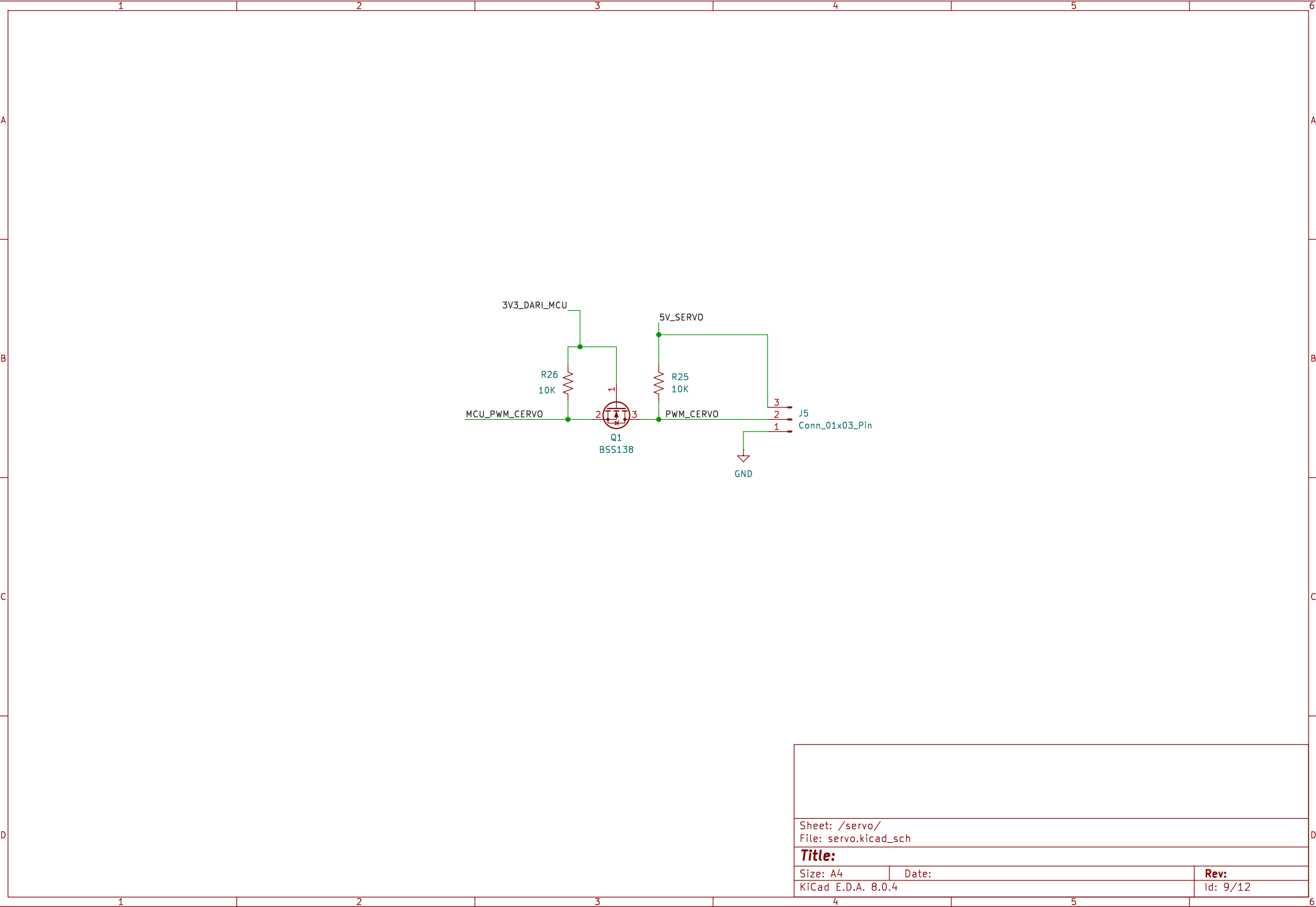
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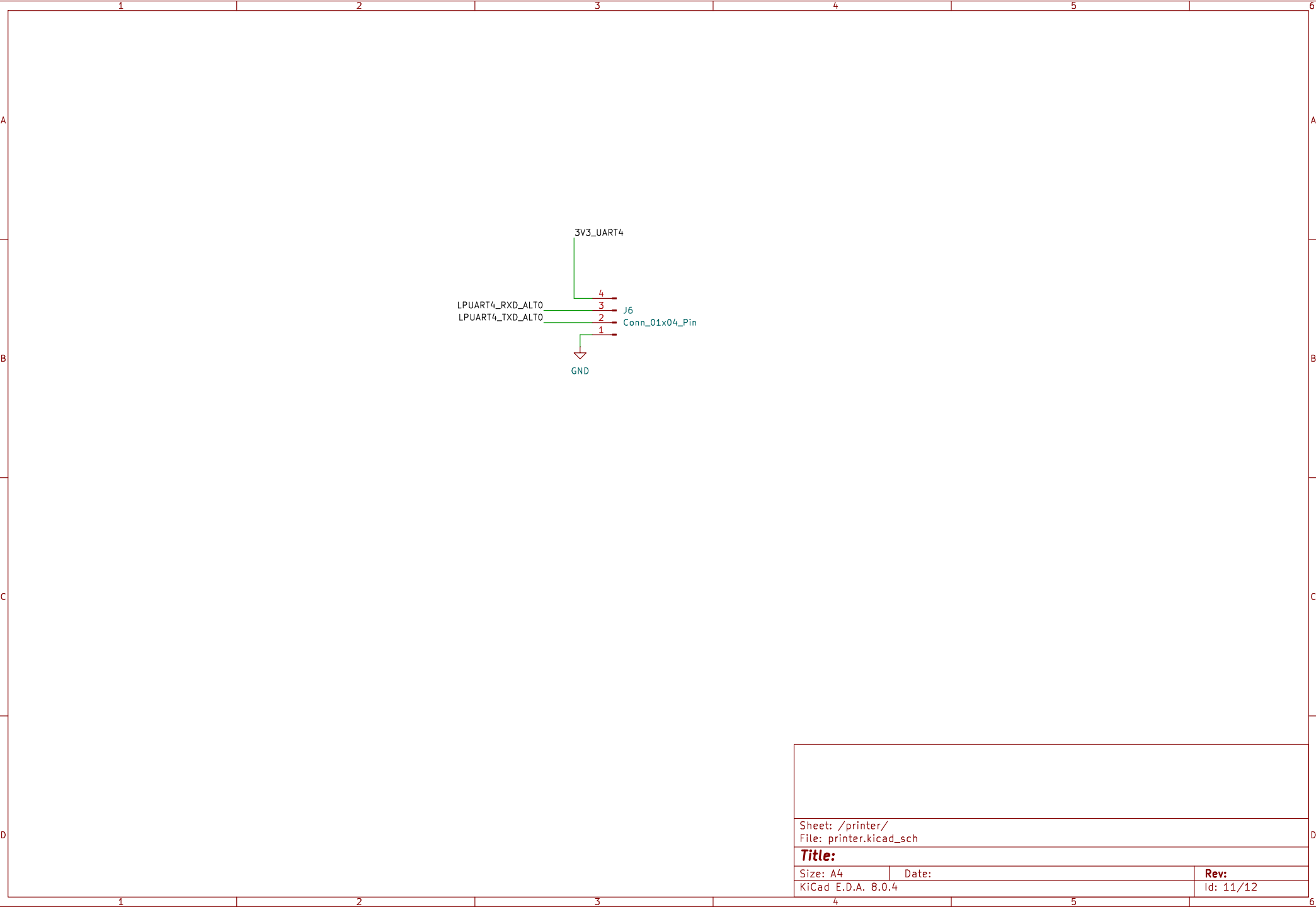
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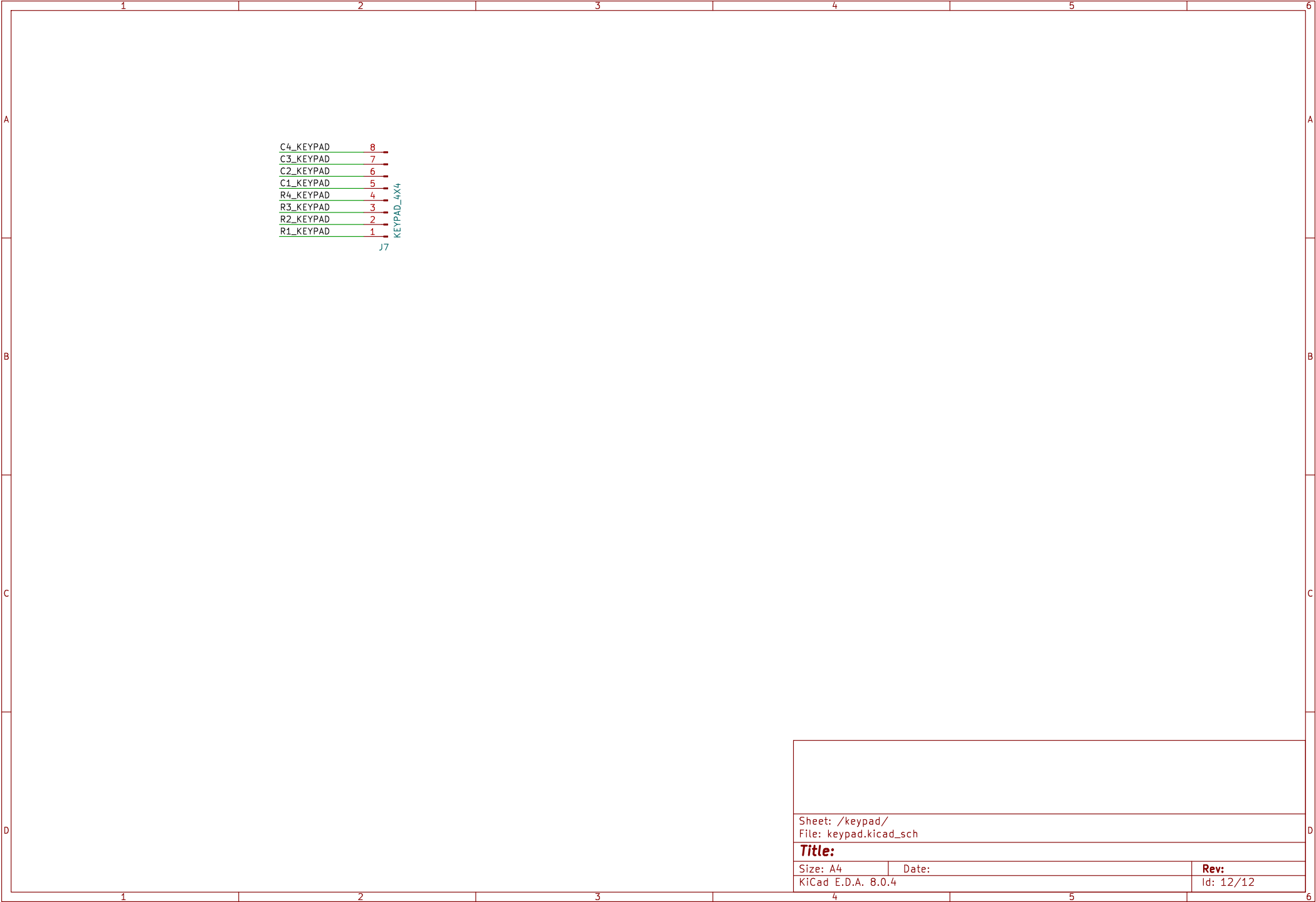
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