

Mounting Holes

- MH1
- MH2
- MH3
- MH4

University of Waterloo
200 University Ave W
Waterloo, Ontario, Canada
N2L 3G1

REV
1.0

PROJECT
LTO 16S BMS.PrjPcb, [No Variations]

DOCUMENT
Top.SchDoc

ENGINEER
Farris Matar

REVIEWER
*

MODIFIED
2023-05-19

SHEET 1 OF 11

1

2

3

4

A

A

B

B

C

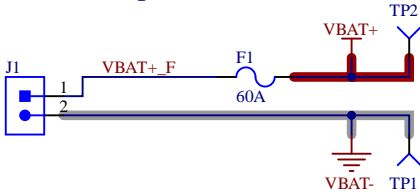
C

D

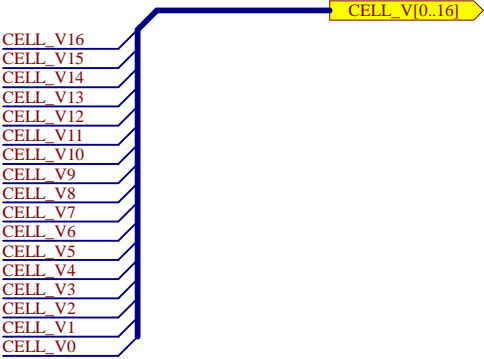
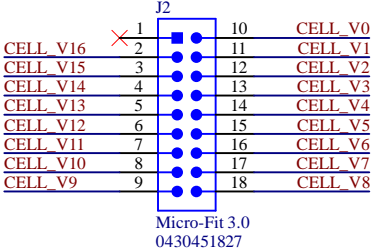
D

Battery specs:
- 16s1p 20Ah LTO battery
- 1.5V - 2.7V cell voltage range, 2.3V nominal

Power Input



Cell Sensing Inputs



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DOCUMENT
Battery_Interface.SchDoc

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2023-05-07

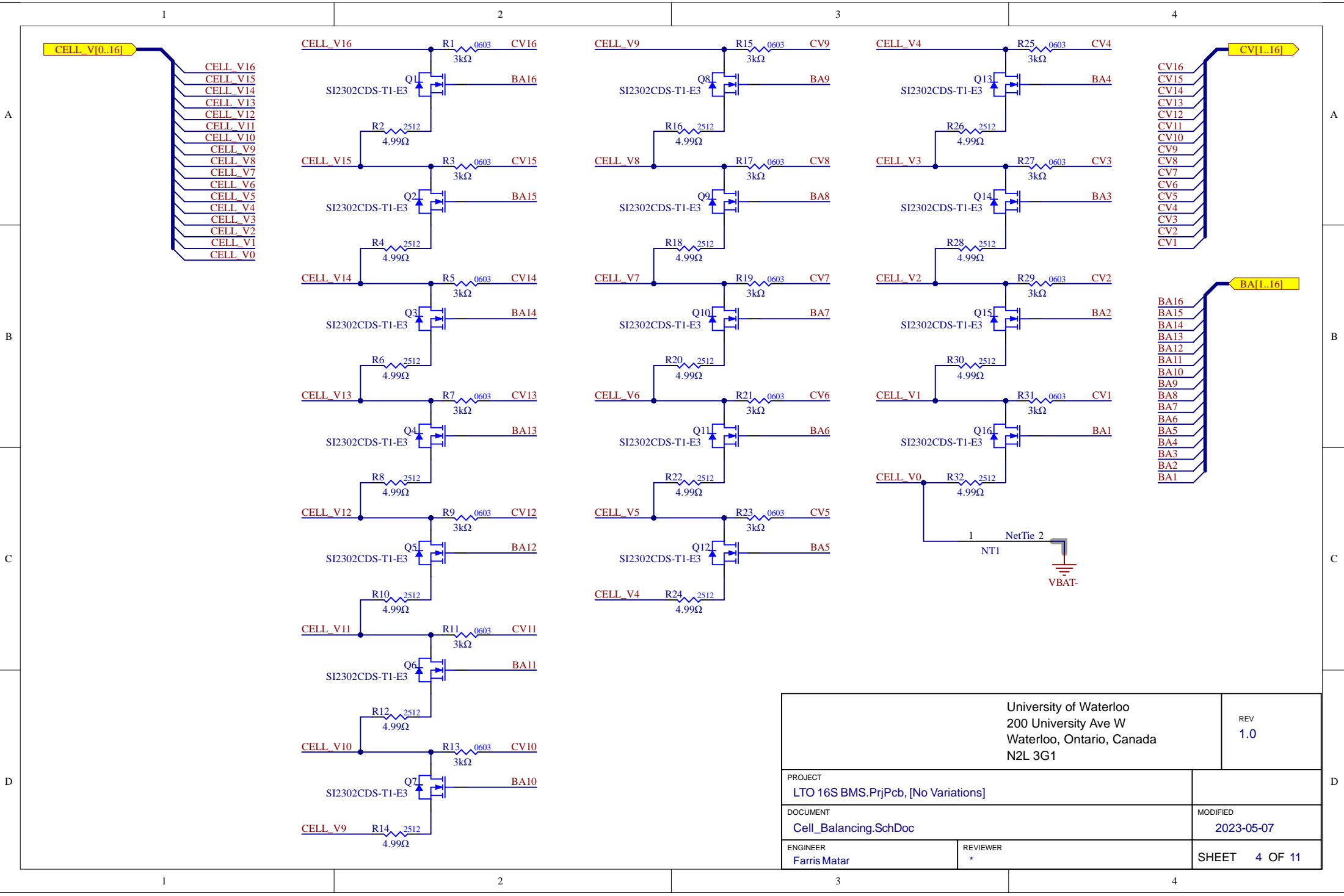
SHEET 2 OF 11

1

2

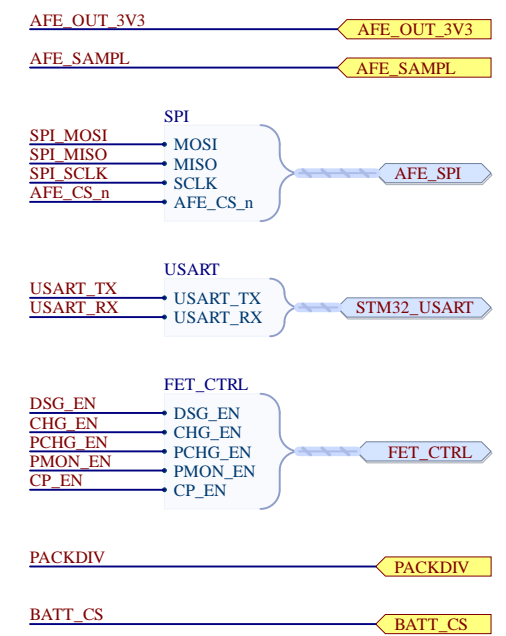
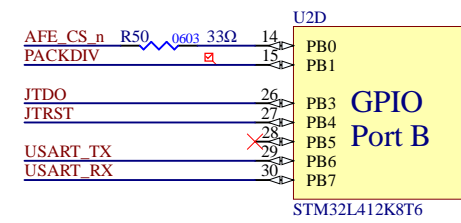
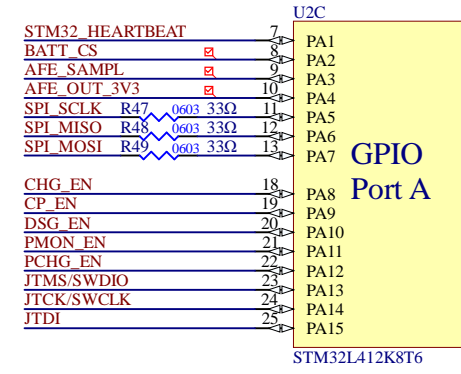
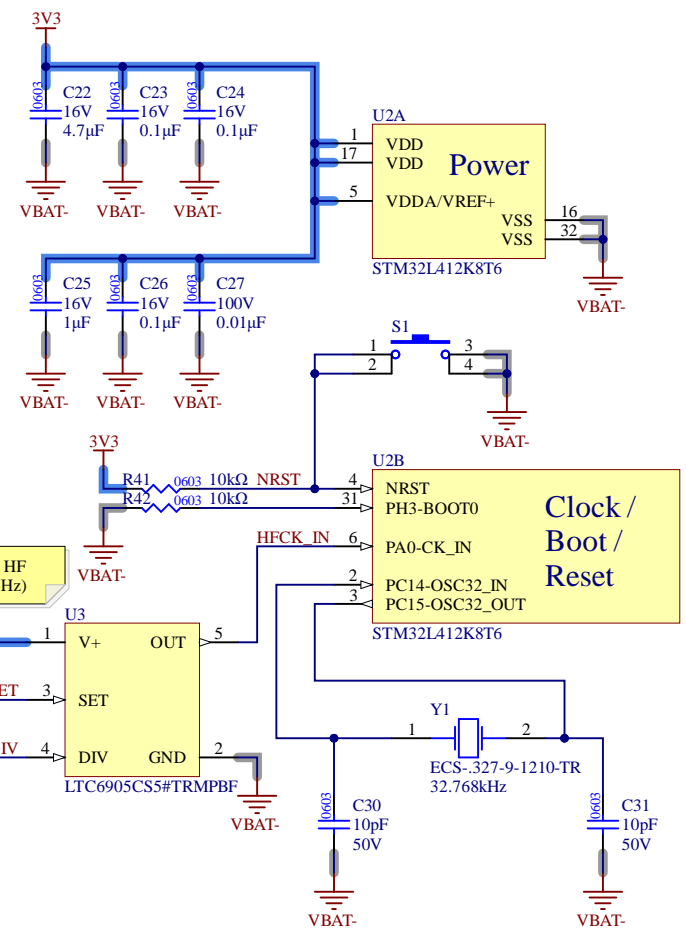
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4

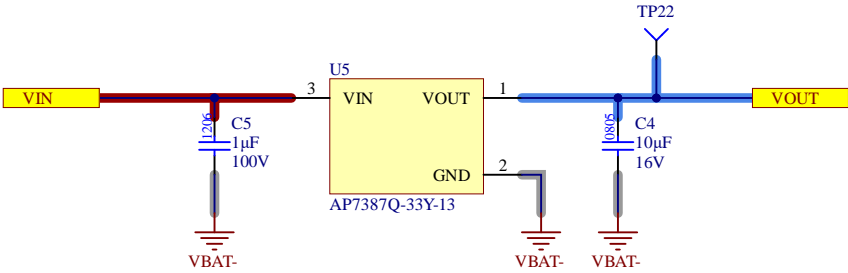


Follows reference design provided in https://www.st.com/resource/en/application_note/an4555-getting-started-with-stm32l4-series-and-stm32l4-series-hardware-development-stmicroelectronics.pdf (Figure 14), minor modifications made to fit selected package

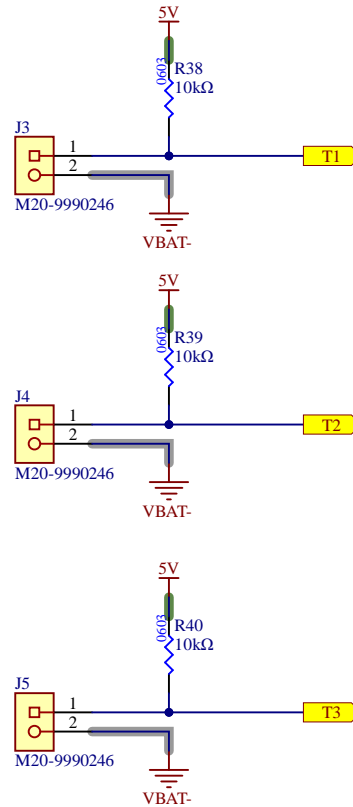
Circuit to provide a HF clock (approx. 24MHz)



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PROJECT LTO 16S BMS.PrjPcb, [No Variations]		
DOCUMENT STM32_MCU.SchDoc	MODIFIED 2023-05-19	
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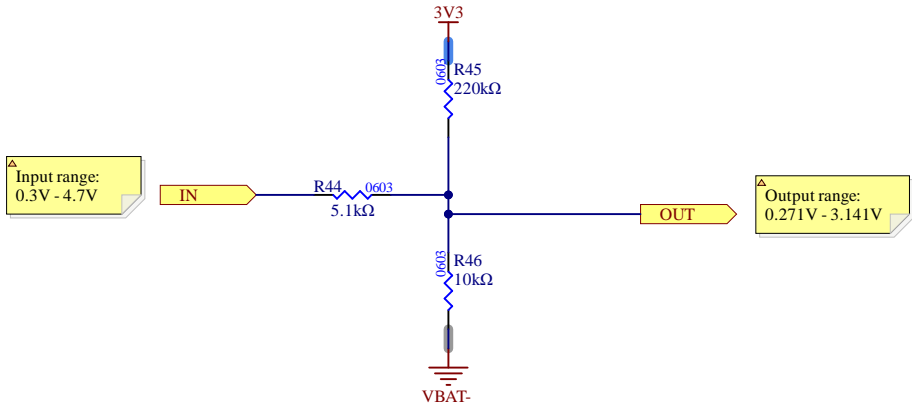


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PROJECT LTO 16S BMS.PrjPcb, [No Variations]		
DOCUMENT Power_3V3.SchDoc		MODIFIED 2023-05-07
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PROJECT LTO 16S BMS.PrjPcb, [No Variations]		
DOCUMENT Temperature_Sense.SchDoc		MODIFIED 2023-05-07
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Δ Analog attenuator circuit, based on this TI post:
https://e2e.ti.com/blogs_/b/analogwire/posts/three-ways-to-scale-an-analog-input-signal
Falstad sim: <https://tinyurl.com/2k2x8zjf>



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PROJECT LTO 16S BMS.PrjPcb, [No Variations]		
DOCUMENT Analog_Attenuator.SchDoc		MODIFIED 2023-05-07
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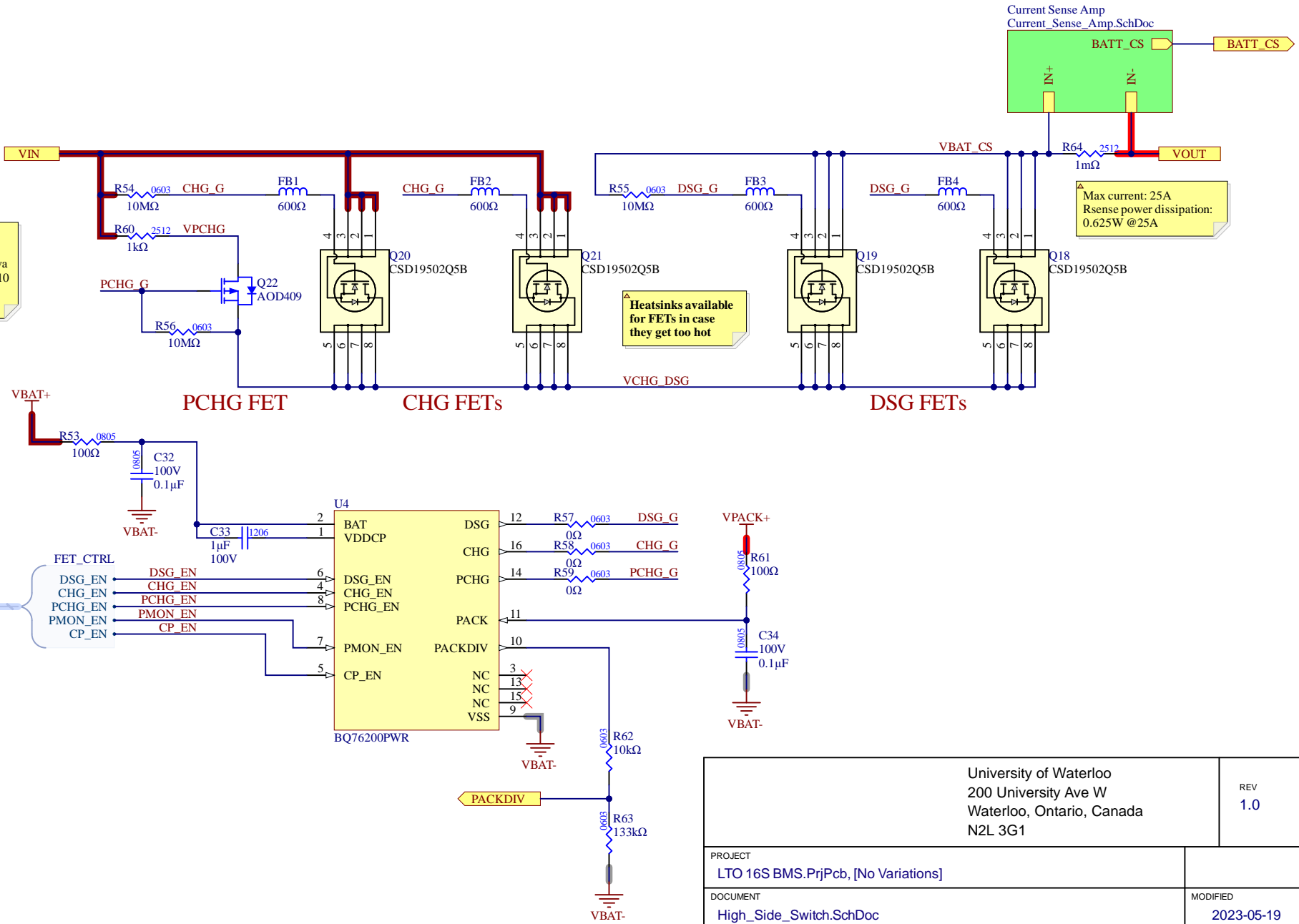
Parallel FETs configured based on TI app note: <https://www.ti.com/lit/an/slva729a/slva729a.pdf?ts=1684104737246>

Heatsinks available for FETs in case they get too hot

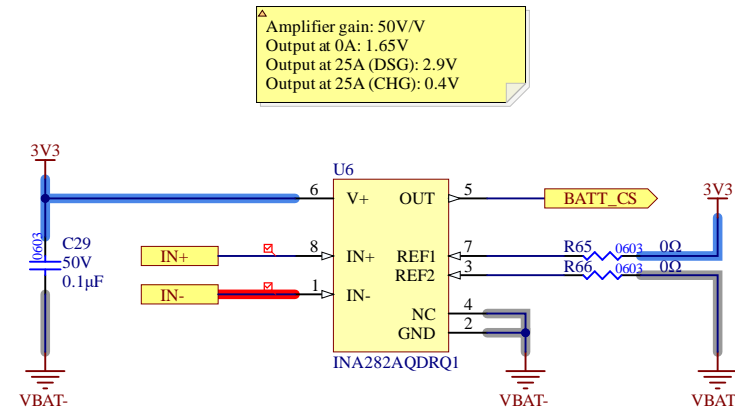
Max current: 25A
Rsense power dissipation: 0.625W @ 25A

FET_CTRL

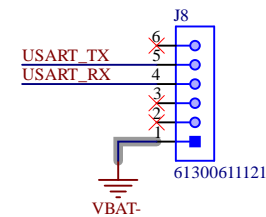
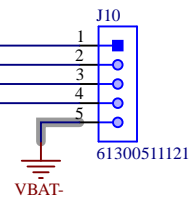
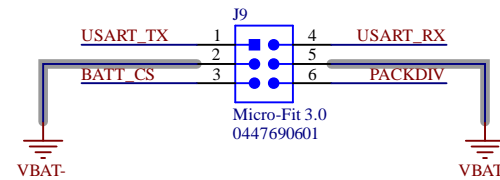
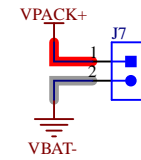
- DSG_EN
- CHG_EN
- PCHG_EN
- PMON_EN
- CP_EN



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PROJECT LTO 16S BMS.PrjPcb, [No Variations]		
DOCUMENT High_Side_Switch.SchDoc		MODIFIED 2023-05-19
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PROJECT LTO 16S BMS.PrjPcb, [No Variations]		
DOCUMENT Current_Sense_Amp.SchDoc		MODIFIED 2023-05-19
ENGINEER Farris Matar	REVIEWER *	SHEET 10 OF 11



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PROJECT LTO 16S BMS.PrjPcb, [No Variations]		
DOCUMENT Pack_Interface.SchDoc		MODIFIED 2023-05-19
ENGINEER Farris Matar	REVIEWER *	SHEET 11 OF 11