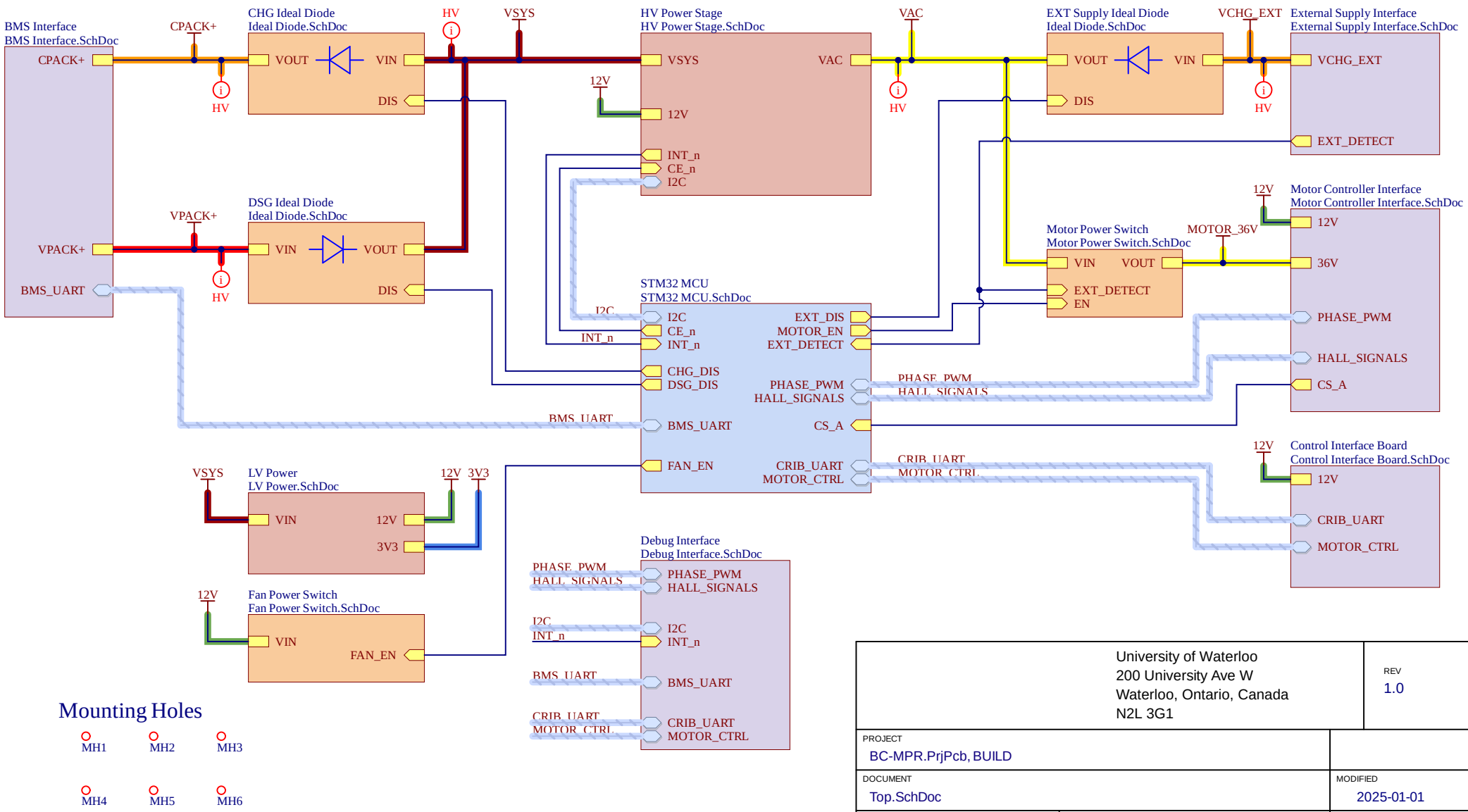
BMS Interface
BMS Interface.SchDoc
CPACK+
VPACK+
BMS_UART
CHG Ideal Diode
Ideal Diode.SchDoc
VOUT
VIN
DIS
DSG Ideal Diode
Ideal Diode.SchDoc
HV
VSYS
HV Power Stage
HV Power Stage.SchDoc
VAC
12V
INT_n
CE_n
I2C
EXT Supply Ideal Diode
Ideal Diode.SchDoc
VCHG_EXT
External Supply Interface
External Supply Interface.SchDoc
EXT_DETECT
Motor Power Switch
Motor Power Switch.SchDoc
EN
MOTOR_36V
Motor Controller Interface
Motor Controller Interface.SchDoc
36V
PHASE_PWM
HALL_SIGNALS
CS_A
STM32 MCU
STM32 MCU.SchDoc
EXT_DIS
MOTOR_EN
CHG_DIS
DSG_DIS
FAN_EN
CRIB_UART
MOTOR_CTRL
LV Power
LV Power.SchDoc
3V3
Fan Power Switch
Fan Power Switch.SchDoc
Debug Interface
Debug Interface.SchDoc
Control Interface Board
Control Interface Board.SchDoc
Mounting Holes
MH1
MH2
MH3
MH4
MH5
MH6
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Waterloo, Ontario, Canada
N2L 3G1
REV
1.0
PROJECT
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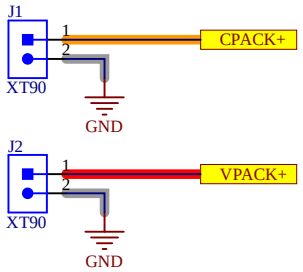
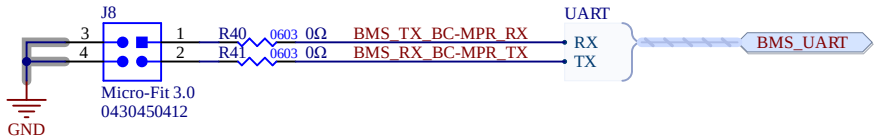
DOCUMENT
Top.SchDoc
MODIFIED
2025-01-01
ENGINEER
Farris Matar
REVIEWER
*
SHEET 1 OF 14

BMS INTERFACE

BMS Power Ports

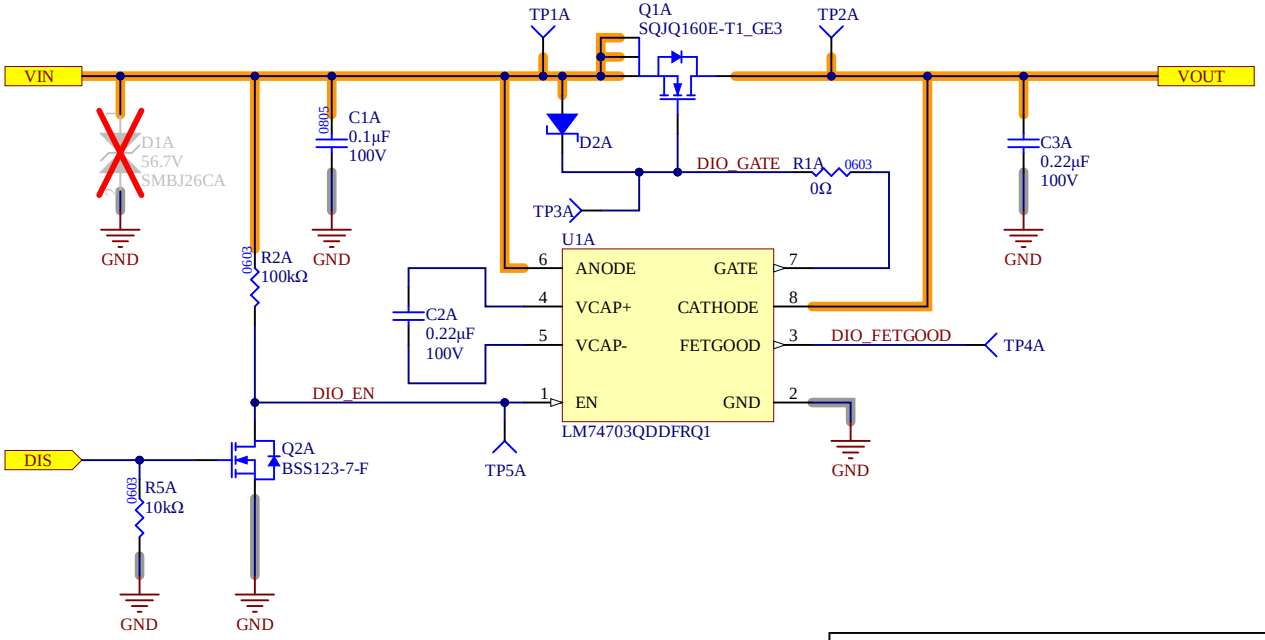


UART Communication



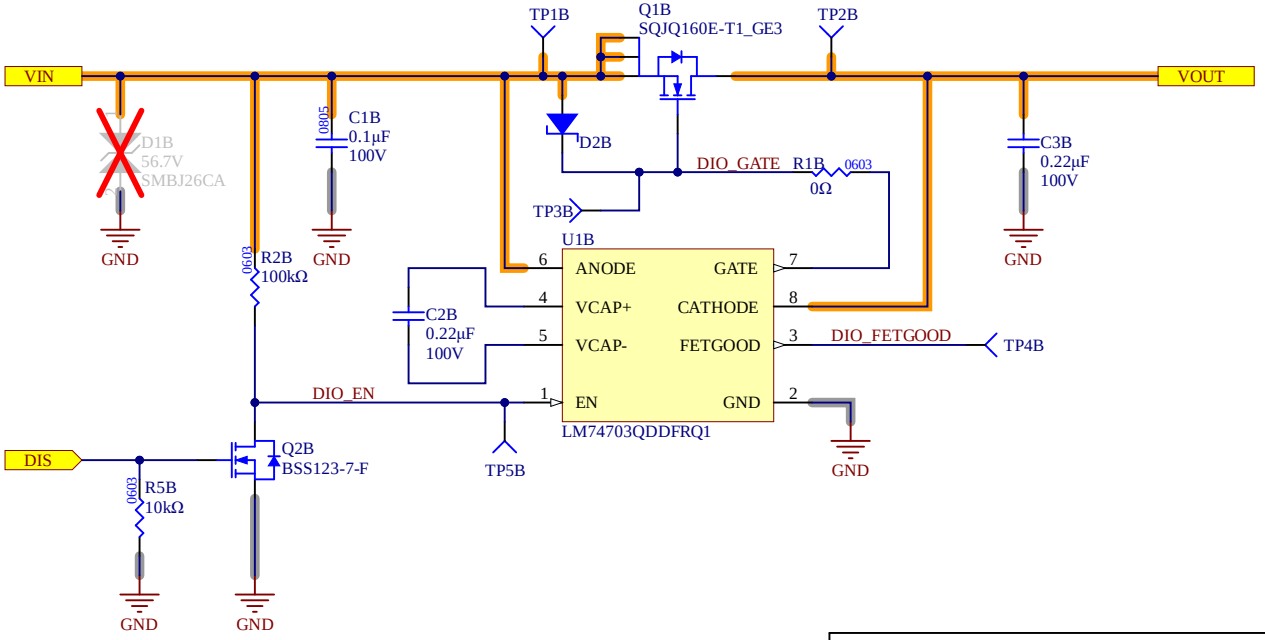
University of Waterloo 200 University Ave W Waterloo, Ontario, Canada N2L 3G1		REV 1.0
PROJECT BC-MPR.PrjPcb, BUILD		
DOCUMENT BMS Interface.SchDoc		MODIFIED 2024-12-27
ENGINEER Farris Matar	REVIEWER *	SHEET 2 OF 14

IDEAL DIODE



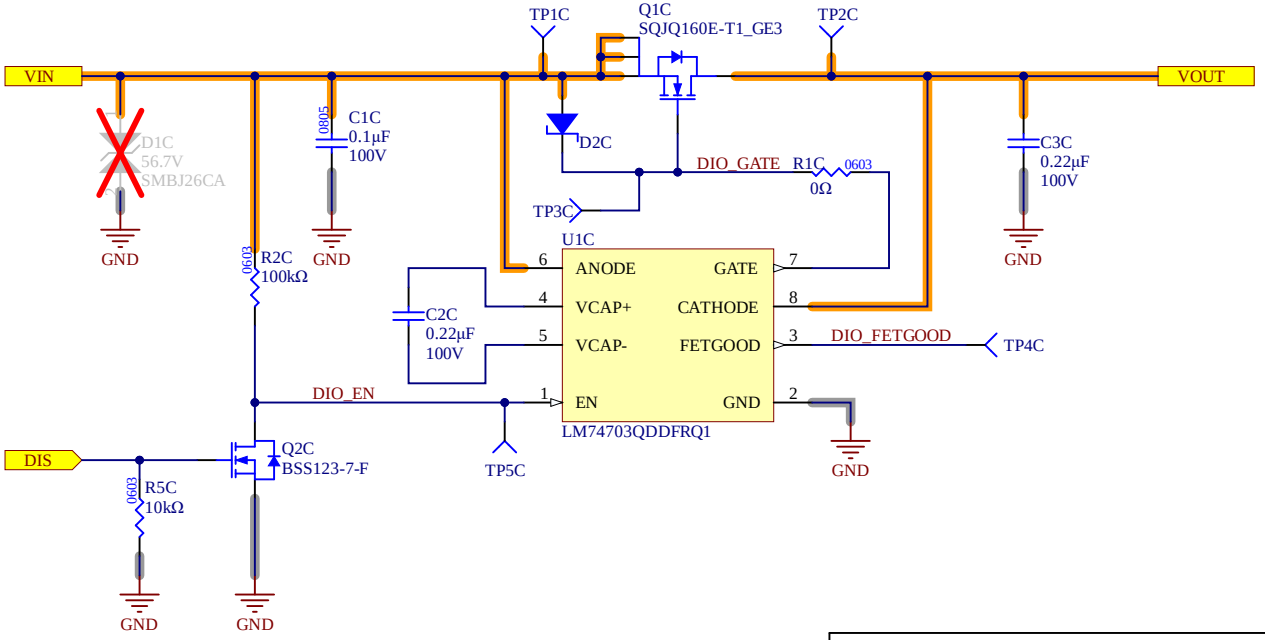
University of Waterloo 200 University Ave W Waterloo, Ontario, Canada N2L 3G1		REV 1.0
PROJECT BC-MPR.PrjPcb, BUILD		
DOCUMENT Ideal Diode.SchDoc		MODIFIED 2024-12-29
ENGINEER Farris Matar	REVIEWER *	SHEET 3 OF 14

IDEAL DIODE



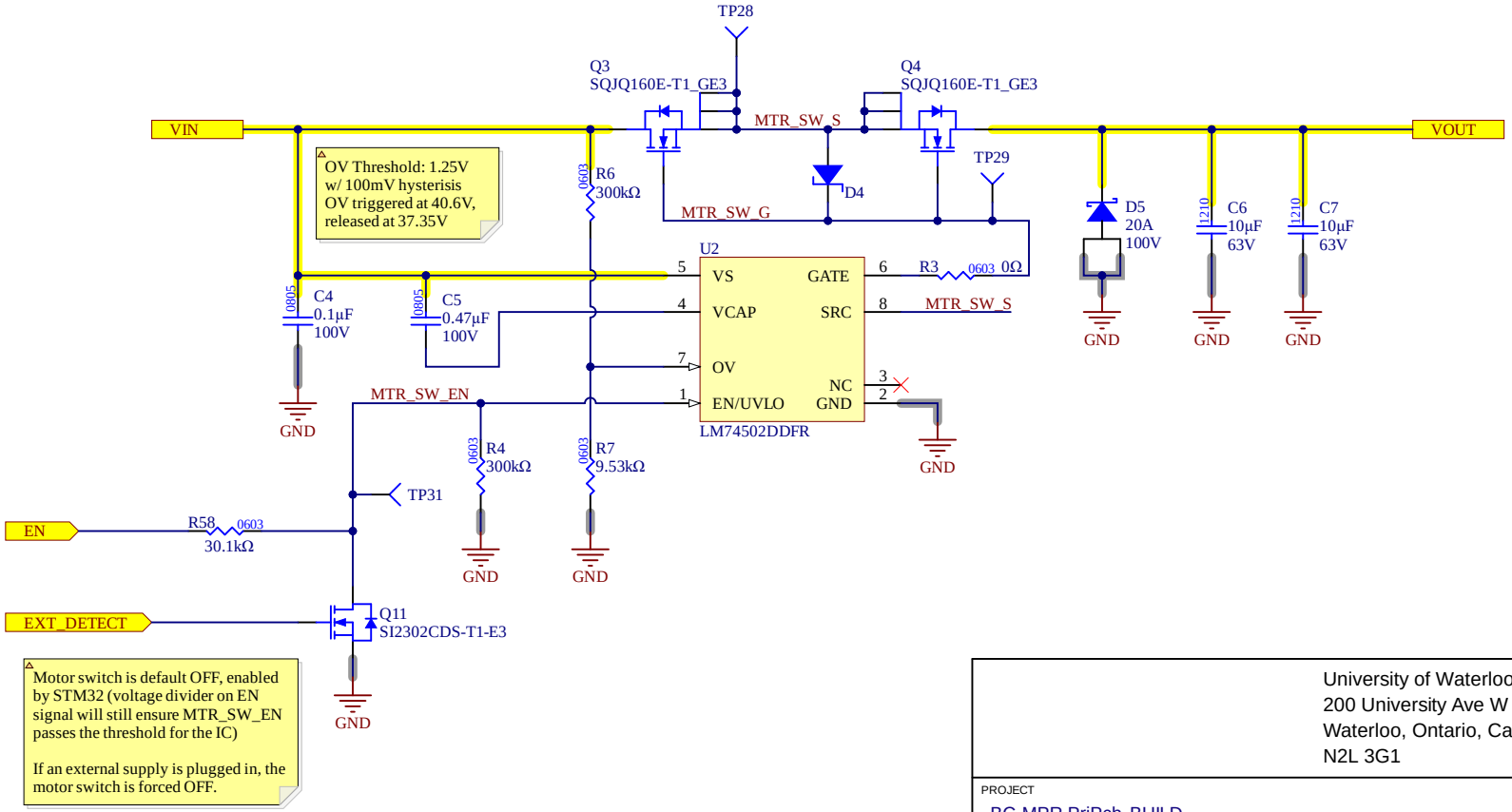
University of Waterloo 200 University Ave W Waterloo, Ontario, Canada N2L 3G1		REV 1.0
PROJECT BC-MPR.PrjPcb, BUILD		
DOCUMENT Ideal Diode.SchDoc		MODIFIED 2024-12-29
ENGINEER Farris Matar	REVIEWER *	SHEET 3 OF 14

IDEAL DIODE



University of Waterloo 200 University Ave W Waterloo, Ontario, Canada N2L 3G1		REV 1.0
PROJECT BC-MPR.PrjPcb, BUILD		
DOCUMENT Ideal Diode.SchDoc		MODIFIED 2024-12-29
ENGINEER Farris Matar	REVIEWER *	SHEET 3 OF 14

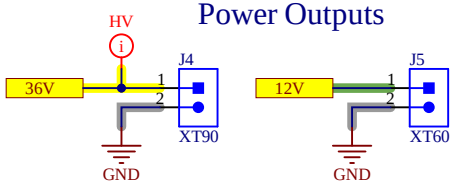
MOTOR POWER SWITCH



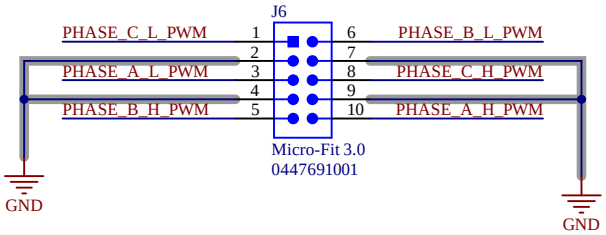
University of Waterloo 200 University Ave W Waterloo, Ontario, Canada N2L 3G1	REV 1.0
PROJECT BC-MPR.PrjPcb, BUILD	
DOCUMENT Motor Power Switch.SchDoc	MODIFIED 2024-12-28
ENGINEER Farris Matar / REVIEWER *	SHEET 4 OF 14

MOTOR CONTROLLER INTERFACE

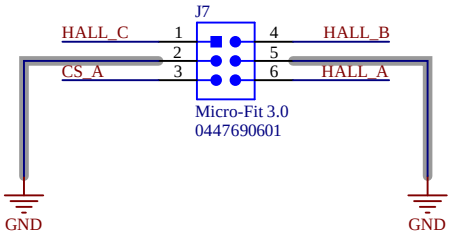
Power Outputs

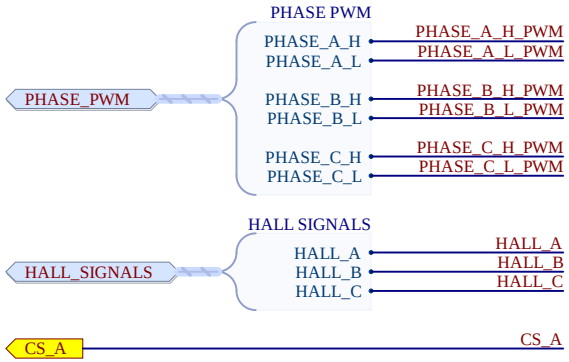


PWM Outputs



Analog Inputs

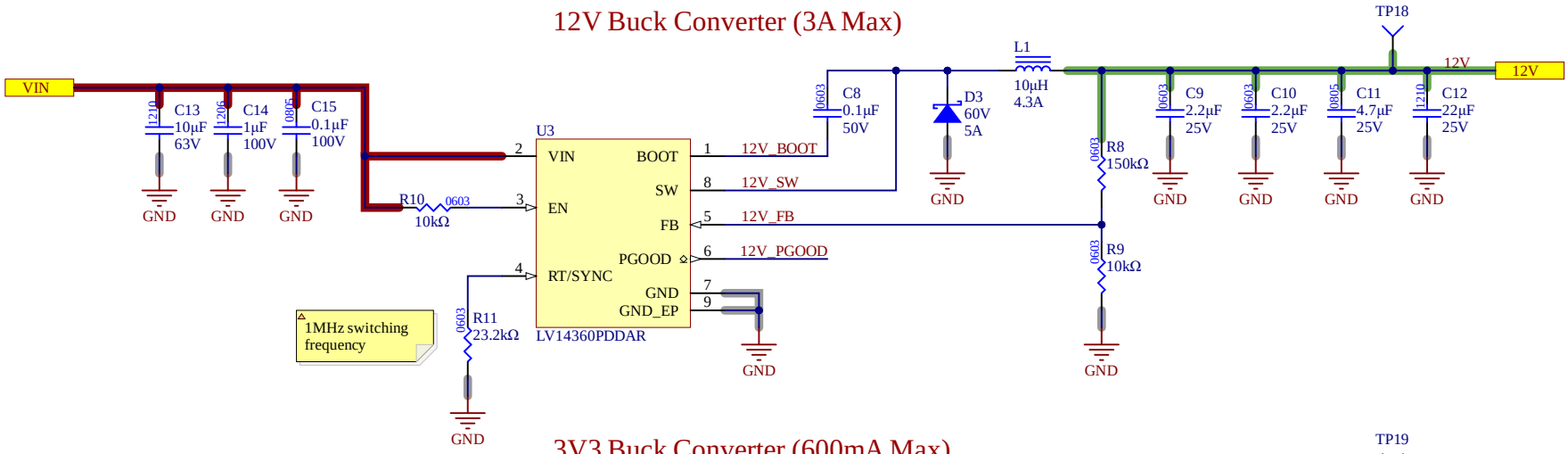




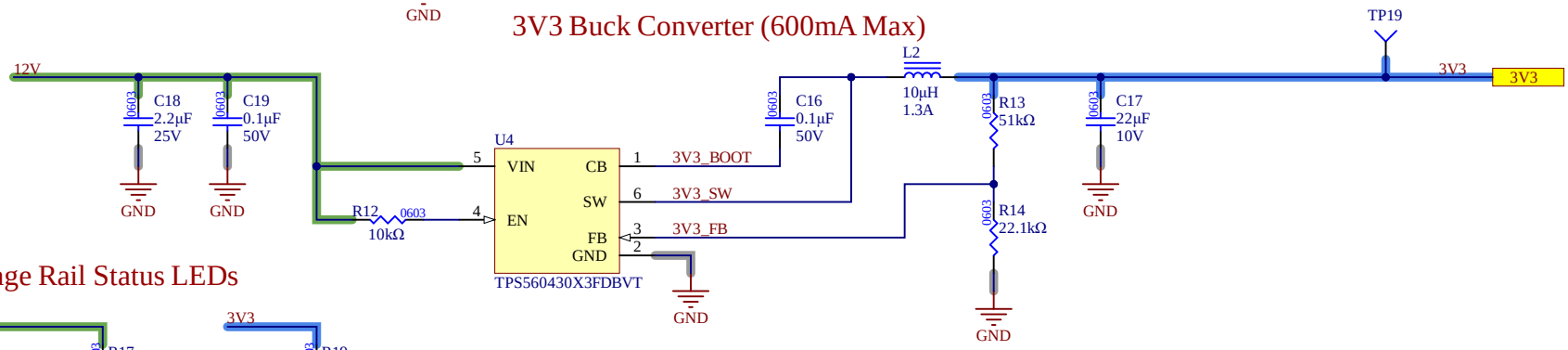
	University of Waterloo 200 University Ave W Waterloo, Ontario, Canada N2L 3G1	REV 1.0
PROJECT BC-MPR.PrjPcb, BUILD		
DOCUMENT Motor Controller Interface.SchDoc		MODIFIED 2024-12-27
ENGINEER Farris Matar	REVIEWER *	SHEET 5 OF 14

LOW VOLTAGE POWER

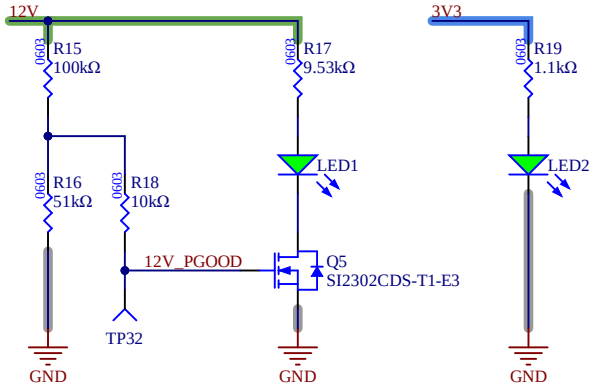
12V Buck Converter (3A Max)



3V3 Buck Converter (600mA Max)

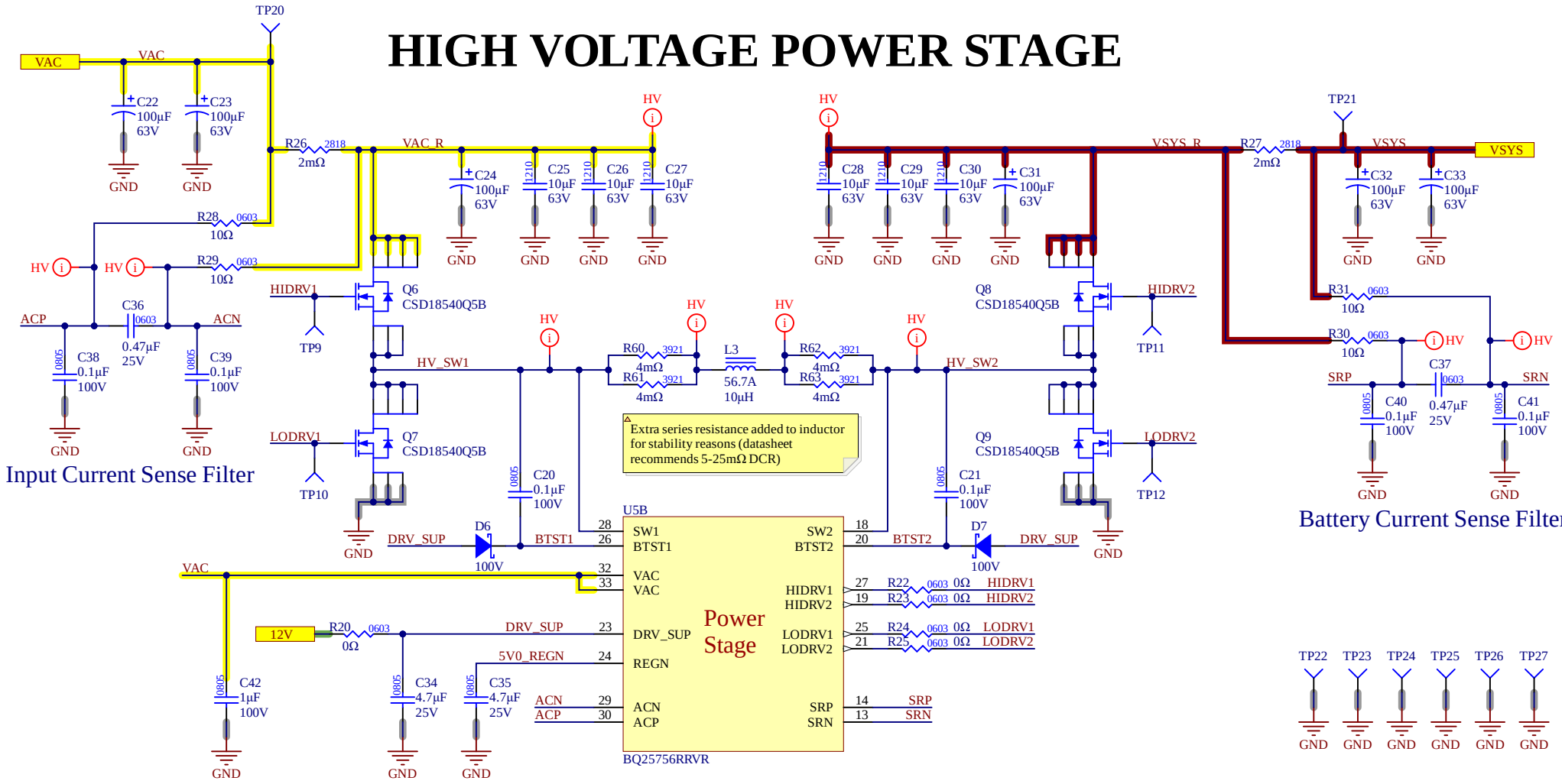


Voltage Rail Status LEDs

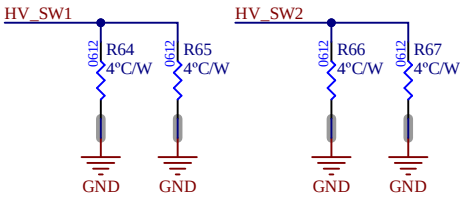


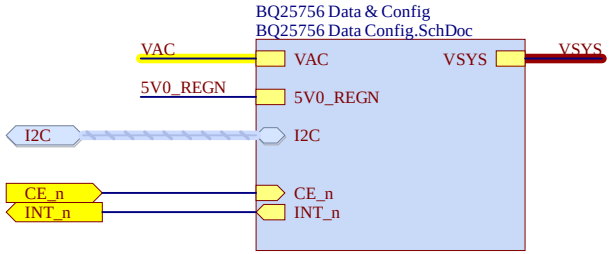
University of Waterloo 200 University Ave W Waterloo, Ontario, Canada N2L 3G1	REV 1.0
PROJECT: BC-MPR.PrjPcb, BUILD	
DOCUMENT: LV Power.SchDoc	MODIFIED: 2024-12-31
ENGINEER: Farris Matar / REVIEWER: *	SHEET 6 OF 14

HIGH VOLTAGE POWER STAGE



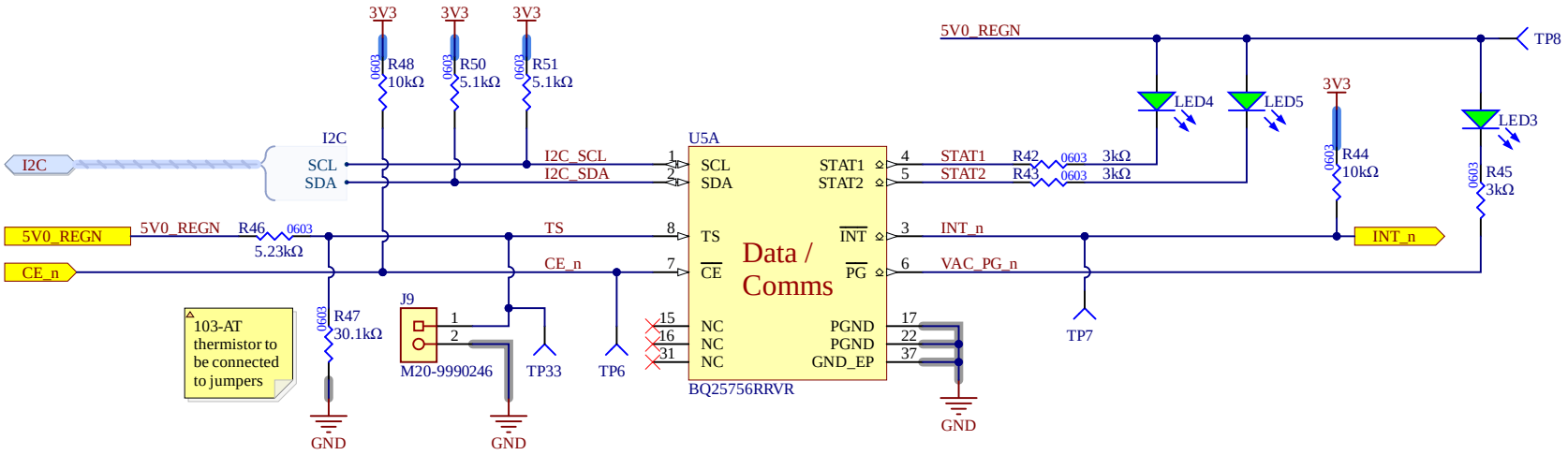
SW Node Thermal Jumpers

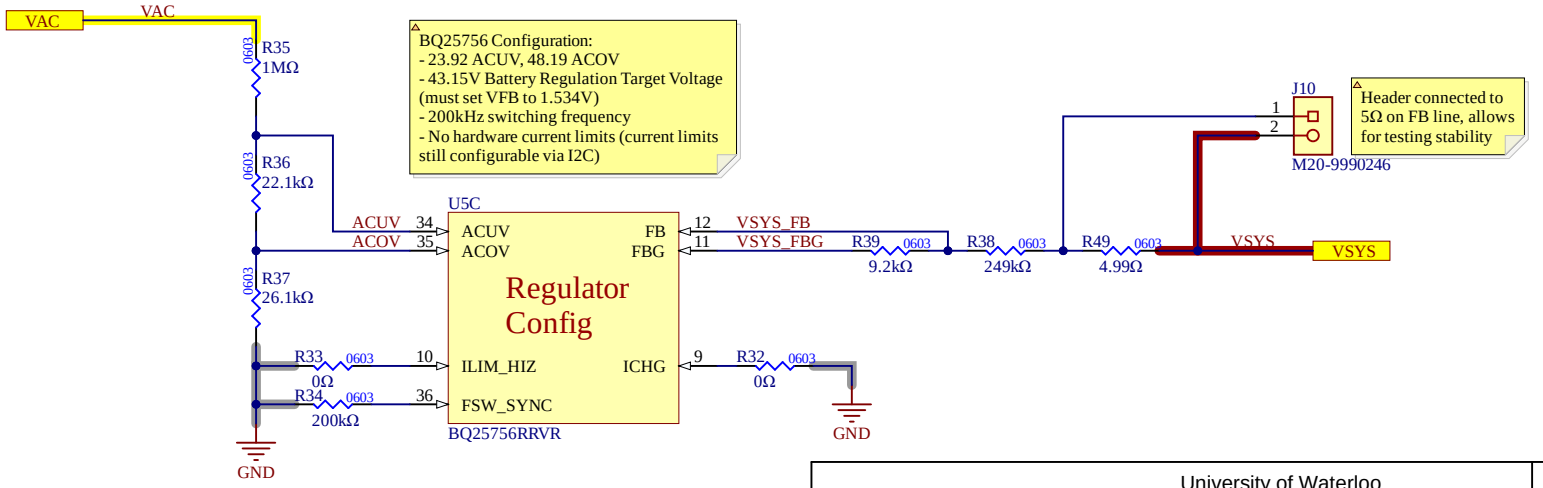




University of Waterloo 200 University Ave W Waterloo, Ontario, Canada N2L 3G1	REV 1.0
PROJECT: BC-MPR.PrjPcb, BUILD	
DOCUMENT: HV Power Stage.SchDoc	MODIFIED: 2025-01-02
ENGINEER: Farris Matar / REVIEWER: *	SHEET 7 OF 14

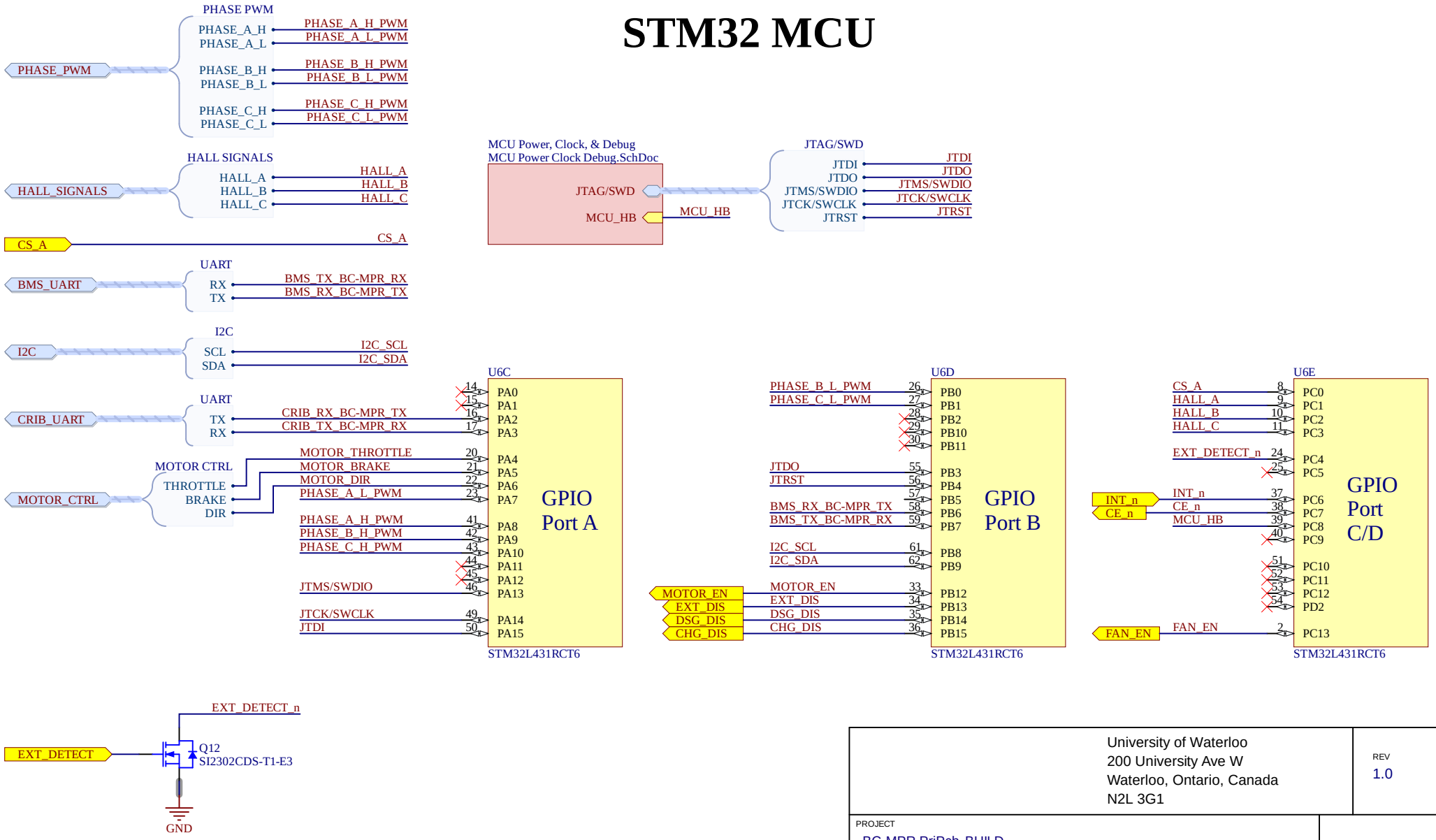
BQ25756 DATA & CONFIG





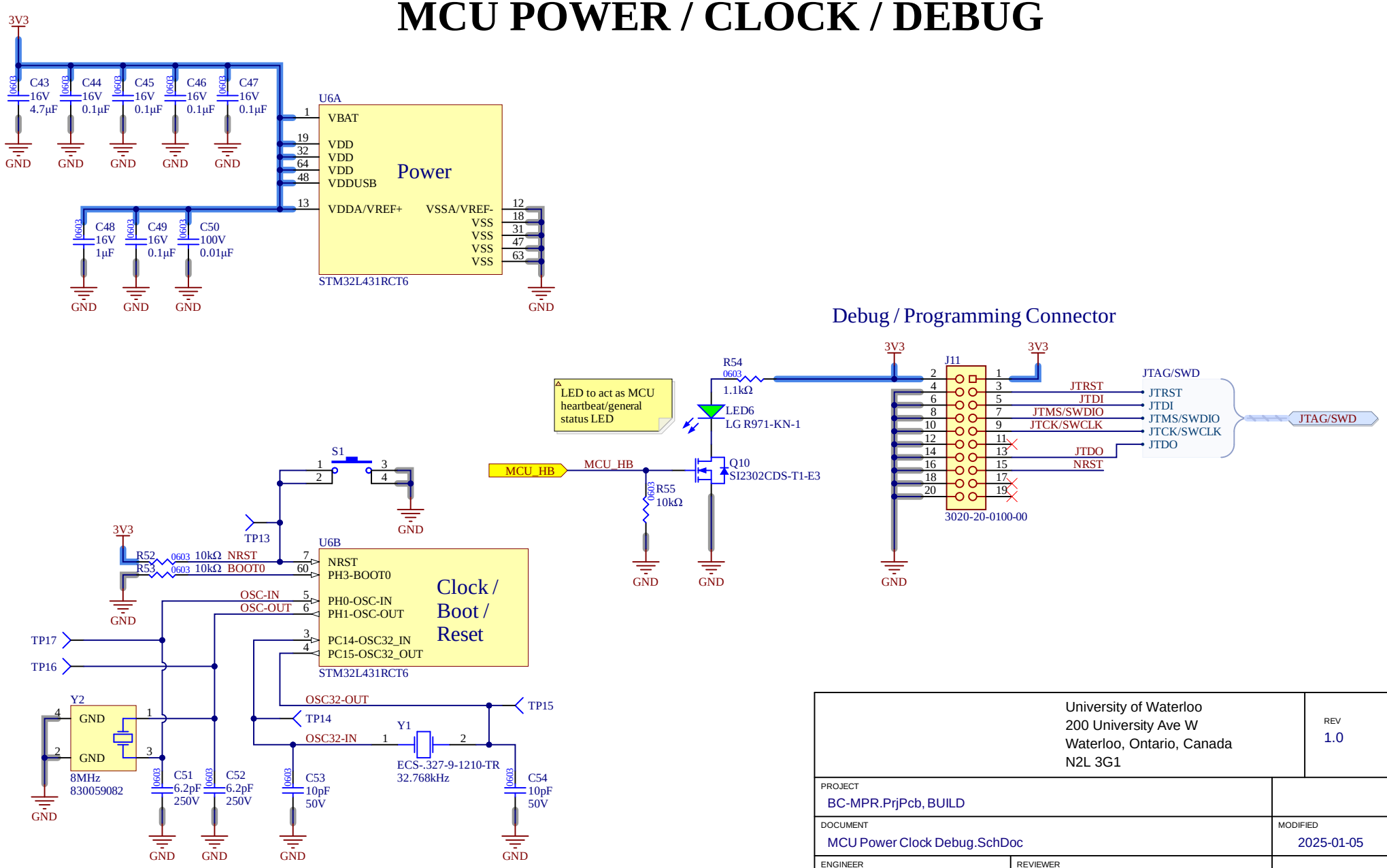
University of Waterloo 200 University Ave W Waterloo, Ontario, Canada N2L 3G1		REV 1.0
PROJECT BC-MPR.PrjPcb, BUILD		
DOCUMENT BQ25756 Data Config.SchDoc		MODIFIED 2024-12-27
ENGINEER Farris Matar	REVIEWER *	SHEET 8 OF 14

STM32 MCU



University of Waterloo 200 University Ave W Waterloo, Ontario, Canada N2L 3G1		REV 1.0
PROJECT BC-MPR.PrjPcb, BUILD		
DOCUMENT STM32 MCU.SchDoc		MODIFIED 2025-01-05
ENGINEER Farris Matar	REVIEWER *	SHEET 9 OF 14

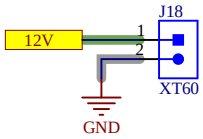
MCU POWER / CLOCK / DEBUG



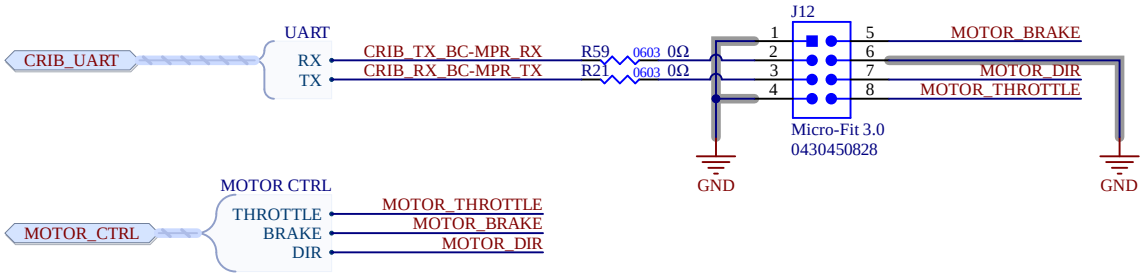
University of Waterloo 200 University Ave W Waterloo, Ontario, Canada N2L 3G1		REV 1.0
PROJECT: BC-MPR.PrjPcb, BUILD		
DOCUMENT: MCU Power Clock Debug.SchDoc		MODIFIED: 2025-01-05
ENGINEER: Farris Matar	REVIEWER: *	SHEET 10 OF 14

CONTROL INTERFACE BOARD

Power Output



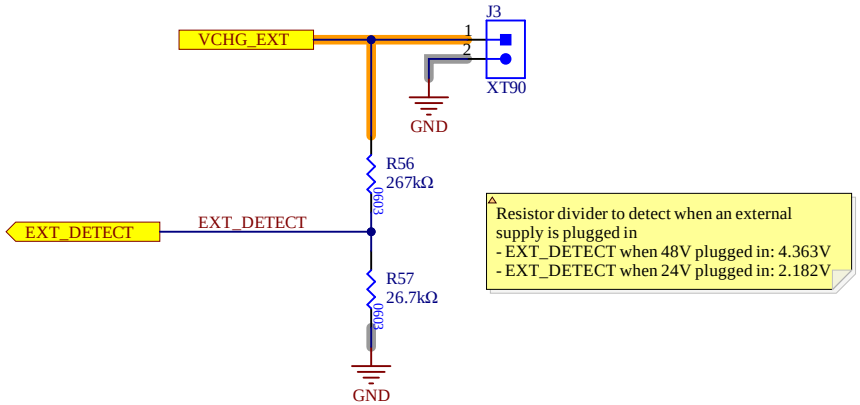
Control Signals



University of Waterloo 200 University Ave W Waterloo, Ontario, Canada N2L 3G1		REV 1.0
PROJECT BC-MPR.PrjPcb, BUILD		
DOCUMENT Control Interface Board.SchDoc		MODIFIED 2025-01-02
ENGINEER Farris Matar	REVIEWER *	SHEET 11 OF 14

EXTERNAL SUPPLY INTERFACE

DC Supply Power Port



University of Waterloo
200 University Ave W
Waterloo, Ontario, Canada
N2L 3G1

REV 1.0

PROJECT: BC-MPR.PrjPcb, BUILD

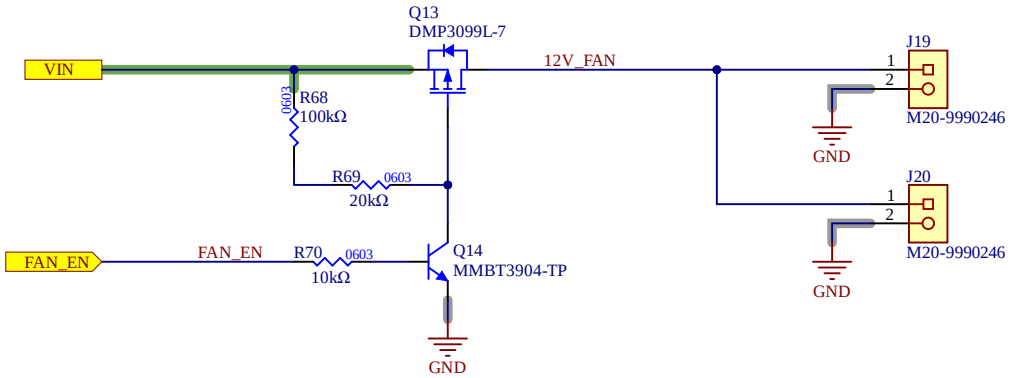
DOCUMENT: External Supply Interface.SchDoc

MODIFIED: 2025-01-01

ENGINEER: Farris Matar

REVIEWER: *

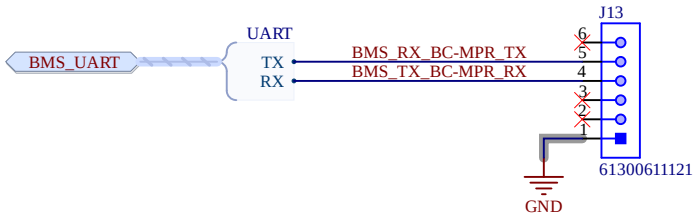
FAN POWER SWITCH

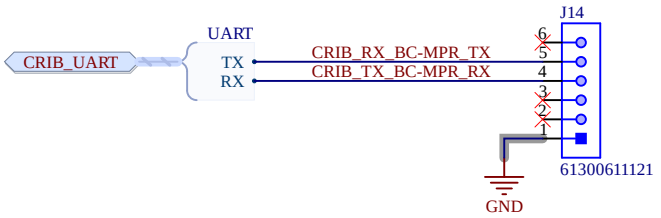


University of Waterloo 200 University Ave W Waterloo, Ontario, Canada N2L 3G1		REV 1.0
PROJECT BC-MPR.PrjPcb, BUILD		
DOCUMENT Fan Power Switch.SchDoc		MODIFIED 2025-01-01
ENGINEER Farris Matar	REVIEWER *	SHEET 13 OF 14

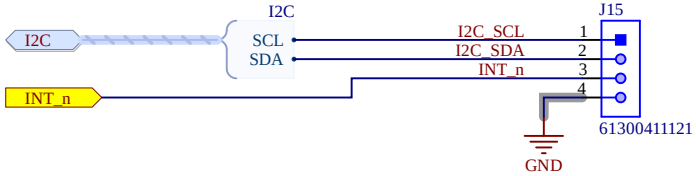
DEBUG INTERFACE

FTDI USB to UART Debug

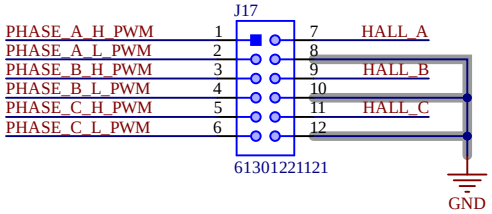




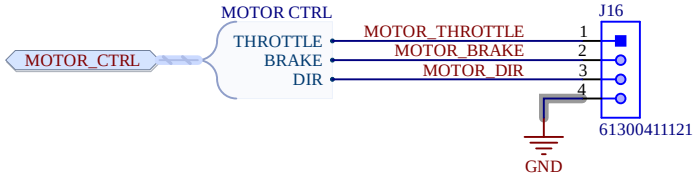
I2C Breakout

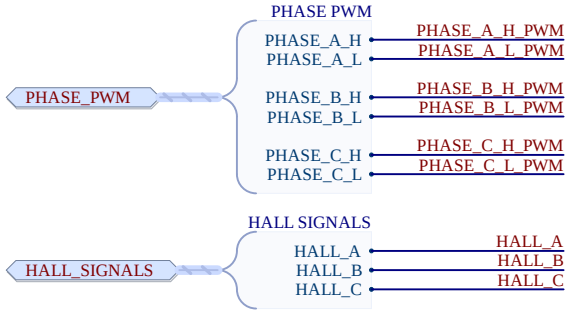


Motor Controller Breakout



Control Interface Breakout





University of Waterloo 200 University Ave W Waterloo, Ontario, Canada N2L 3G1		REV 1.0
PROJECT BC-MPR.PrjPcb, BUILD		
DOCUMENT Debug Interface.SchDoc		MODIFIED 2024-12-27
ENGINEER Farris Matar	REVIEWER *	SHEET 14 OF 14