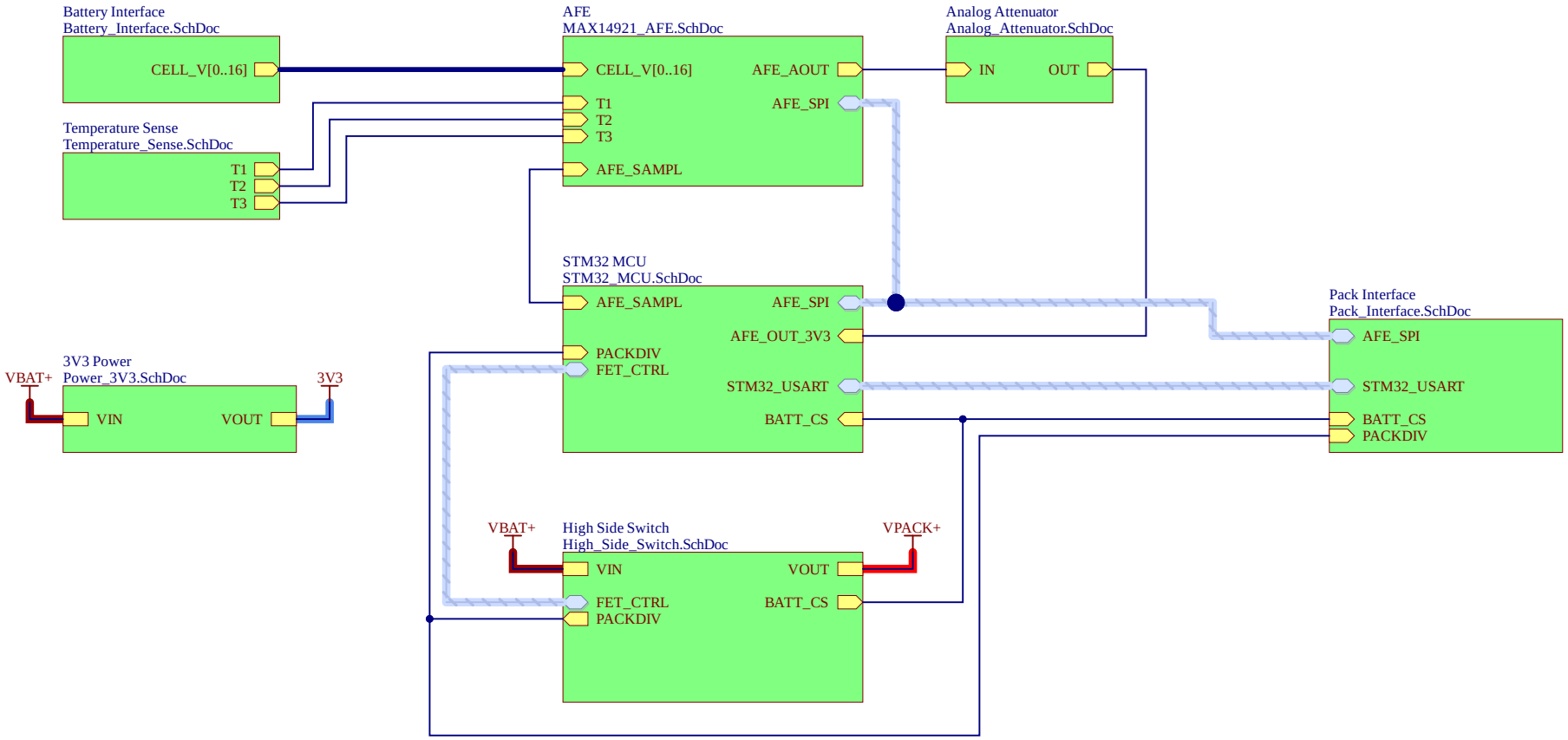

Mounting Holes

MH1 MH2

MH3 MH4

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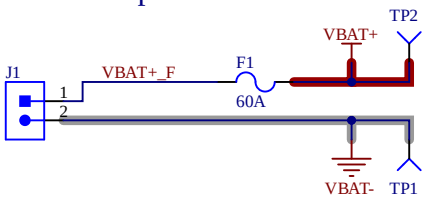
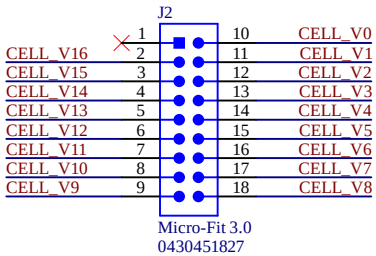
PROJECT LTO 16S BMS.PrjPcb, [No Variations]		
DOCUMENT Top.SchDoc		MODIFIED 2023-05-19
ENGINEER Farris Matar	REVIEWER *	SHEET 1 OF 11

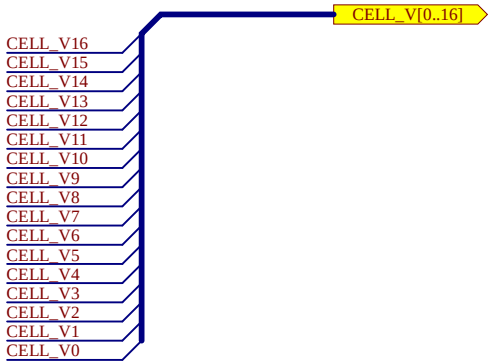
Battery specs:
- 16s1p 20Ah LTO battery
- 1.5V - 2.7V cell voltage range, 2.3V nominal

Power Input



Cell Sensing Inputs





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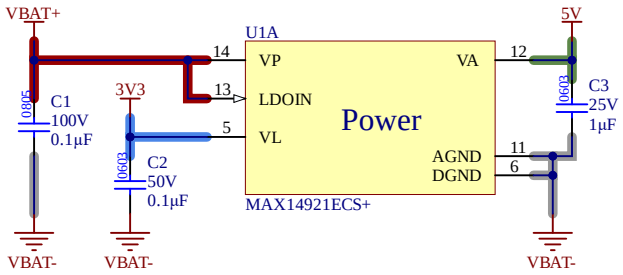
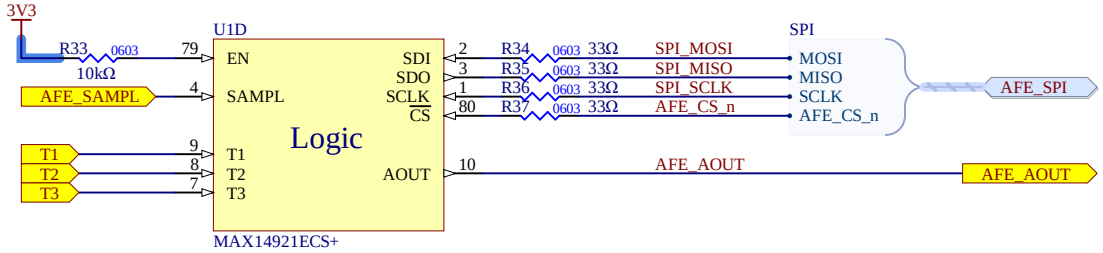
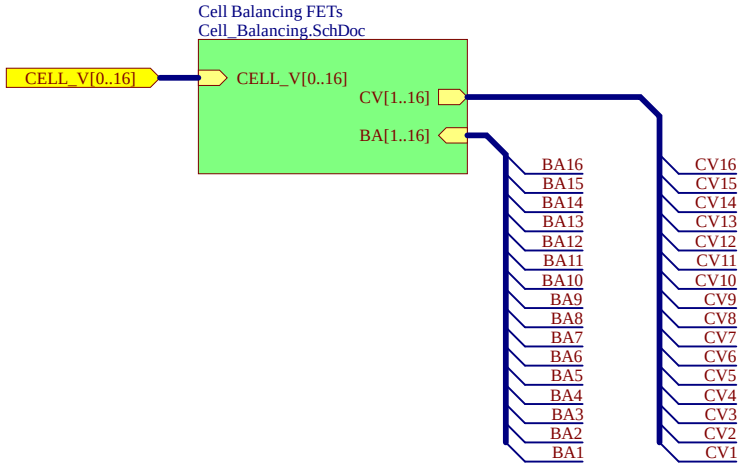
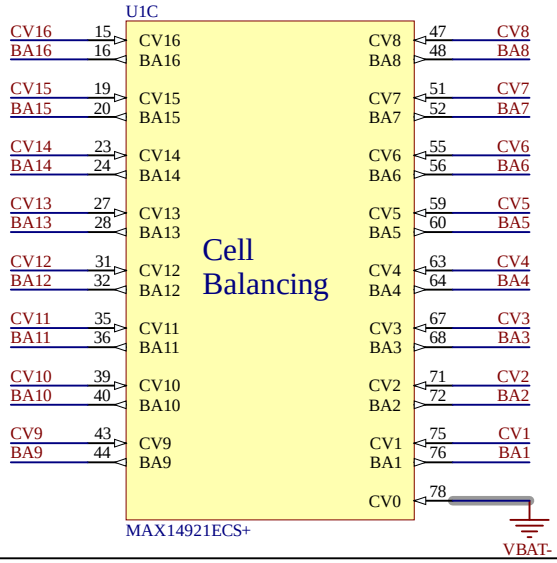
PROJECT LTO 16S BMS.PrjPcb, [No Variations]		
DOCUMENT Battery_Interface.SchDoc		MODIFIED 2023-05-07
ENGINEER Farris Matar	REVIEWER *	SHEET 2 OF 11









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PROJECT LTO 16S BMS.PrjPcb, [No Variations]	
DOCUMENT MAX14921_AFE.SchDoc	MODIFIED 2023-05-14
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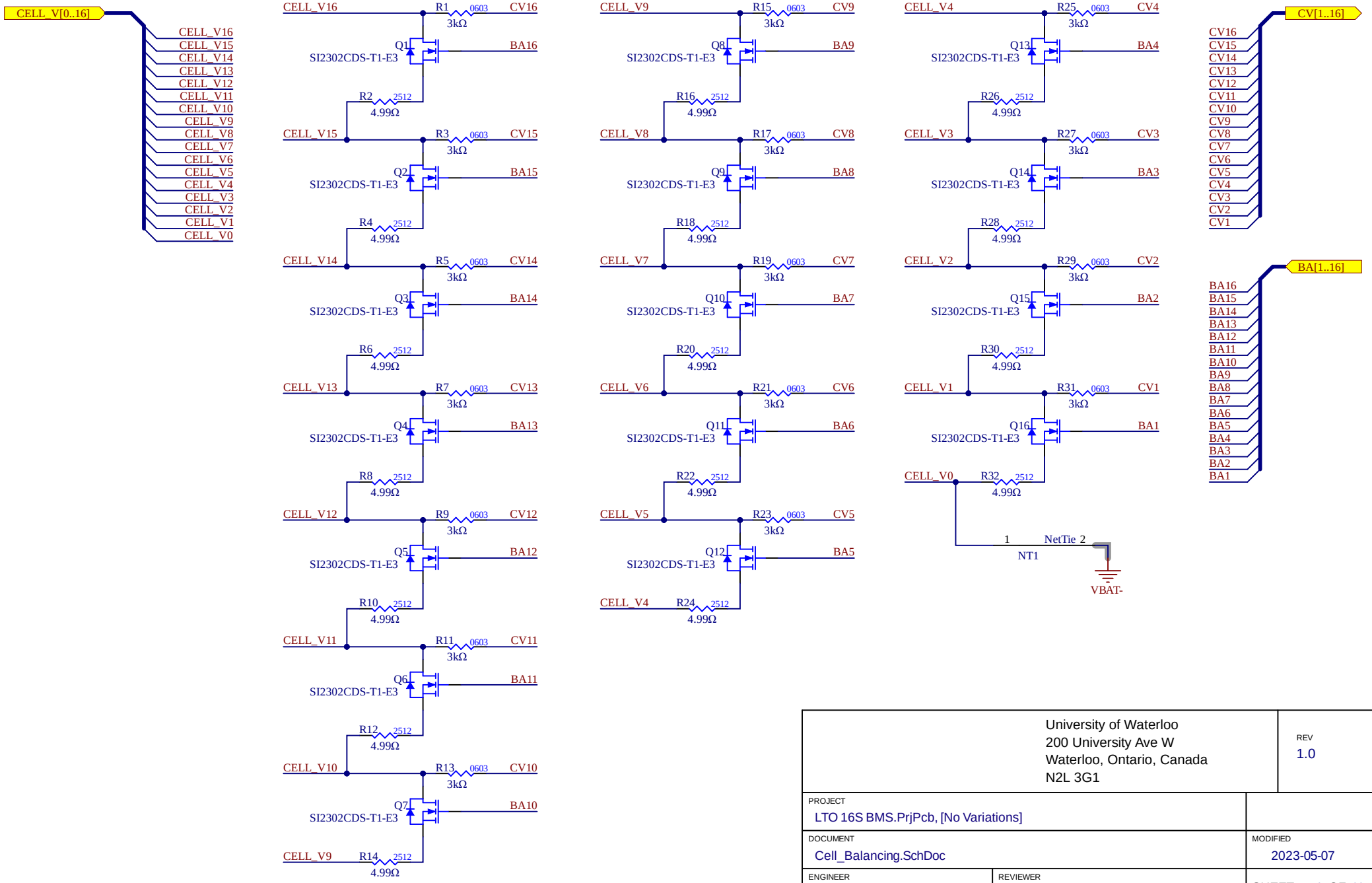
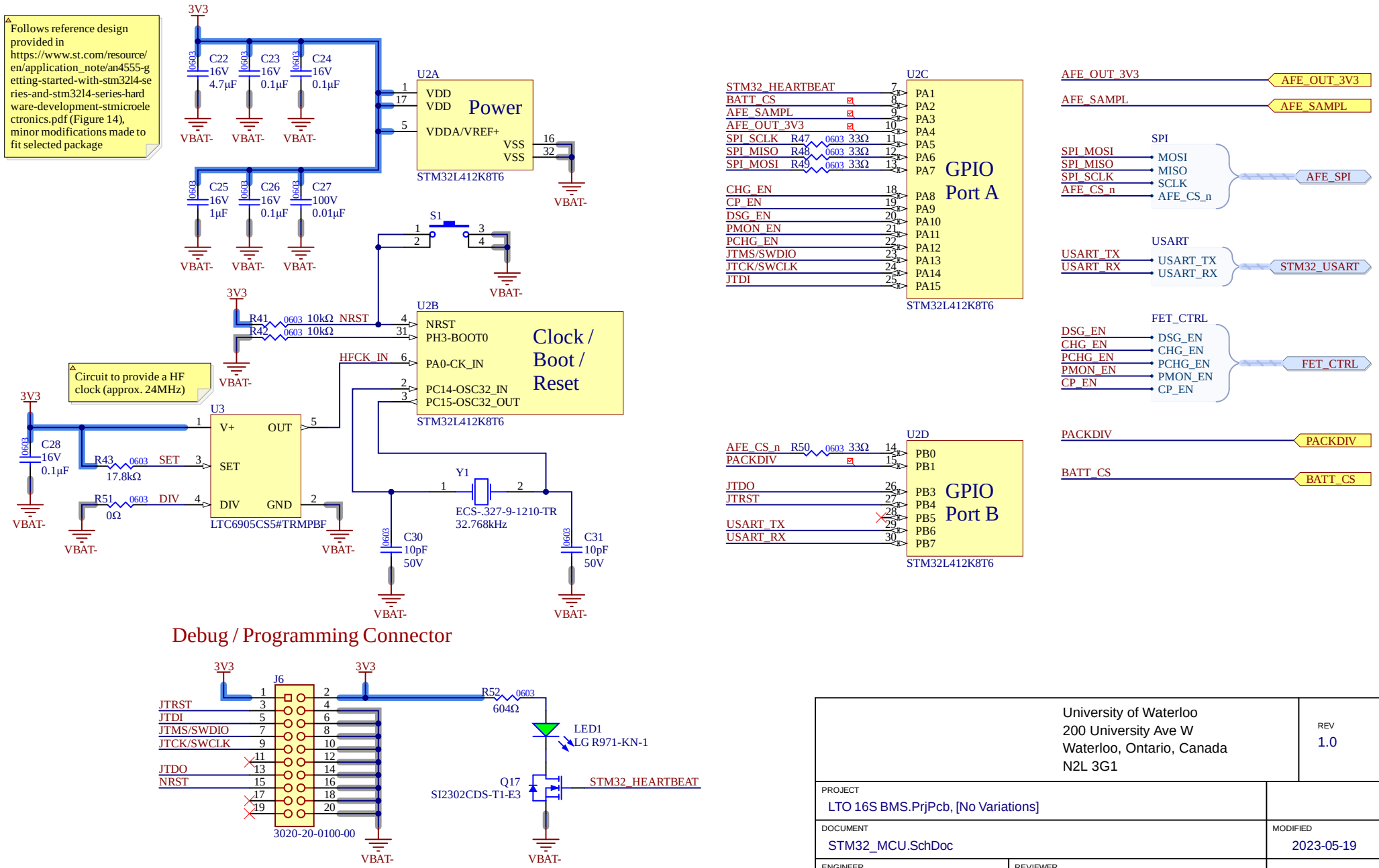
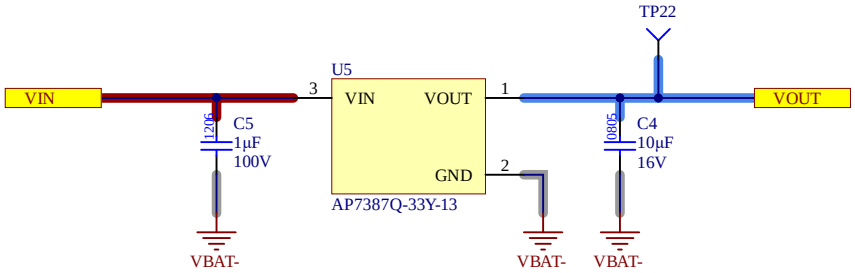


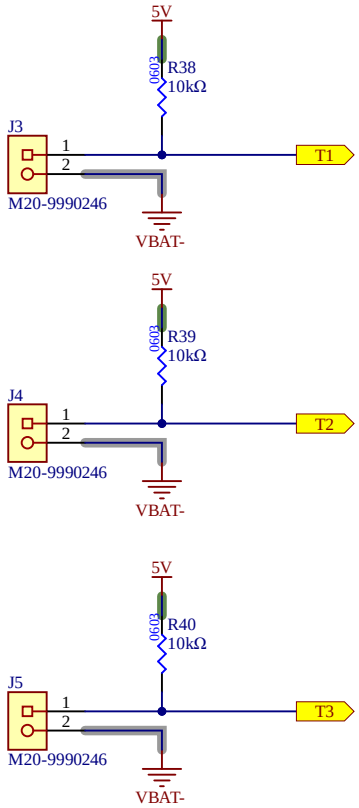
University of Waterloo 200 University Ave W Waterloo, Ontario, Canada N2L 3G1	REV 1.0
PROJECT: LTO 16S BMS.PrjPcb, [No Variations]	
DOCUMENT: Cell_Balancing.SchDoc	MODIFIED: 2023-05-07
ENGINEER: Farris Matar / REVIEWER: *	SHEET 4 OF 11



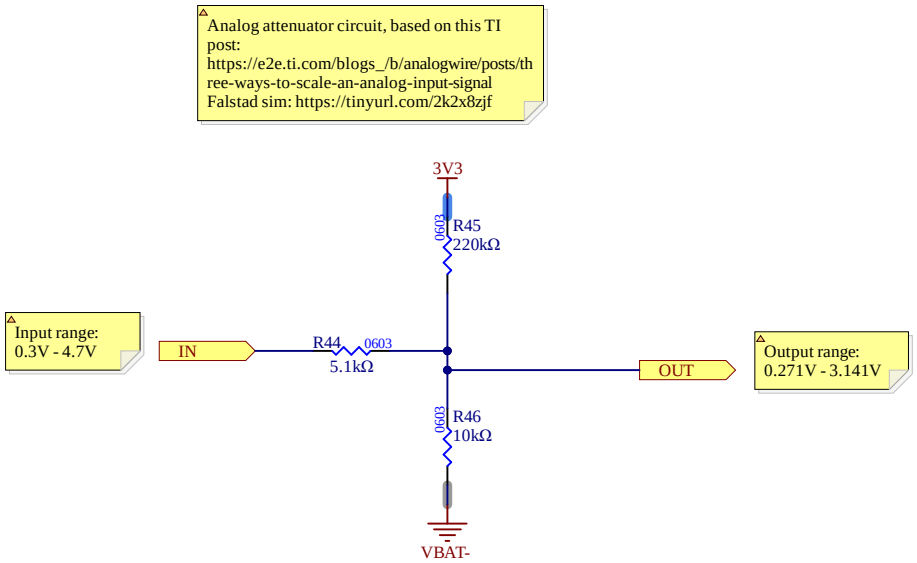
University of Waterloo 200 University Ave W Waterloo, Ontario, Canada N2L 3G1		REV 1.0
PROJECT: LTO 16S BMS.PrjPcb, [No Variations]		
DOCUMENT: STM32_MCU.SchDoc		MODIFIED: 2023-05-19
ENGINEER: Farris Matar	REVIEWER: *	SHEET 5 OF 11



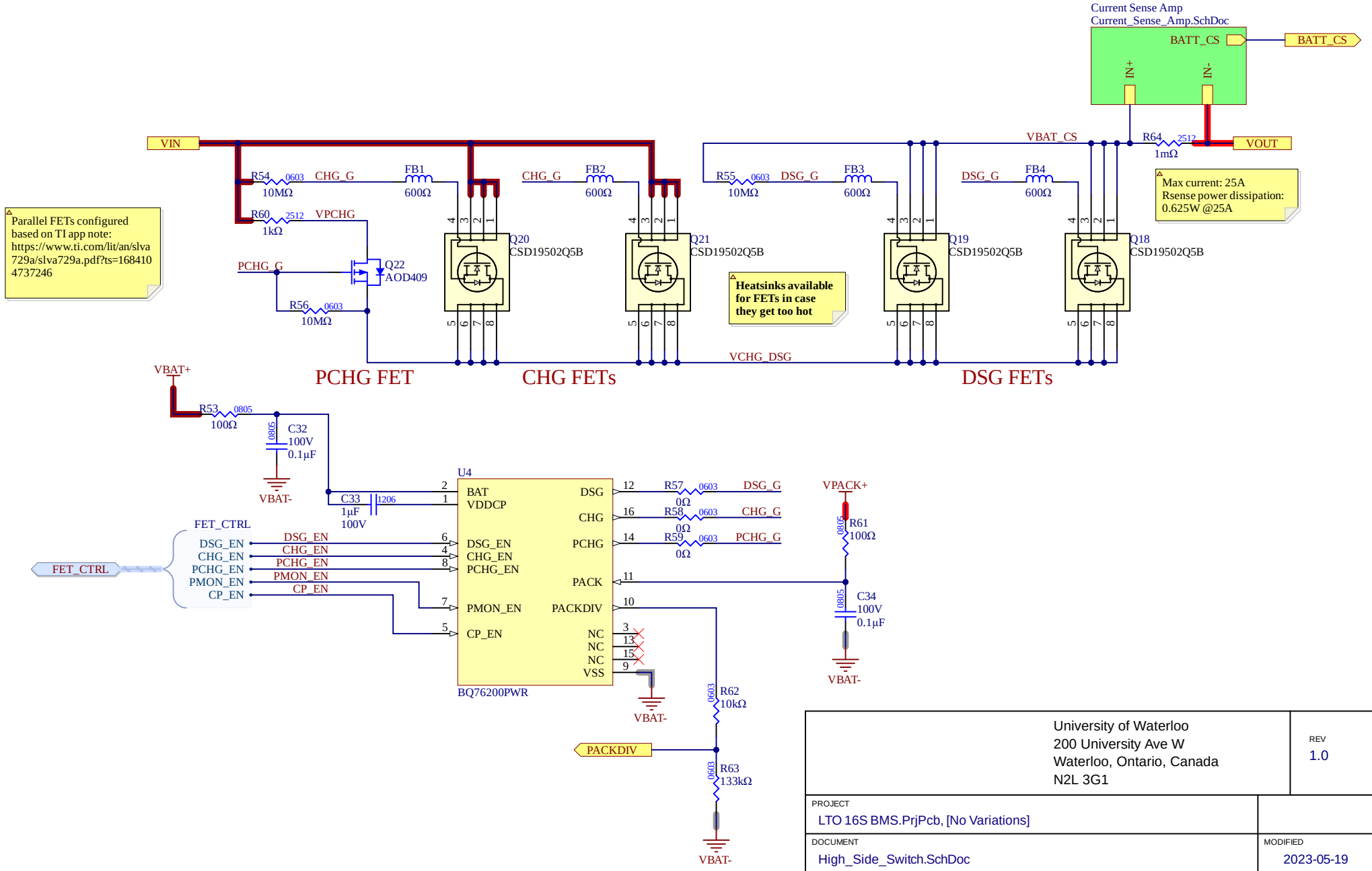
University of Waterloo 200 University Ave W Waterloo, Ontario, Canada N2L 3G1		REV 1.0
PROJECT LTO 16S BMS.PrjPcb, [No Variations]		
DOCUMENT Power_3V3.SchDoc		MODIFIED 2023-05-07
ENGINEER Farris Matar	REVIEWER *	SHEET 6 OF 11



University of Waterloo 200 University Ave W Waterloo, Ontario, Canada N2L 3G1		REV 1.0
PROJECT LTO 16S BMS.PrjPcb, [No Variations]		
DOCUMENT Temperature_Sense.SchDoc		MODIFIED 2023-05-07
ENGINEER Farris Matar	REVIEWER *	SHEET 7 OF 11

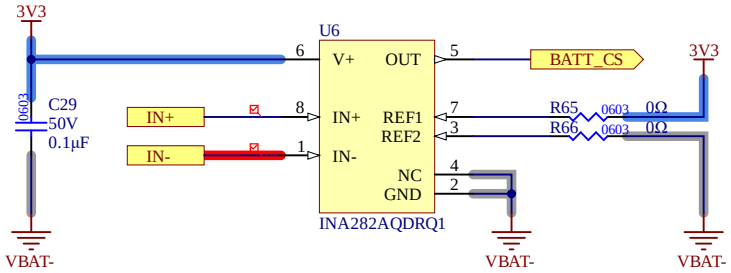


University of Waterloo 200 University Ave W Waterloo, Ontario, Canada N2L 3G1		REV 1.0
PROJECT LTO 16S BMS.PrjPcb, [No Variations]		
DOCUMENT Analog_Attenuator.SchDoc		MODIFIED 2023-05-07
ENGINEER Farris Matar	REVIEWER *	SHEET 8 OF 11



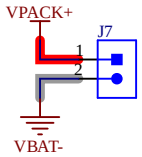
University of Waterloo 200 University Ave W Waterloo, Ontario, Canada N2L 3G1		REV 1.0
PROJECT: LTO 16S BMS.PrjPcb, [No Variations]		
DOCUMENT: High_Side_Switch.SchDoc		MODIFIED: 2023-05-19
ENGINEER: Farris Matar	REVIEWER: *	SHEET 9 OF 11

Amplifier gain: 50V/V
Output at 0A: 1.65V
Output at 25A (DSG): 2.9V
Output at 25A (CHG): 0.4V

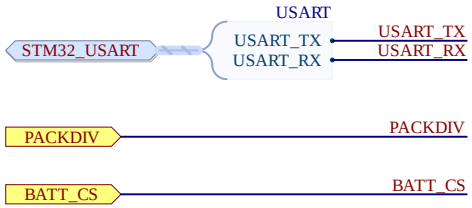


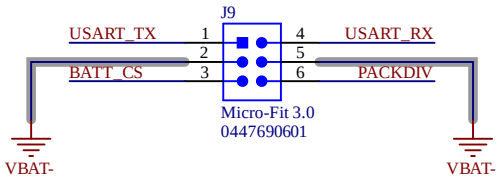
University of Waterloo 200 University Ave W Waterloo, Ontario, Canada N2L 3G1		REV 1.0
PROJECT LTO 16S BMS.PrjPcb, [No Variations]		
DOCUMENT Current_Sense_Amp.SchDoc		MODIFIED 2023-05-19
ENGINEER Farris Matar	REVIEWER *	SHEET 10 OF 11

Power Output



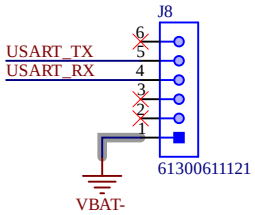
Data Output





SPI Debug

FTDI USB to UART Debug



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PROJECT LTO 16S BMS.PrjPcb, [No Variations]		
DOCUMENT Pack_Interface.SchDoc		MODIFIED 2023-05-19
ENGINEER Farris Matar	REVIEWER *	SHEET 11 OF 11