

1

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A

A

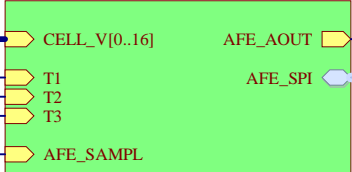
Battery Interface
Battery_Interface.SchDoc



Temperature Sense
Temperature_Sense.SchDoc



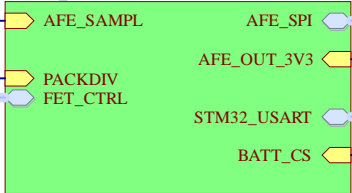
AFE
MAX14921_AFE.SchDoc



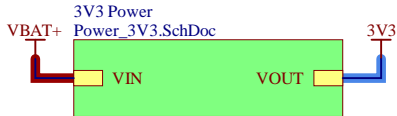
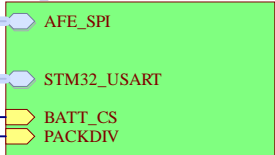
Analog Attenuator
Analog_Attenuator.SchDoc



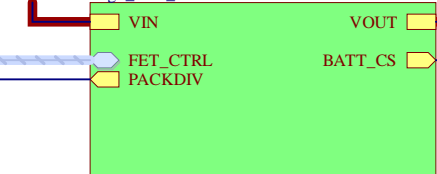
STM32 MCU
STM32_MCU.SchDoc



Pack Interface
Pack_Interface.SchDoc



High Side Switch
High_Side_Switch.SchDoc



Mounting Holes

- MH1
- MH2
- MH3
- MH4

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PROJECT LTO 16S BMS.PrjPcb, [No Variations]		
DOCUMENT Top.SchDoc		MODIFIED 2023-05-19
ENGINEER Farris Matar	REVIEWER *	SHEET 1 OF 11

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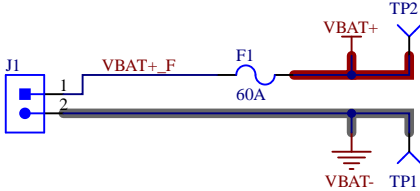
D

D

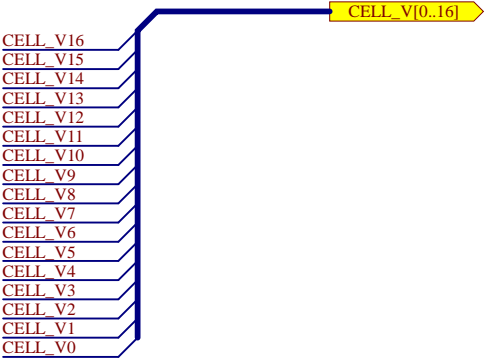
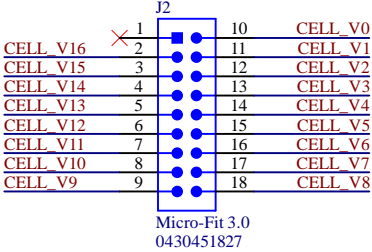
BATTERY INTERFACE

Battery specs:
- 16s1p 20Ah LTO battery
- 1.5V - 2.7V cell voltage range, 2.3V nominal

Power Input

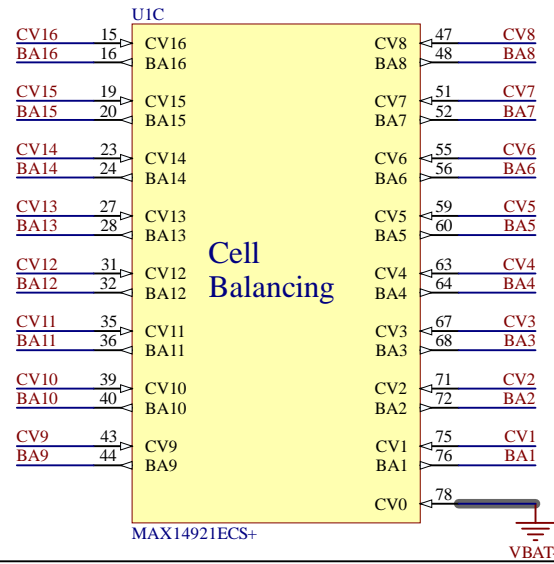
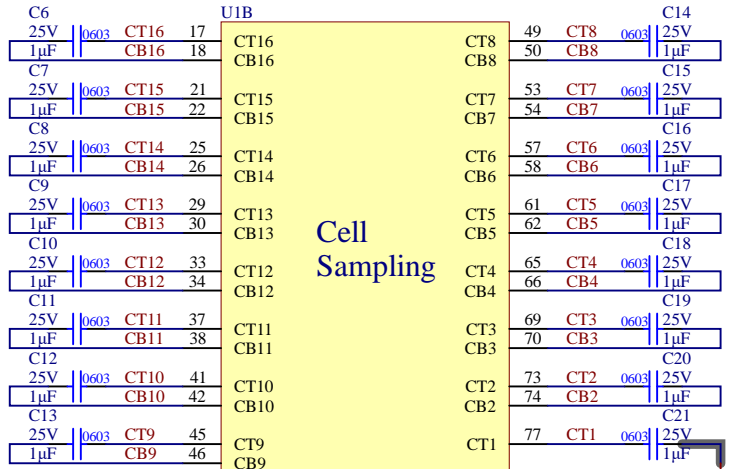
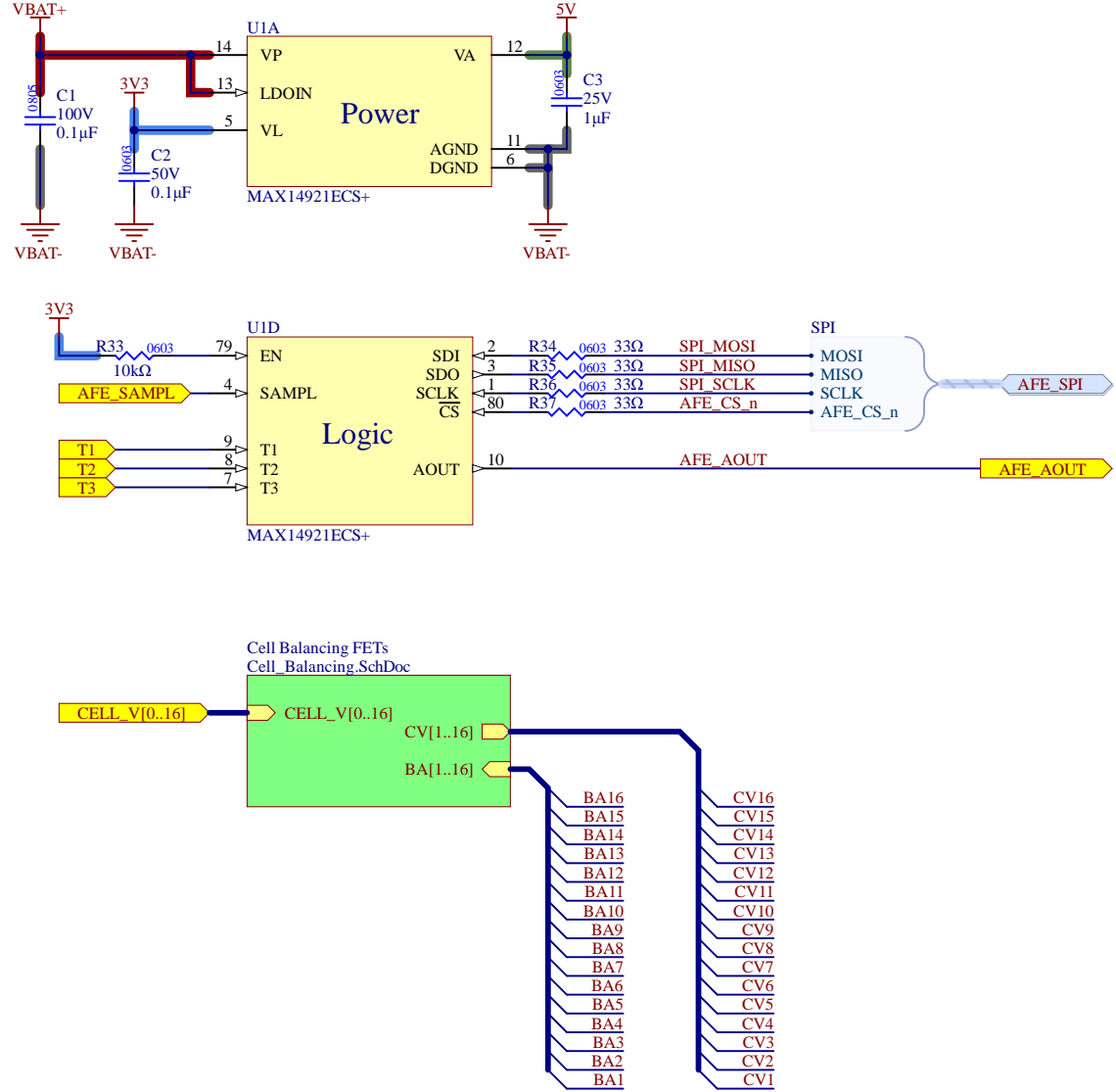


Cell Sensing Inputs



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PROJECT LTO 16S BMS.PrjPcb, [No Variations]		
DOCUMENT Battery_Interface.SchDoc		MODIFIED 2023-06-15
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MAX19421 AFE



University of Waterloo 200 University Ave W Waterloo, Ontario, Canada N2L 3G1		REV 1.0
PROJECT LTO 16S BMS.PrjPcb, [No Variations]		
DOCUMENT MAX19421_AFE.SchDoc	MODIFIED 2023-06-15	
ENGINEER Farris Matar	REVIEWER *	SHEET 3 OF 11

A

B

C

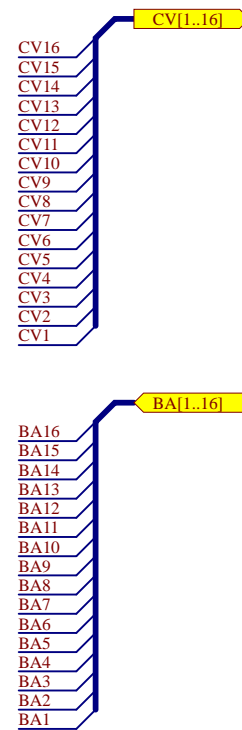
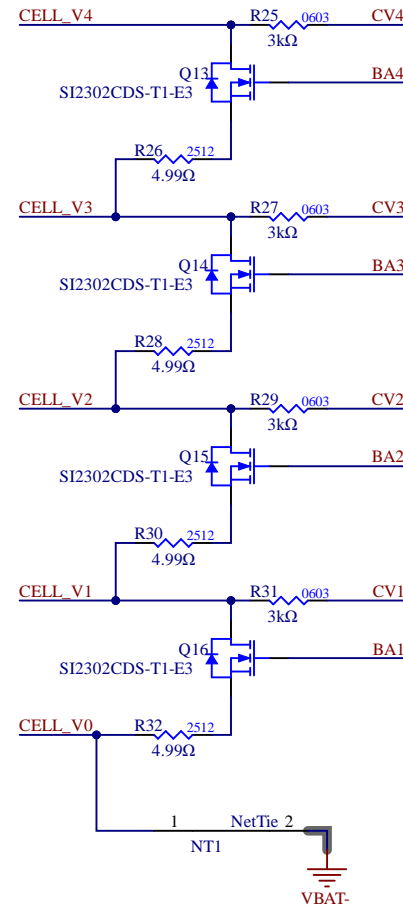
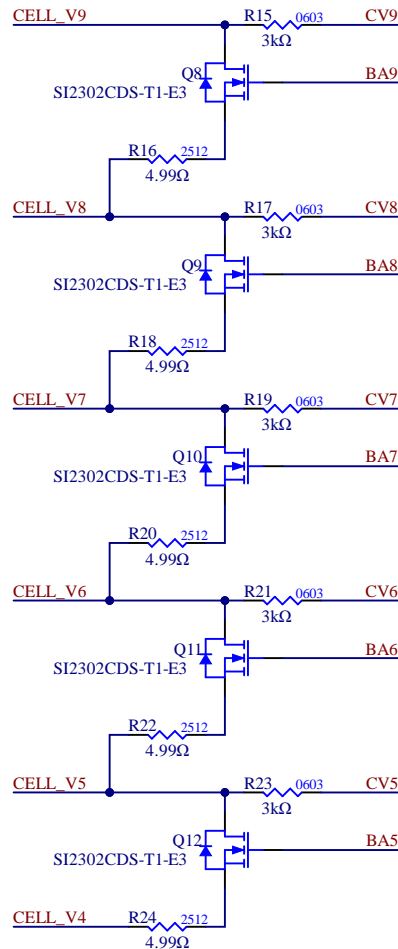
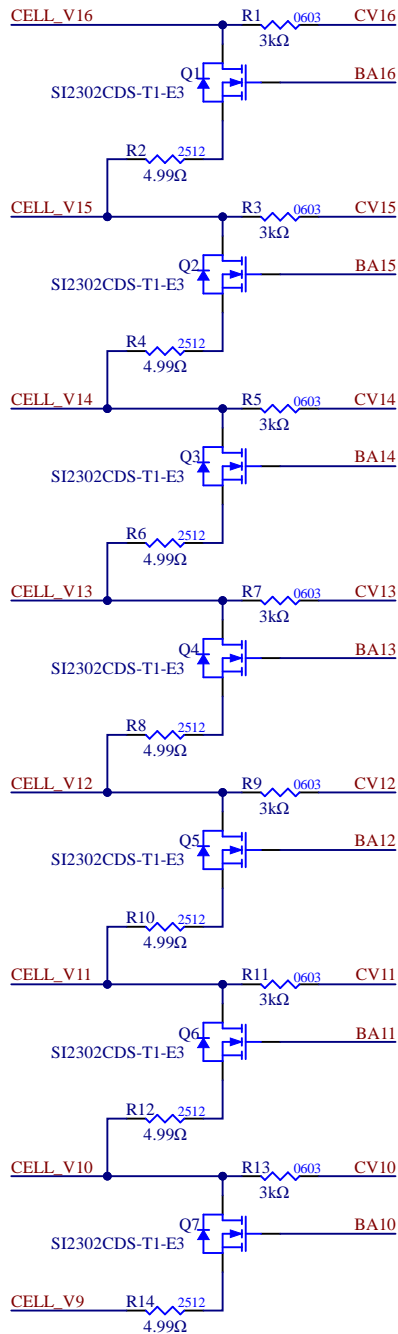
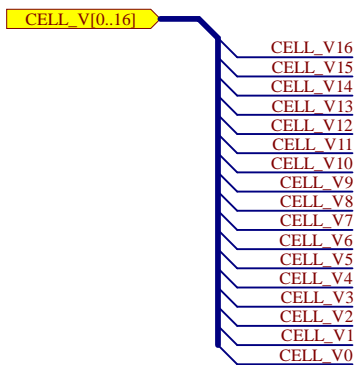
D

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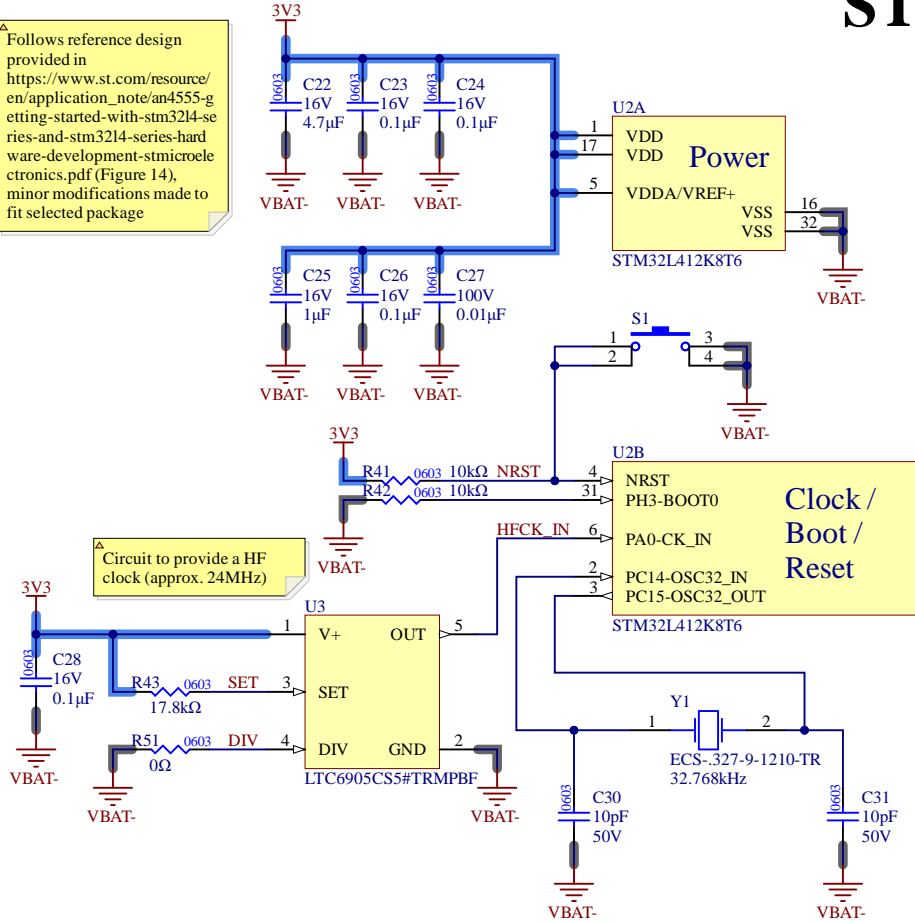


CELL BALANCING

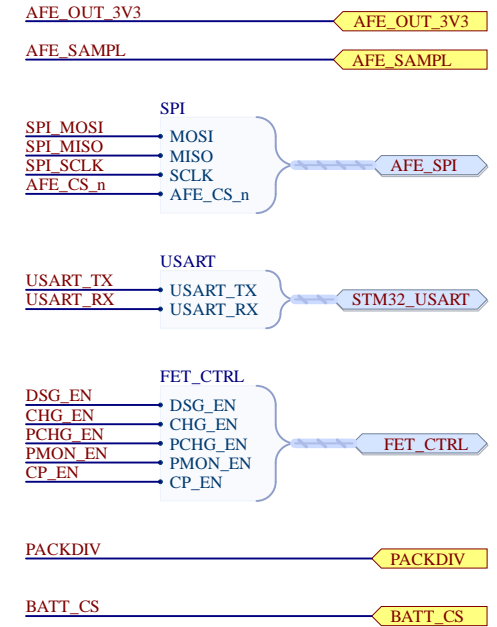
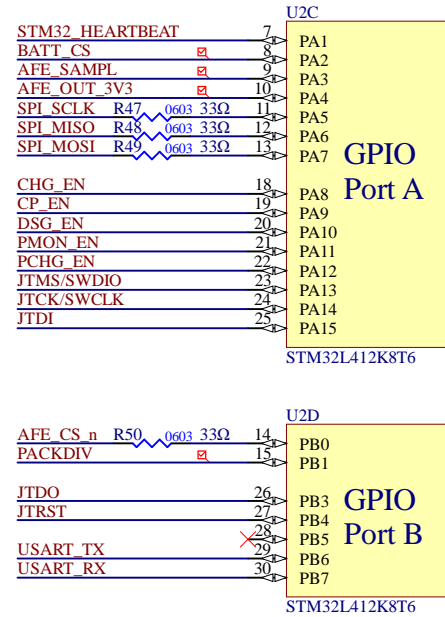
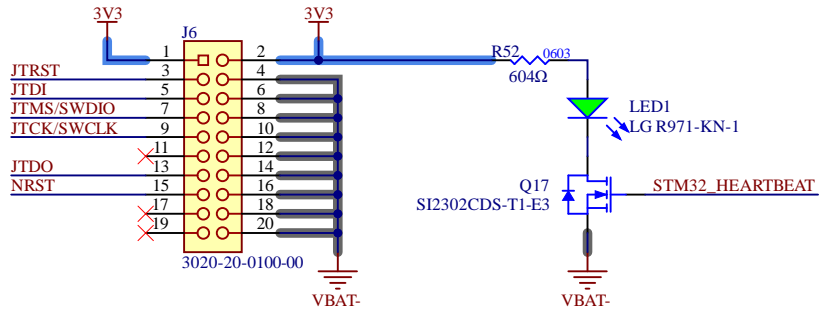
University of Waterloo 200 University Ave W Waterloo, Ontario, Canada N2L 3G1		REV 1.0
PROJECT LTO 16S BMS.PrjPcb, [No Variations]		
DOCUMENT Cell_Balancing.SchDoc		MODIFIED 2023-06-15
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STM32 MCU

Follows reference design provided in
https://www.st.com/resource/en/application_note/an4555-getting-started-with-stm32l4-series-and-stm32l4-series-hard-ware-development-stmicroelectronics.pdf (Figure 14),
 minor modifications made to fit selected package

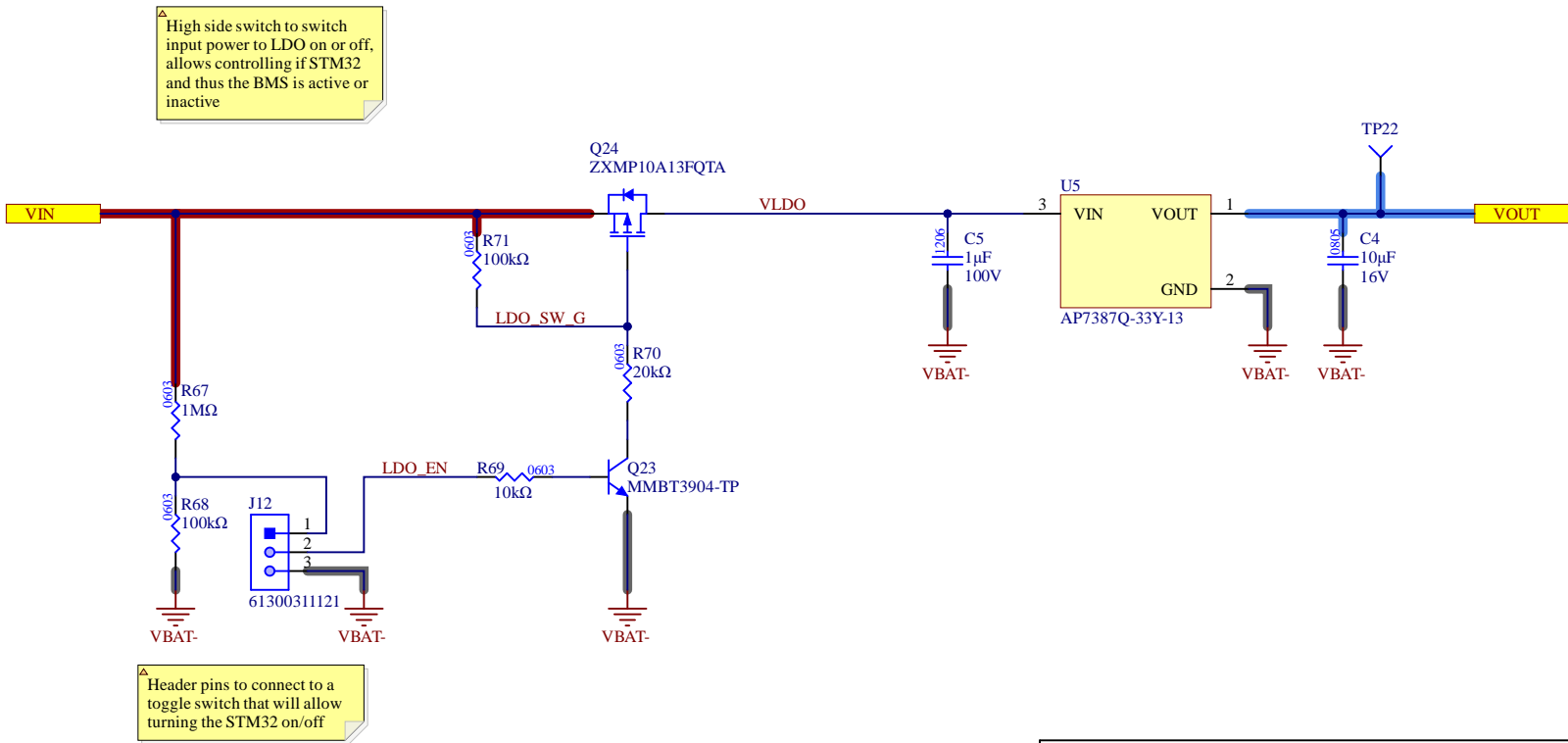


Debug / Programming Connector



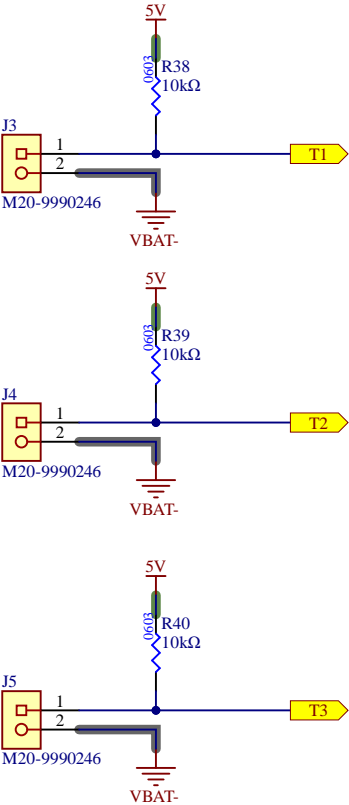
University of Waterloo 200 University Ave W Waterloo, Ontario, Canada N2L 3G1		REV 1.0
PROJECT LTO 16S.BMS.PrjPcb, [No Variations]		
DOCUMENT STM32_MCU.SchDoc		MODIFIED 2023-06-15
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3.3V POWER



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PROJECT LTO 16S BMS.PrjPcb, [No Variations]		
DOCUMENT Power_3V3.SchDoc		MODIFIED 2023-06-15
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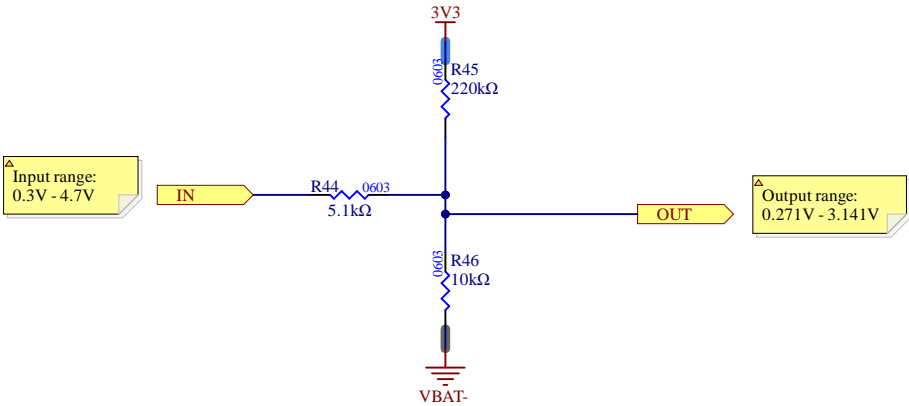
TEMPERATURE SENSING



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PROJECT LTO 16S BMS.PrjPcb, [No Variations]		
DOCUMENT Temperature_Sense.SchDoc		MODIFIED 2023-06-15
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ANALOG ATTENUATOR

Δ Analog attenuator circuit, based on this TI post:
https://e2e.ti.com/blogs_/b/analogwire/posts/three-ways-to-scale-an-analog-input-signal
Falstad sim: <https://tinyurl.com/2k2x8zjf>



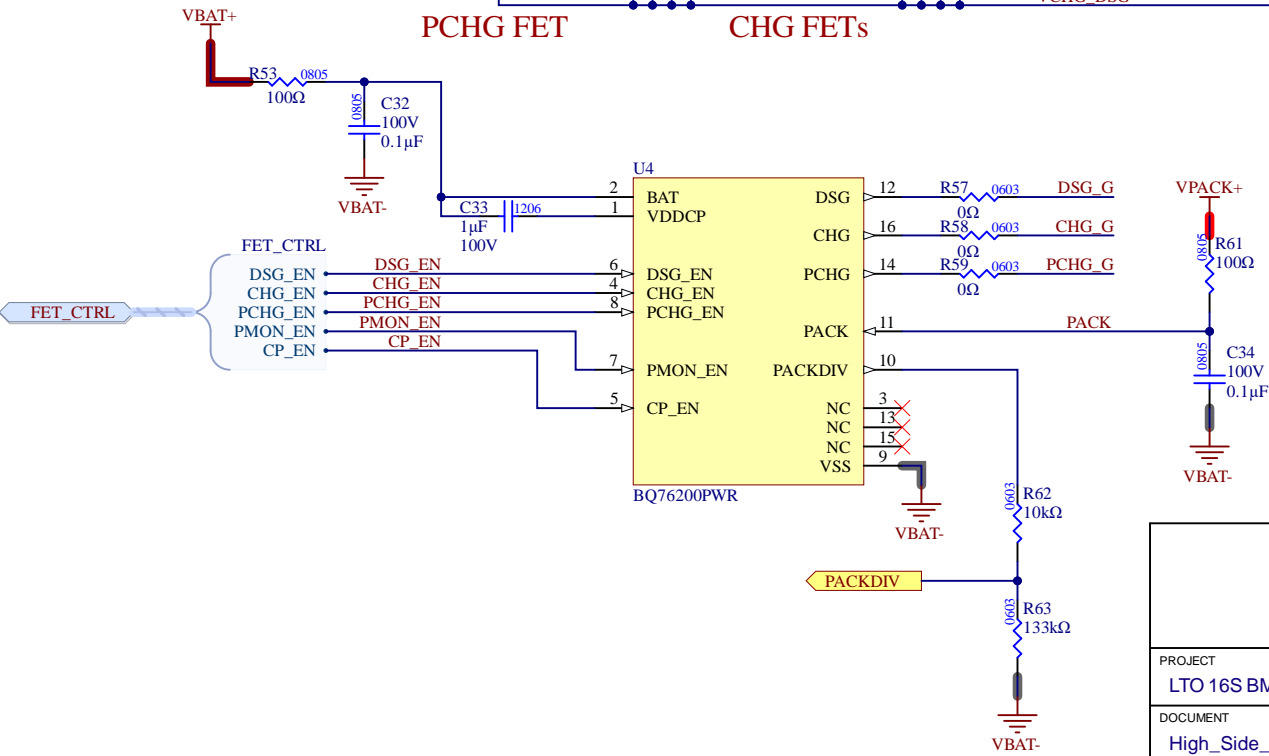
University of Waterloo 200 University Ave W Waterloo, Ontario, Canada N2L 3G1		REV 1.0
PROJECT LTO 16S BMS.PrjPcb, [No Variations]		
DOCUMENT Analog_Attenuator.SchDoc		MODIFIED 2023-06-15
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HIGH SIDE POWER SWITCH

Parallel FETs configured based on TI app note: <https://www.ti.com/lit/an/slva729a/slva729a.pdf?ts=1684104737246>

Heatsinks available for FETs in case they get too hot

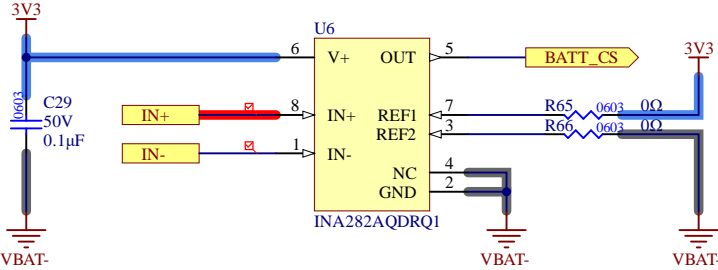
Max current: 25A
Rsense power dissipation: 0.625W @ 25A



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PROJECT LTO 16S BMS.PrjPcb, [No Variations]		
DOCUMENT High_Side_Switch.SchDoc		MODIFIED 2023-06-15
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CURRENT SENSE AMP

△ Amplifier gain: 50V/V
Output at 0A: 1.65V
Output at 25A (CHG): 2.9V
Output at 25A (DSG): 0.4V



University of Waterloo 200 University Ave W Waterloo, Ontario, Canada N2L 3G1		REV 1.0
PROJECT LTO 16S BMS.PrjPcb, [No Variations]		
DOCUMENT Current_Sense_Amp.SchDoc		MODIFIED 2023-06-15
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